Silicon and Substrates

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Chapters 4, 23.1

Outline I

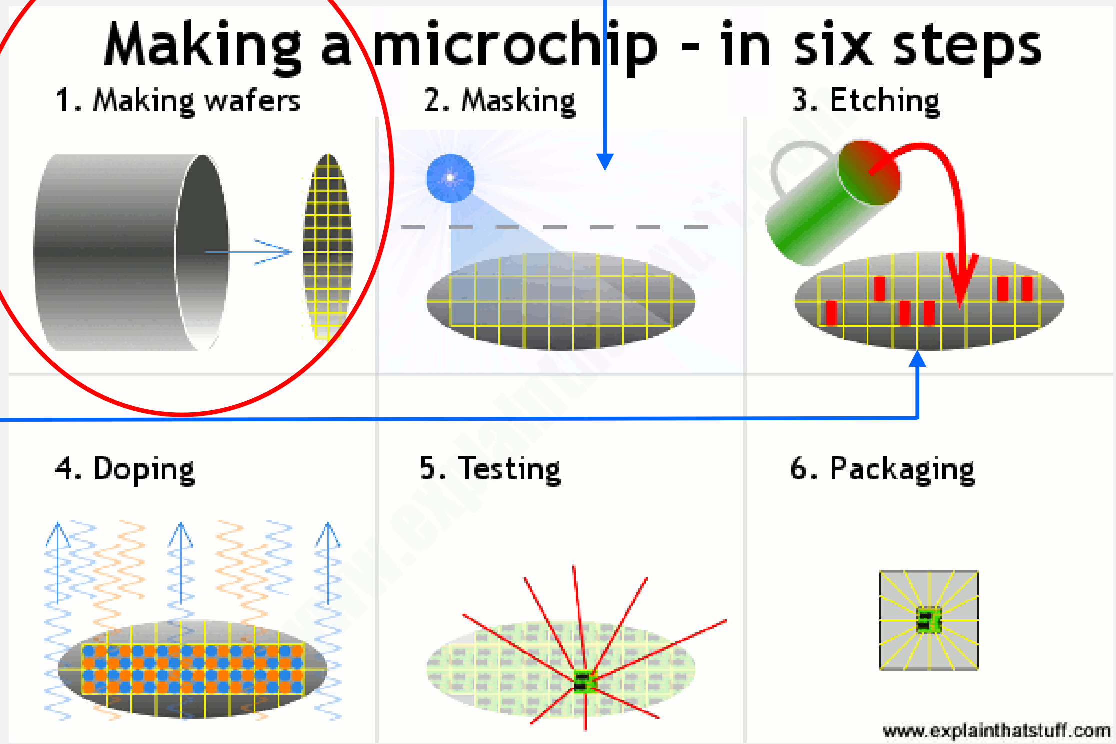
Previous lecture

- Introduction

Current lecture

- Litho and Etching

Next lecture



Outline II

- Silicon unique status and properties
- Silicon production:
  - growth
  - wafering
- Miller indices
- Defects
- Substrate materials

Silicon I

Natural

16 x 26 mm^2

Melted poly

32 x 45 mm^2

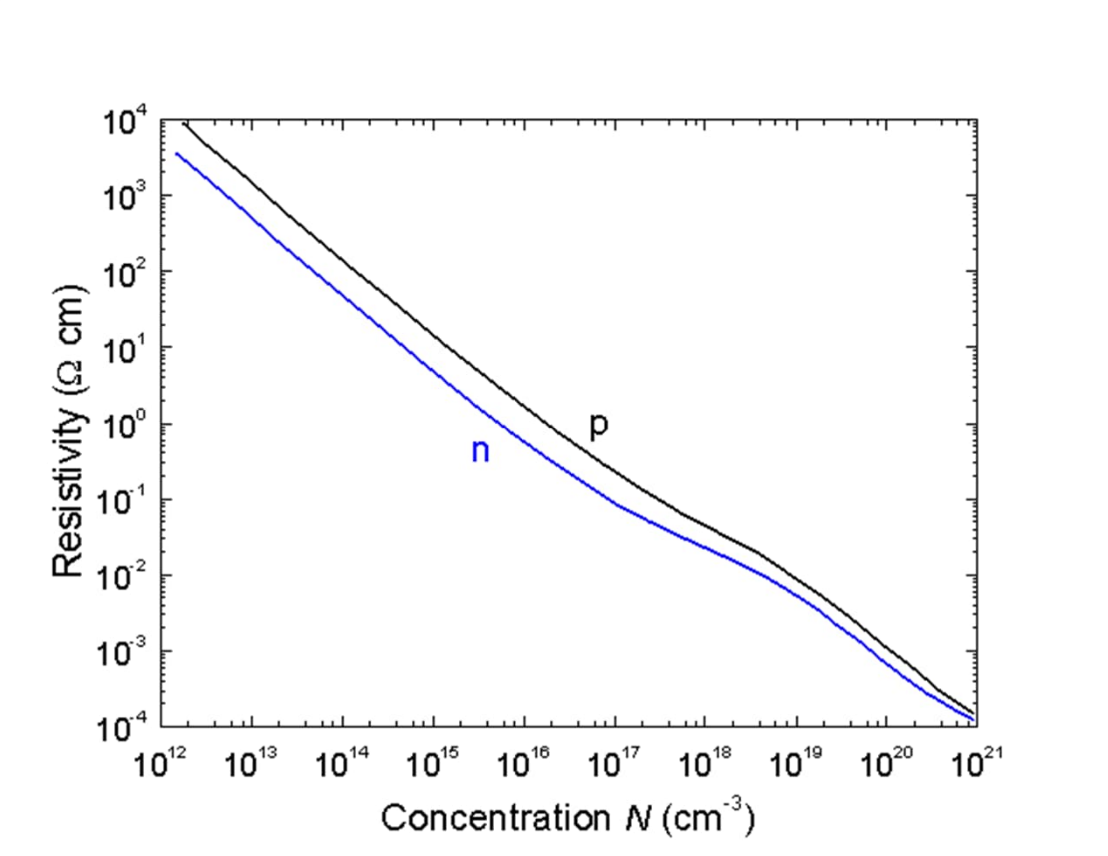
Single crystal

Silicon II

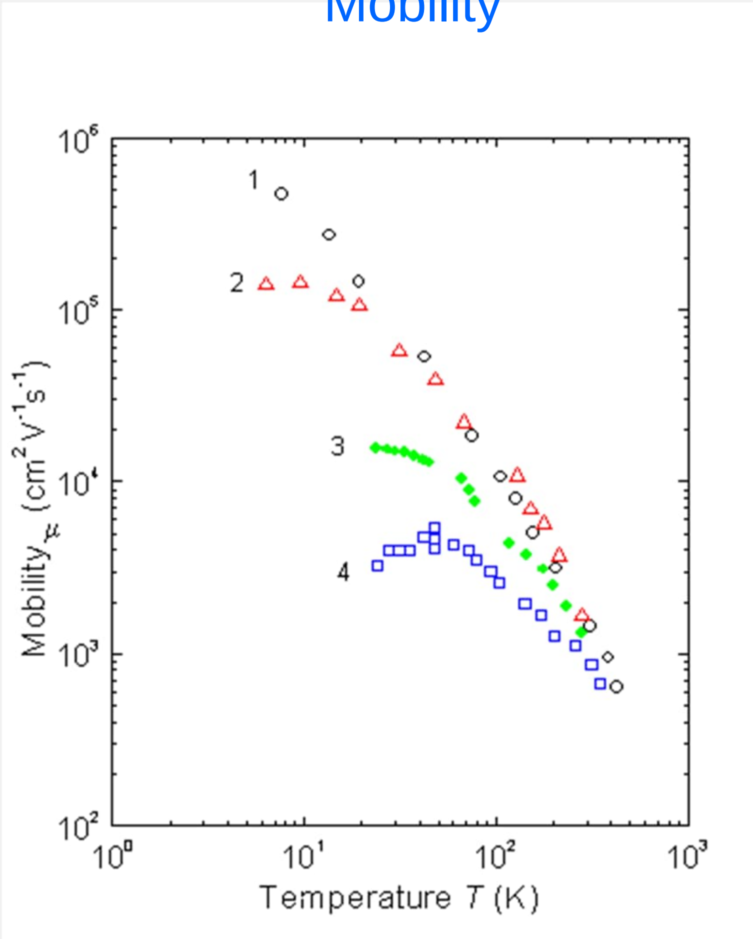
- Silicon is useful (see Introduction)
- Silicon is monocrystalline
- Silicon is used as a flat circular substrate

Electronic properties

Resistivity



Mobility



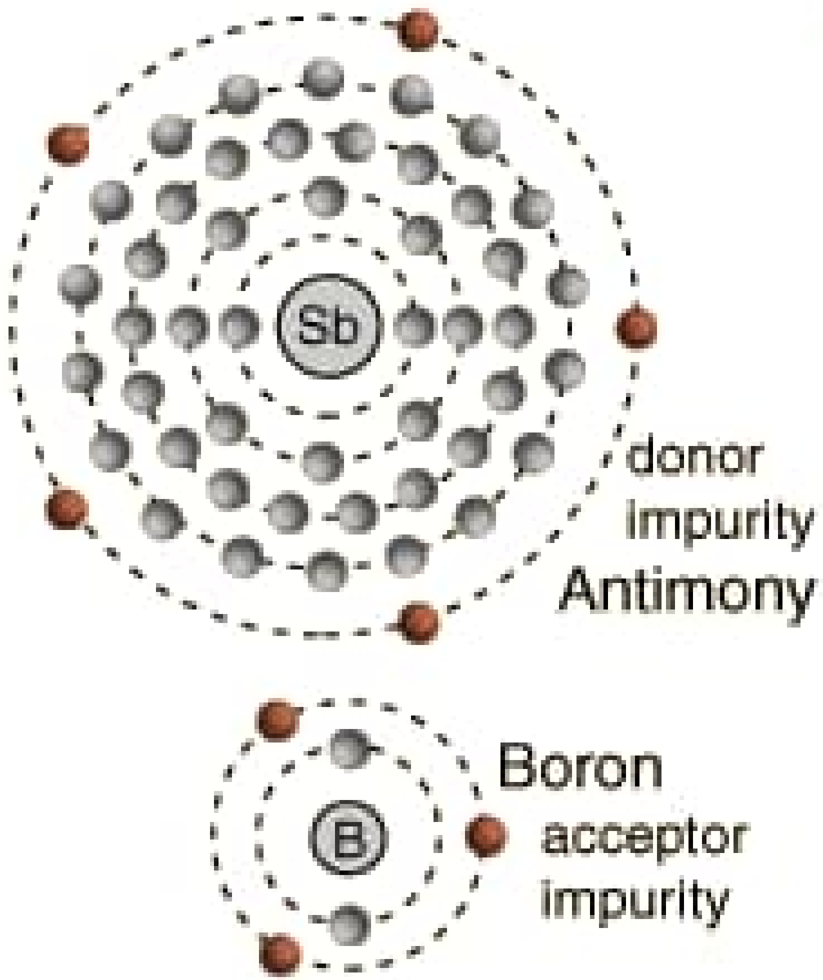
1. High purity Si ($N_d < 10^{-12}$ cm^{-3}); time-of-flight technique (Canali *et al.* [1973])
2. High purity Si ($N_d < 4 \cdot 10^{-13}$ cm^{-3}): photo-Hall effect (Norton *et al.* [1973])
3. $N_d = 1.75 \cdot 10^{16}$ cm^{-3}; $N_a = 1.48 \cdot 10^{15}$ cm^{-3}; Hall effect (Morin and Maita [1954])
4. $N_d = 1.3 \cdot 10^{17}$ cm^{-3}; $N_a = 2.2 \cdot 10^{15}$ cm^{-3}; Hall effect (Morin and Maita [1954])

Donors and acceptors for Si

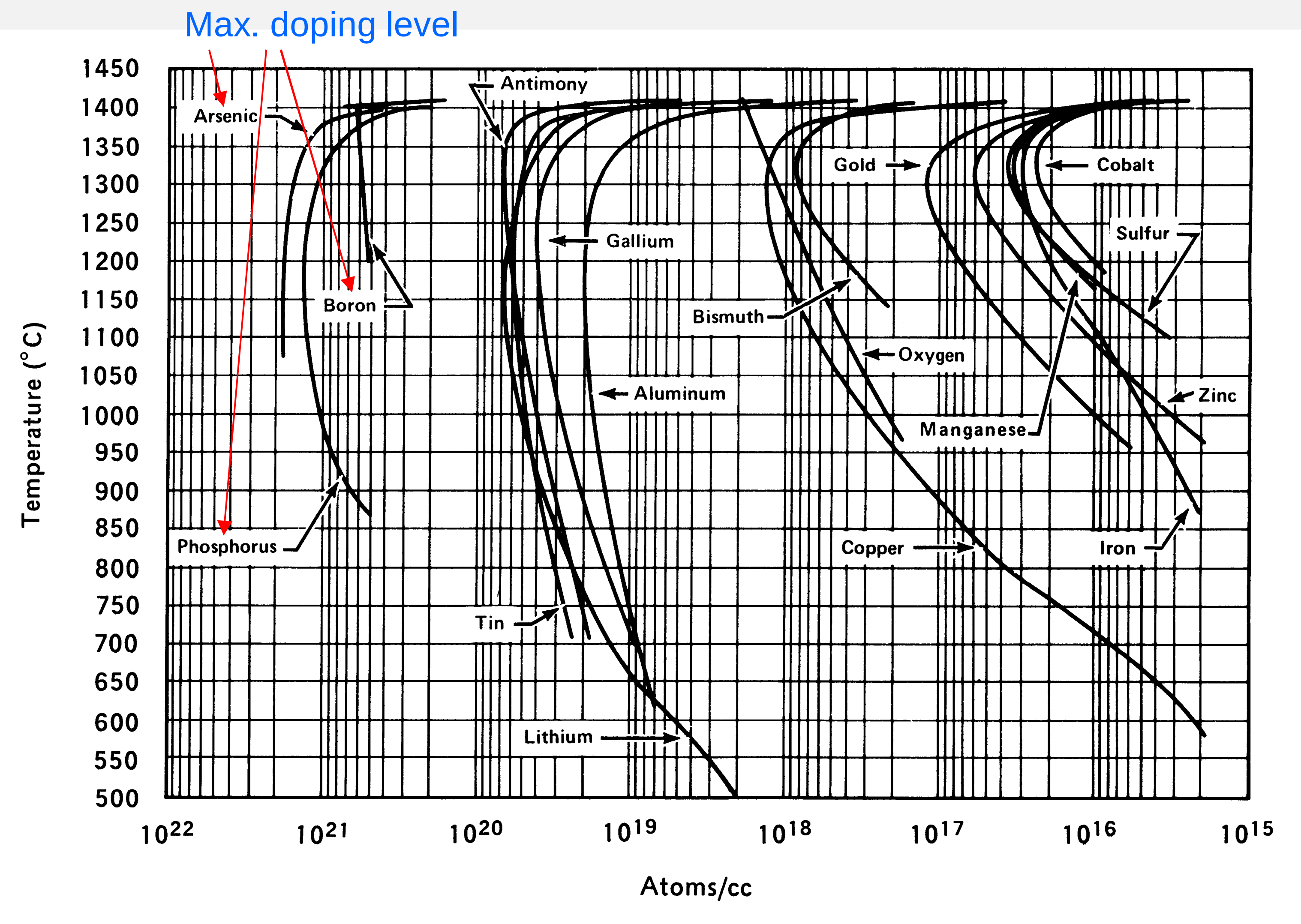
Antimony
Arsenic
Phosphorous

In use. Why?

Boron
Aluminum
Gallium



Solid solubility – maximum dopant concentration in *c*-Si

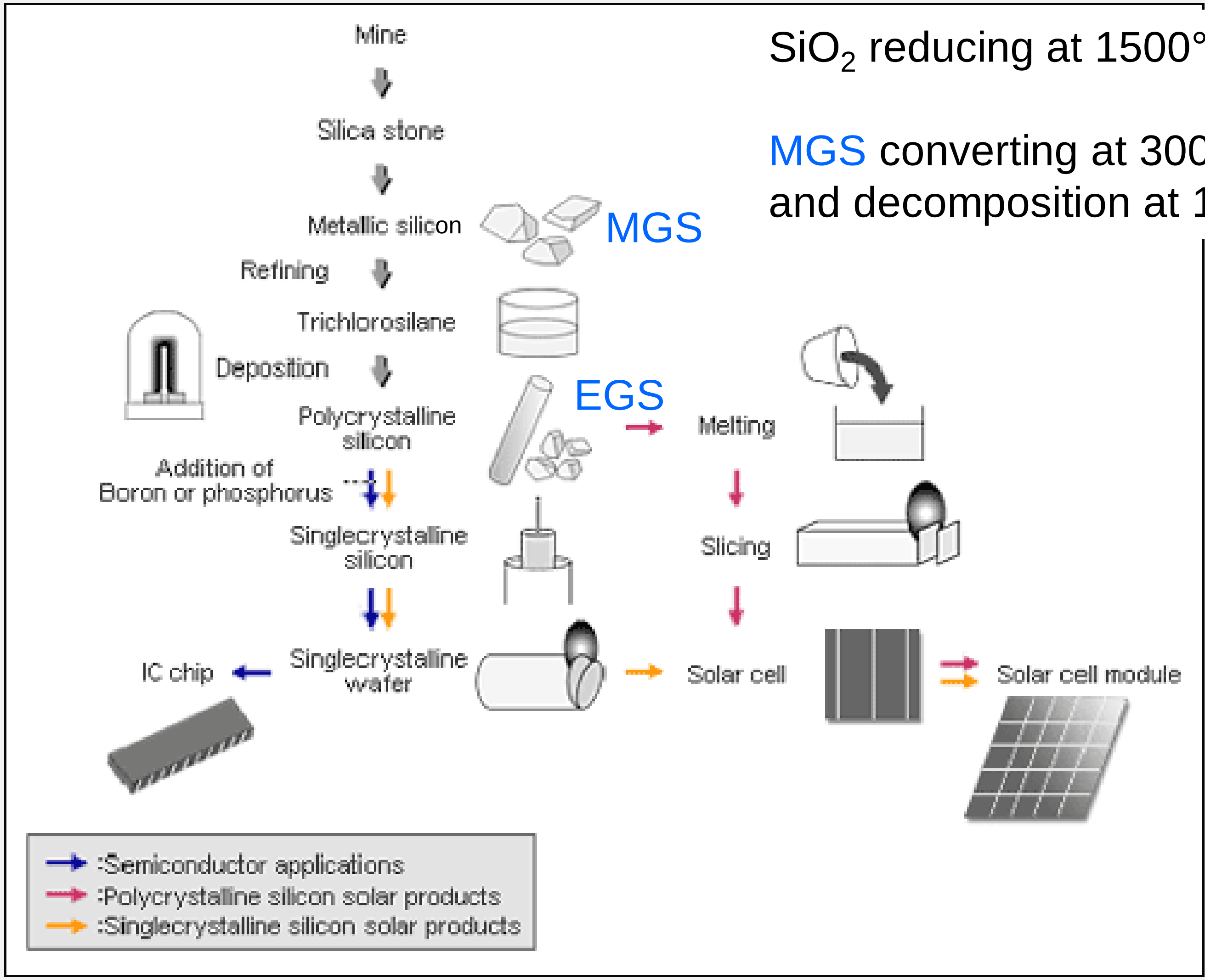


Types of doping

- Blank doping
  - during crystal growth (doped raw Si)
  - during epitaxy - > lecture 8

- Selective doping - > lecture 8
  - by ion implantation
  - by diffusion

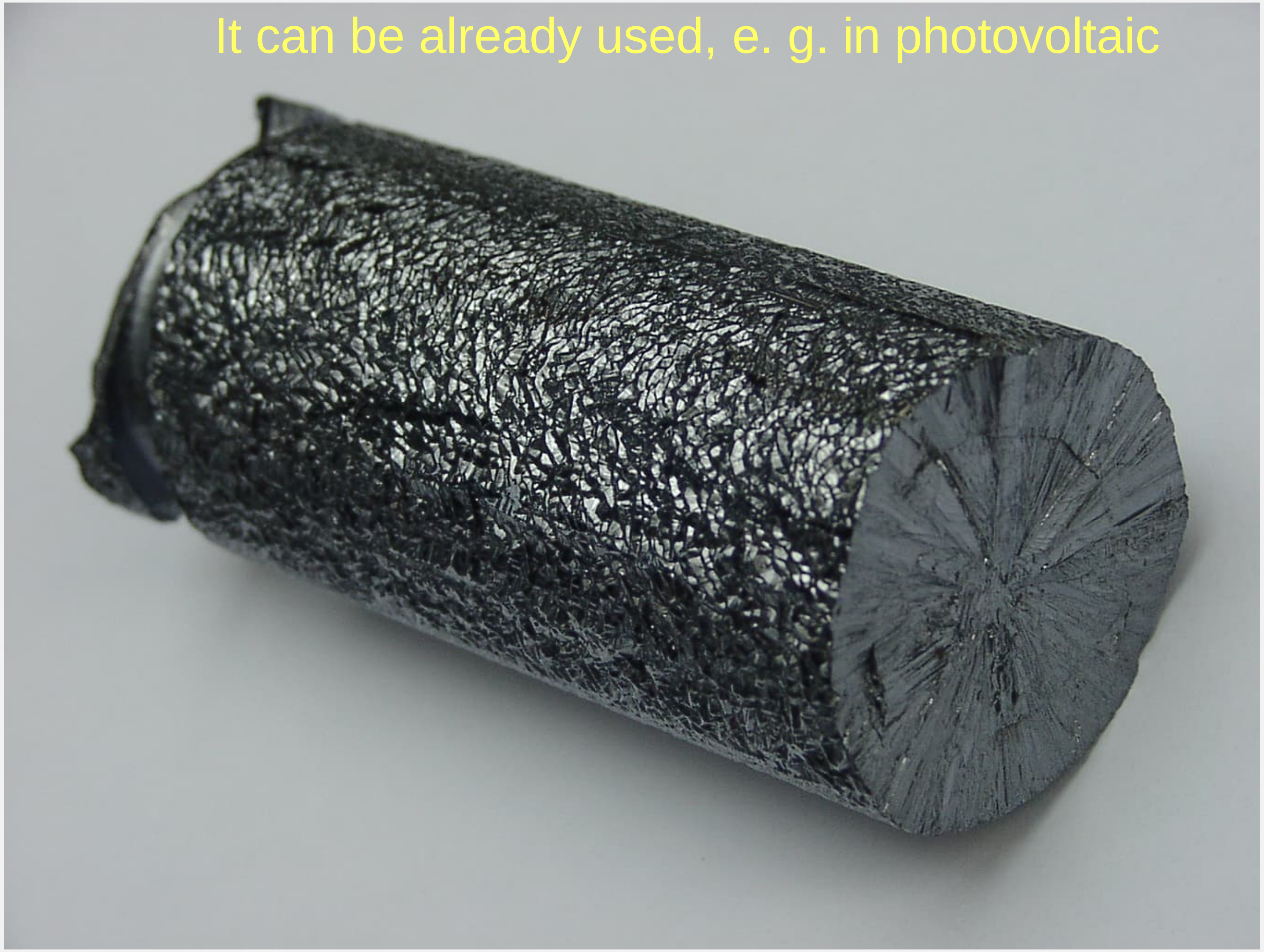
Si purification and production



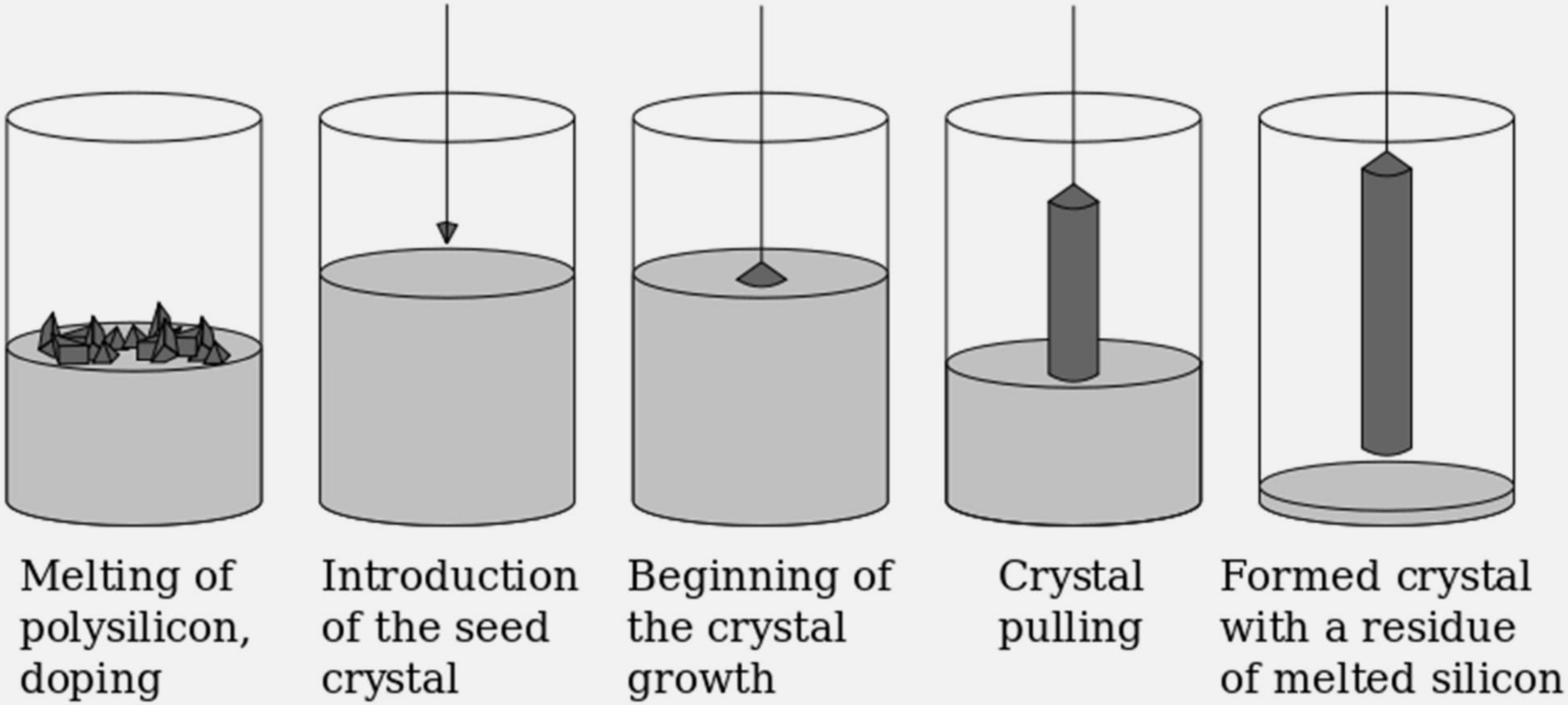
SiO_2 reducing at 1500°C -> MGS, 98% pure Si

MGS converting at 300°C to $SiHCl_3$, distillation and decomposition at 1100°C to Si -> EGS, ppb purity

EGS polysilicon



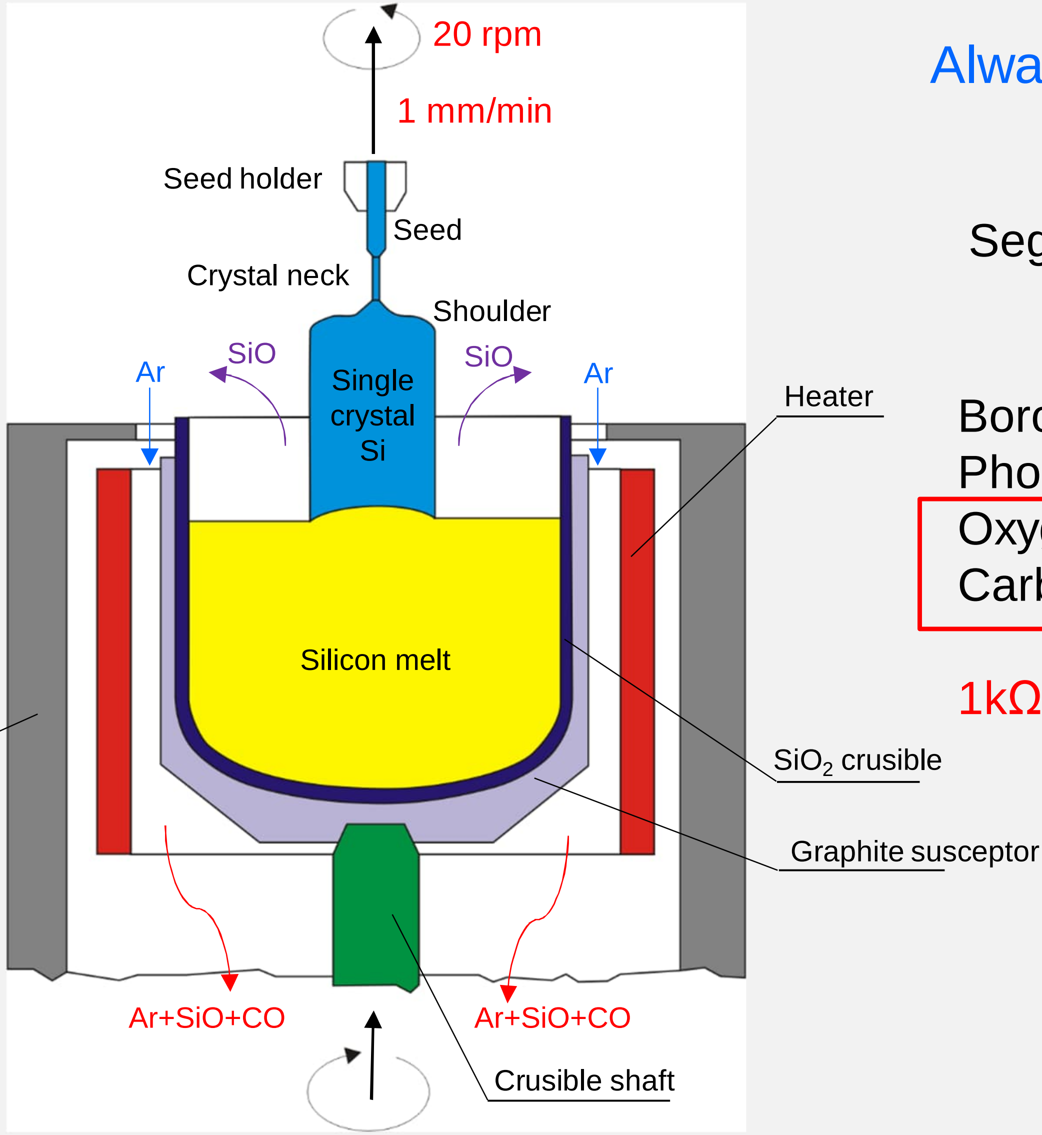
Czochralski crystal growth : liquid phase epitaxy



The method is 100 years old!

Czochralski (CZ) *c*-Si growth

Increasing of dopants
Decreasing of oxygen



1420 ºC
30 hours

Always there is O_2 !

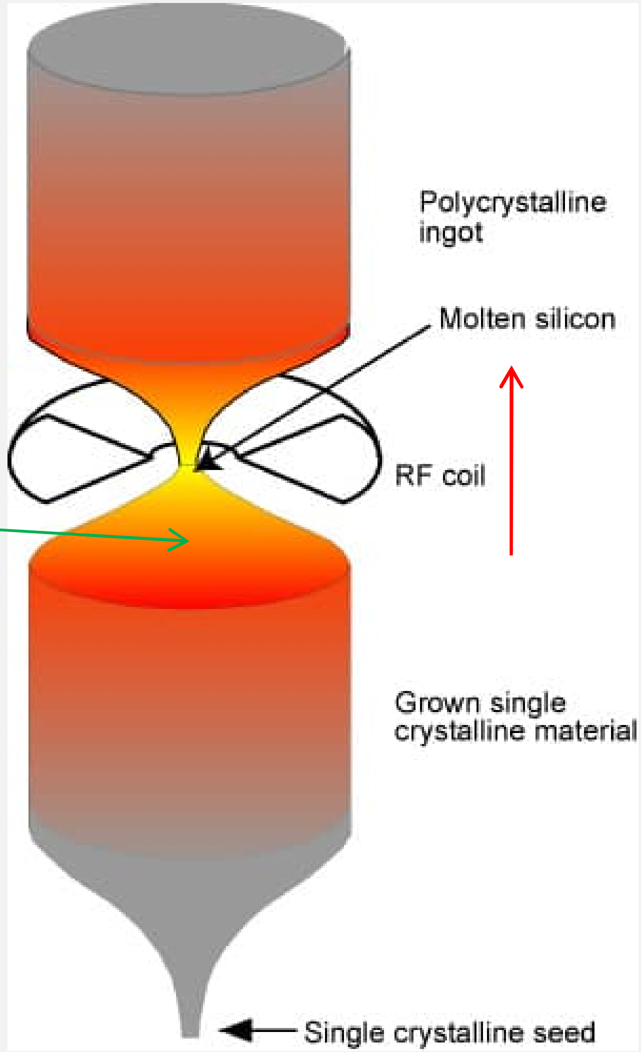
Segregation coefficient
$k_0 = C_{solid}/C_{liquid}$

Boron	0.8
Phosphorous	0.35
Oxygen	1.25
Carbon	0.07

1kΩ-cm – max resistivity

c-Si ingots

Float zone (FZ) growth



There is no O_2 !

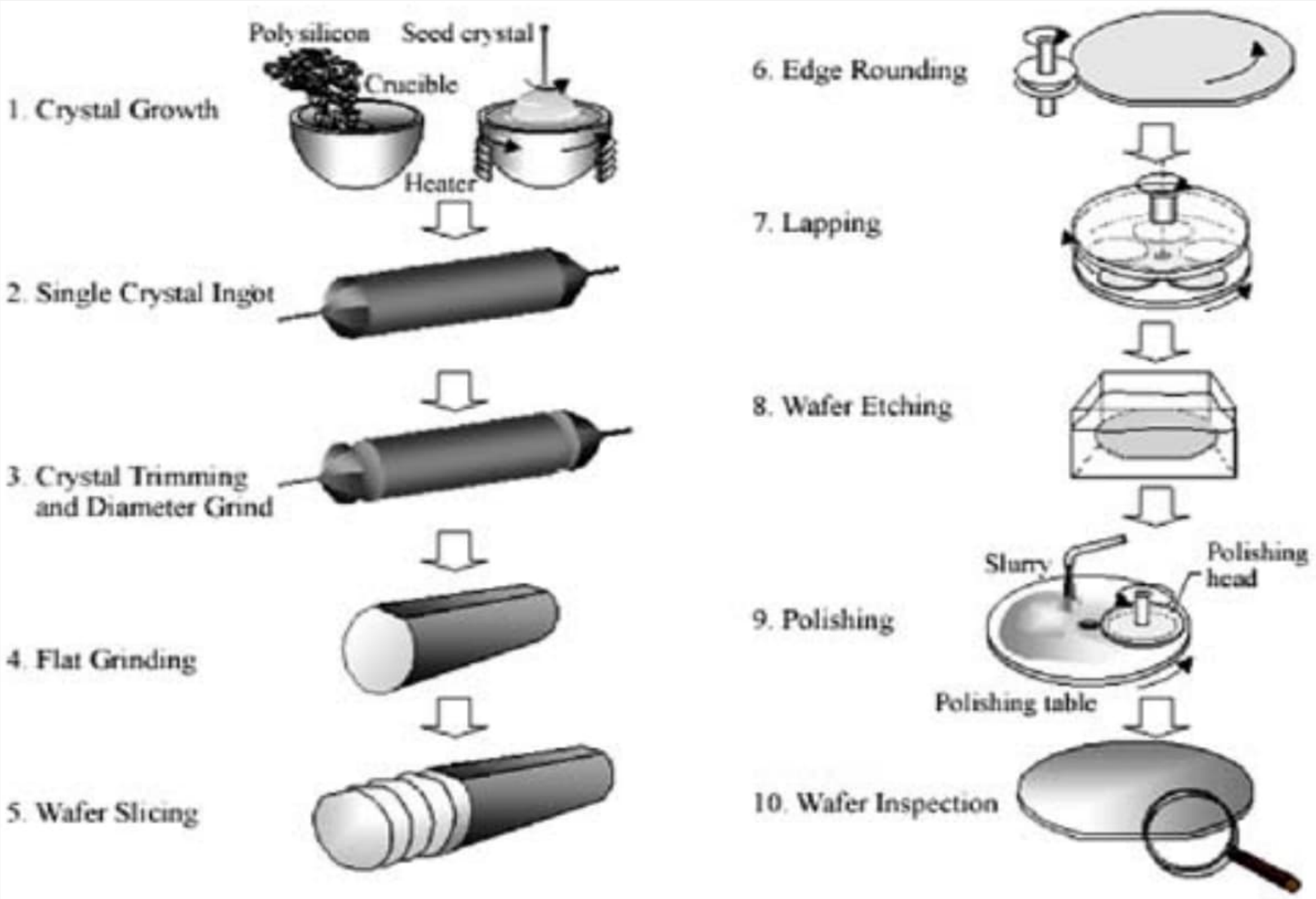
Impurities move with melted region

max 20kΩ-cm

max 150 mm (450 mm MCZ)

Vacuum or Ar ambient

Silicon wafering



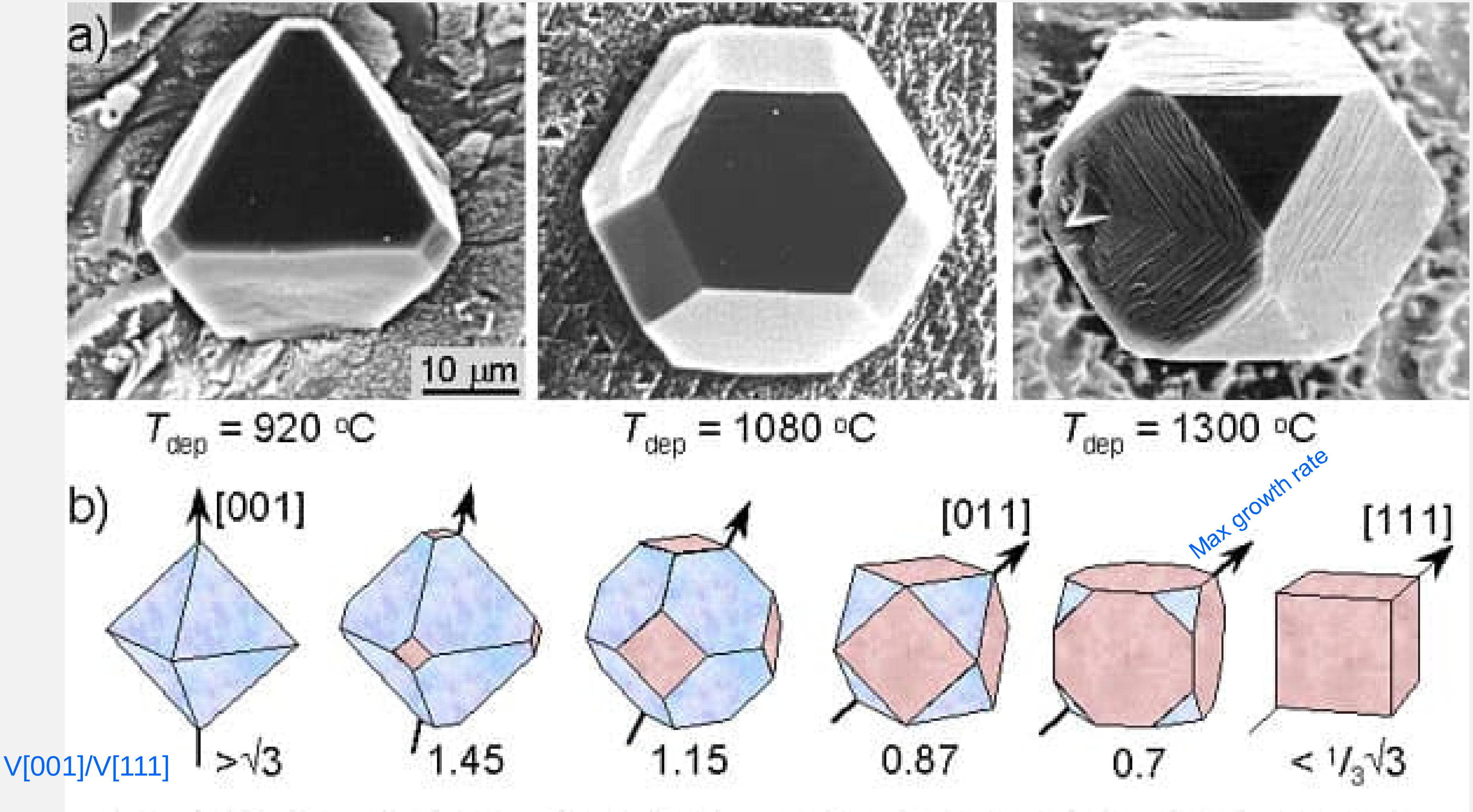
http://www.southalabama.edu/engineering/ece/faculty/akhan/Courses/EE539-Fall04/Lecture-slides/lecture-4-crystal%20growth.pdf

Video

- 4 min <Si> crystal growth & wafering:
- https://www.youtube.com/watch?v=AMgQ1-HdElM

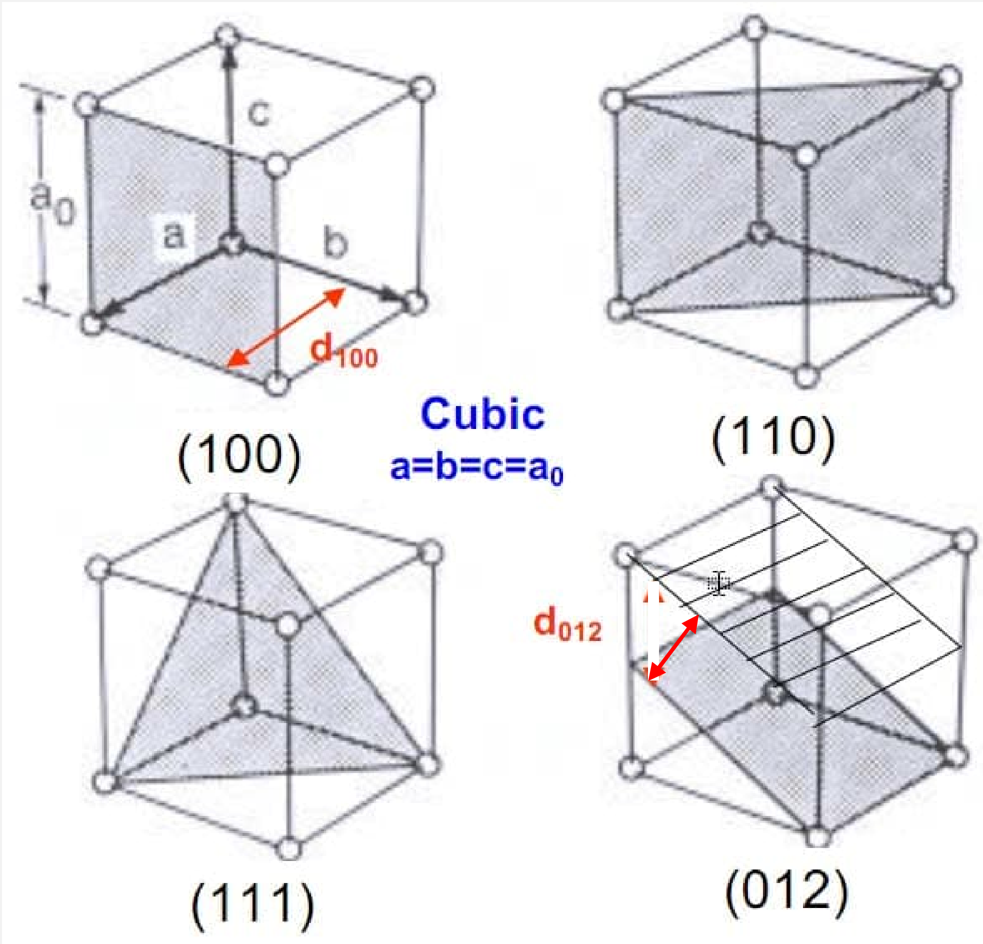
Crystal variety

Diamond shape variation



Si Miller indices

a	b	c
1	∞	∞
1	0	0



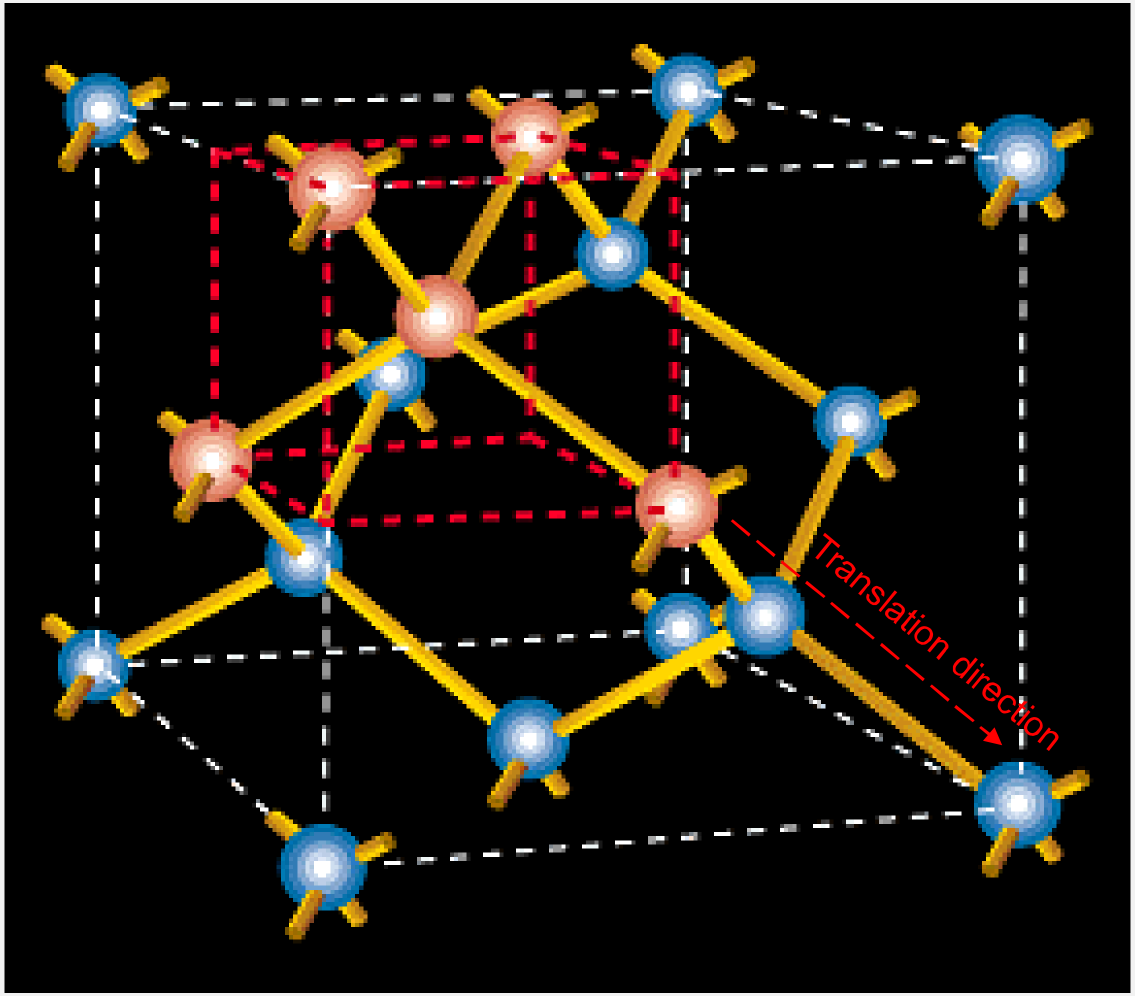
a	b	c
1	1	∞
1	1	0

a	b	c
1	1	1
1	1	1

a	b	c
∞	1	½
0	1	2

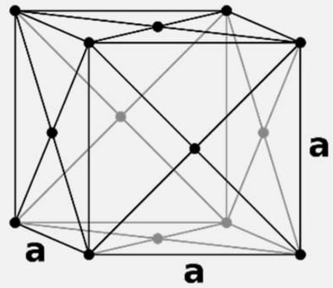
Black numbers - fractional intercepts, Blue numbers - Miller indices

Si unit cell



www-inst.eecs.berkeley.edu/~ee130/sp07

FCC face-centered cubic



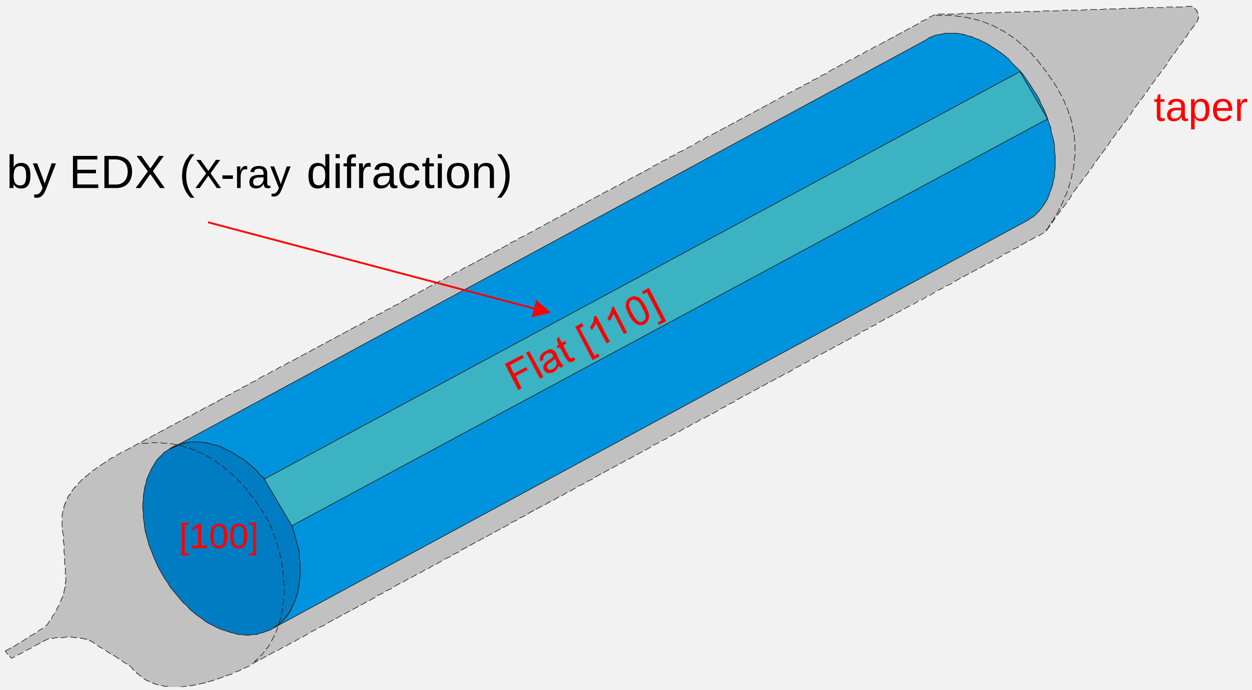
Two ¼ shifted FCC or
"diamond cubic" lattice

a=5.43Å

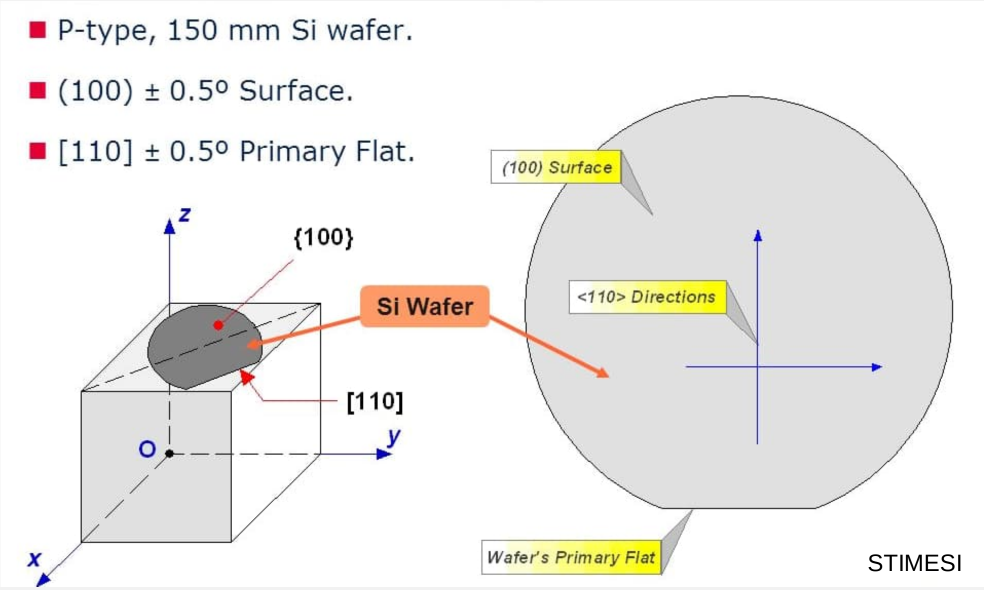
filled space 34%
(hexagonal 74%)

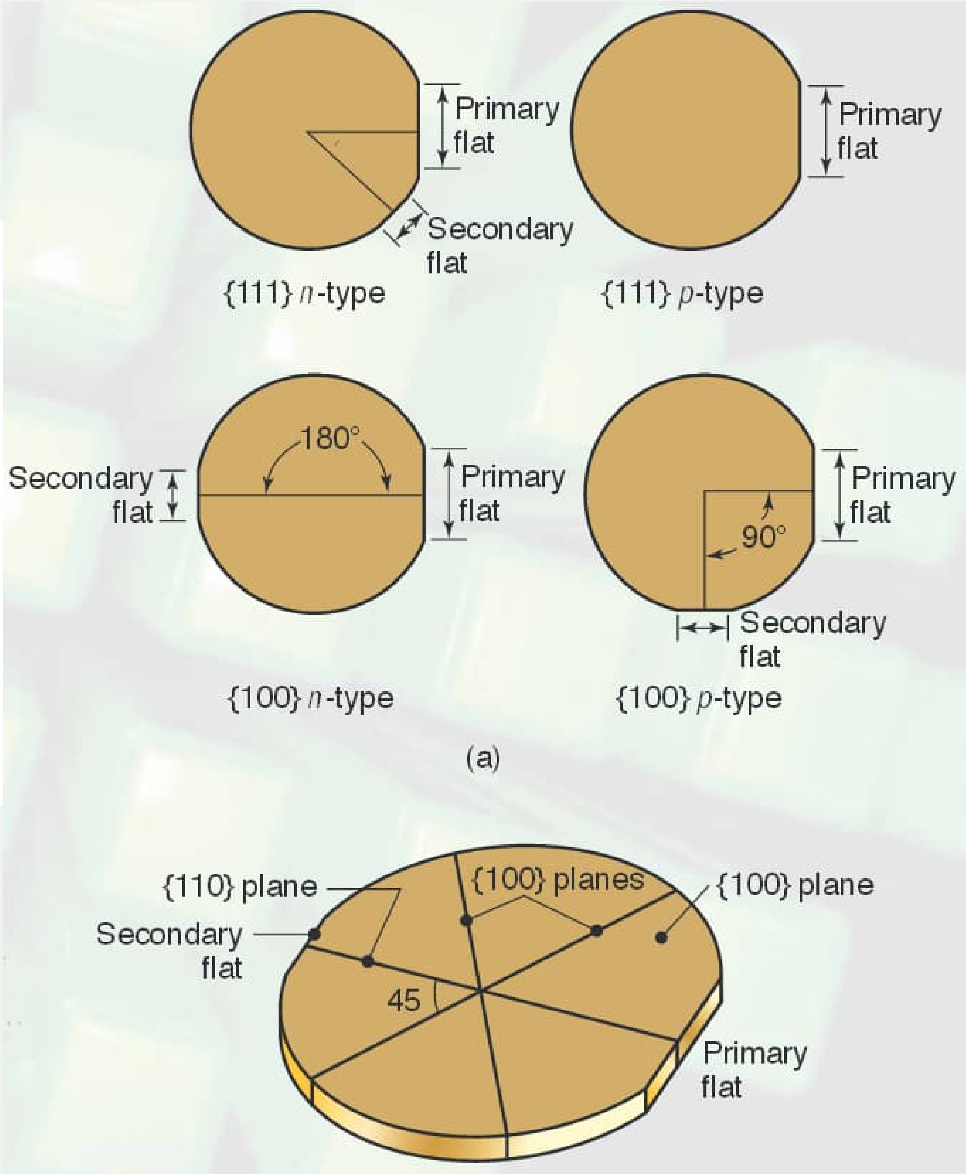
Crystal shaping and flat grinding for Si (100) wafers

Flat is found by EDX (X-ray difraction)



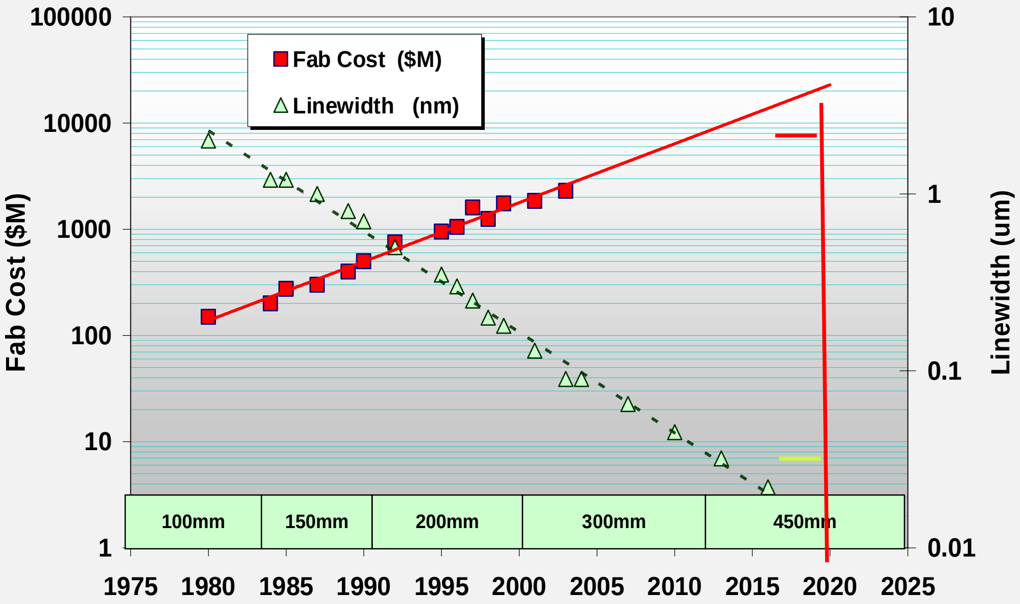
Si wafer flats





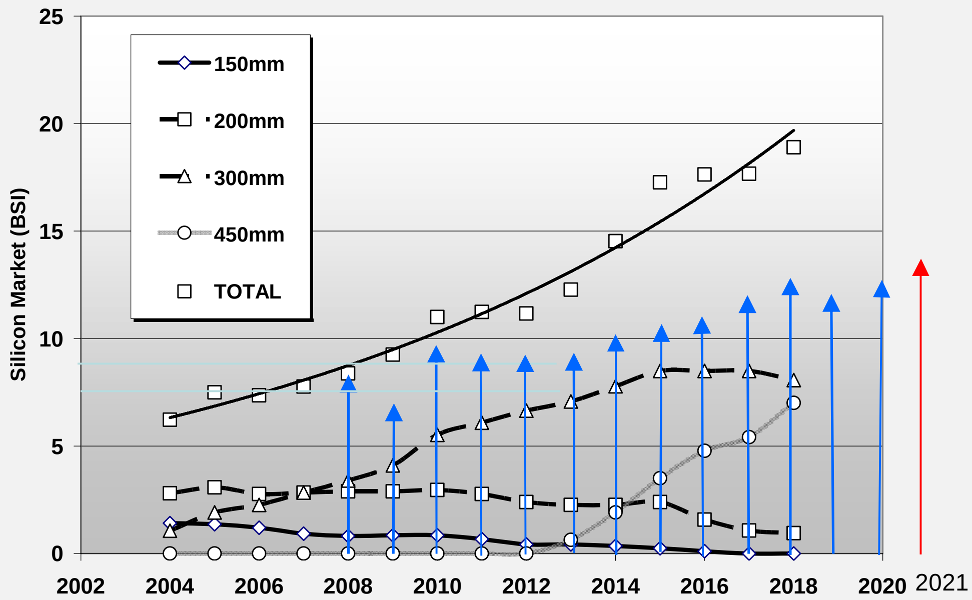
Silicon. Trends and forecast

Fab cost and wafer size



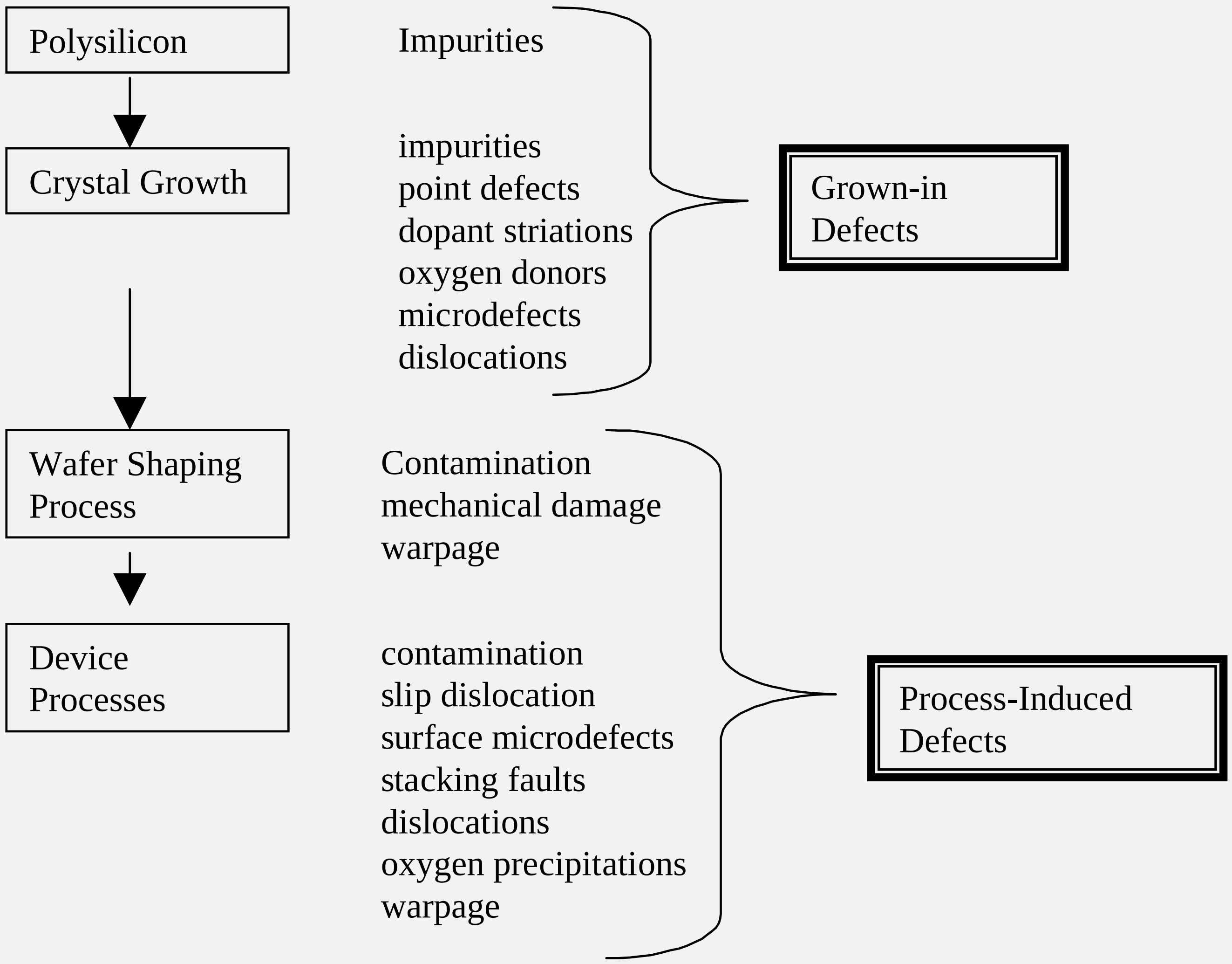
14,7 BSI - 2022

Si wafer production



200 mm - 1/3 of market
300 mm – 1/3 of market
Mainly for solar cells
US$ 11.6 Billion
BSI – billion square inches

Defect generation



Point defects

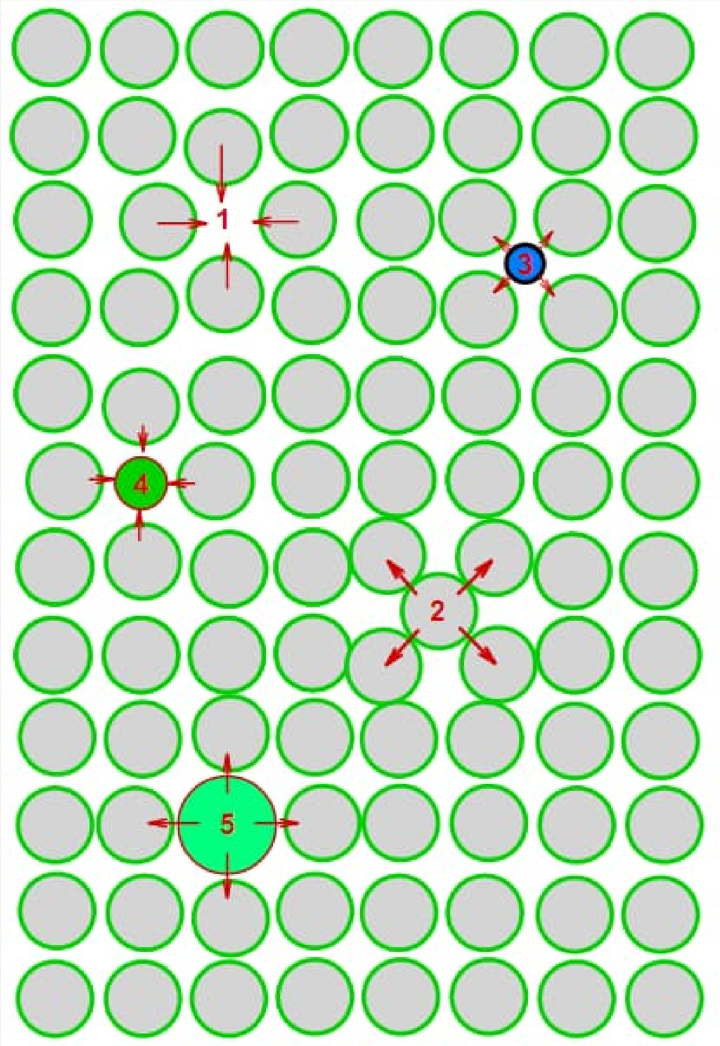
(1) vacancy

(2) self-interstitial

(3) interstitial impurity

(4),(5) substitutional impurities

arrows – local stresses



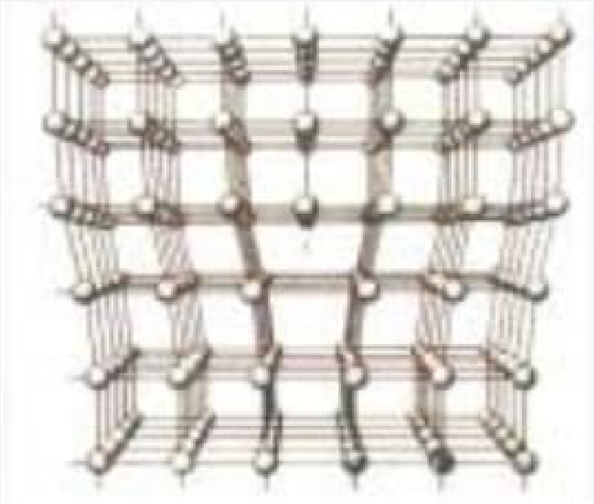
Substitutional impurities

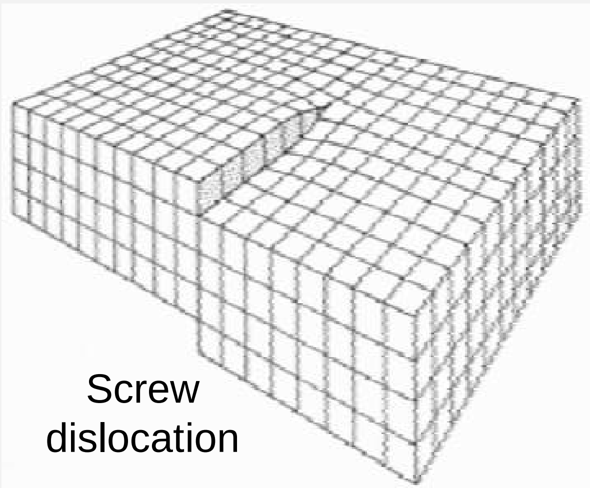
Ruby – Cr in Al_2O_3 matrix

Sapphire – Ti and Fe in Al_2O_3

Line defects (dislocations)

Edge dislocation





Damascus steel

Summary I

- Silicon posses unique set of functional properties
- Silicon is easily processed during fabrication
- Si forms thermal oxide with excellent functional properties and the oxide can be used as a mask
- Si is cheap and abundant on the Earth

-> as a result

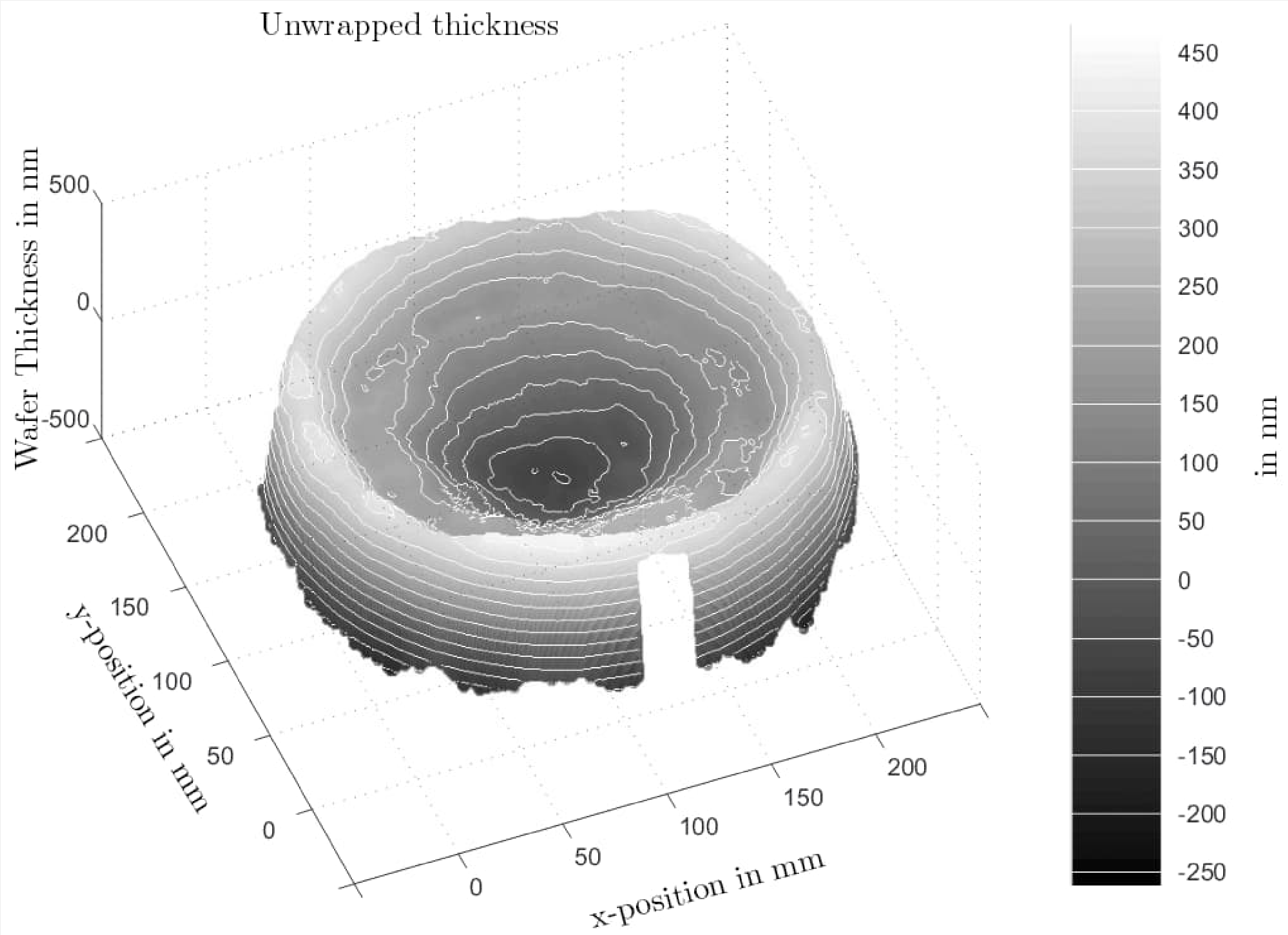
- The best ratio ”usefullness to price”

Substrates

- Functions: mechanical support and providing functional properties (electronic, optical etc.)
- Circular wafer
  - Si, GaAs, SiC, Ge, quartz, glass
- Square plate
  - glass, polysilicon, ceramics
- Film, foil
  - polymers: polyimide, PDMS, kapton
  - metals: Al, Cu

Substrate and wafer. What is the difference?

Wafer thickness measurements



Maarten J. Jansen, HanHaitjema, Peter H.J. Schellekens
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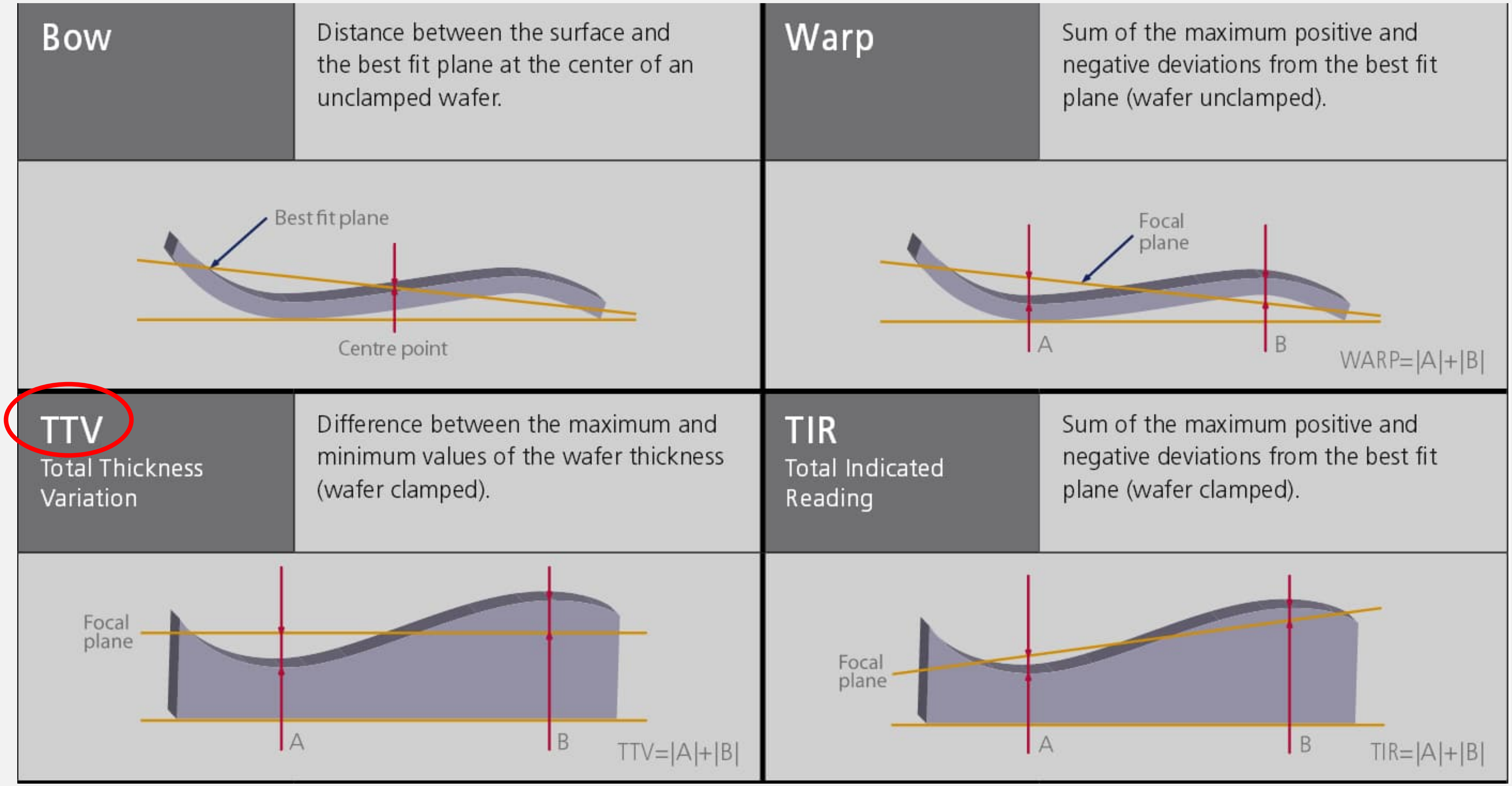
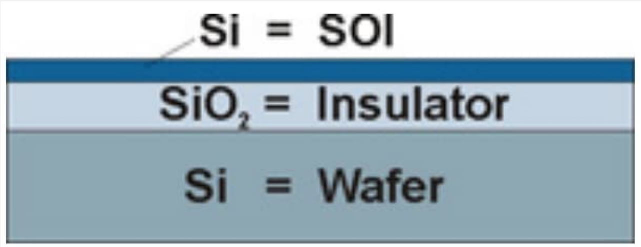
Global flatness specifications



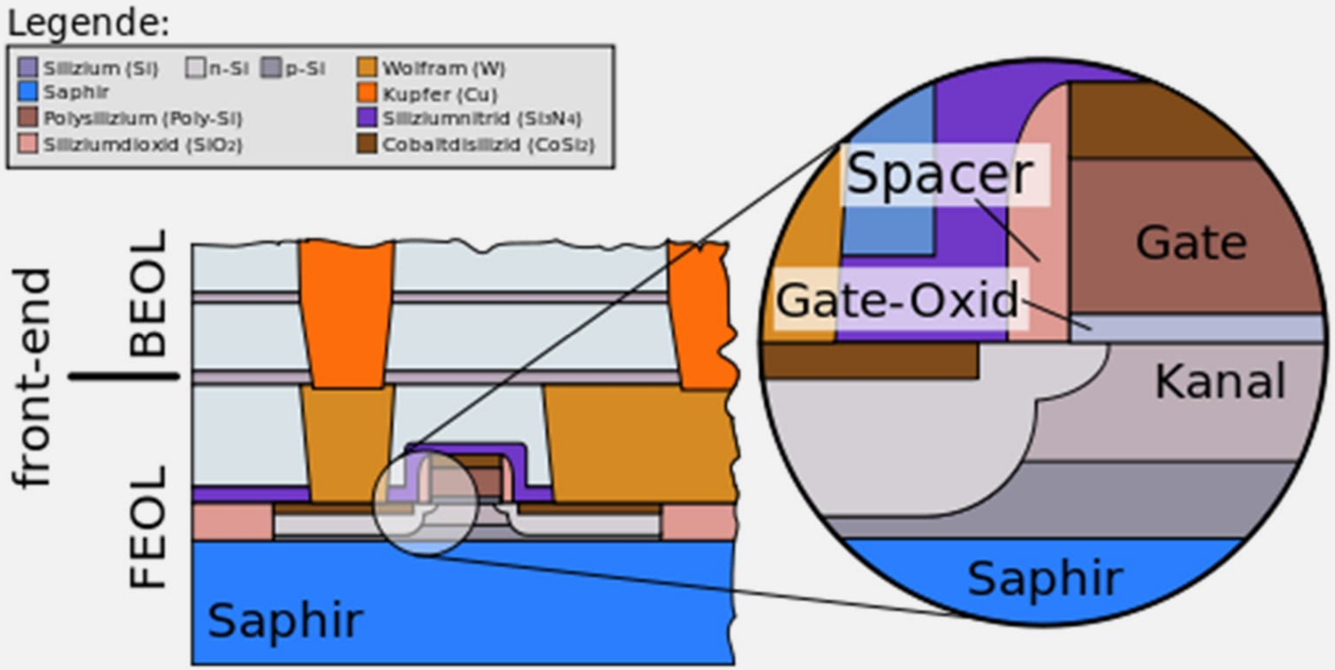
SOI and SOS wafers

Silicon on isolator (SOI)



Simplifies chip fabrication, but wafers are very expenssive!

Silicon on sapphire (SOS)



Unusual substrates

Mobility enhancement

Thermal management

System-on-chip

Memory solutions

Table 1. Emerging materials status*

Emerging material	First year coverage	Chip products on market	Close to mainstream acceptance	Change of importance since 2005		
				Increased	No change	Decreased
Global strained Si	2003	No	No		•	
Global strained SOI	2003	No	No	•		
Germanium channel transistors	2003	No	No	•		
III-V channel transistors	2007	No	No		N/A	
Isotopically pure Si	2003	No	No	Quantum computing		•
Silicon on diamond	2005	No	No		•	
Silicon on SiC	2005	No	No		•	
Silicon on alumina	2005	No	No		•	
Channel orientation	2005	Yes	Yes	•		
Surface orientation	2005	No	No		•	
Carbon nanotubes	2005	No	No		•	
High resistivity Si	2003	Yes	Yes	•		
Optical interconnection on Si	2003	No	No		•	
Phase change memory	2007	No	No	Non-volatile memory	N/A	$Ge_2Sb_2Te_5$

*listing the technologies that have been covered by the *ITRS* Emerging Materials committee since its inception in 2003, along with several status columns.

Summary II

- Wafers can be distinguished by:
  - material
  - doping
  - crystal orientation
  - shape
  - size
  - polished sides
  - grown layers