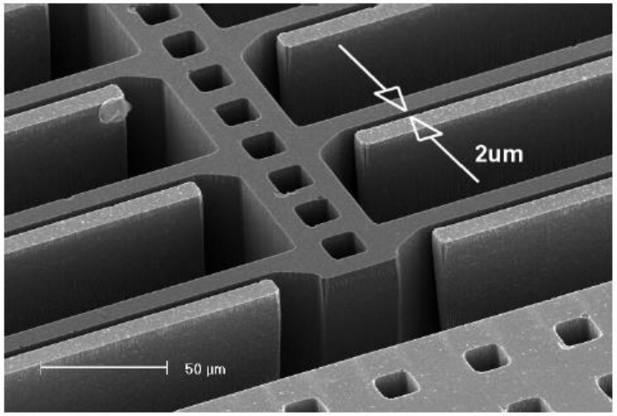
Introduction to microfabrication
(Based on chapter 1)

sami.franssila@aalto.fi

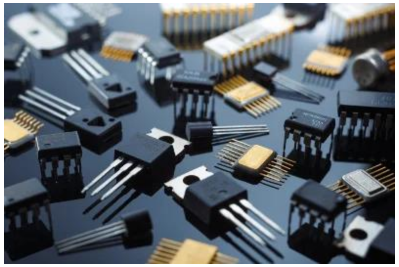
Figures from: Franssila: Introduction to Microfabrication unless indicated otherwise.

Tools, wafers, devices

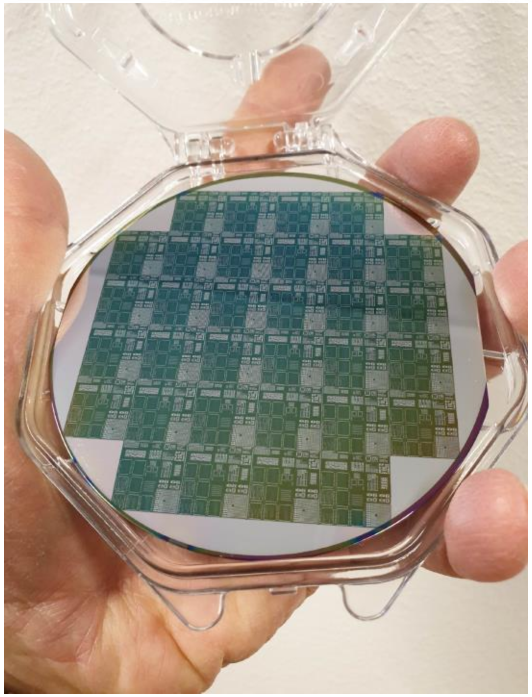
These are called tools, or equipment; they are reactors, furnaces, chambers,…



These are devices, accelerometers, transistors, filters…



These are components. Not part of this course.



This is a wafer. This particular wafer has 32 chips (a.k.a. die) on it.

Dimension in microworld

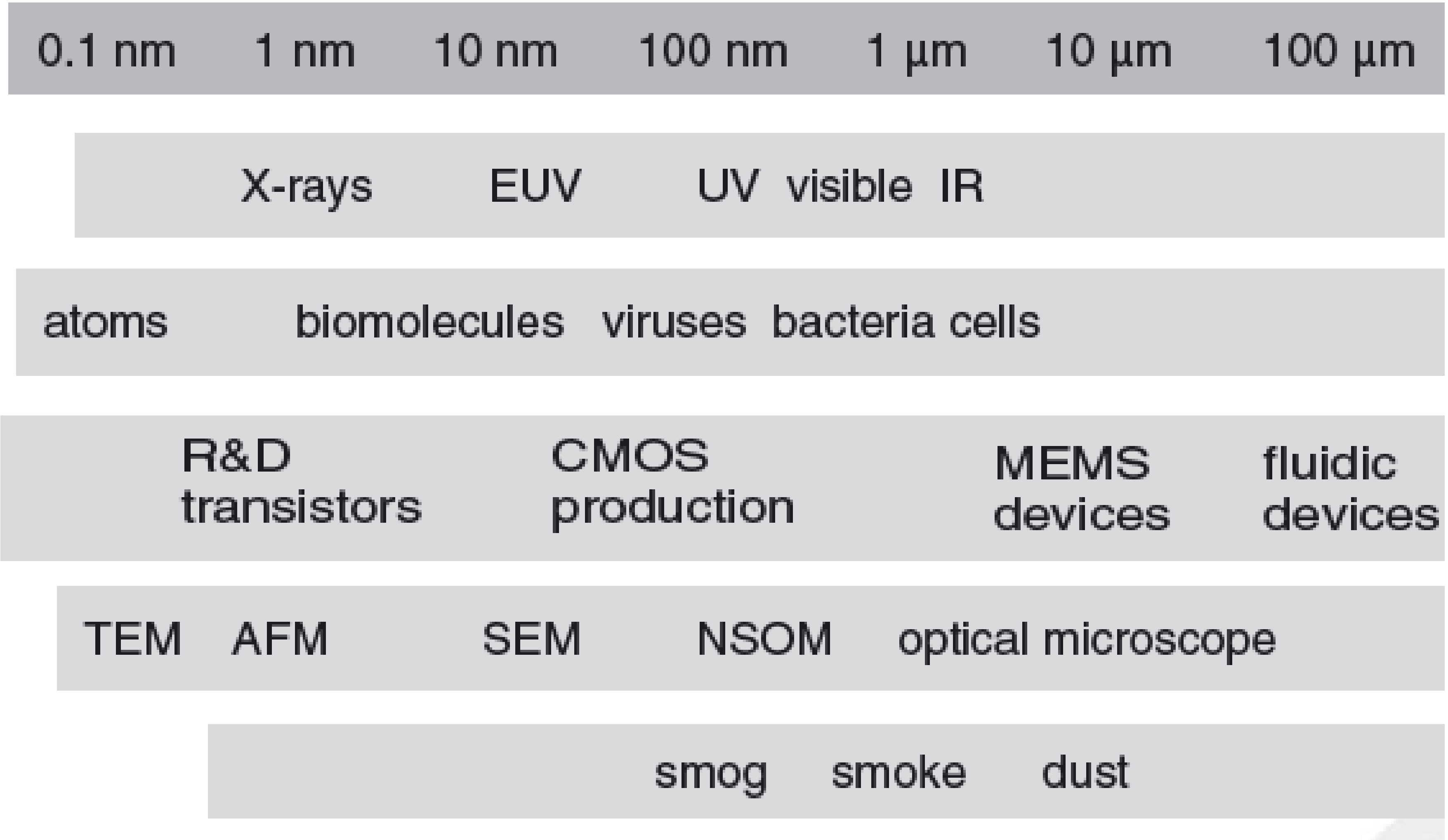


Fig. 1.12

Microfabrication vs. Nanofabrication ?

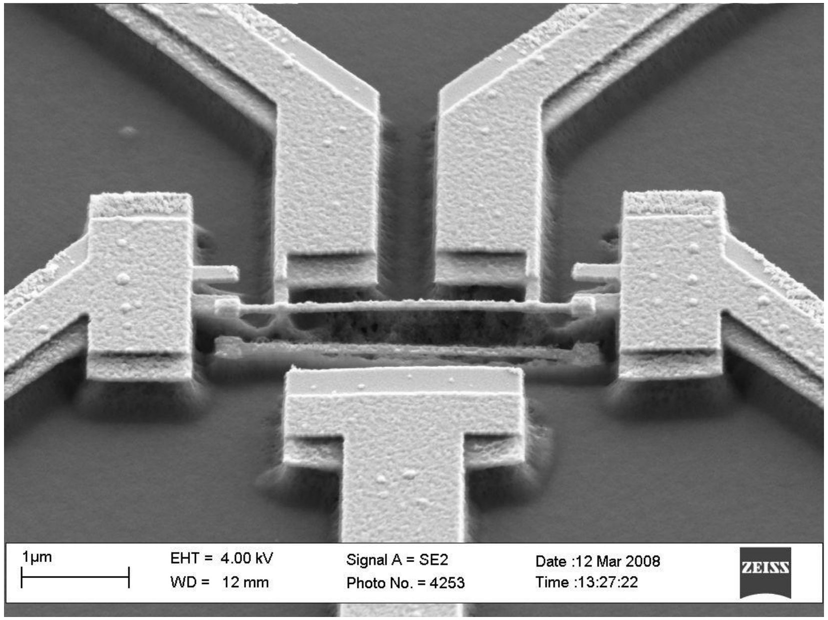


Fig. 1.3**:** Electron beam lithography defined gold-palladium nanobridge

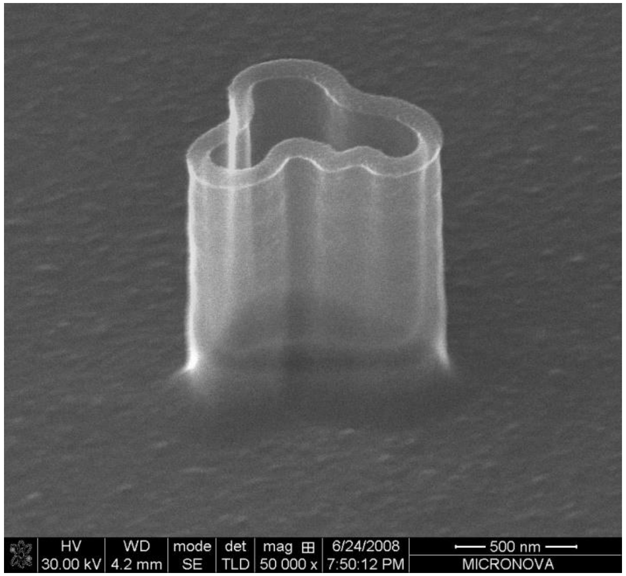


Fig. 24.4: Focussed ion beam patterned Aalto vase

Materials

thin film 2

thin film 1

1-1000 nm

Diffusions,
0.1-5 µm

silicon,
most often

substrate:
thick piece of material
(0.5 mm = 500 µm)

Common materials

Substrates:

Silicon

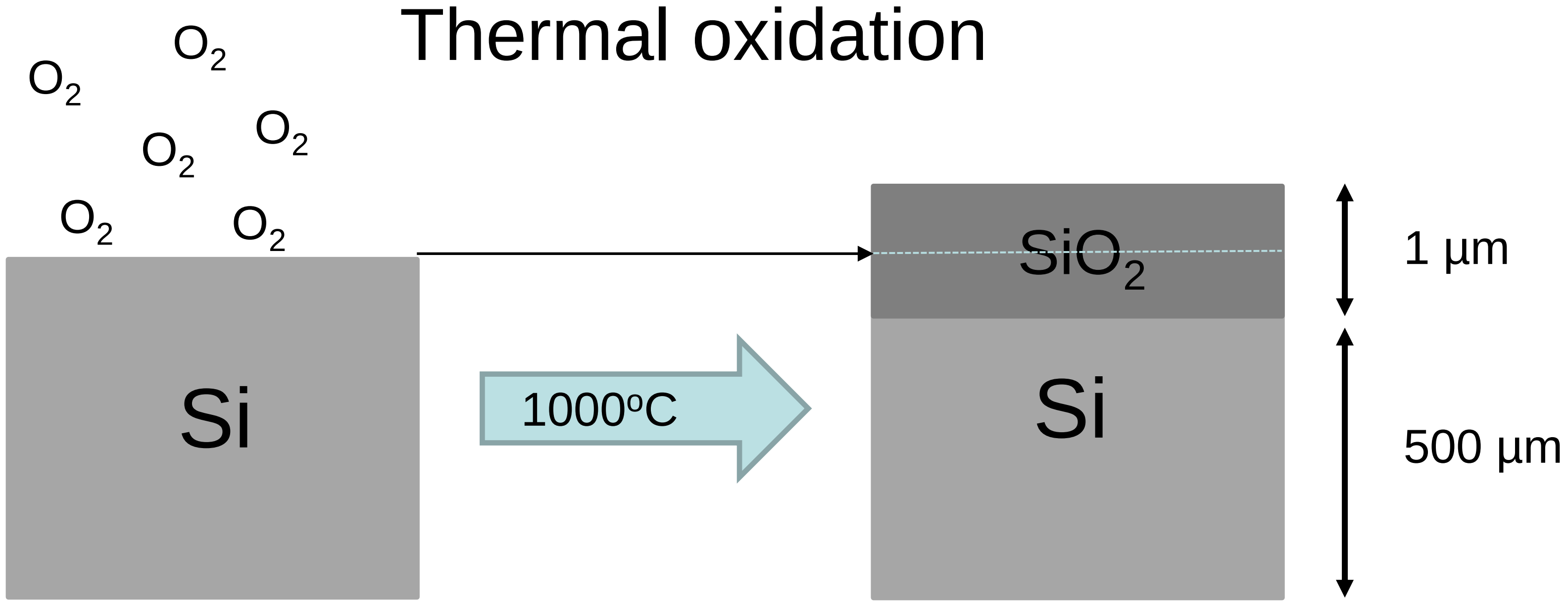
Thin films:

SiO_2
SiN_x
Polysilicon
Al
Cu
W
Pt

Others:

Photoresist

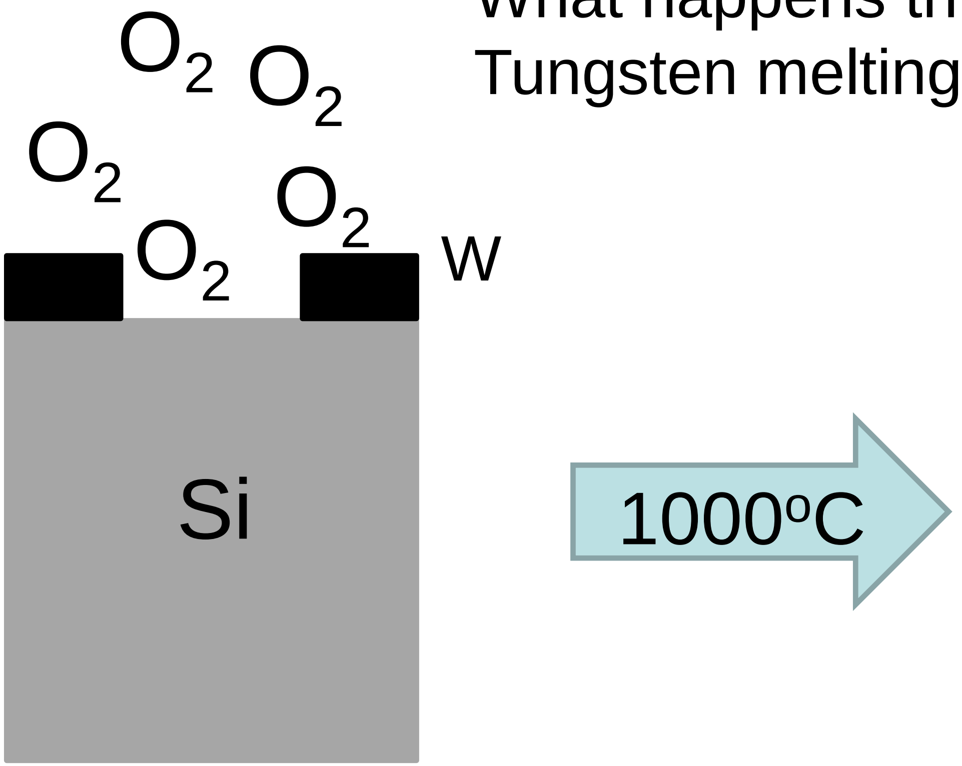
The most important film: SiO_2



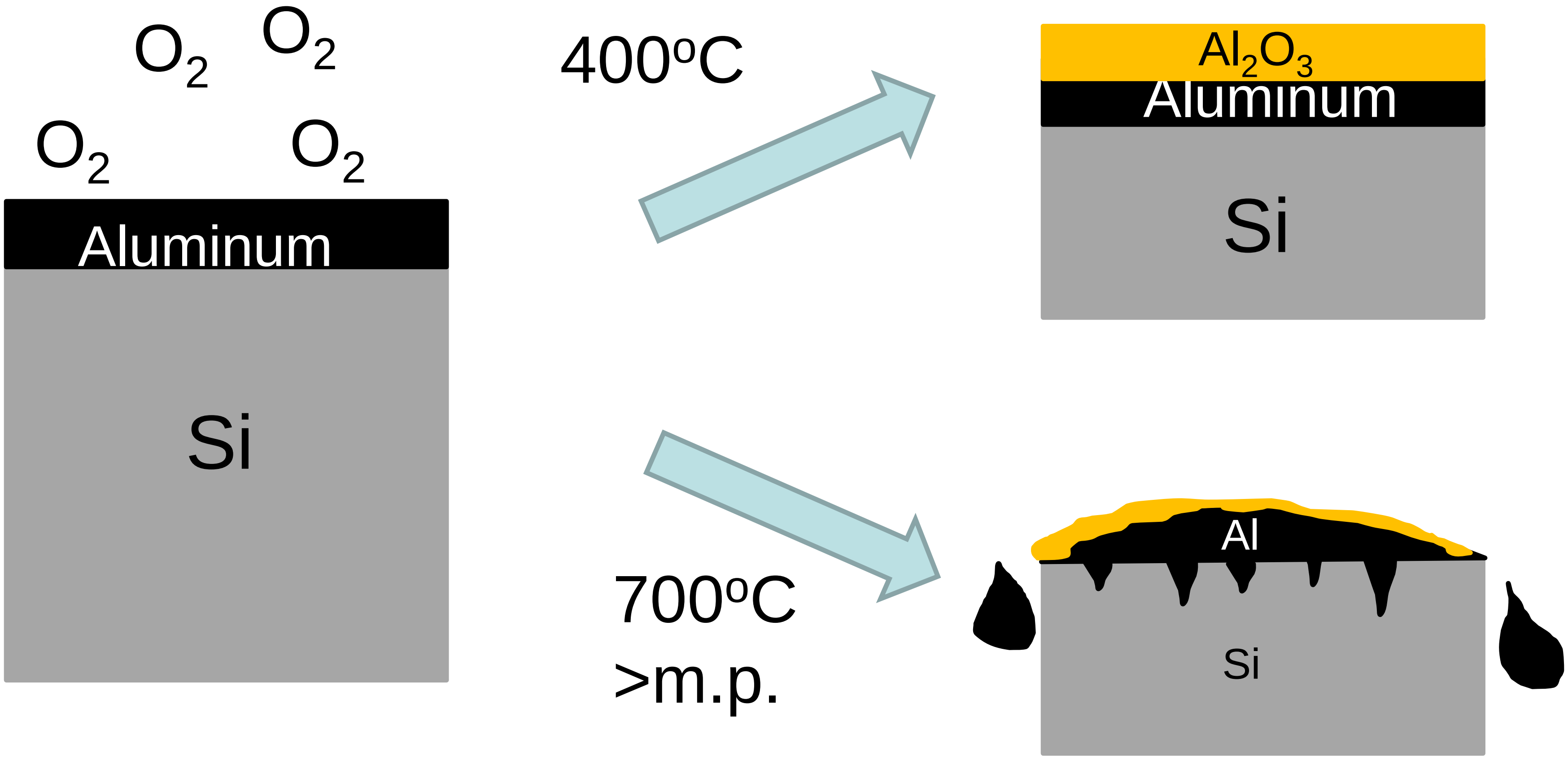
$$Si + O_2 \rightarrow SiO_2$$

Oxygen atmosphere (1)

What happens this structure at 1000^{o}C ?
Tungsten melting point is 3 422°C



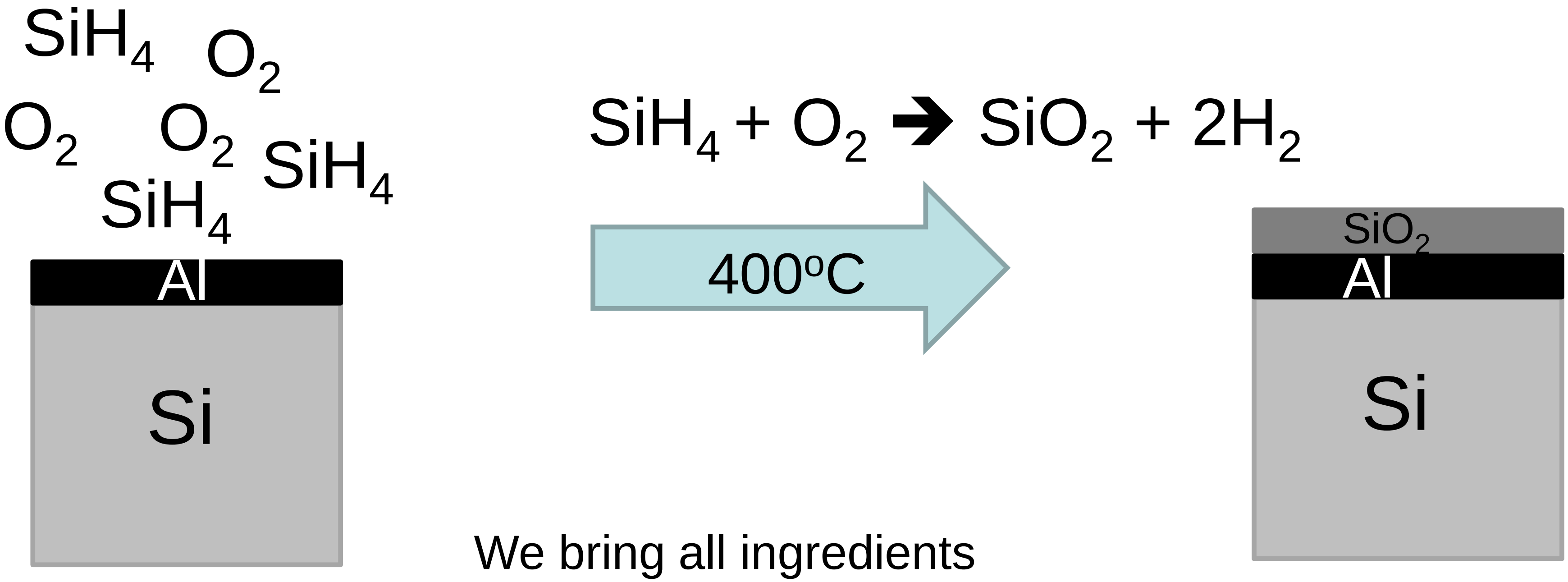
Oxygen atmosphere (2)



400°C

700°C
>m.p.

Solution: CVD
Chemical Vapor Deposition



$SiH_4 + O_2 \rightarrow SiO_2 + 2H_2$

We bring all ingredients needed in gas phase, and no material on the wafer is consumed.

Insulator films

SiO_2

Si_3N_4

Al_2O_3

HfO_2

Thicknesses range from ~1 nm to 1 µm

By Chemical Vapor Deposition (CVD)

Or Atomic Layer Depostion (ALD)

Metallic films

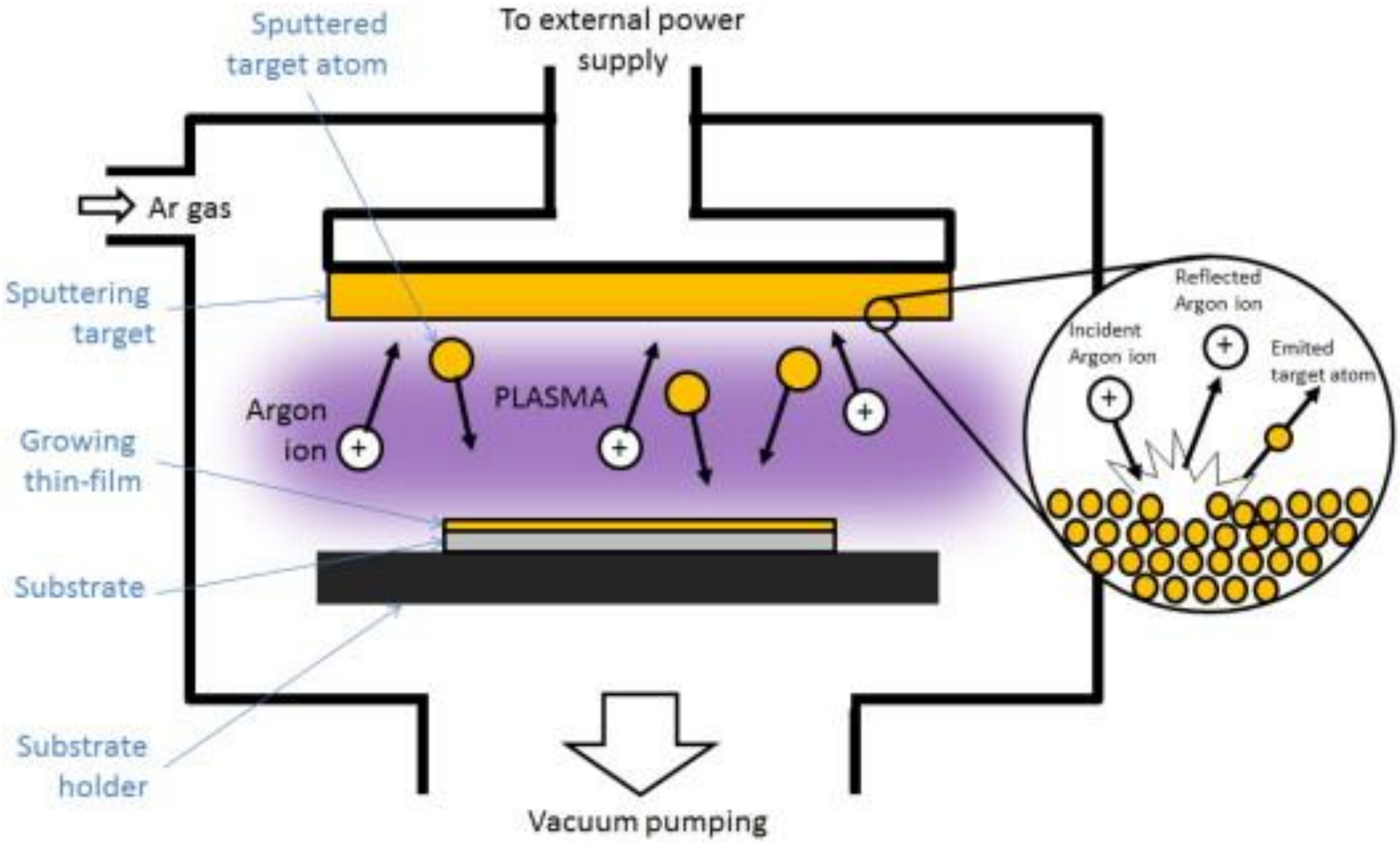
conductors (Al, Au, Cu):
low resistivity

resistors (Ta, W, Pt, Si)
high and stable resistivity

capacitor electrodes (poly-Si, Al, Mo)
good interface against the dielectric

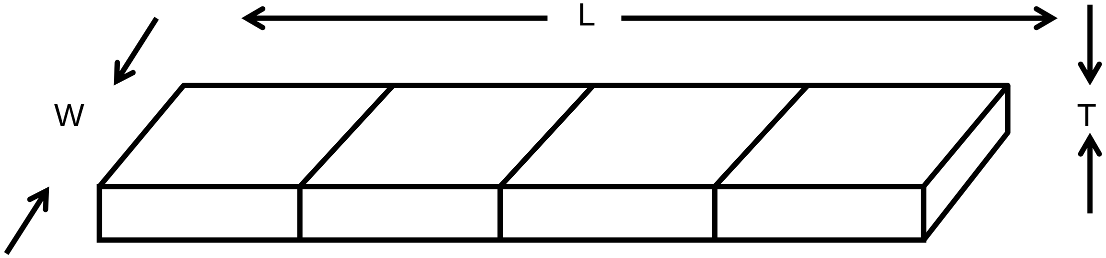
other uses:
mirrors, protective coatings, catalysts,…

Sputter deposition: most generic method for metal films



Resistor design, homework

$$R = \rho \frac{L}{WT}$$



How to change resistor resistance ?

1. Change L: vary its length
2. Change W: vary its width

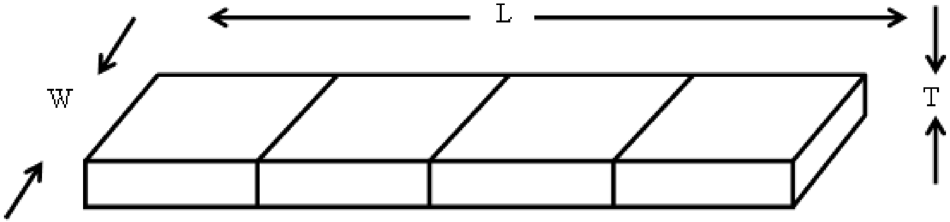
} Easy to vary on wafer

3. Change T: vary its thickness
4. Change ρ: try another material

} Everything on wafer is identical

Sheet resistance

$$R_s \equiv \rho / T$$



R_s is in units of Ohm, but it is usually denoted by Ohm/square to emphasize the concept of sheet resistance.

R_s is useful because it is direct measurement.

Resistance of a conductor line can now be easily calculated by breaking down the conductor into n squares: $R = nR_s$

Patterning: lithography and etching

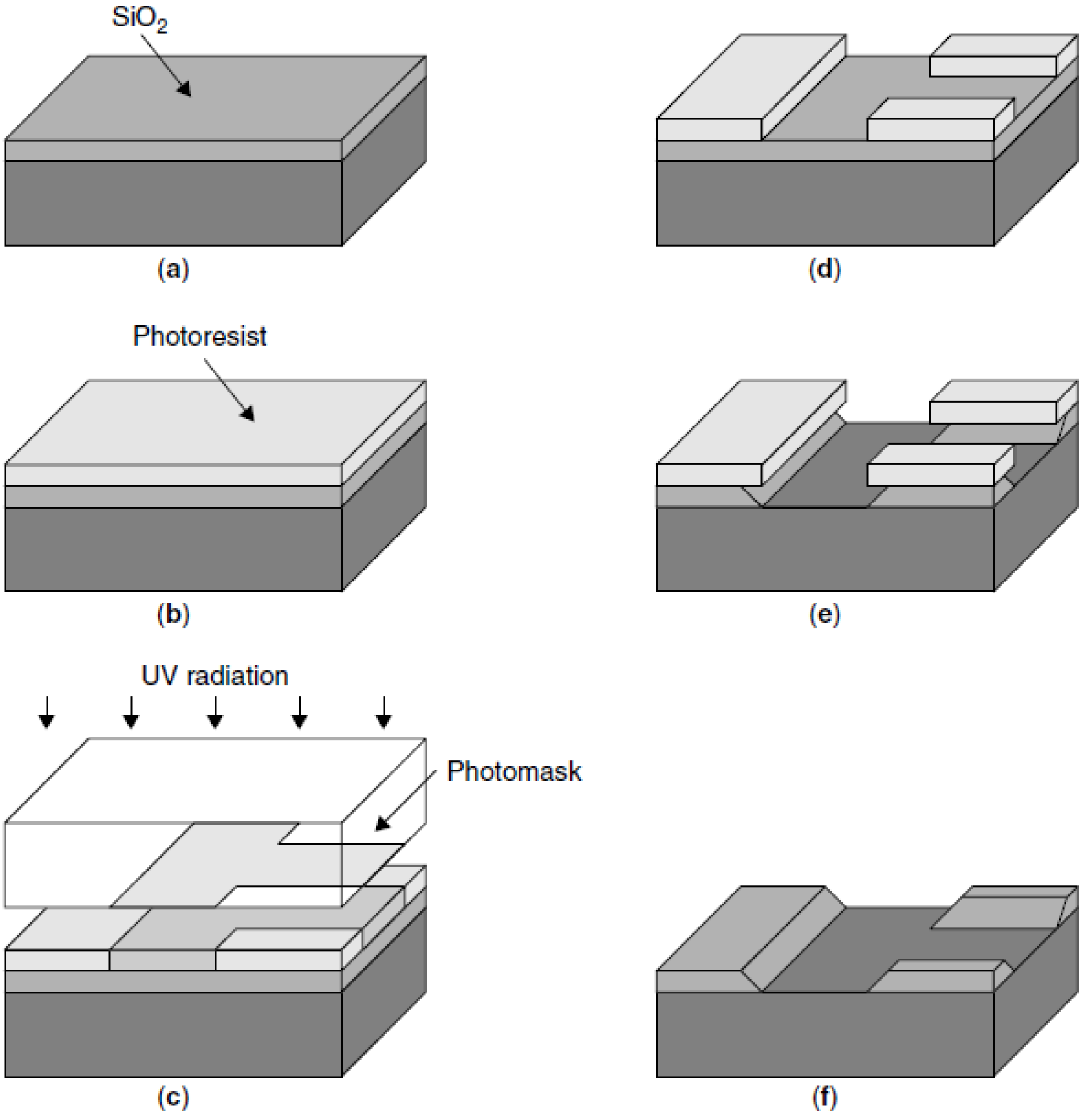
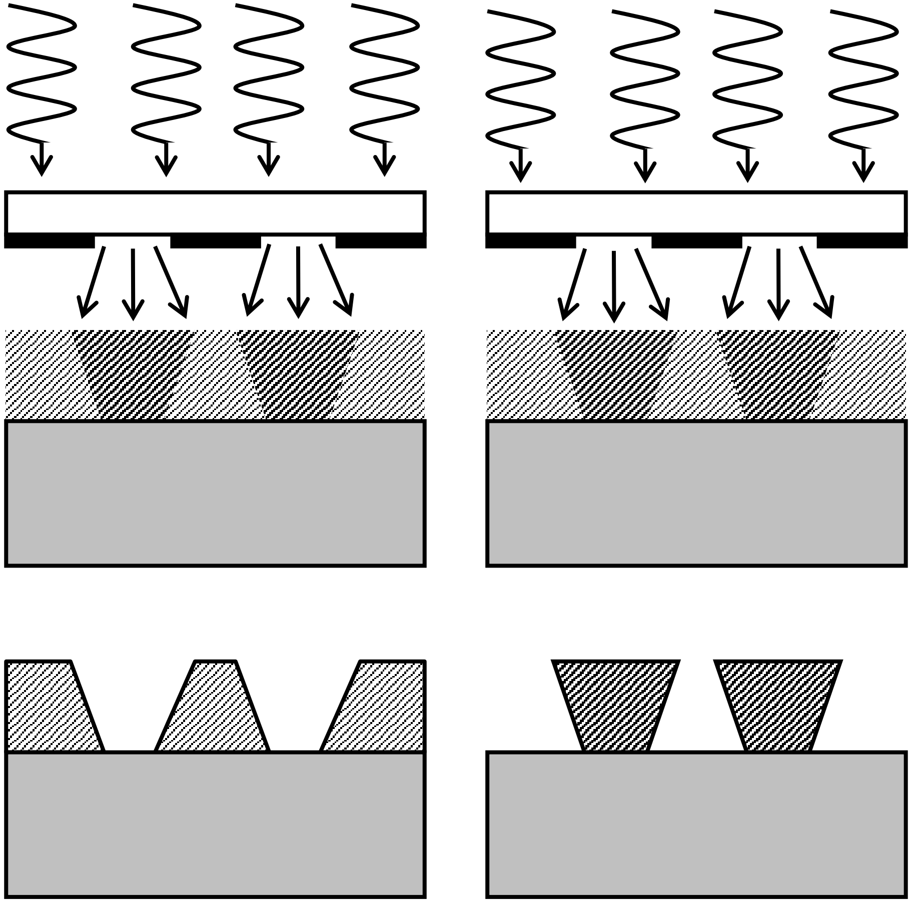


Fig. 9.1

Photoresist exposure



UV light

photomask

photoresist

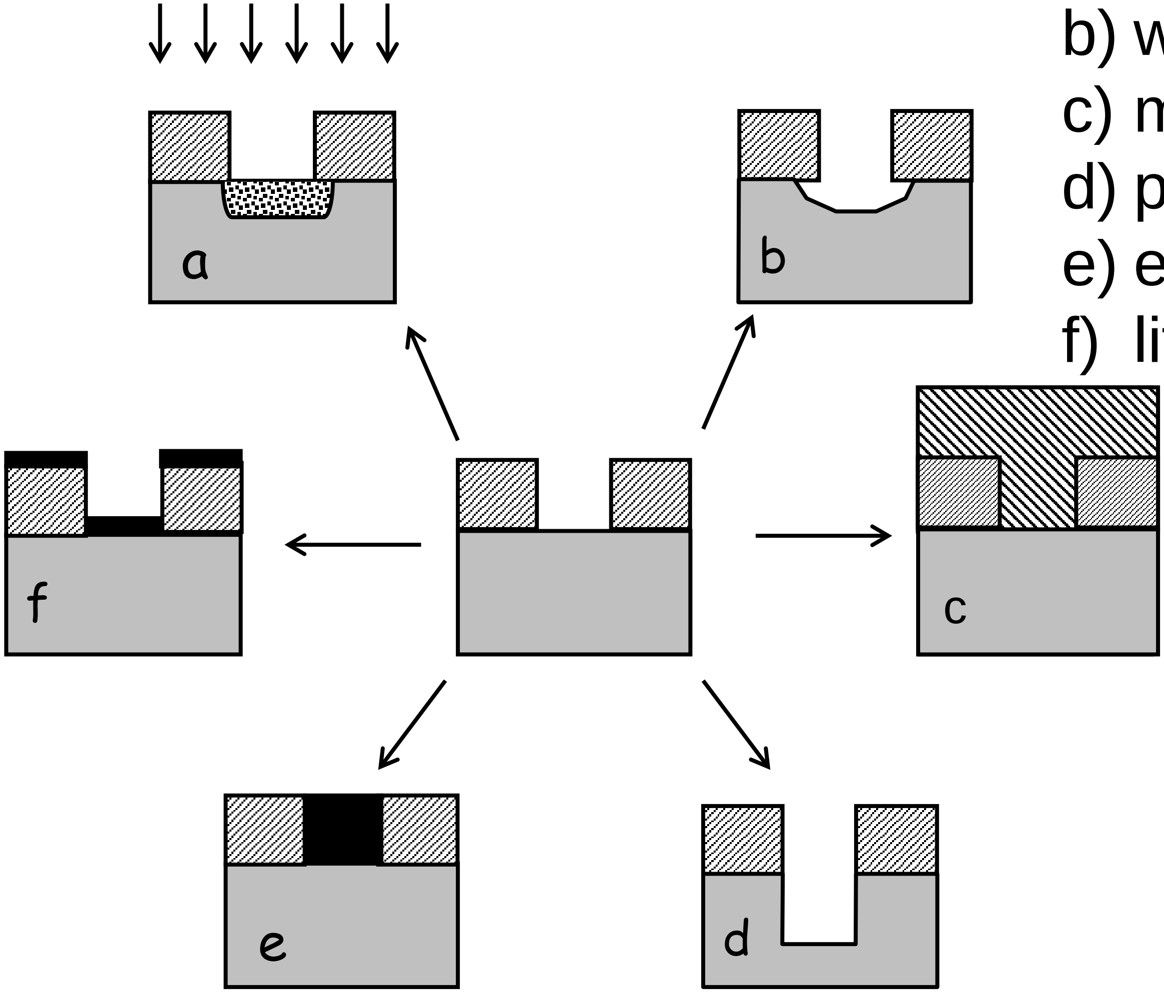
silicon wafer

Positive resist: exposed parts become soluble

Negative resist: exposed parts cross-linked and insoluble

Fig. 9.10

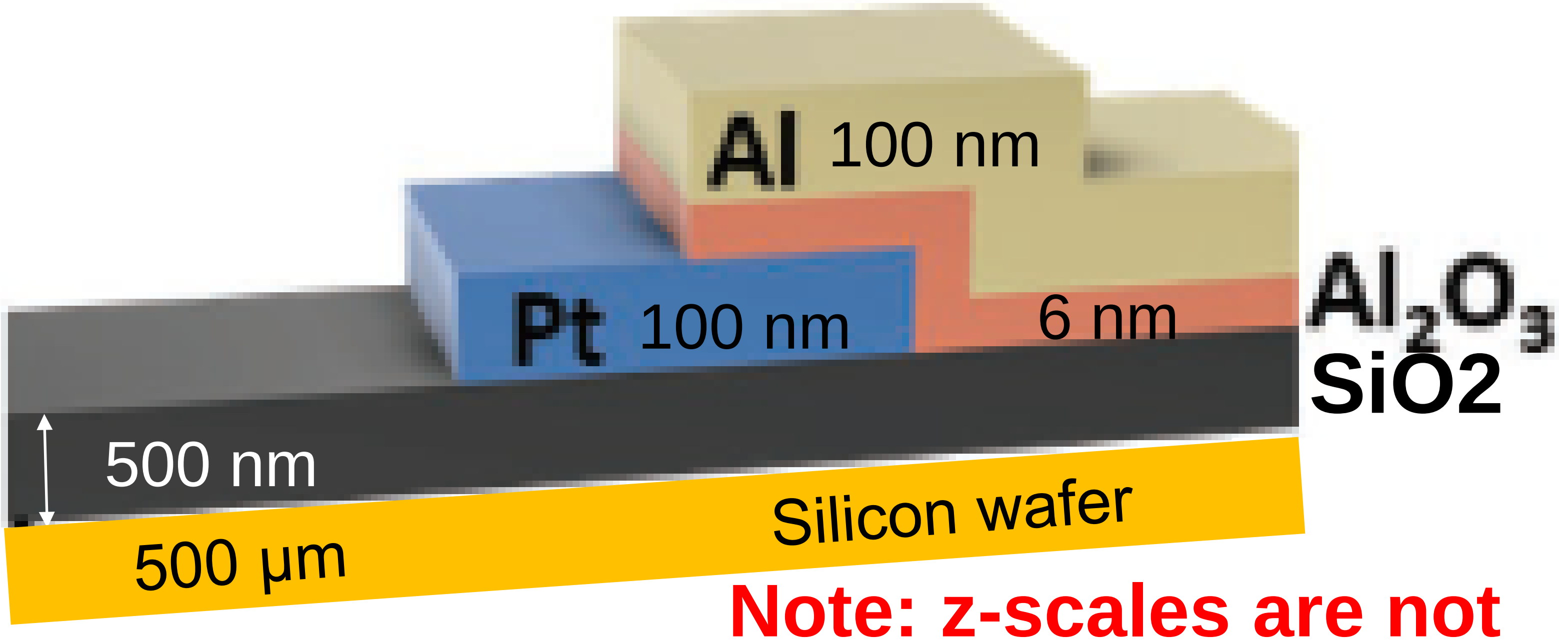
After lithography



a) ion implantation (Ch 15)
b) wet etching (Ch 11)
c) moulding (Ch 18)
d) plasma etching (Ch 11)
e) electroplating (Ch 29)
f) lift-off (Ch 23)

Fig. 9.14

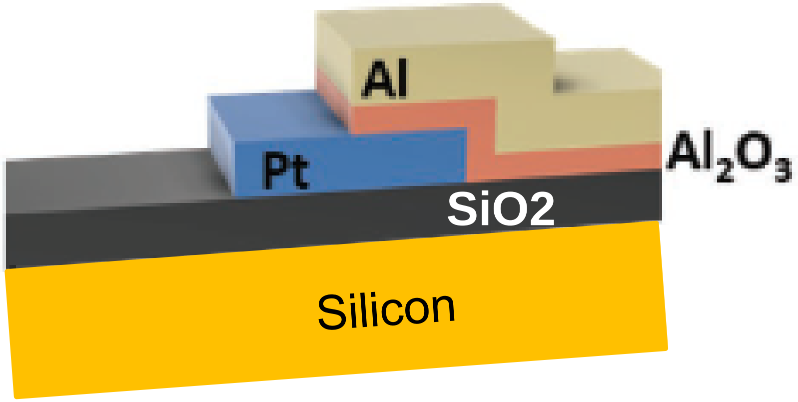
Quantum-Tunneling Metal-Insulator-Metal Diodes



Note: z-scales are not drawn to scale (practically never !!)

Abdullah H. Alshehri et al:Advanced Functional Materials 2019

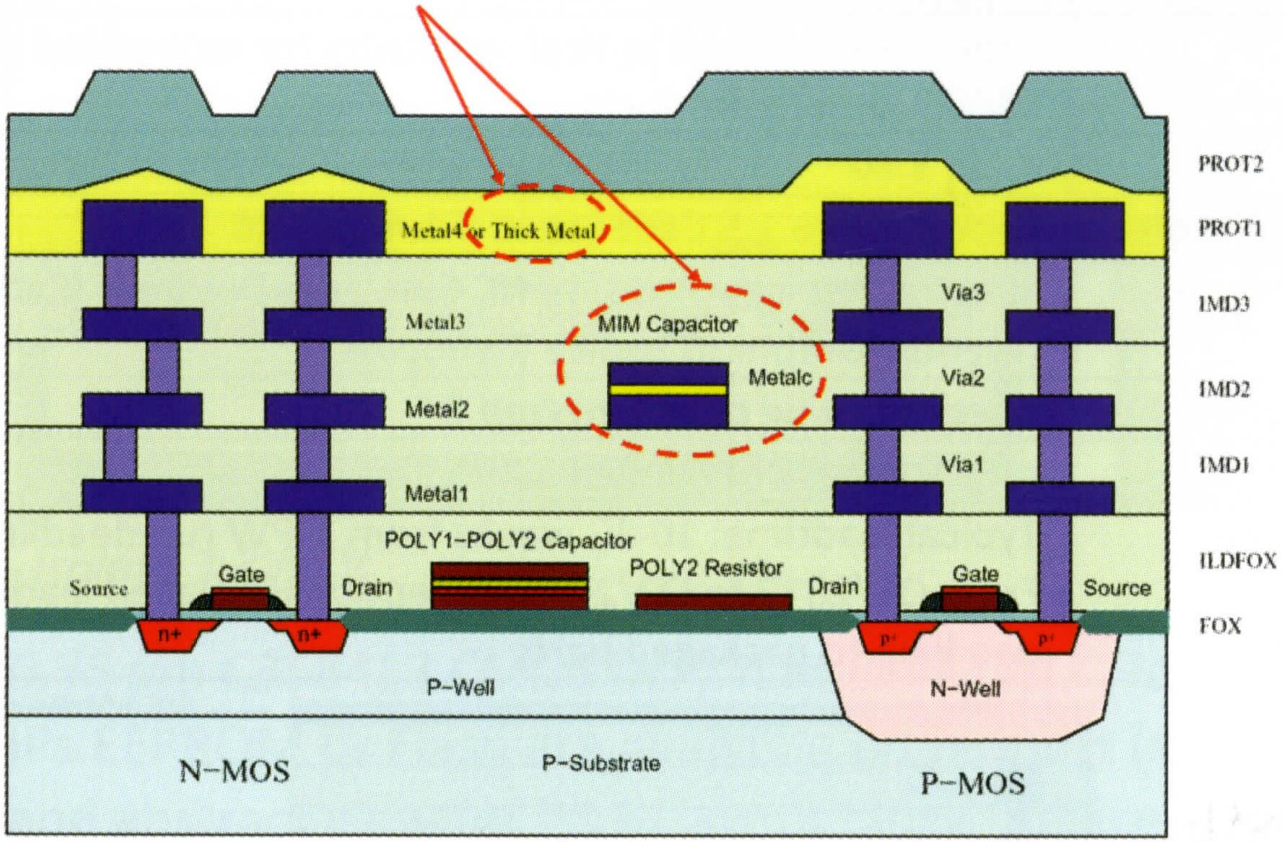
Diode process flow



1. Thermal oxidation SiO_2
2. Pt deposition
3. Lithography
4. Pt etching aqua regia
5. Resist strip
6. Al_2O_3 deposition by ALD
7. Al deposition
8. Lithography
9. Al and Al_2O_3 etching
10. Resist strip

IC multilevel metallization

Thick Metal and MIM available in C35B4M3



CMOS RF Process cross section

CMP Grenoble

Silicon wafers

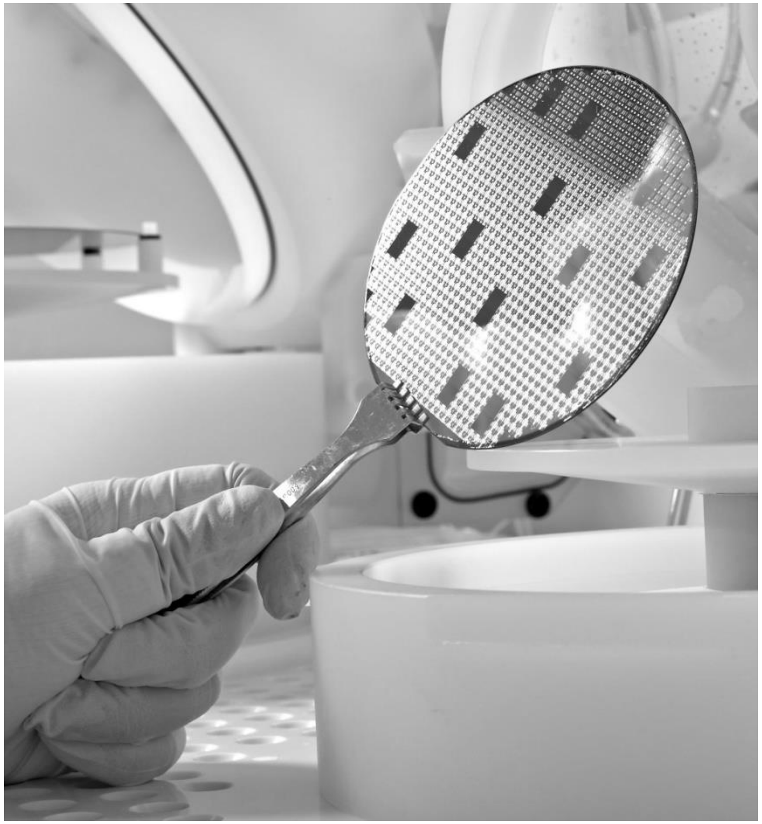


Fig. 1.4: 100 mm diameter silicon wafer

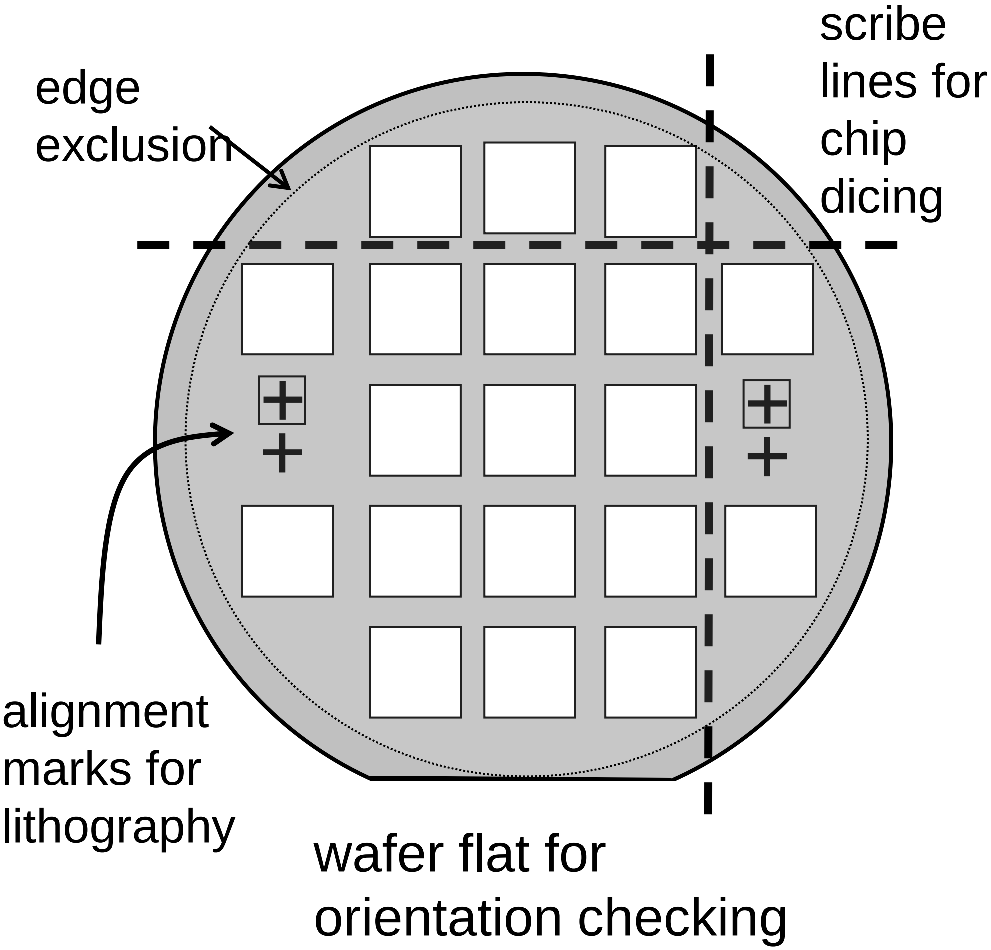


Fig. 1.20 Real estate allocation on a wafer

Silicon strengths

- silicon is a good mechanical material
- silicon is good thermal conductor
- silicon is transparent in infrared
- silicon is a semiconductor
- silicon is optically smooth and flat
- silicon is known inside out

➔ consider silicon first, alternatives then

Single crystalline silicon (a.k.a. monocrystalline)

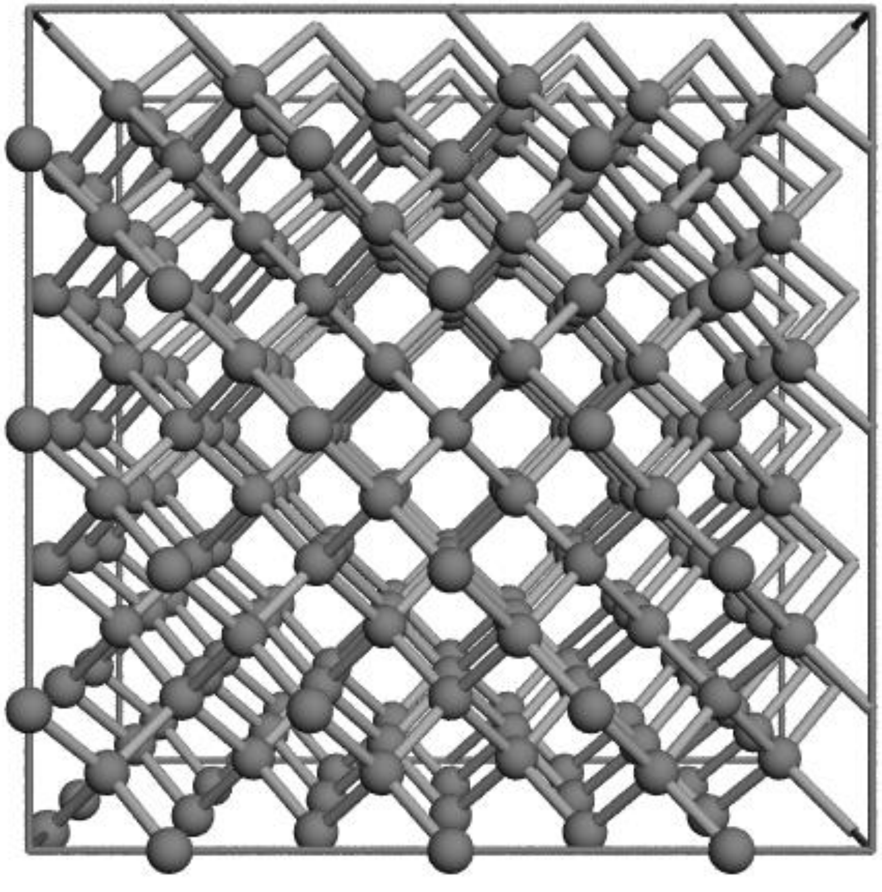


Fig. 4.6

<100>
silicon

Real silicon wafers

Almost perfect, but ***ALWAYS*** contain:

-dopants (B, P, at least 1 dopant atom per billion silicon atoms ≈ $5*10^{13}$ cm^{-3}/$5*10^{22}$ cm^{-3})

-oxygen from silica crucible (15 pmma)

-carbon from graphite heaters (1 ppma)

-impurities (C, Fe, Zn, … e.g. 10^{10} cm^{-3}, or ppta)

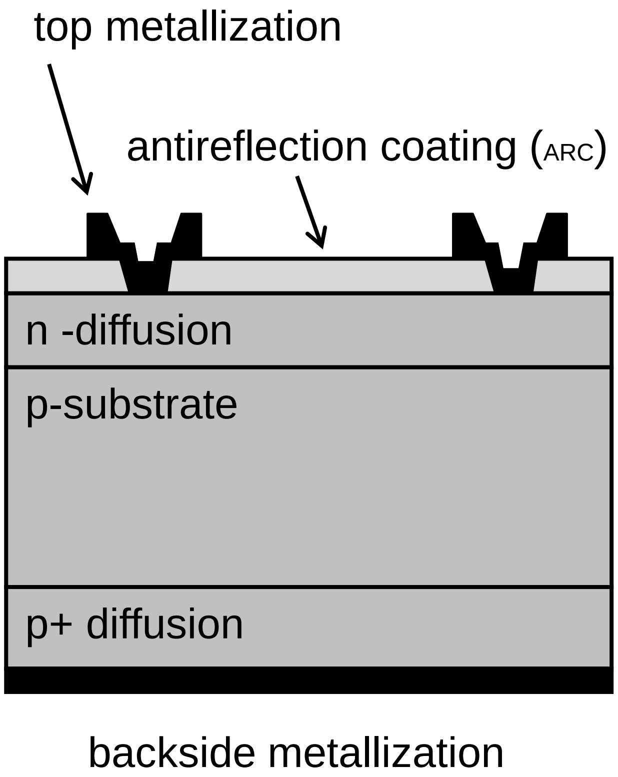
-defects (voids, dislocations, precipitates,…)

-intentional dopants, B, P typically 10^{15}-10^{18} cm^{-3}

Videos

- Doping: if you need to refresh your memory about semiconductors and doping, this video is useful:
- https://www.youtube.com/watch?v=k12GMjtN8aA

Doping



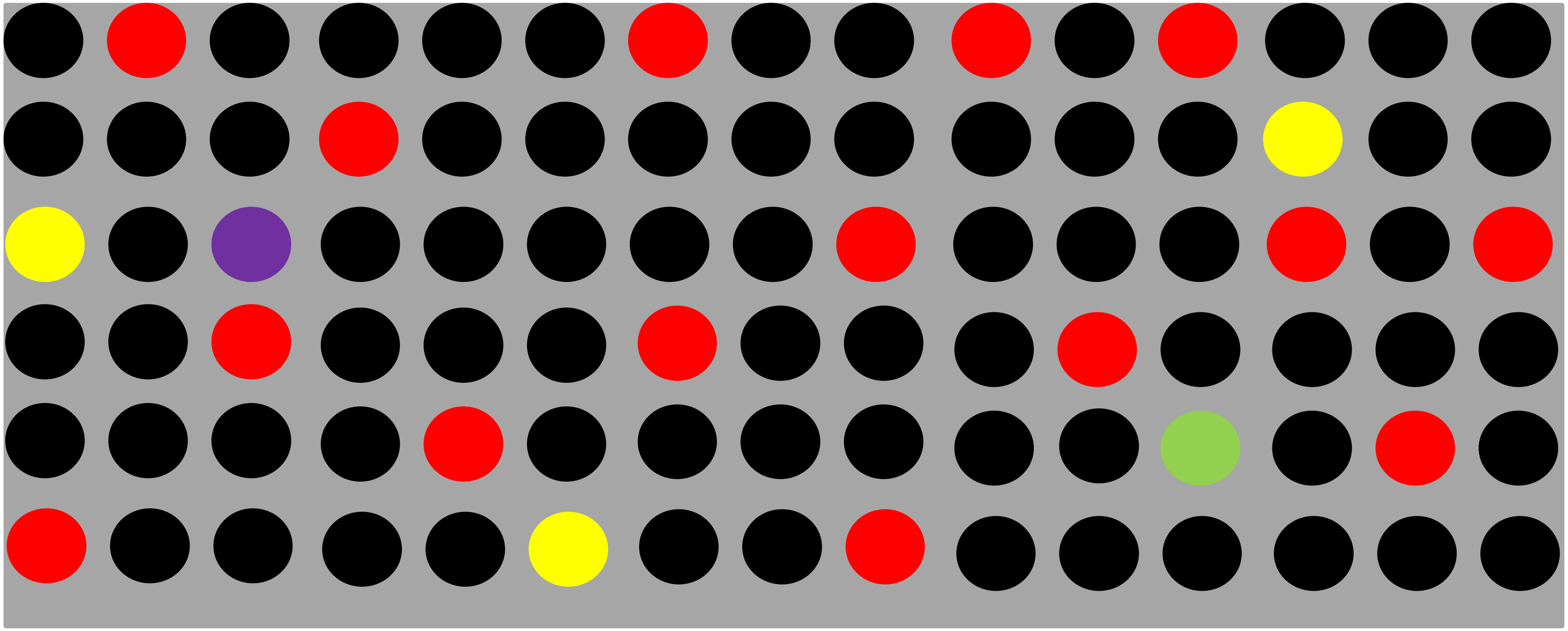
n-diffusion (e.g. 10^{16} cm^{-3} phosphorous)

p-substrate (e.g. 10^{15} cm^{-3} boron)

p+ diffusion (e.g. 10^{18} cm^{-3} boron)

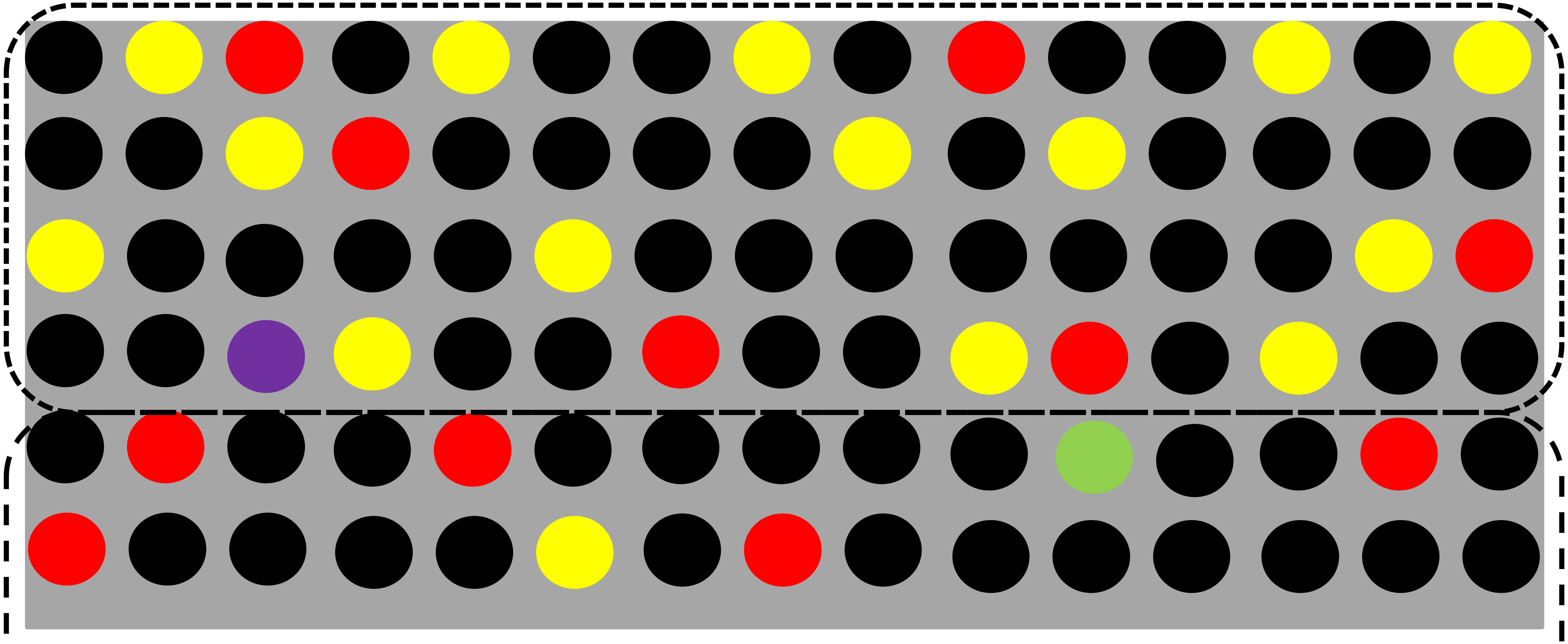
Fig. 25.2

Silicon substrate ⚫
(p-type with boron 🔴 majority)



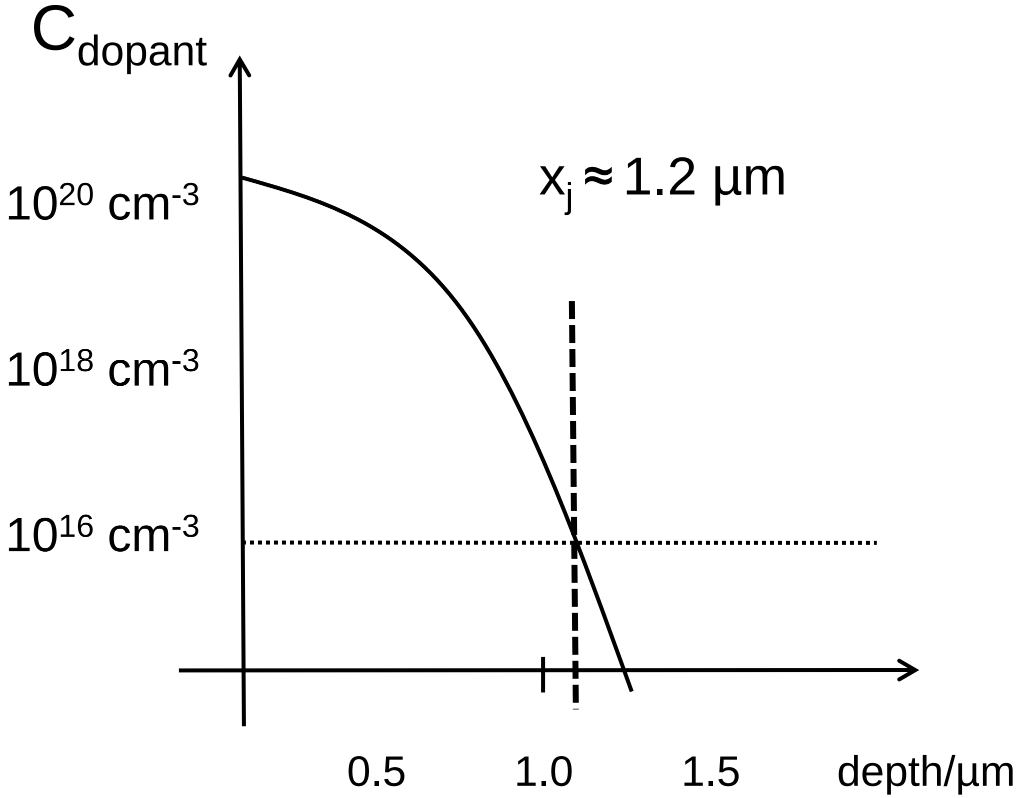
🔴 boron 🟡 phosporous 🟣 🟢 Impurities (e.g. Fe, Cu)

Phosphorous ● diffusion➔ top layer turned into n-type



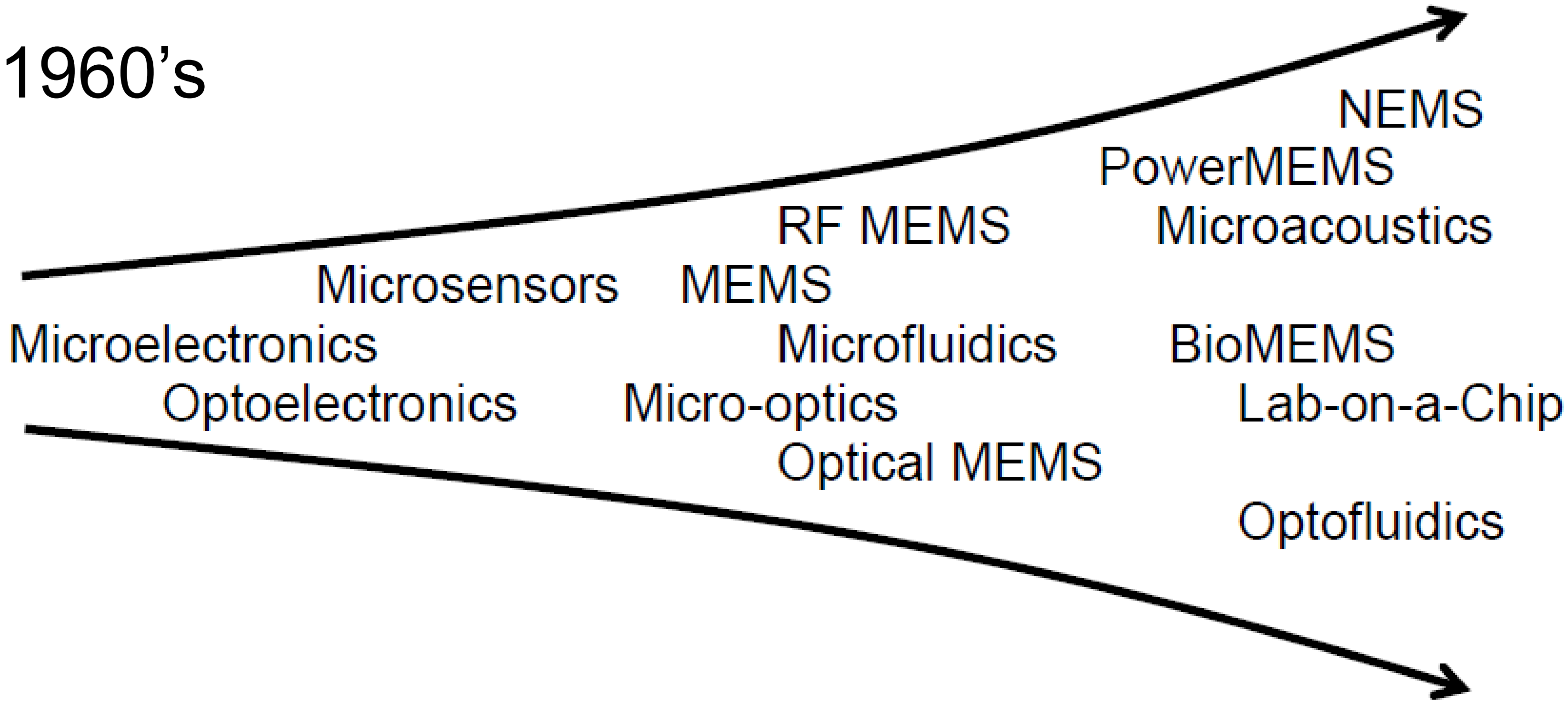
Bulk of the wafer remains p-type,
because diffusion does not extent to depth of wafer.

Junction depth x_j



X_j is the depth where diffused dopant concentration equals wafer dopant concentration (of opposite type).

Microtechnology evolution



1960’s

NEMS

PowerMEMS

RF MEMS

Microacoustics

Microsensors

MEMS

Microelectronics

Microfluidics

BioMEMS

Optoelectronics

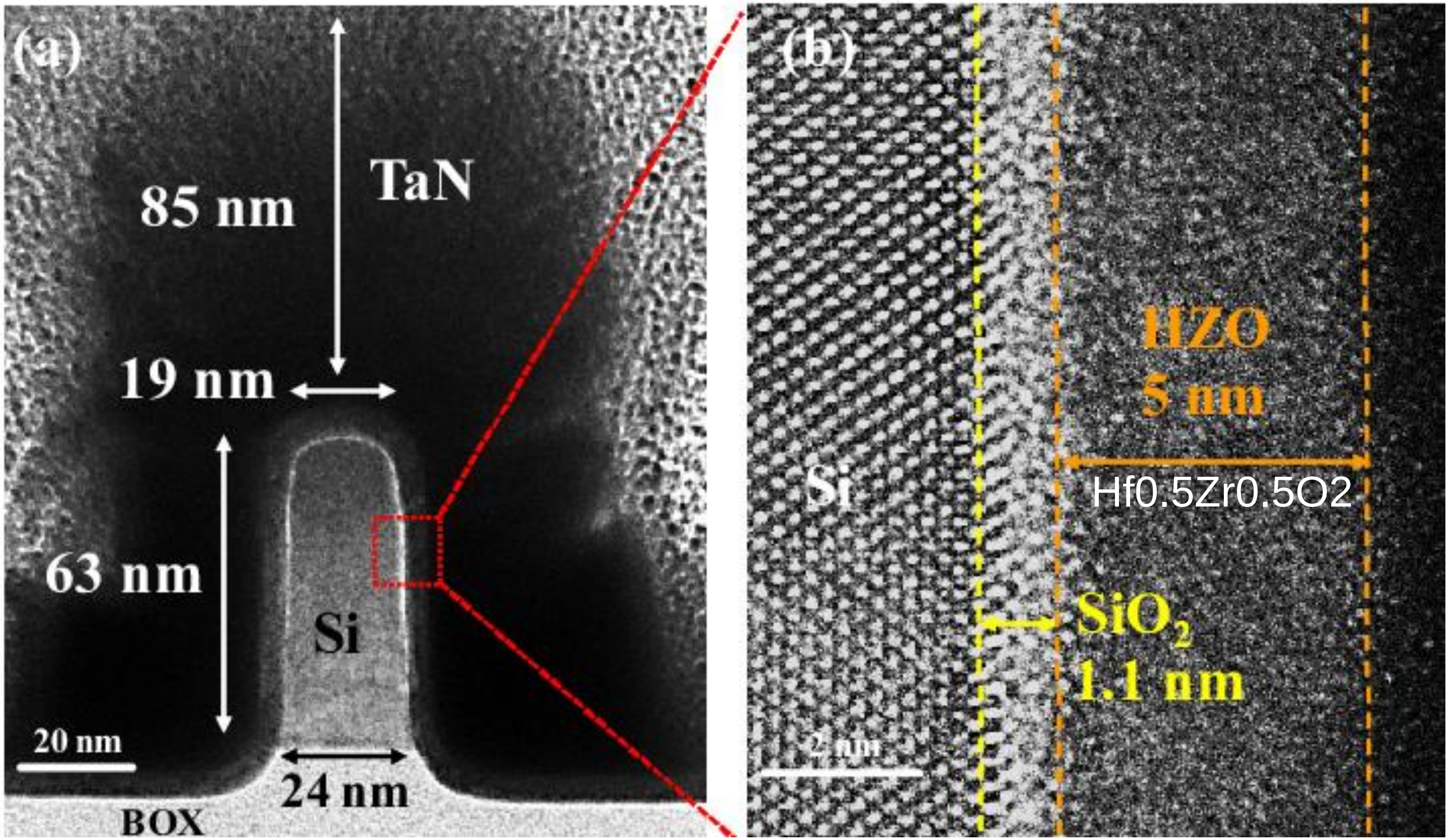
Micro-optics

Lab-on-a-Chip

Optical MEMS

Optofluidics

Silicon FinFET



M. -J. Tsai *et al.*, *IEEE Journal of the Electron Devices Society*, vol. 7, pp. 1033-1037, 2019, doi: 10.1109/JEDS.2019.2942381.

Optoelectronics

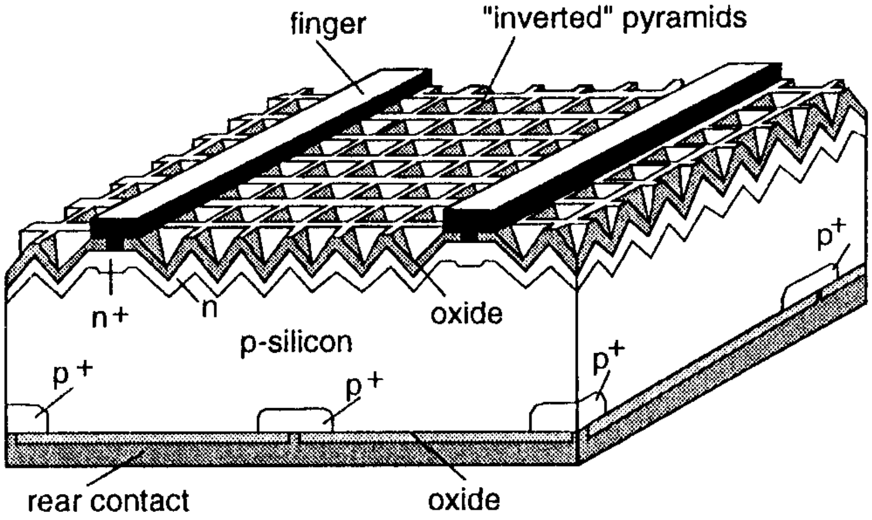


Fig. 1.14: Silicon solar cell

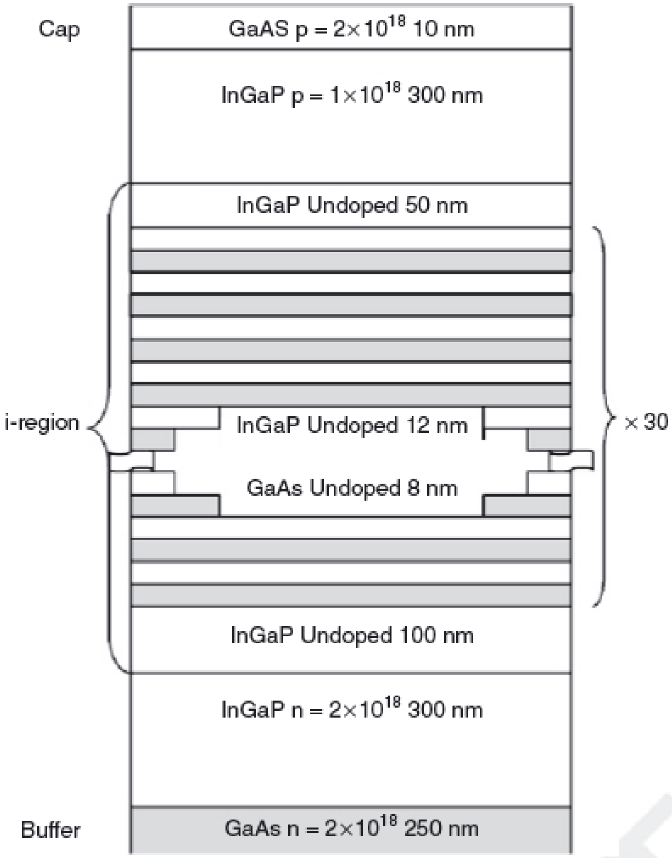


Fig. 6.2: GaAs multiple quantum well solar cell

MEMS: Micro Electro Mechanical Systems

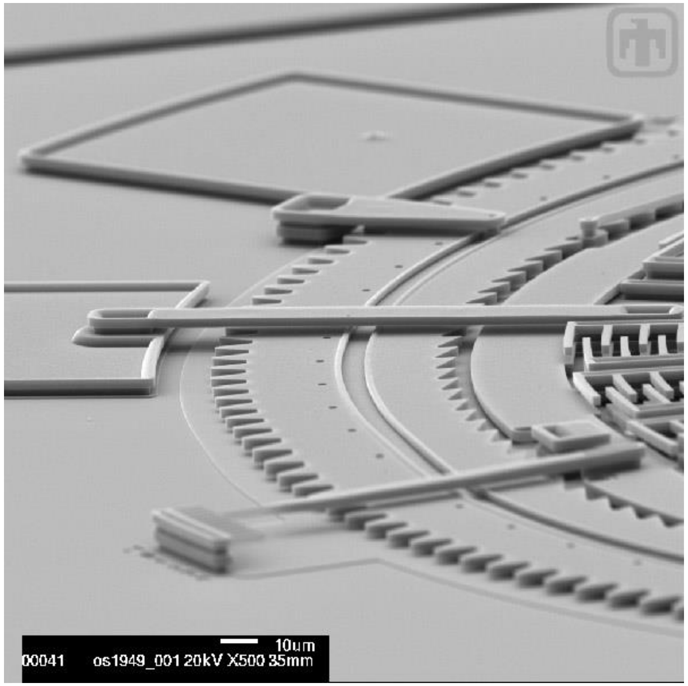


Fig. 29.21: Microgears, courtesy Sandia National Labs.

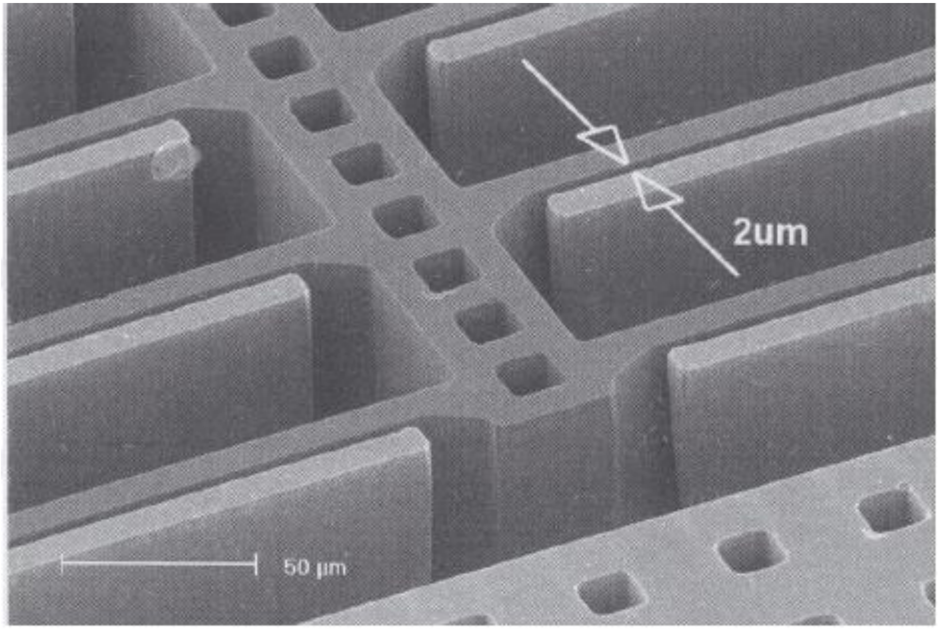
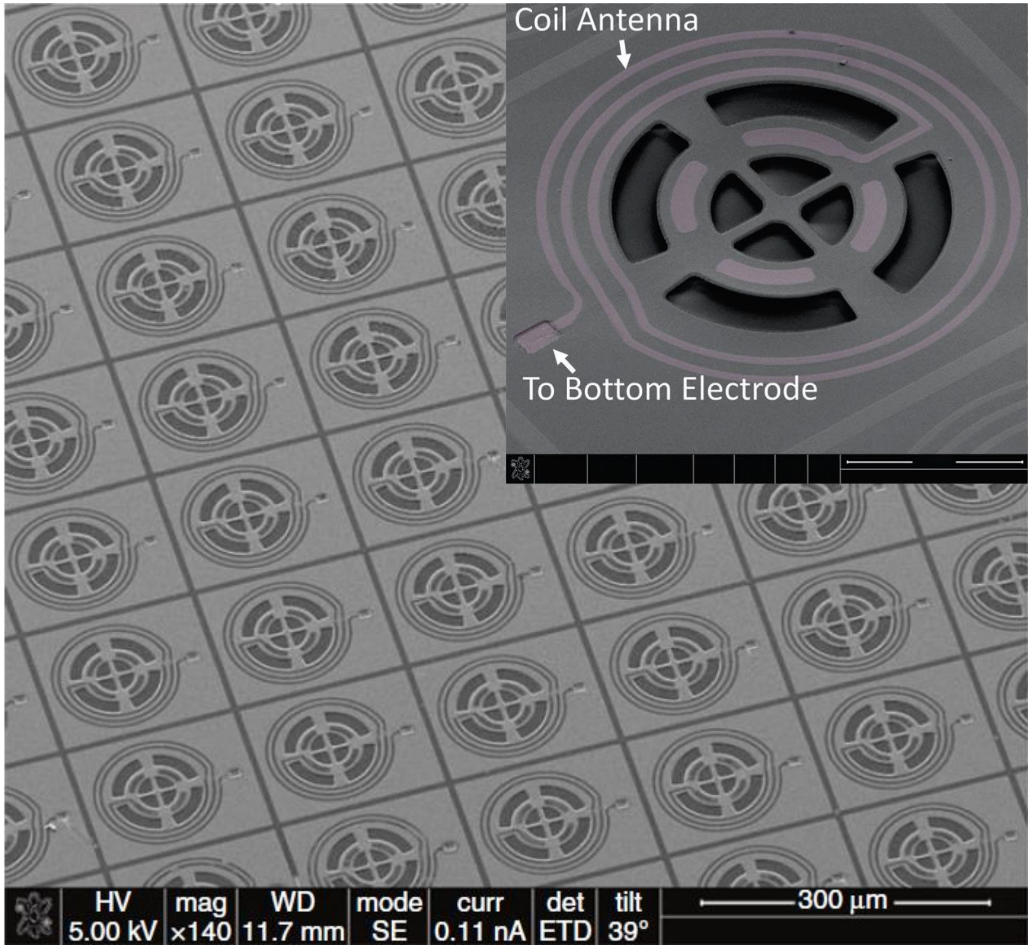


Fig. 21.3: comb-drive actuator

Clandestine NEMS tags.



"Tags exploit the electromechanical spectral signature as a fingerprint that is characterized by inherent randomness in fabrication processing."

Rassay et al. Microsystems & Nanoengineering (2020) 6:103

Power MEMS

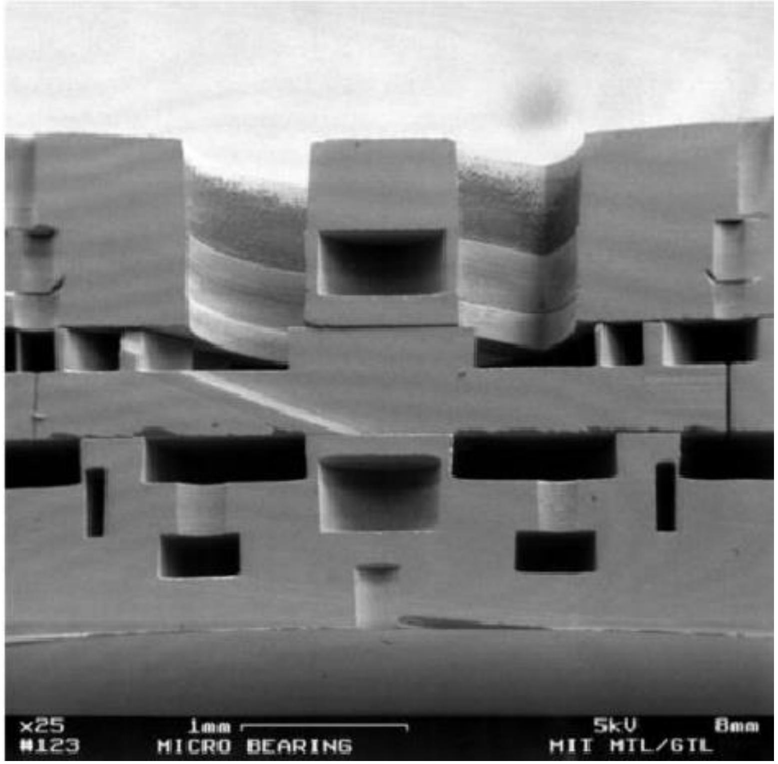


Fig. 1.17: Microturbine

Fabricated by bonding together 5 silicon wafers.

MOEMS (Micro Opto Electro Mechanical Systems)

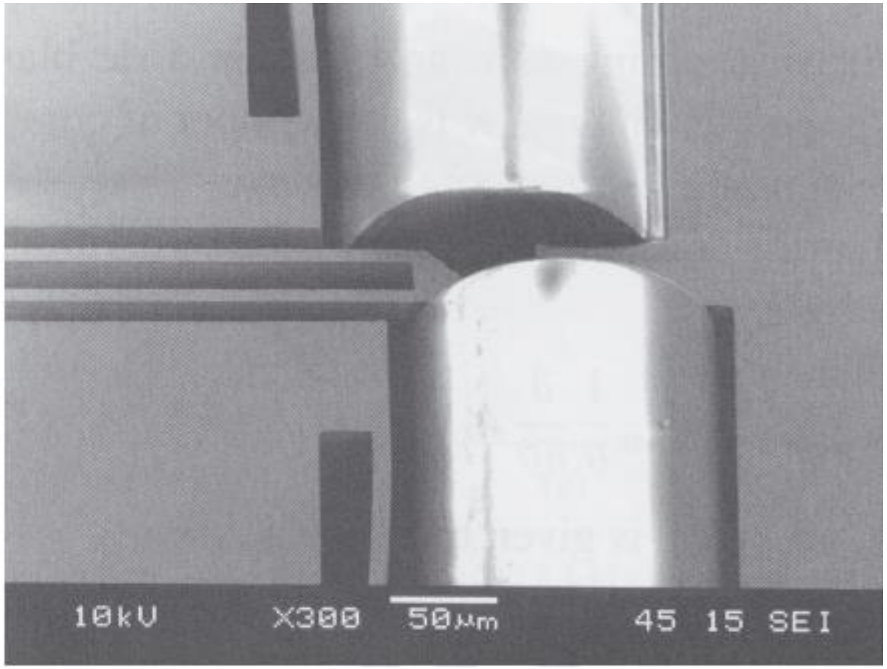


Fig. 21.4: variable optical attenator

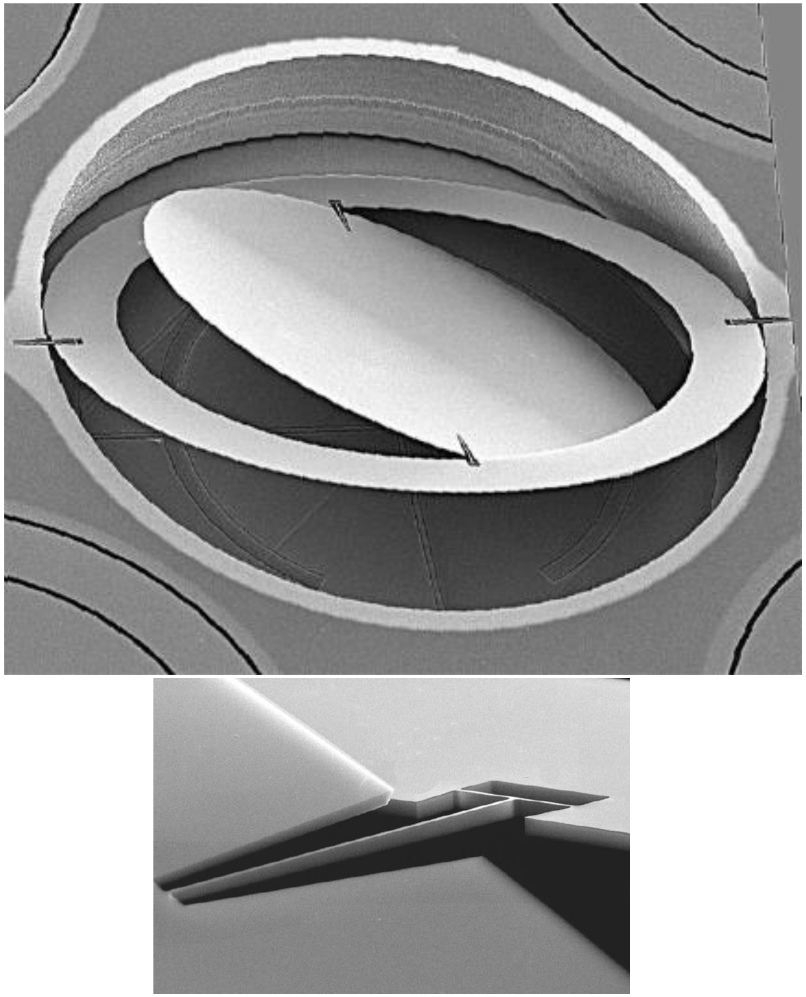


Fig. 1.2: Micromirror made of silicon, 1 mm diameter, supported by 1.2 µm wide, 4 µm thick torsion bars

Micro-optics

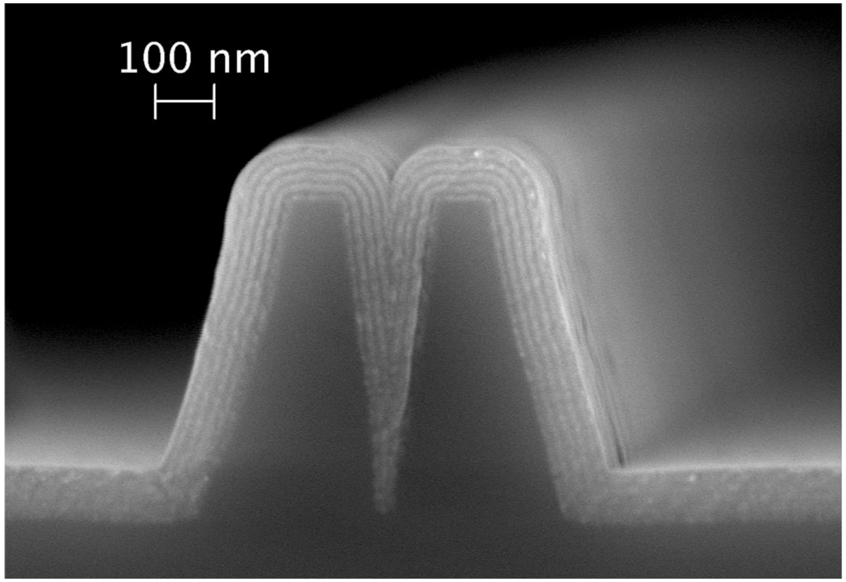


Fig. 1.7: Aluminum oxide and titanium oxide thin films deposited over silicon waveguide ridges, courtesy Tapani Alasaarela.

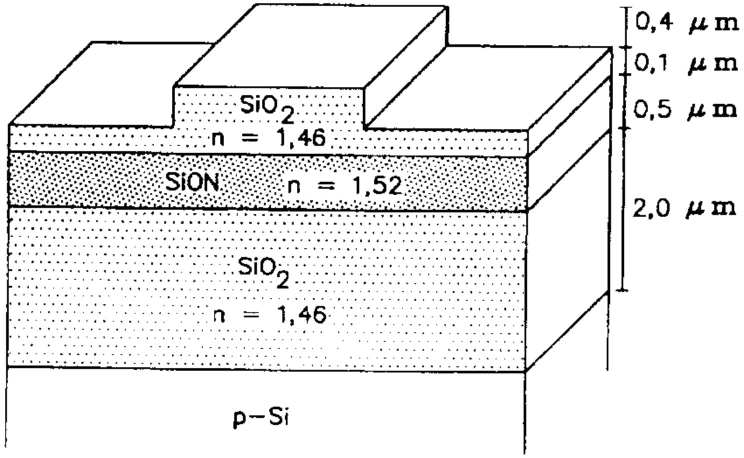


Fig. 7.13: Refractive index $SiO_2/SiO_xN_y/SiO_2$ waveguide: n_f 1.46/1.52/1.46. From ref. Hilleringmann.

Microfluidics and BioMEMS

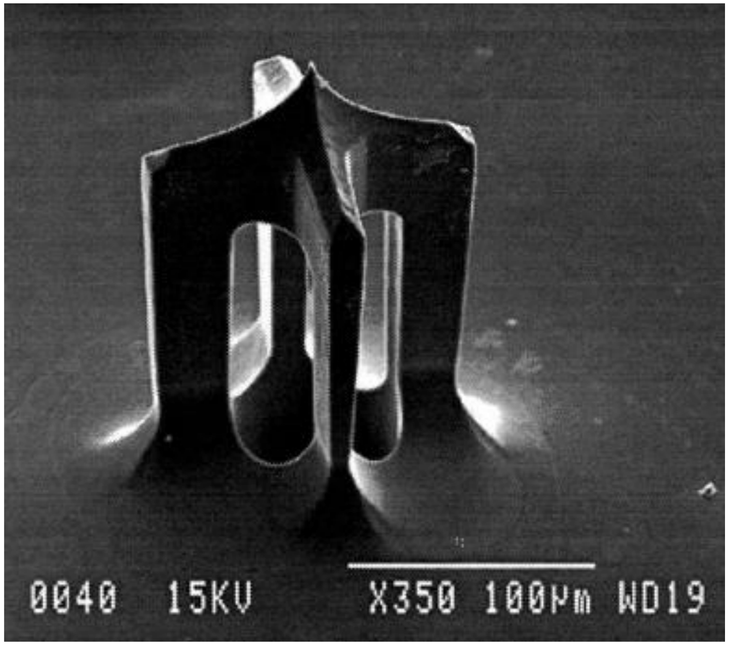


Fig. 1.13: silicon microneedle

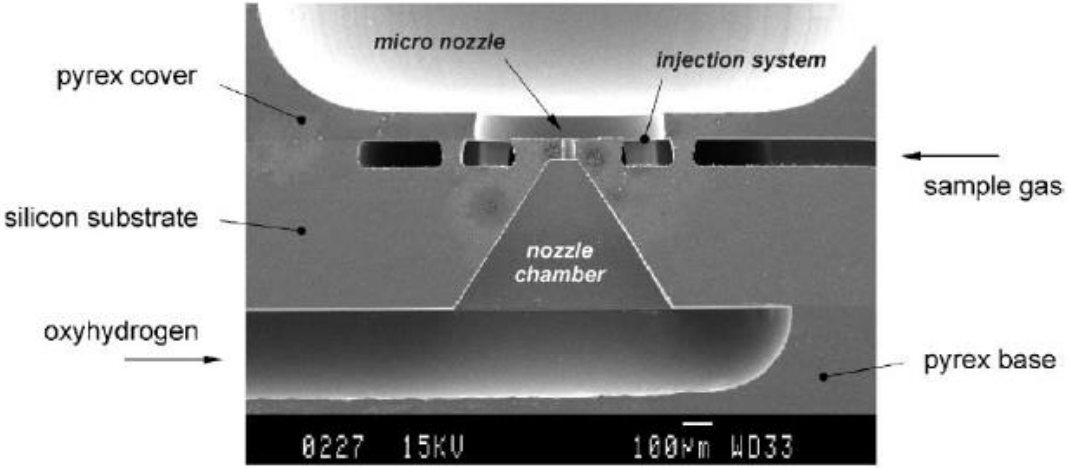


Fig. 1.11: Oxy-hydrogen burner flame ionization detector

Cleanrooms

Fig. 1.19

Yield

$$Y = Y_0^n$$

Yield of a total process (Y) is a product of yield of individual process steps (Y_o)

50 step MEMS process, $Y_0 = 0.999$
➔ $Y = 0.999^{50} = 95\%$

500 step DRAM process, $Y_0 = 0.999$
➔ $Y = 0.999^{500} = 61\%$

Yield (2)

$$Y = e^{-DA}$$

Yield depends on chip area (A) and defect density (D)

D = 0.01 mm^{-2} (= 1/cm^2)

A= 10 mm^2 ➔Y = 90%

A= 100 mm^2 ➔ Y = 37%

Microindustries are big

Integrated circuits	$550 B (2021)
Other semiconductors	$115 B
(of which MEMS/sensors	$24 B)
Flat panels displays	$130 B
Solar cells	$170 B
Hard disks	$35 B
Equipment	$100 B
Materials	$50 B*

Best source: semi.org

* Includes packaging materials, leadframes etc.