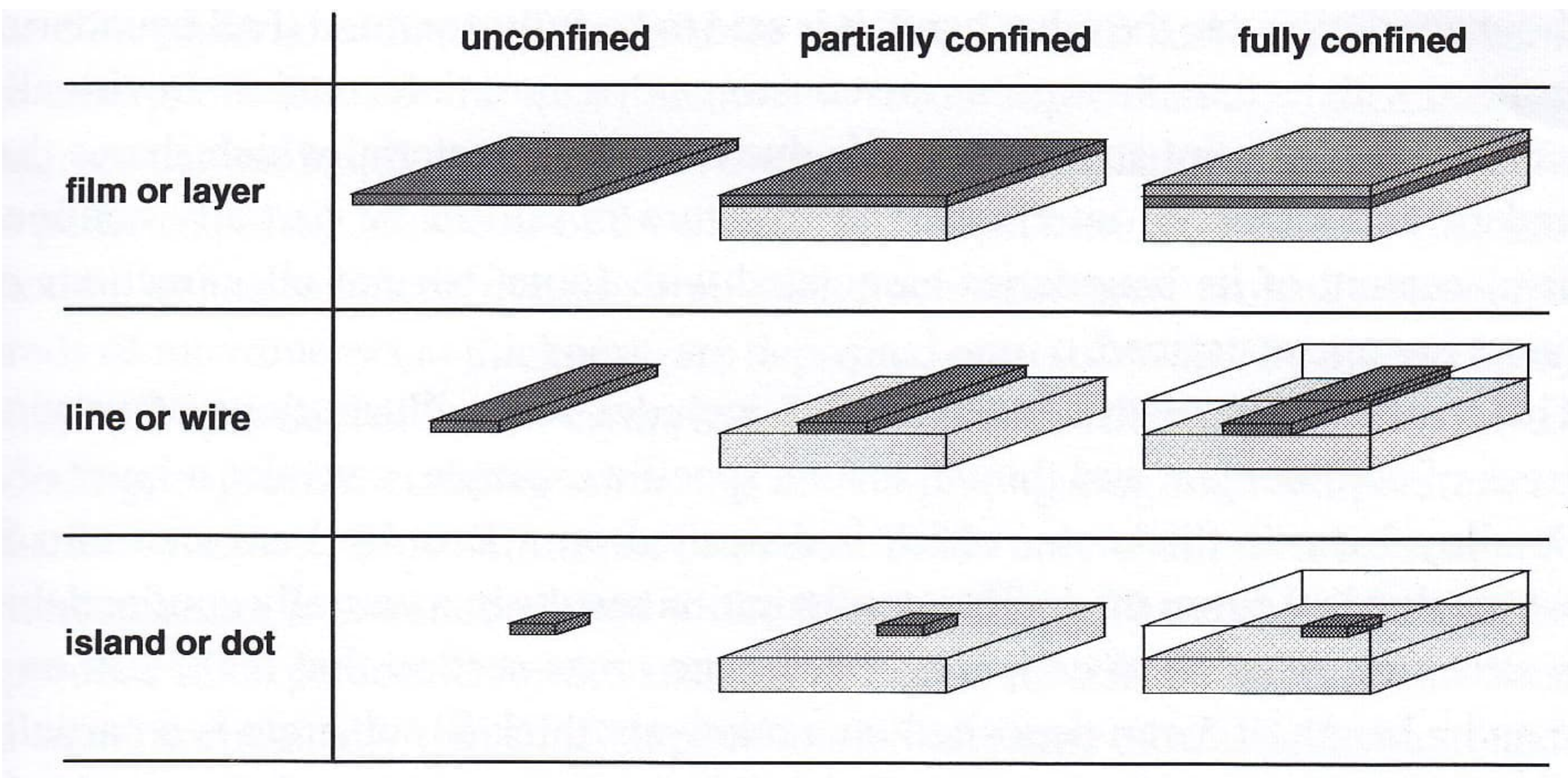
Thin films 2023

sami.franssila@aalto.fi

1D & 2D structures



Freund & Suresh

Generic thin film structure

surface →

interface 2 →

interface 1 →

thin film 2

thin film 1

substrate

Film 2 could be:
Antireflective coating
e.g. SiNx

Film 1 could be:
solar cell active layer, e.g. a-Si

Substrate e.g. glass

Generic thin film structure (2)

surface →

interface 2 →

interface 1 →

thin film 2

thin film 1

substrate

Film 2 could be:
Capacitor top plate,
e.g. molybdenum

Film 1 could be:
Capacitor dielectric,
SiO_2

Silicon substrate
acts as bottom
capacitor plate

Generic thin film structure (3)

surface →

interface 2 →

interface 1 →

thin film 2

thin film 1

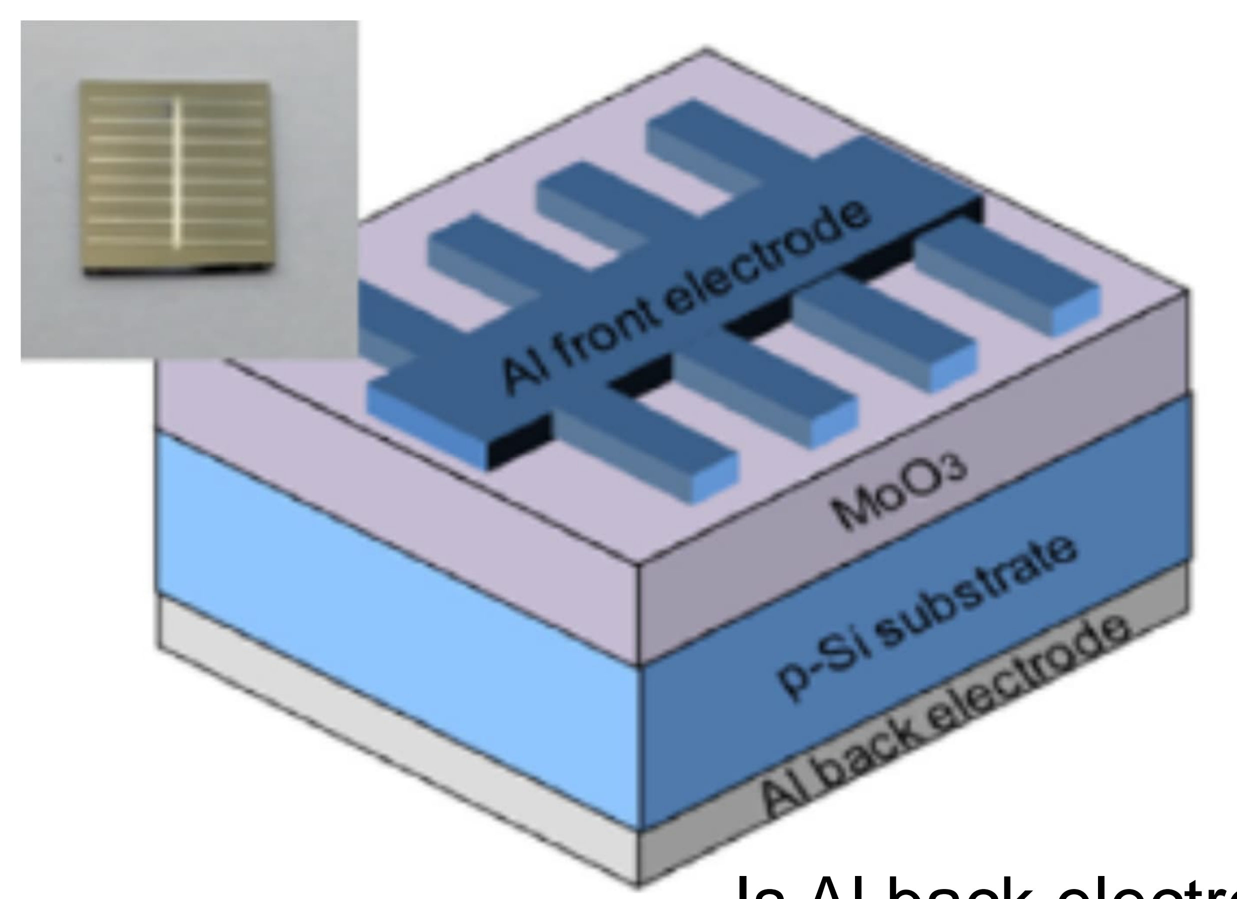
substrate

Film 2 could be cantilever sensor

Film 1 would be sacrificial layer to be etched away to release the cantilever

Substrate anything (which tolerates film 1 & 2 deposition and film 1 etching)

Infrared photodetector



Silicon substrate

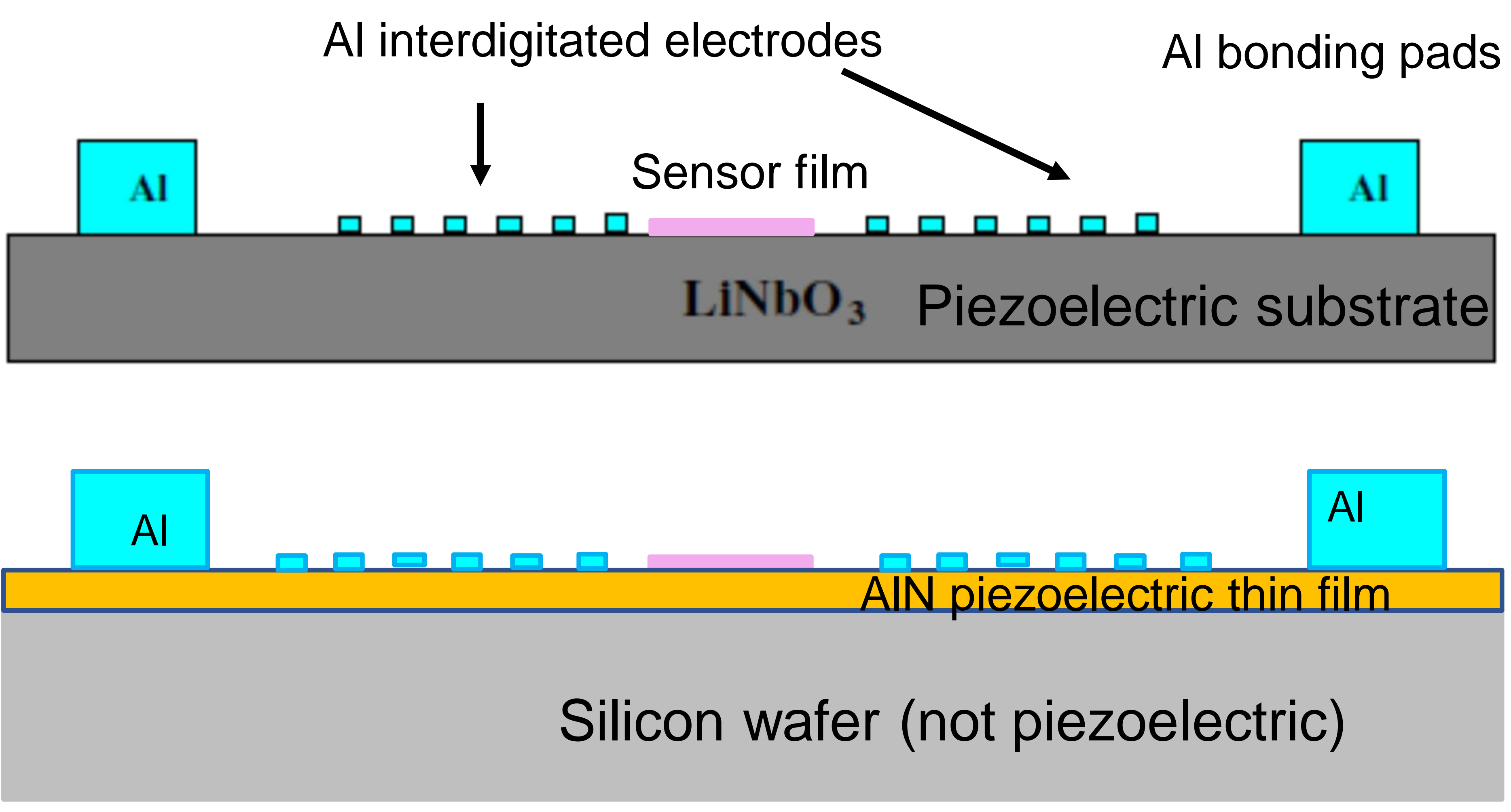
Three thin films
(Al front and Al back
need separate steps)

One lithography step
One etching step

Is Al back electrode
done first or last ?

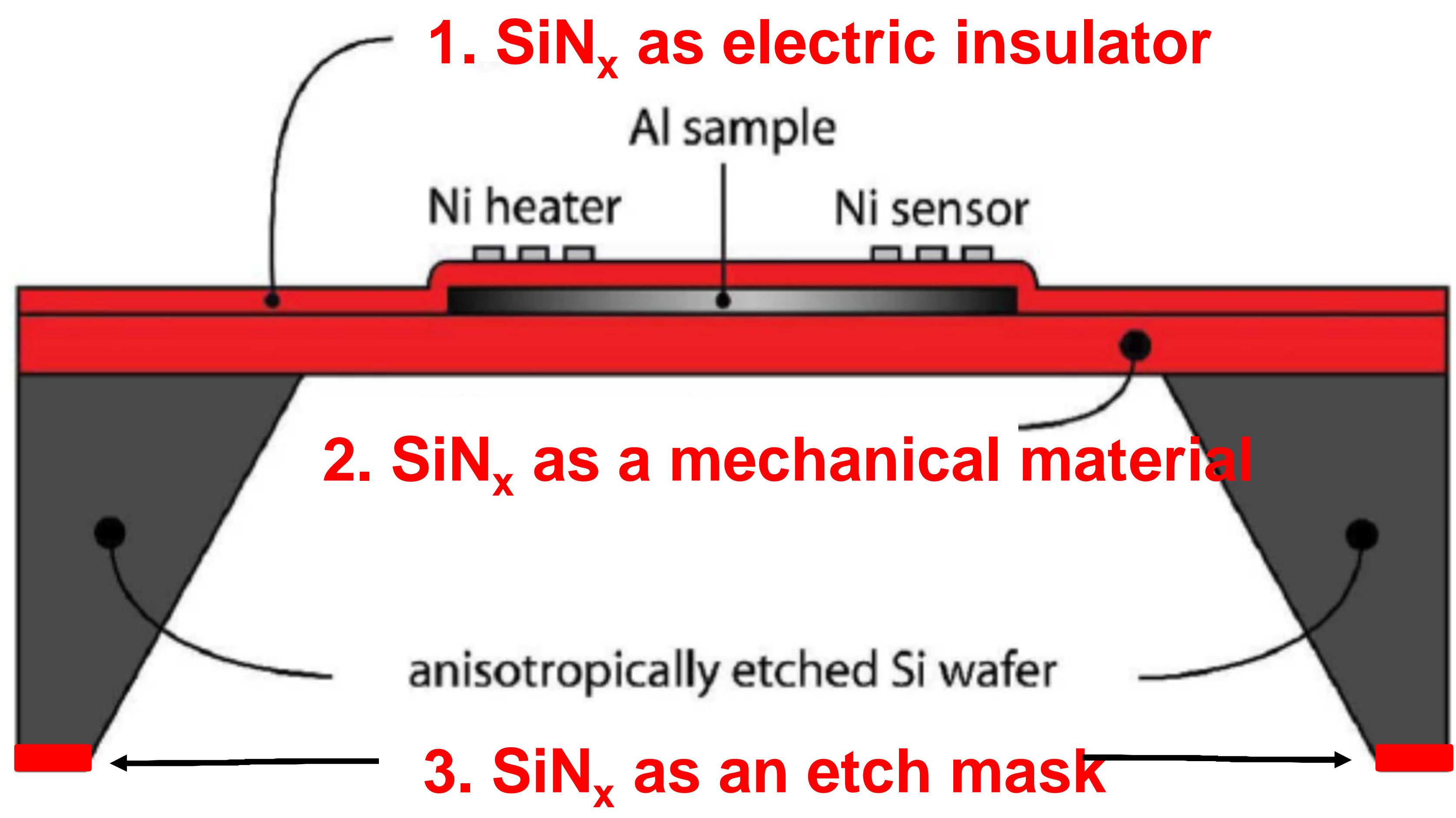
W.-H. Park et al. / Sensors and Actuators A 271 (2018) 251–256

Surface acoustic wave device



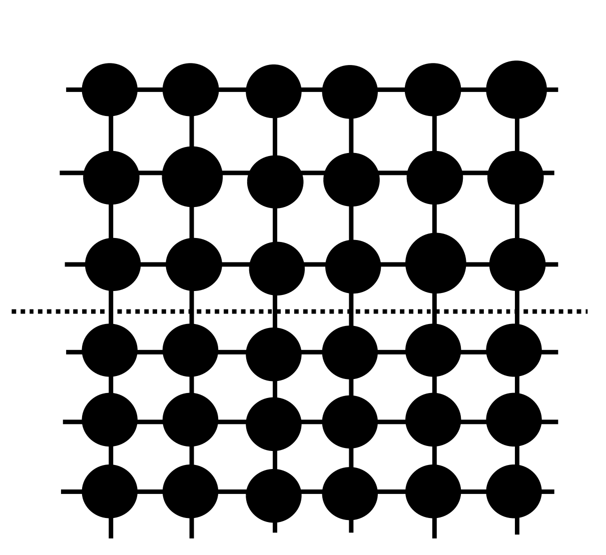
Chen et al: J. Micromech. Microeng. 21 (2011) 045021 (9pp)

Micro hot plate



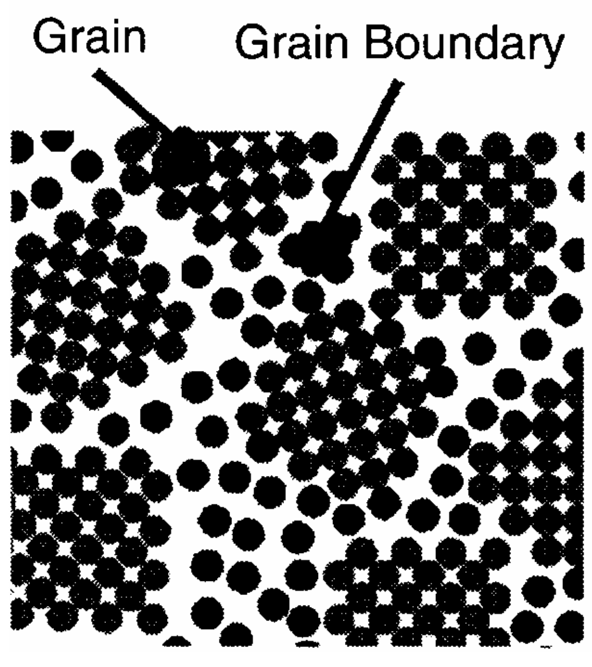
JMEMS VOL. 16, NO. 5, OCTOBER 2007, p.1269

Structure of thin films



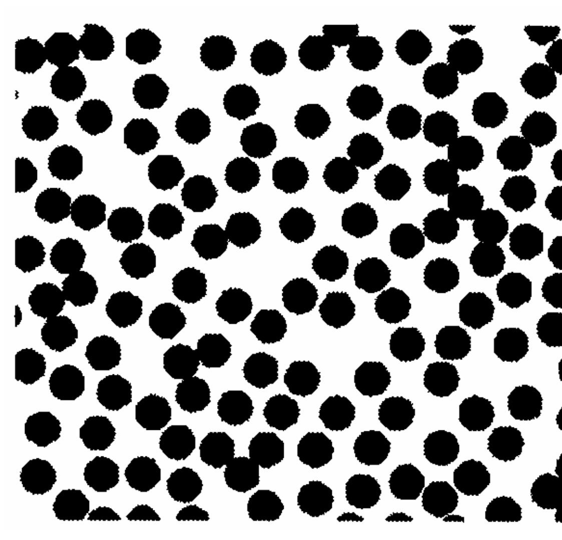
Epitaxial films are produced under special conditions only

SiH_4 (g) ➔ Si (s) + 2 H_2 (g)



Most metals are polycrystalline, and CVD polysilicon, too, obtained by reaction

SiH_4 (g) ➔ Si (s) + 2 H_2



Amorphous materials include many oxides, e.g. CVD oxide and nitride, also a-Si by

SiH_4 (g) ➔ Si (s) + 2 H_2

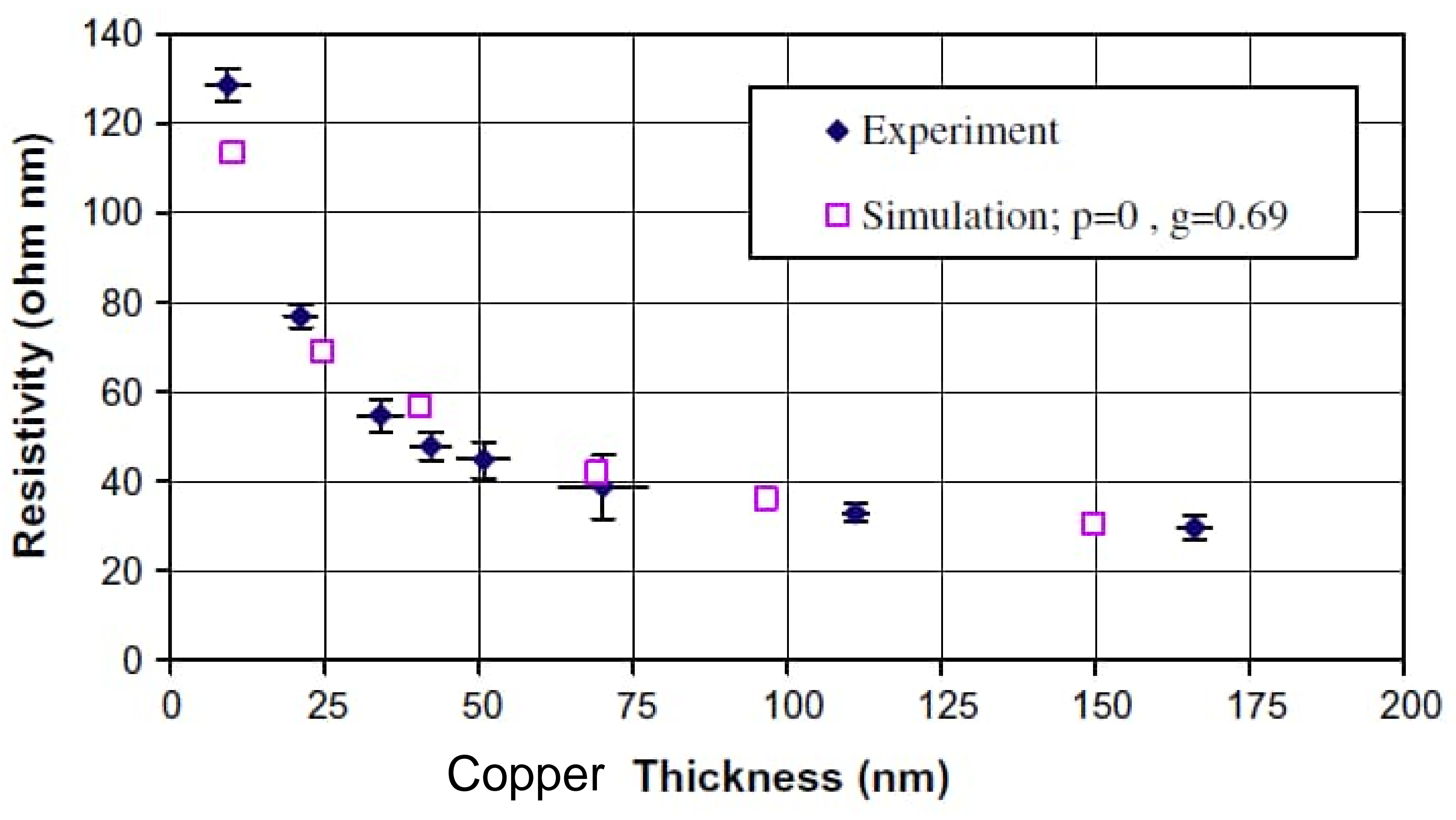
Thin films vs. bulk

Properties different from bulk materials

- Density
- Resistivity
- Thermal conductivity
- Refractive index
- Dielectric constant
- …

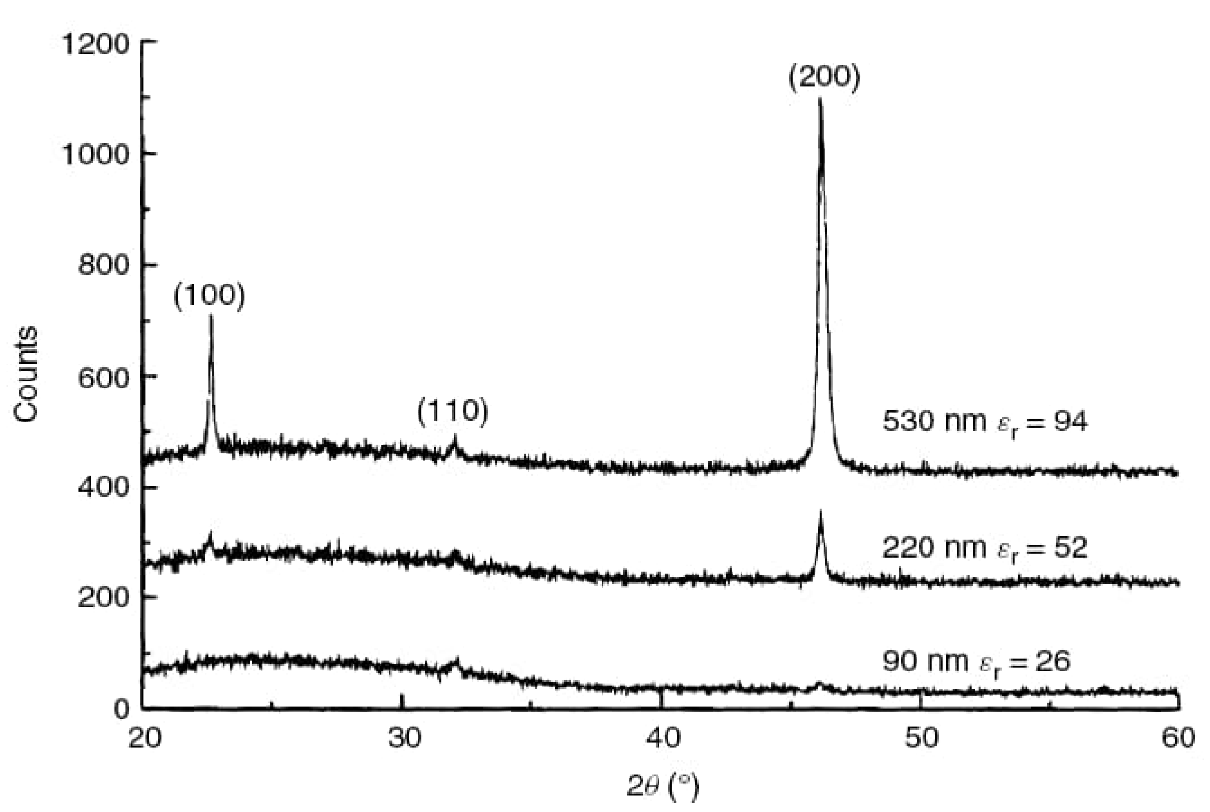
Properties & structure thickness dependent

Thickness dependent resistivity



A. Emre Yarimbiyik et al., Microelectronics Reliability 49 (2009) 127–134

Thickness dependent dielectric constant



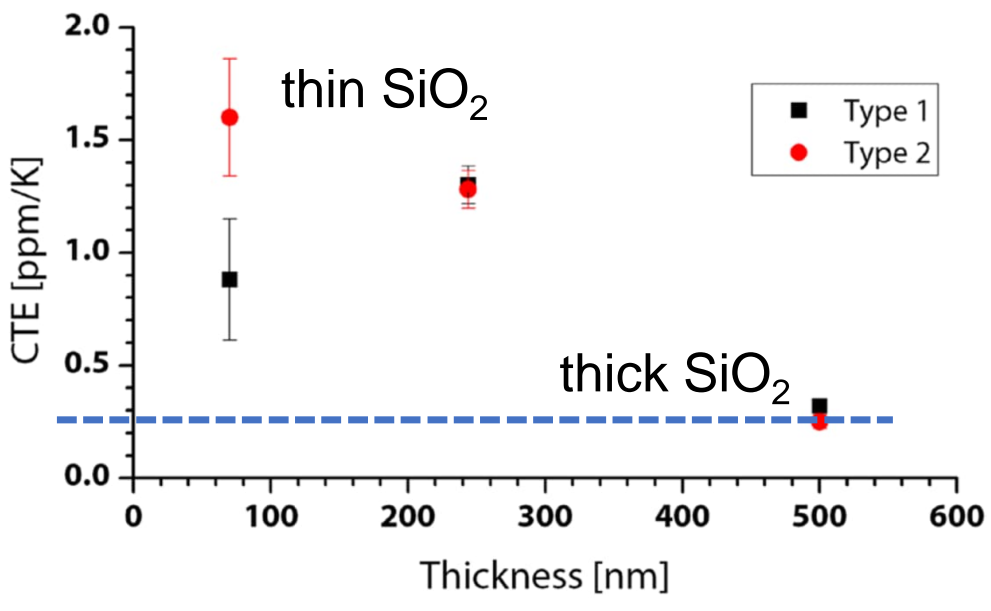
Crystallinity changes as a function of thickness ➔ dielectric constant changes

Other process parameters also affect structure, e.g. pressure or RF power.

Atomic Layer Deposited $SrTiO_3$

Vehkamäki

Thickness dependent CTE



Compared to thick layers, the CTE of the thin layers is found to be significantly higher.

Table 1. Deposition parameters of PECVD silicon-oxide films.

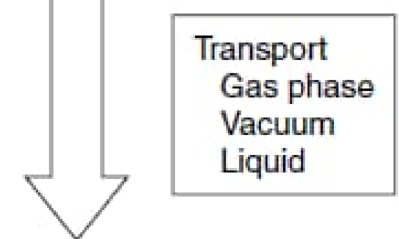
	Type 1	Type 2
Substrate temperature	400 °C	400 °C
SiH_4	210 sccm	300 sccm
N_2O	6000 sccm	9500 sccm
N_2	3150 sccm	1500 sccm
Power	1 kW	0.75 kW
Total pressure	2.2 Torr	2.4 Torr
Deposition rate	8.5 nm sec^{-1}	9.5 nm sec^{-1}
Uniformity	~1%	~1%
Residual stress (as-dep.)	−100 MPa	0 MPa

Ghaderi et al: J. Micromech. Microeng. **26** (2016) 084009 (10pp)

Generic thin film process

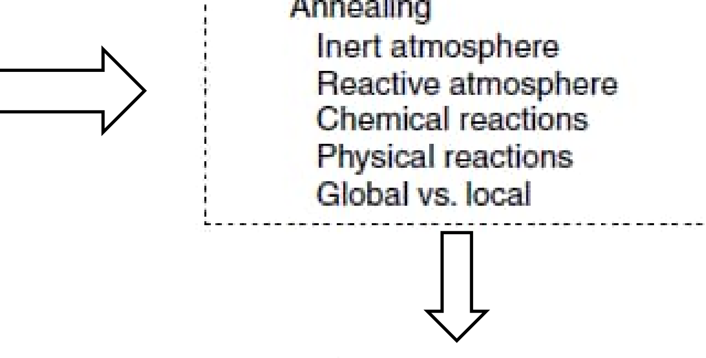
Excitation
- Thermal
- Plasma
- Ion bombardment
- Electron bombardment
- Laser
- Voltage
- Chemical potential

Source: Solid, Liquid, Vapor, Gas



Transport
- Gas phase
- Vacuum
- Liquid

Surface processes
- Deposition of film specie
- Deposition of contaminants
- Ion bombardment
- Desorption
- Energy from depositing specie
- External heating



Annealing
- Inert atmosphere
- Reactive atmosphere
- Chemical reactions
- Physical reactions
- Global vs. local

Analysis
- Physical
- Chemical
- Electrical
- Optical

Physical vapor deposition (PVD)

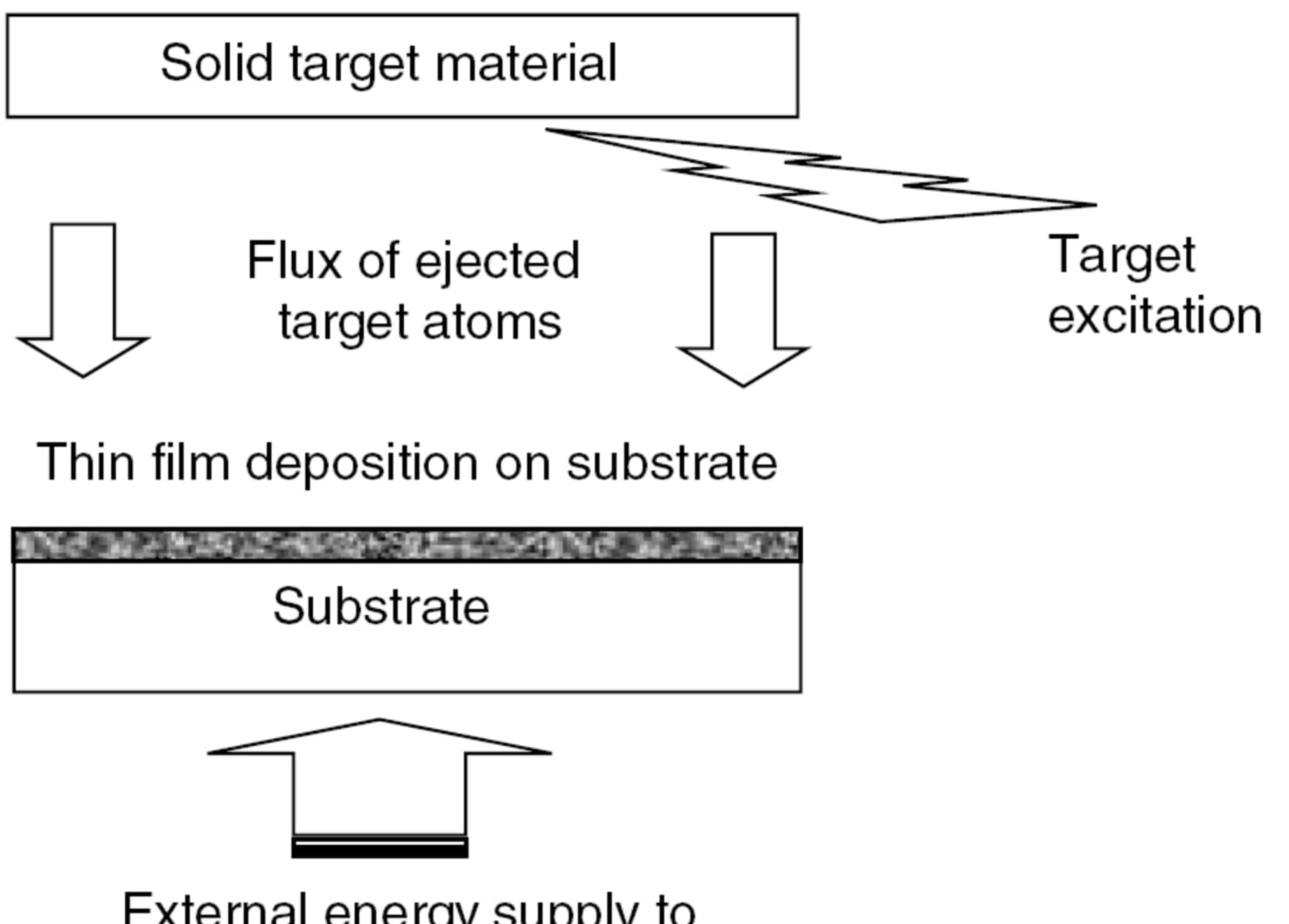
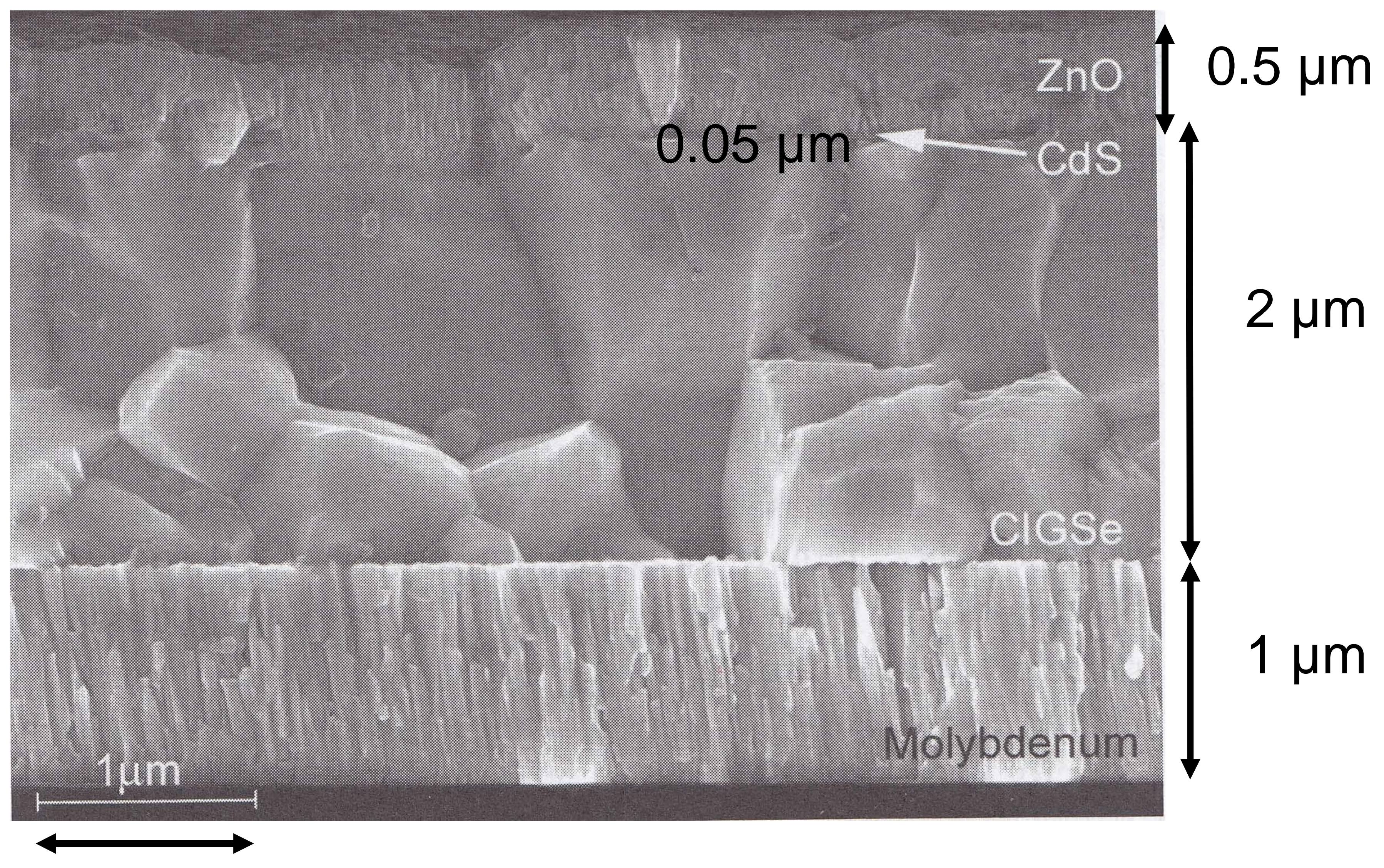


Fig. 5.2 IMF 1st edition

PVD deposited solar cell films

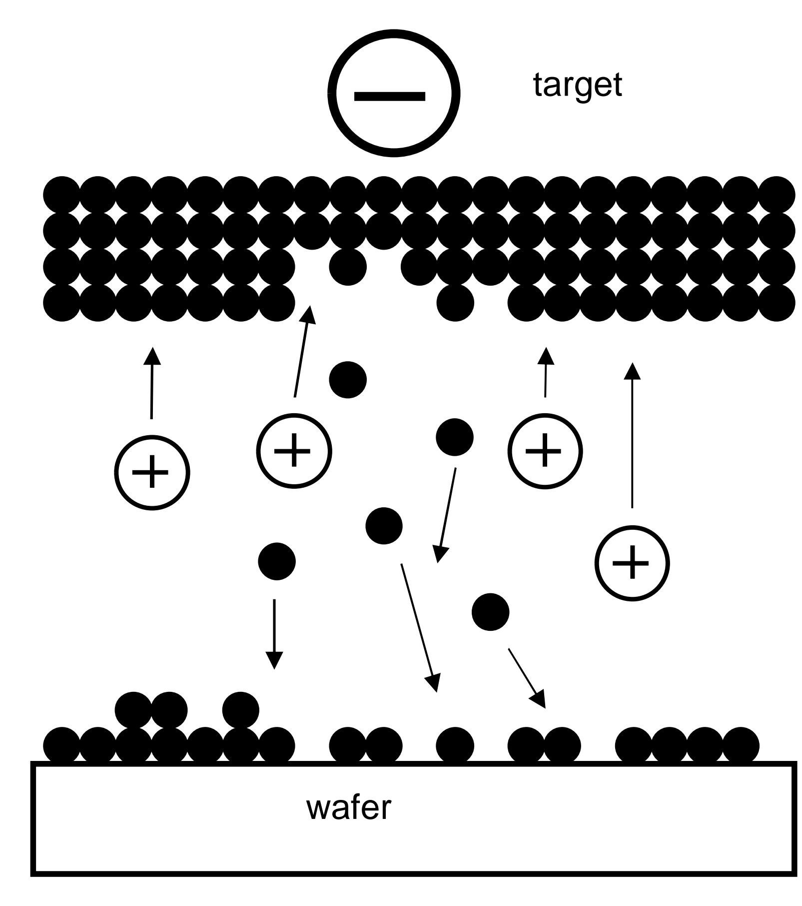


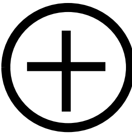
Poortmans: Thin film solar cells

Sputtering

- Argon plasma excited by electric fields
- Argon ions hit atoms loose from metallic target
- metal atoms travel in vacuum to substrate

- **Parameters to vary:**
- field/voltage
- pressure
- substrate temperature
- gas: N_2, O_2, Kr, Xe





Metallic thin films by PVD

- conductors (Al, Au, Cu)
- resistors (Ta, W, Pt)
- capacitor electrodes (poly-Si, Al, Mo)
- mechanical materials (Al-movable mirrors)
- magnetic materials (Ni coils)
- protective coatings (Cr, Ni etch masks)
- adhesive layers (thin Ti, Cr layers)
- optical materials (reflectors, IR filters)
- catalysts (Pt, Pd in chemical sensors)

Resistor design

$$R = \rho \frac{L}{WT}$$

How to change resistor resistance R ?

1. Change L: vary its length
2. Change W: vary its width
3. Change T: vary its thickness
4. Change ρ: choose a different material

Sheet resistance

$$R_s \equiv \rho/T$$

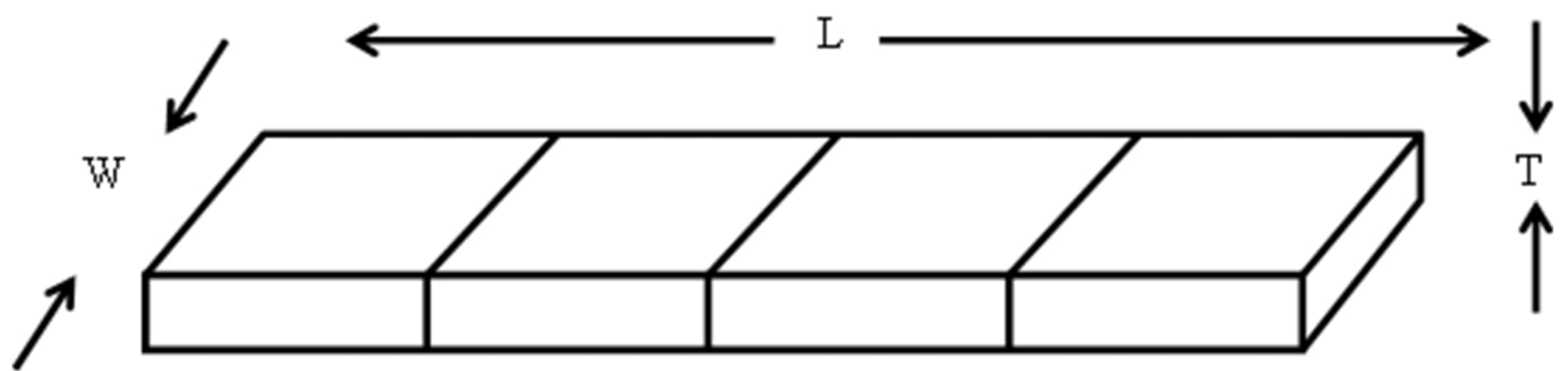
R_s is in units of Ohm, but it is usually denoted by Ohm/square (or Ω/□) to emphasize the concept of sheet resistance.

R_s is used a lot since it is directly measurable by four point probe.

Aluminum film 1 μm thick, sheet resistance ?
R_s = 3 μOhm-cm/1 μm = 3*10-8 Ohm-m/1*10-6 m =0.03 Ohm

Tungsten film, 1Ω resistance, thickness ? T = 10 μOhm-cm/1 Ohm = 10*10-8 Ohm-m/1 Ohm = 100 nm

Resistor sheet resistance



Resistance of a conductor line can now be easily calculated by breaking down the conductor into n squares: $R = nR_s$

If we have Al wire, 3 µm wide, 100 µm long (n=100/3), with sheet resistance of 0.2 Ohm/sq, its resistance R = 33.3*0.2 Ohm = 6.7 Ohm

Resistor design

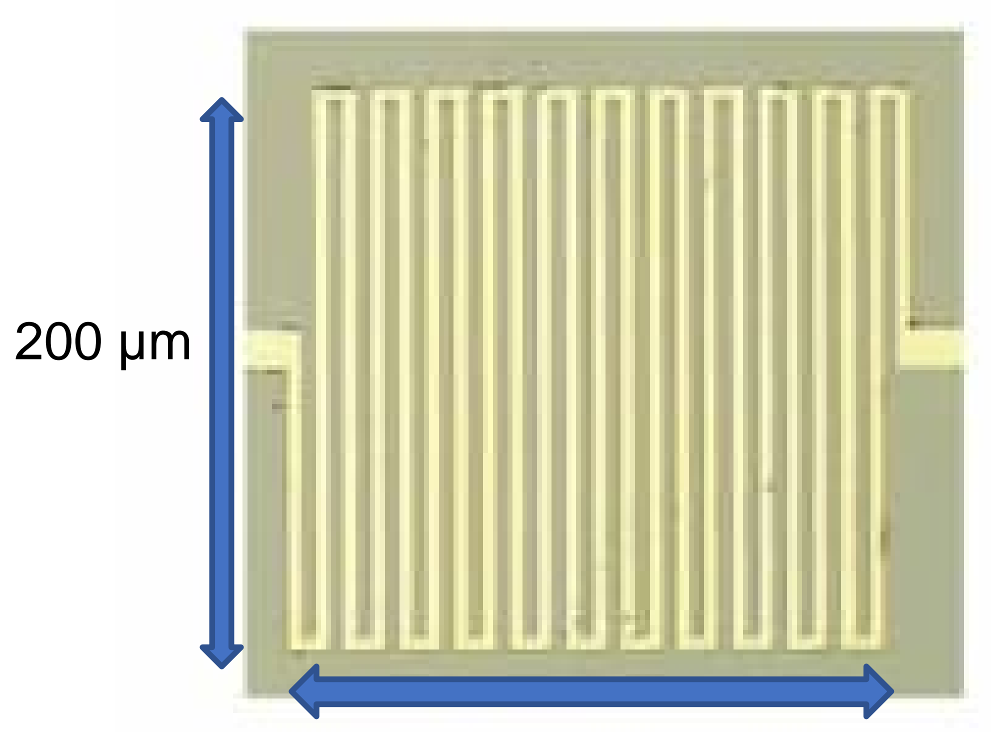
Platinum resistor.
Thickness 100 nm
ρ = 20 µOhm-cm

$R_s = \rho / T$ = 0.2 Ohm/sq

$R = n^* R_s$

Calculate number of squares:

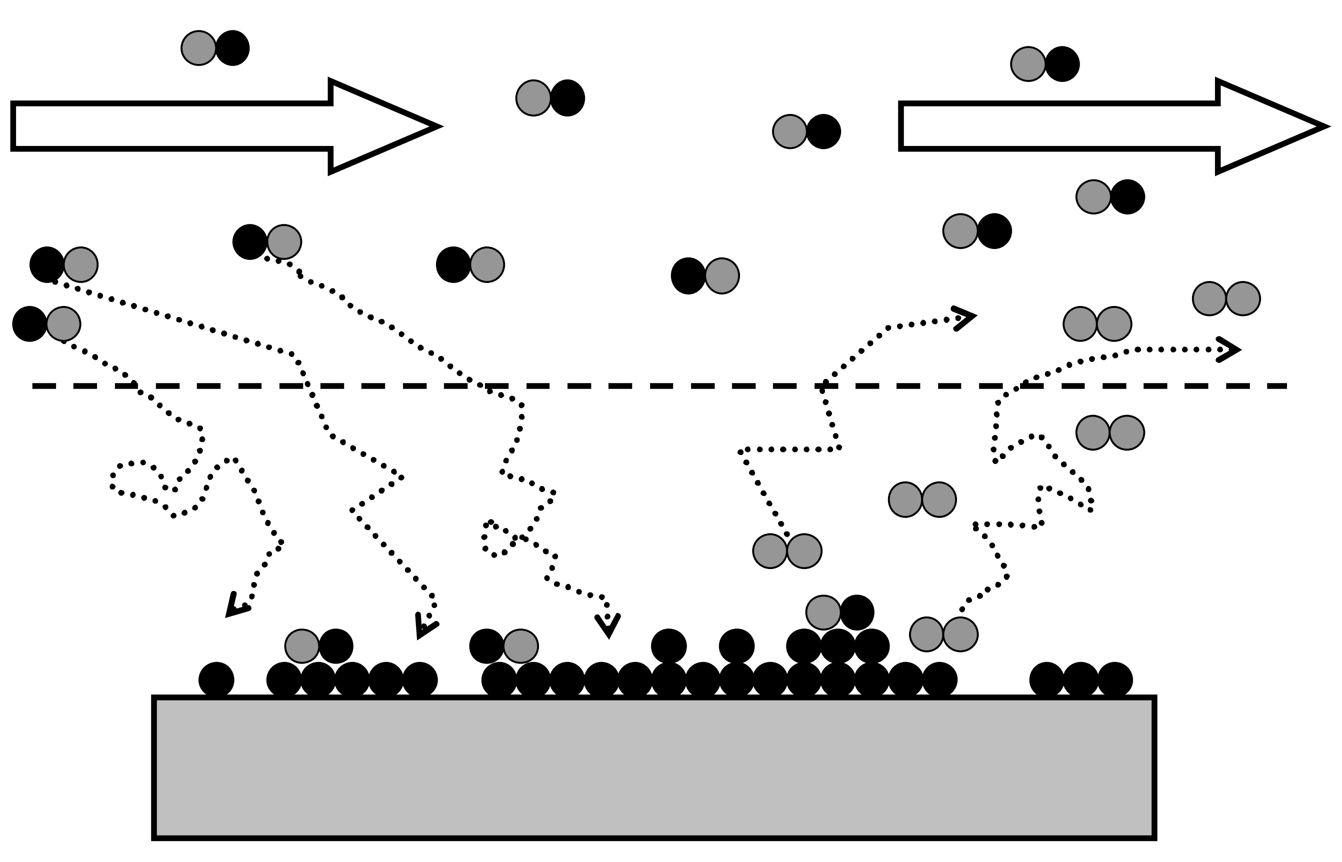
One vertical wire:
200 µm/5 µm = 40 squares
22 wires ➔ 880 squares
Add 22 squares from end segments
➔ ≈900 squares
➔ R = 900*0.2 Ohm = 180 Ohm



22 wires, 21 spaces between them, each line and space 5 µm wide. 22 end segments.

CVD: Chemical Vapor Deposition

Gaseous precursor + surface reaction ➔ solid film + gaseous byproducts



gas phase
convection

diffusion
through
boundary layer

surface
processes
(adsorption,
film deposition,
desorption)

Common CVD processes

CVD is used for common dielectrics, oxides and nitrides.
Also polysilicon.
Tungsten is the only metal commonly deposited by CVD.

Oxide at 425°C:

SiH_4 (g) + N_2O (g) ➔ SiO_2 + N_2 + $2H_2$

Nitride @800°C:

3 SiH_2Cl_2 (g) + 4 NH_3 (g) ➔
Si_3N_4 (s) + 6 H_2 (g) + 6 HCl (g)

Silicon @625°C:

SiH_4 (g) ➔ Si (s) + $2H_2$ (g)

Tungsten @400°C:

WF_6 (g) ➔ W(s) + $3H_2$ (g)

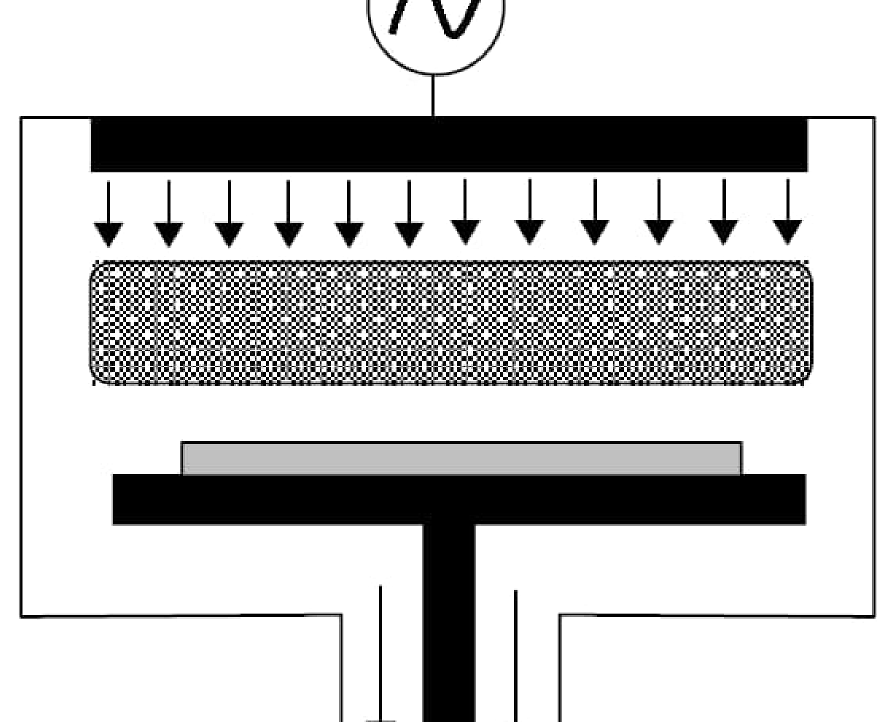
PECVD @300°C

Oxide:

SiH_4 (g) + N_2O (g) ==> SiO_2 + N_2 + $2H_2$

Nitride:

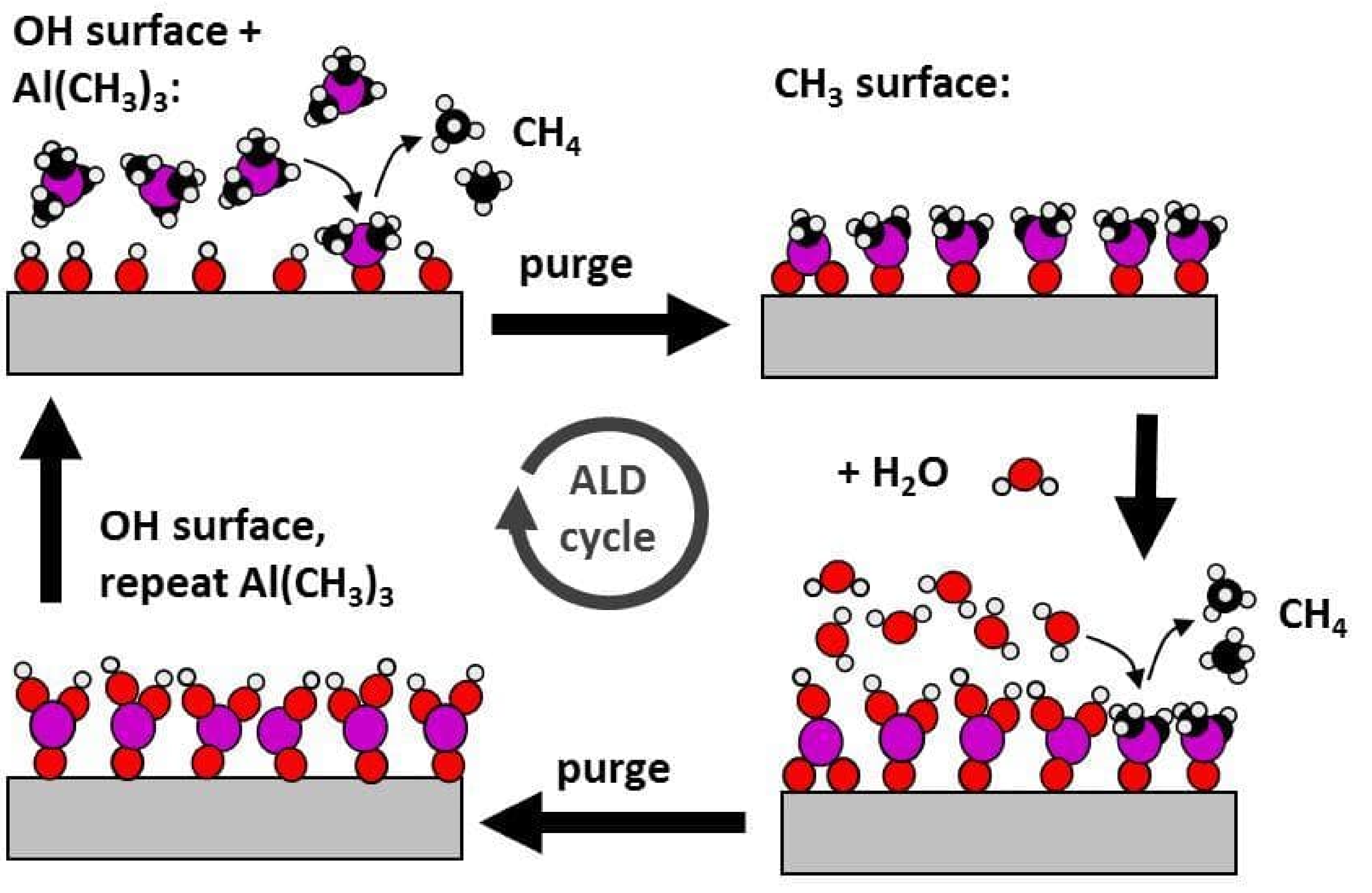
3 SiH_4 (g) + 4 NH_3 (g) ==> Si_3N_4 (s) + 12 H_2 (g)



PECVD: Plasma Enhanced CVD

- Plasma excites source gas
- ➔ reactive specie
- Done at low temperatures (~ 300°C)
- Al melts at 650°C ➔ thermal CVD too hot
- Wide deposition parameter range (pressure, RF power, power pulsing,…)
- High rates (1-10 nm/s) (10X thermal)

ALD: Atomic Layer Deposition



Precursors introduced in pulses, with purging in-between

ALD features

Excellent thickness control, just count the cycles

Very slow: growth per cycle typically 1 Å/cycle = 0.1 nm/cycle

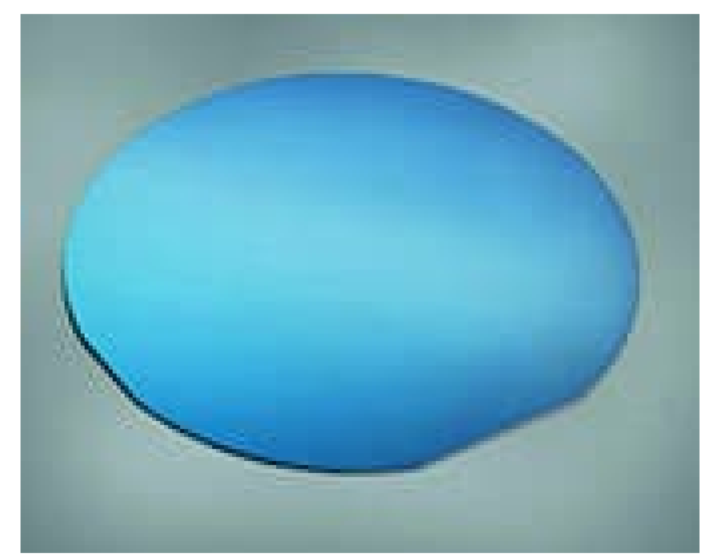
Pulses typically 1 sec ➔ 1.5 nm/min

Chemical bonds formed ➔ excellent adhesion

Surface controlled growth ➔ conformal over steps

Deposition temperature lower than even PECVD

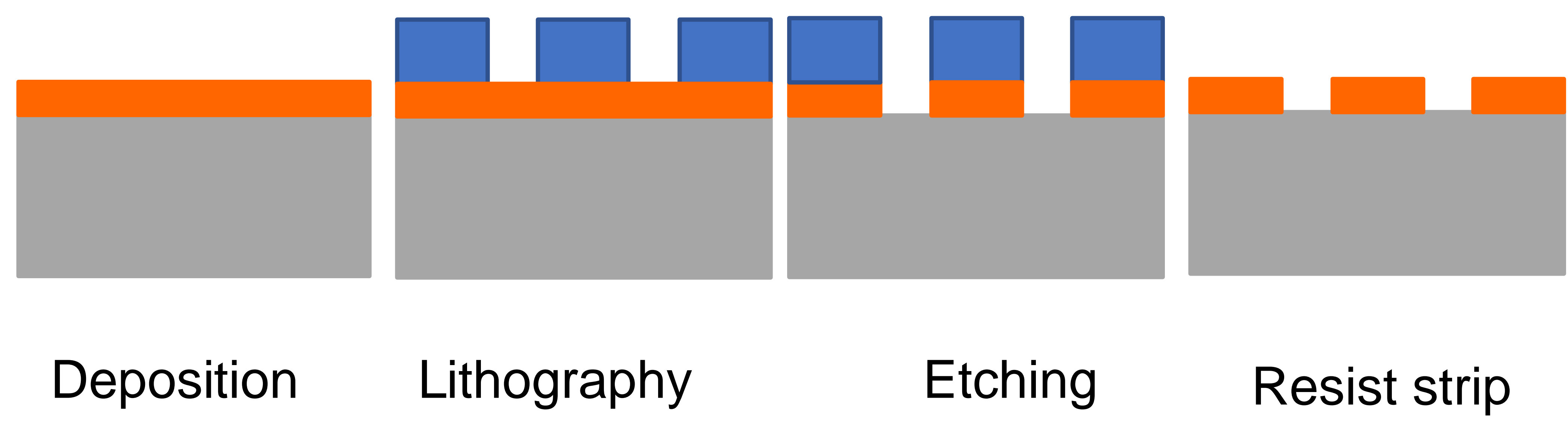
Thin film deposition covers the whole wafer.



This applies to all deposition methods !
But you can use resist patterns to block some areas ➔ plating or lift-off. But these are exceptions.

Thin film patterns

If you want film only locally, you have to do lithography and etching after deposition.



Electroplating

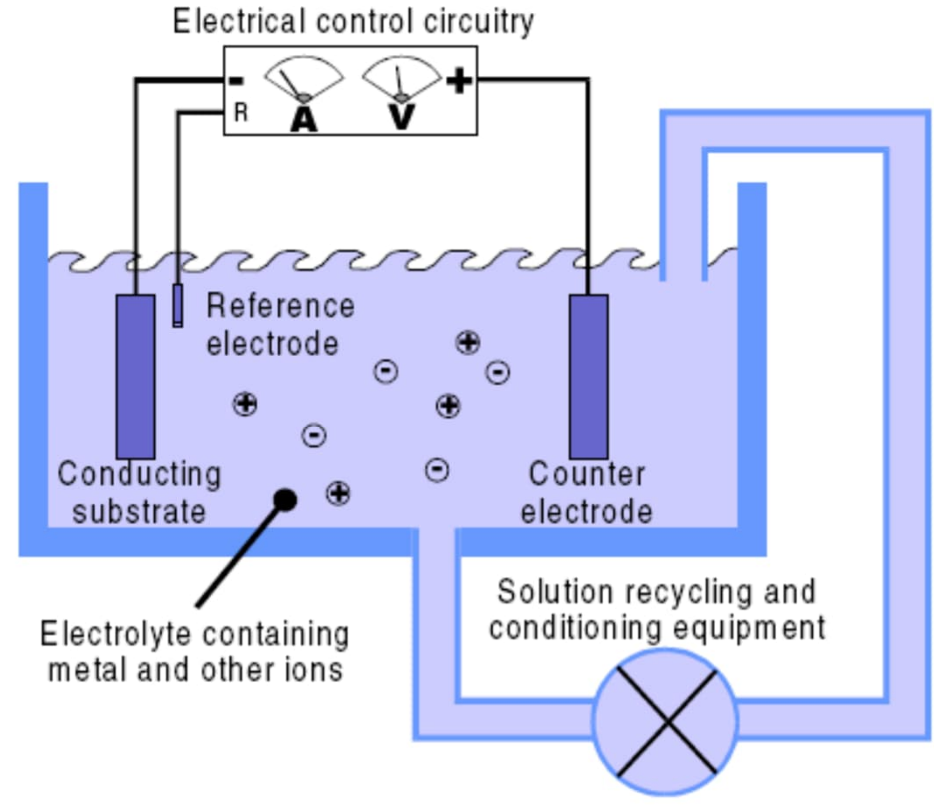


Figure 1. Schematic representation of a set-up for electrochemical deposition.

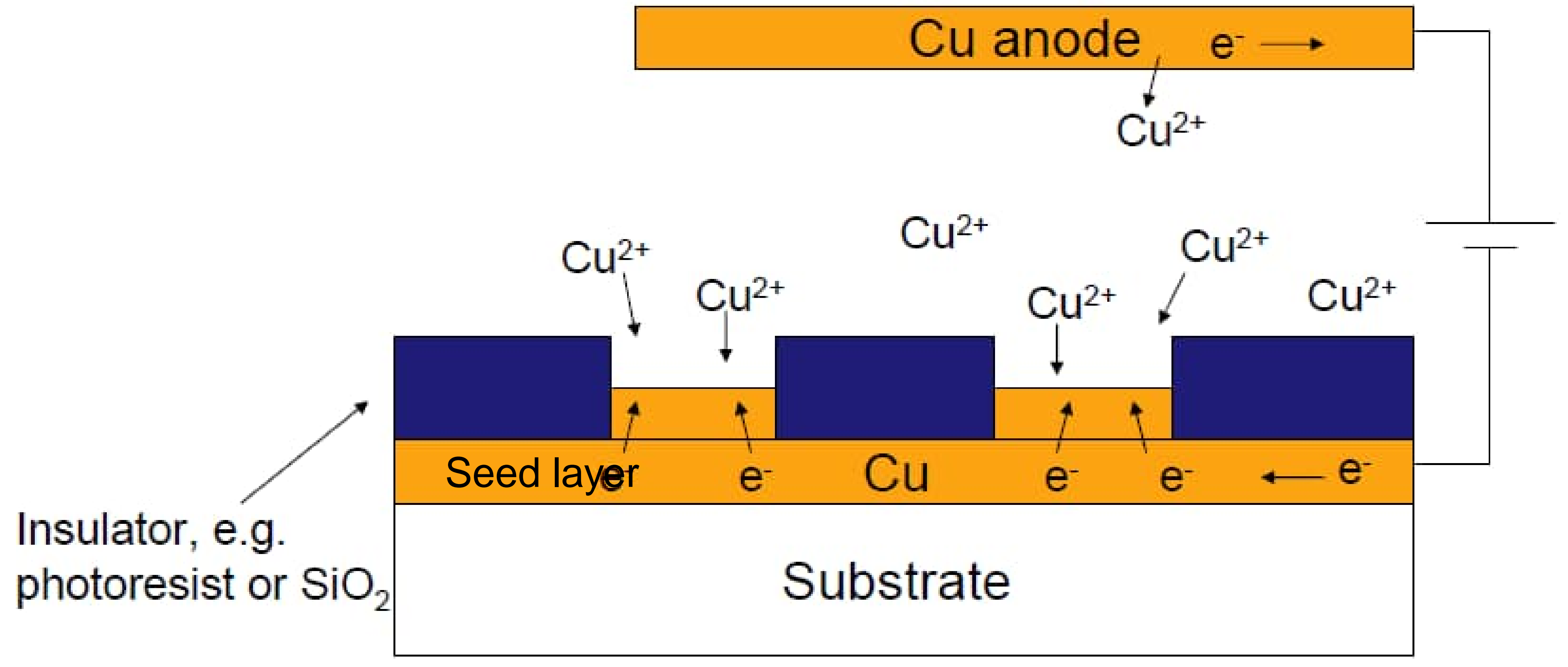
Typical plated metals:

-nickel (Ni), NiFe,
-CoP
-copper (Cu)
-gold (Au)

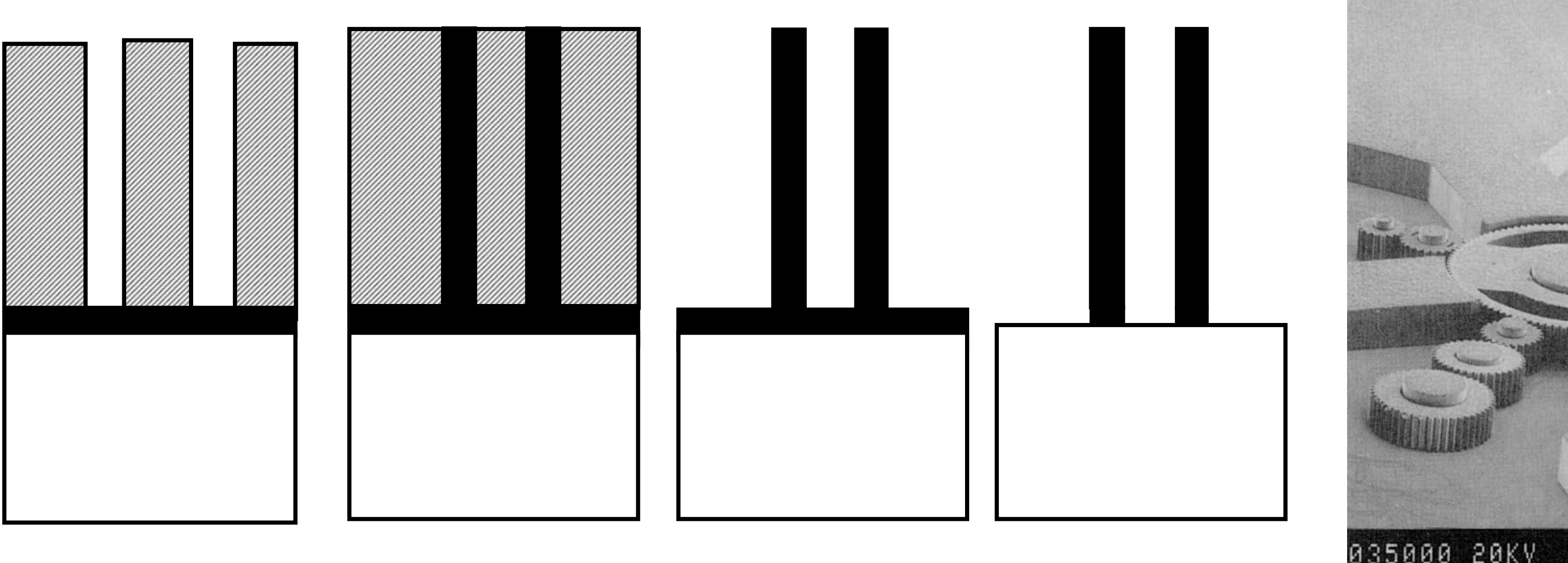
Not applicable to:
-aluminum (Al)
-most refractory metals (W, Ti, ...)

Selective area deposition

Electrodeposition occurs only in those areas where electrons are available
→ selective area deposition



Electroplated structures



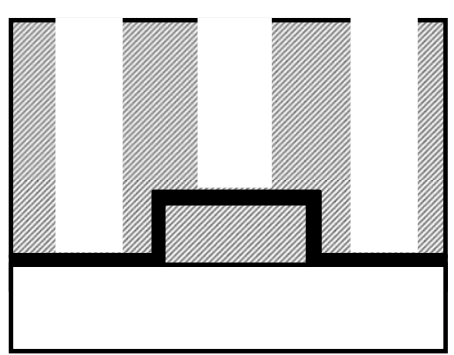
1. Seed layer sputtering
2. Lithography
3. Electroplating metal
4. Resist stripping
5. Seed layer removal

Nickel gear structures on silicon made by electroplating.

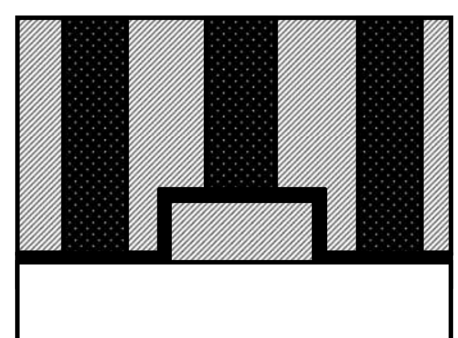
Reproduced from Guckel, H. (1998),

Released plated metals

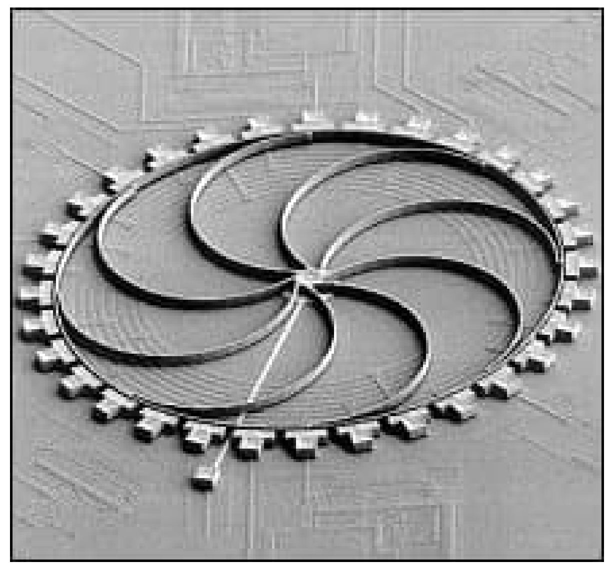
Resist pattern +
Seed metal +
resist pattern

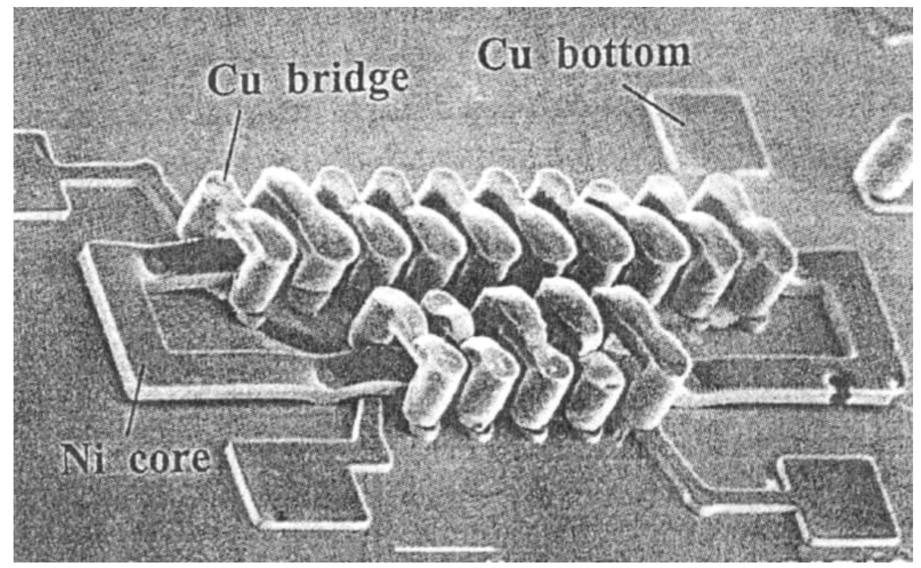


Electroplating



Resist removal ➔ free-standing metal



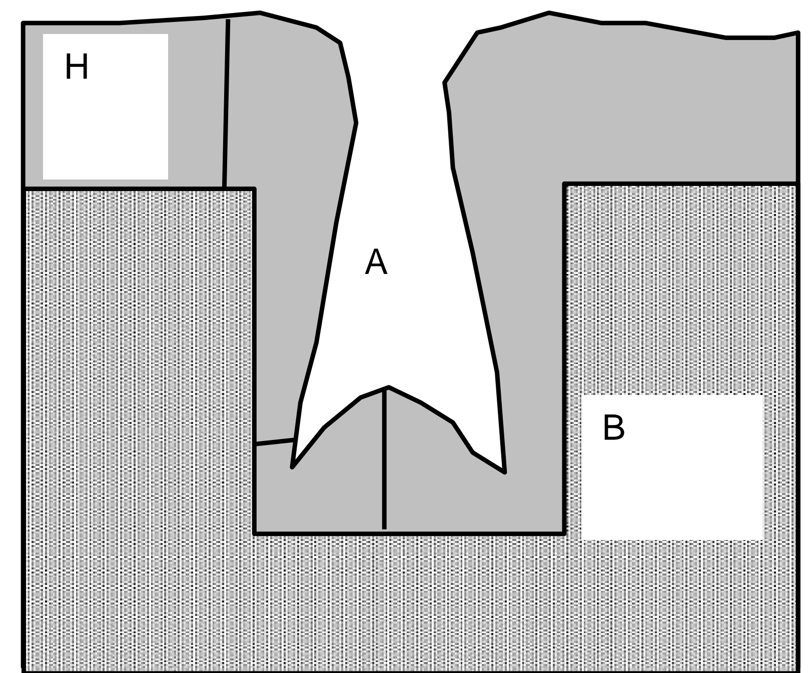


Step coverage

Physical bombardment different on horizontal and vertical walls

Transport of gas molecules into grooves limited by shadowing

At low temperature arriving atoms stick where they hit



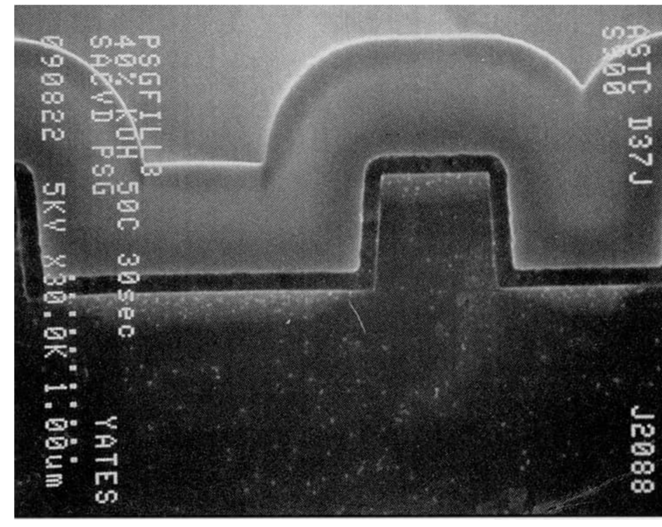
Ratio of film thickness on sidewall to horizontal = A:H

In sputtering, A:H ≈ 20-30%

100% step coverage is called ***conformal***

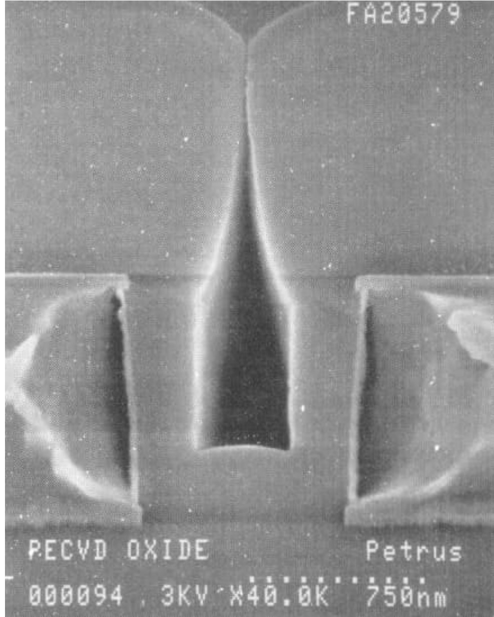
CVD oxide step coverage

Conformal, near 100% step coverage



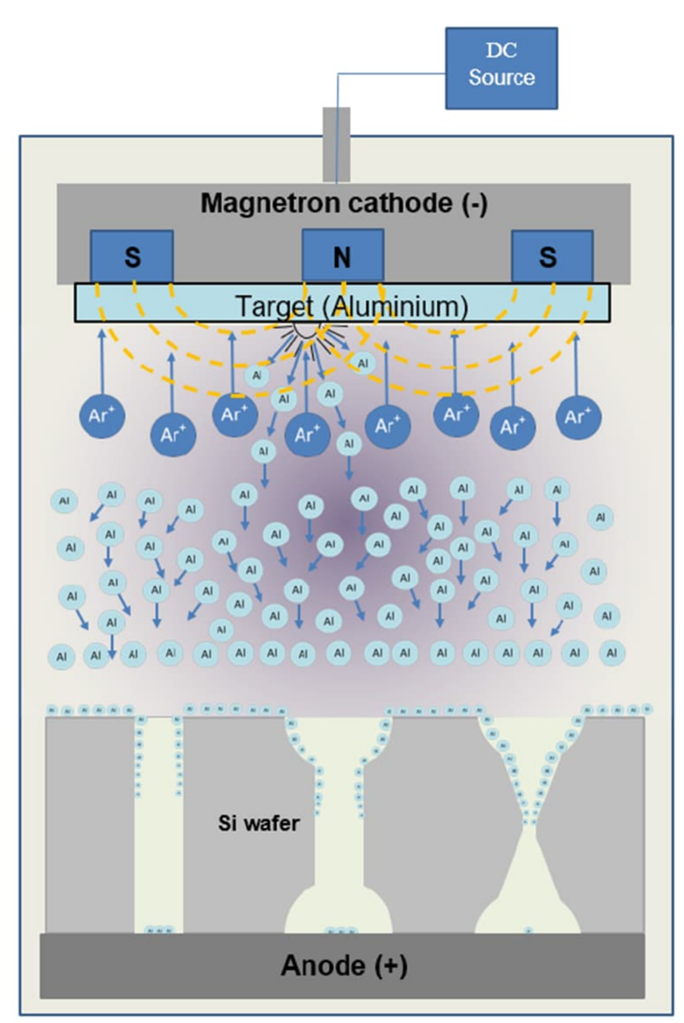
- ALD
- Thermal CVD

Satisfactory step coverage, e.g. 50%



- Sputtering
- PECVD

Step coverage vs. sidewall slope



Alfaro-Barrantes, JMEMS 2021

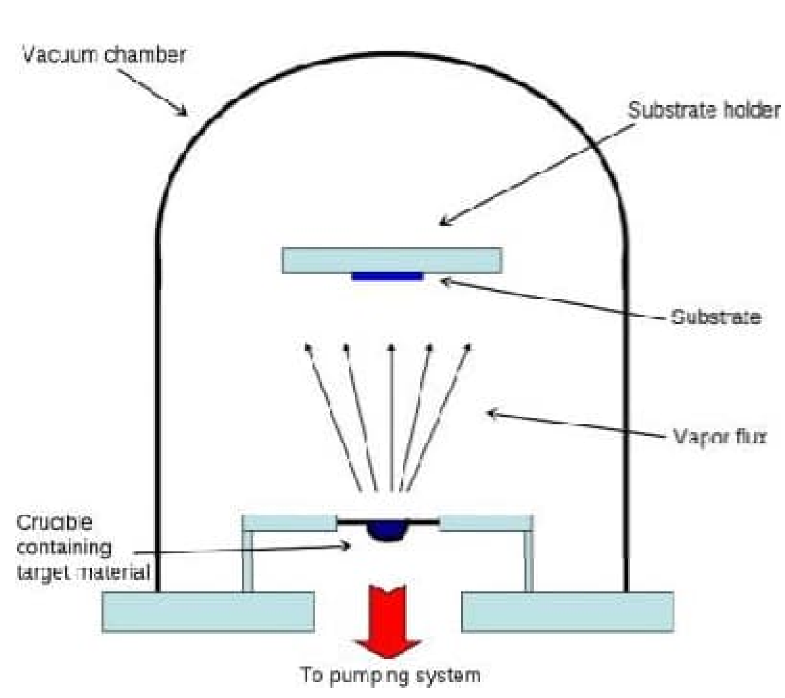
Vertical (and retrograde !) wall is difficult to cover.

Sharp corners are difficult to cover.

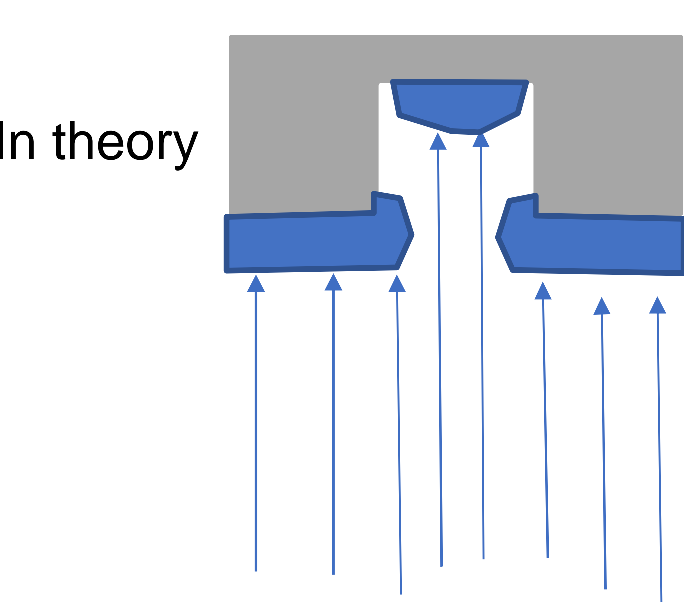
Positively sloped wall is easier.

But positively sloped wall wastes chip area (in the figure, sloped wall via takes up 4X area compared to vertical walls).

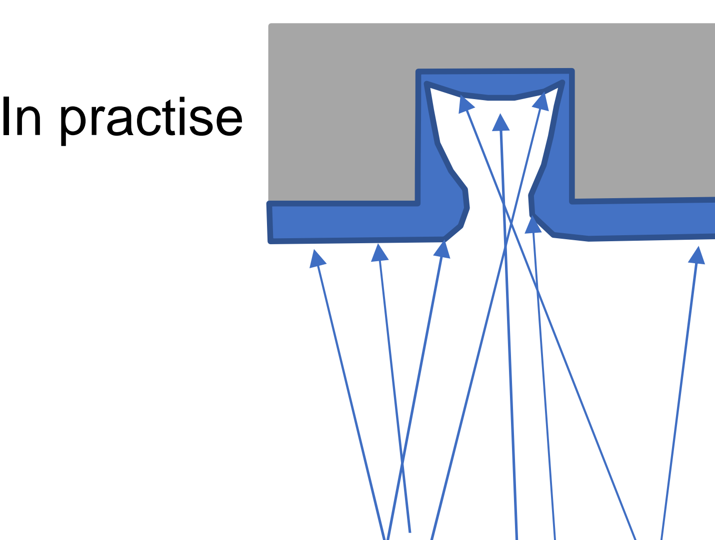
Evaporation: poor step coverage



In theory

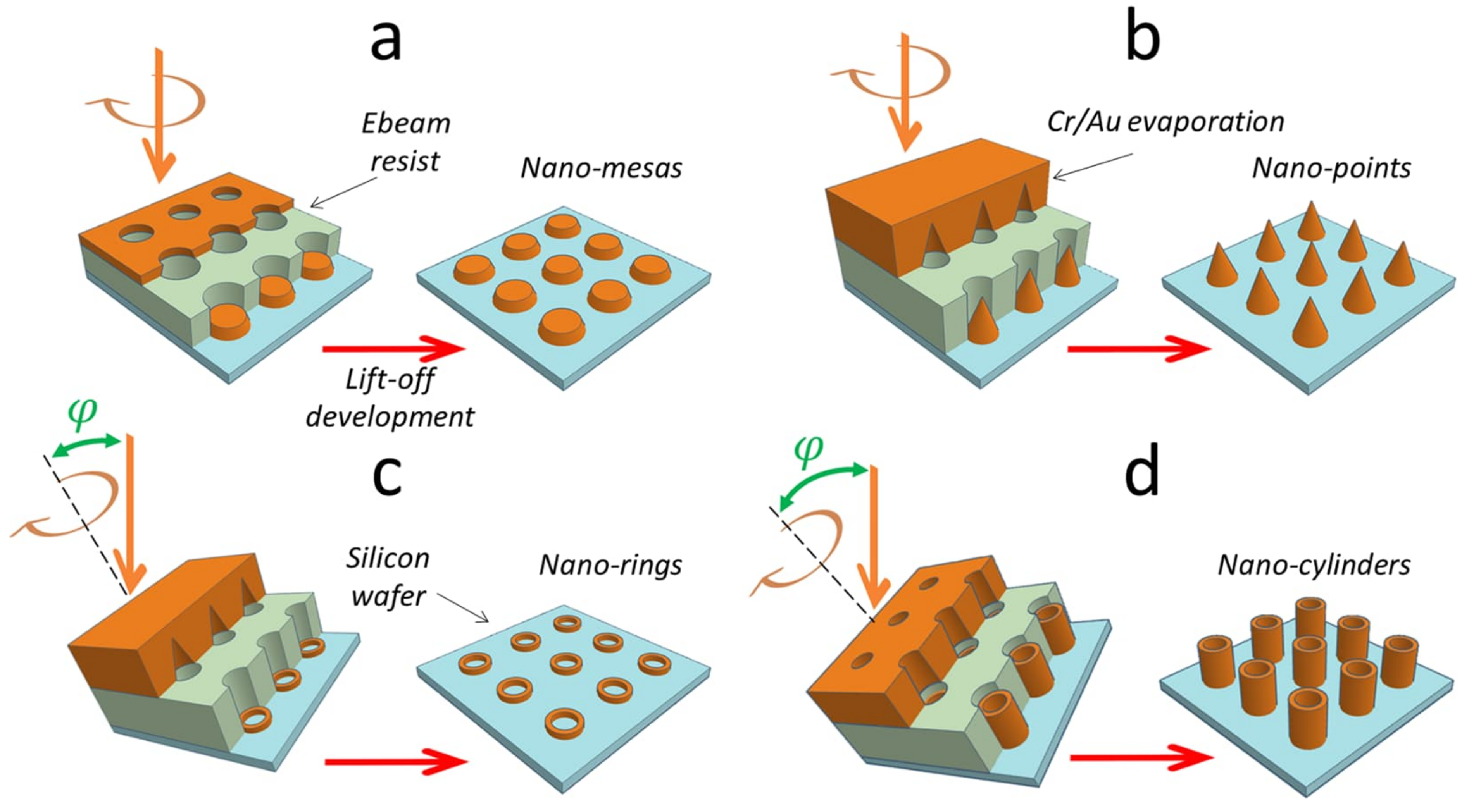


In practise



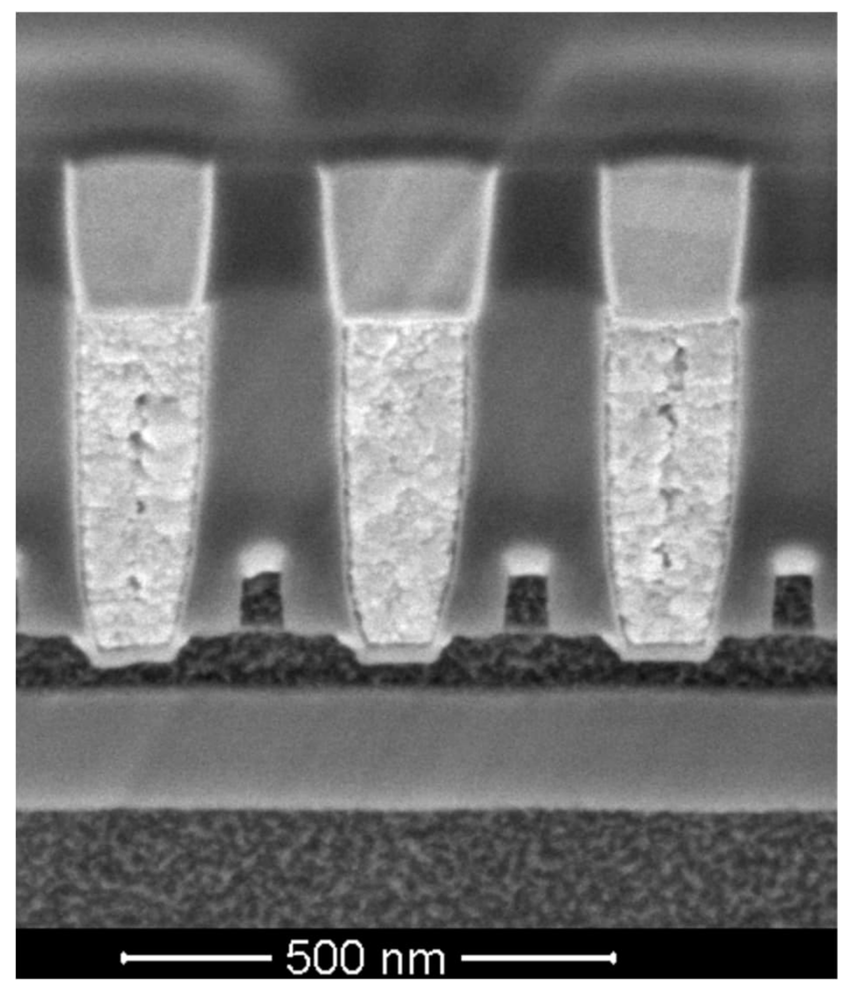
Line of sight –method:
Atoms travel like light rays,
without any collisions, and
deposit where they hit the wafer.

Inclined evaporation



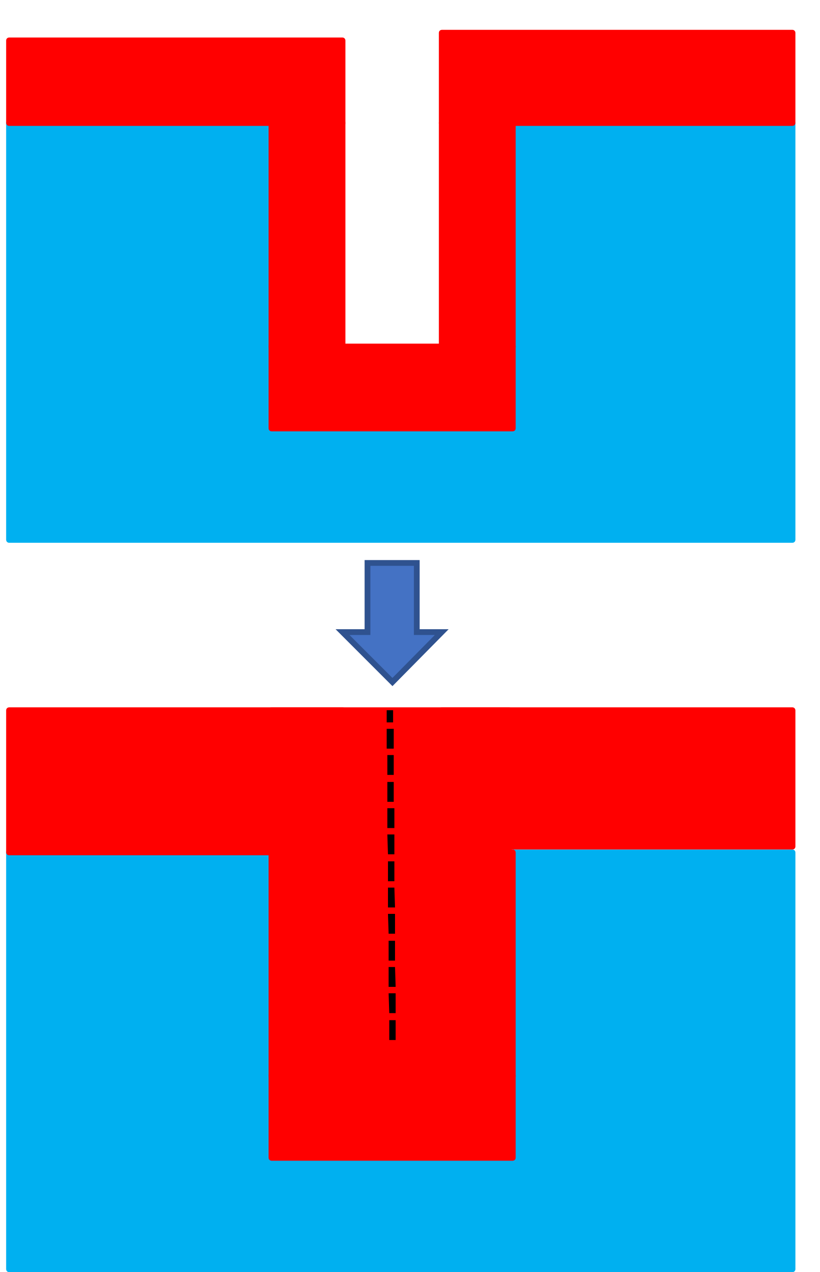
Eschimese, D. et al. *Sci Rep* **9,** 7682 (2019). https://doi.org/10.1038/s41598-019-44074-w

Thermal CVD: good step coverage

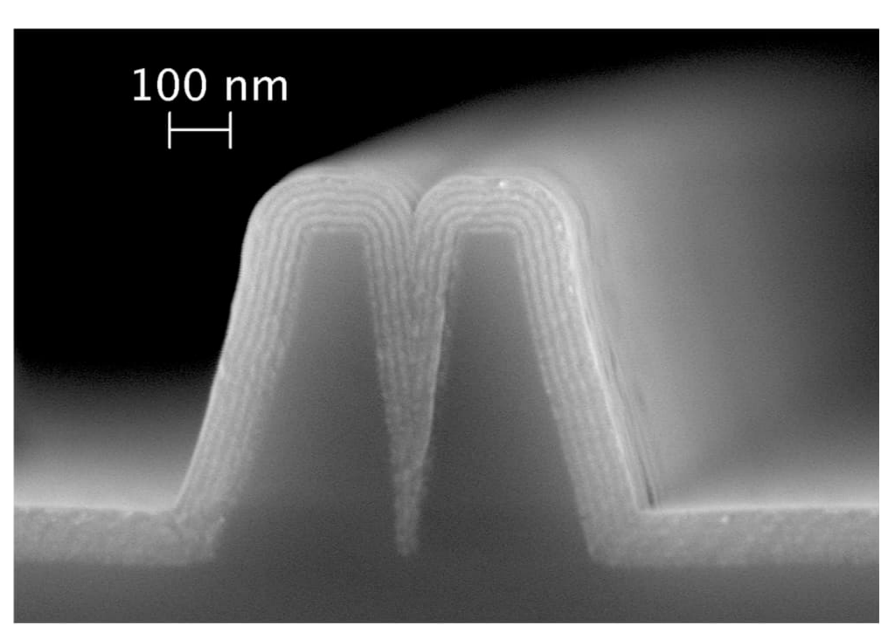


Tungsten:

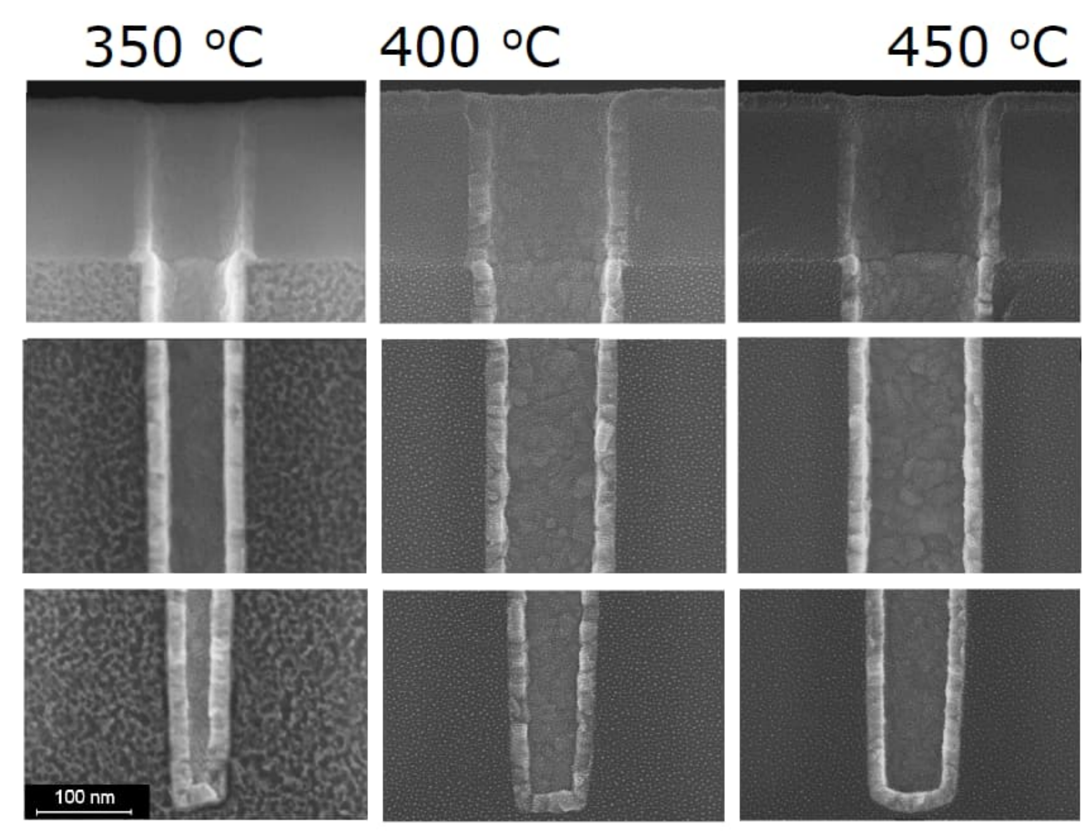
WF_6 (g) ➔ W(s) + $3H_2$ (g)



ALD: excellent step coverage

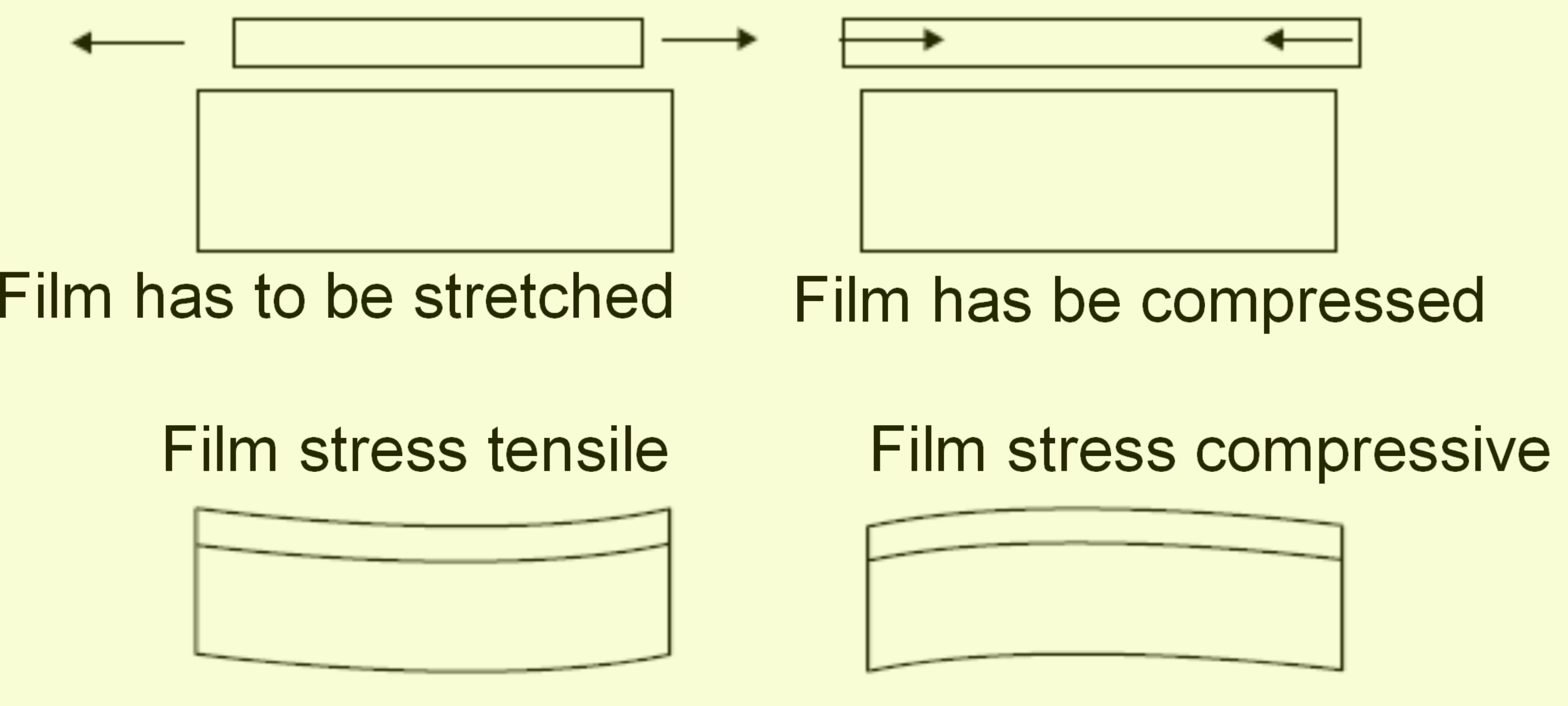


Al_2O_3/TiO_2 nanolaminate



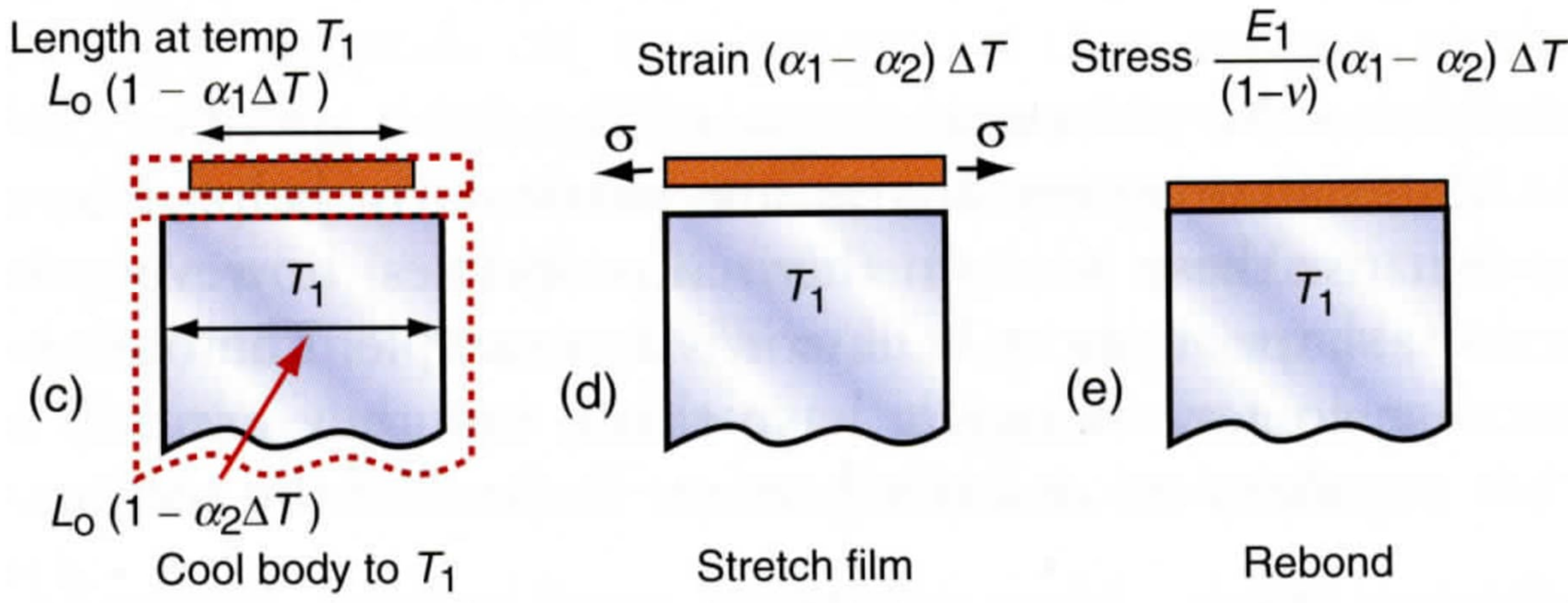
TiN barrier in deep groove

Stresses in thin films



The substrate is in opposite stress state !

Thermal stresses



Film has larger CTE than substrate ➔ film wants to contract more upon cooling, but is prevented by massive substrate ➔ film under tensile stress

Origin of stress: $\sigma = \sigma_i + \sigma_{th}$

- Extrinsic stresses:

  thermal expansion mismatch

$$\sigma = E_f/(1-\nu) \times (\alpha_f - \alpha_s) \times \Delta T$$

Intrinsic stresses: deposition process dependent

- low energy deposition

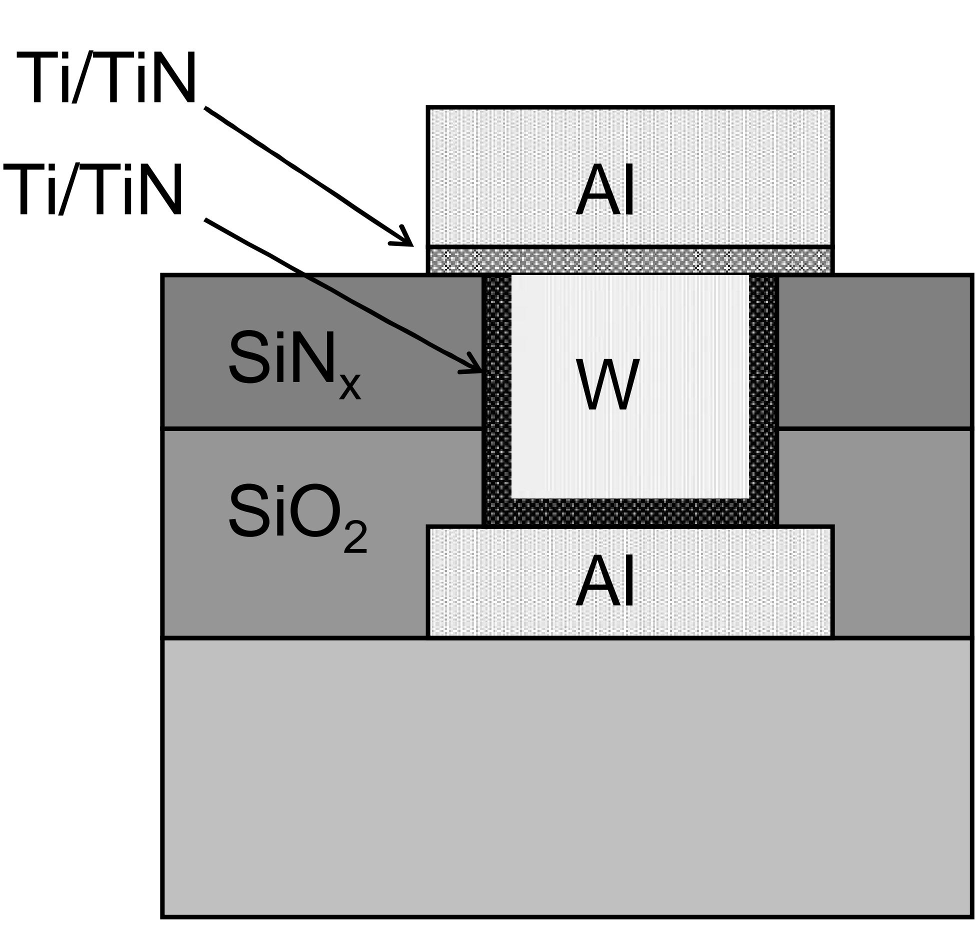
  ➔ no energy for relaxation process

- high energy deposition

  ➔ non-equilibrium, forced positions

- impurities, voids, grain boundaries

Multilevel metallization with Ti/TiN barriers



1st deposition: Al 500 nm

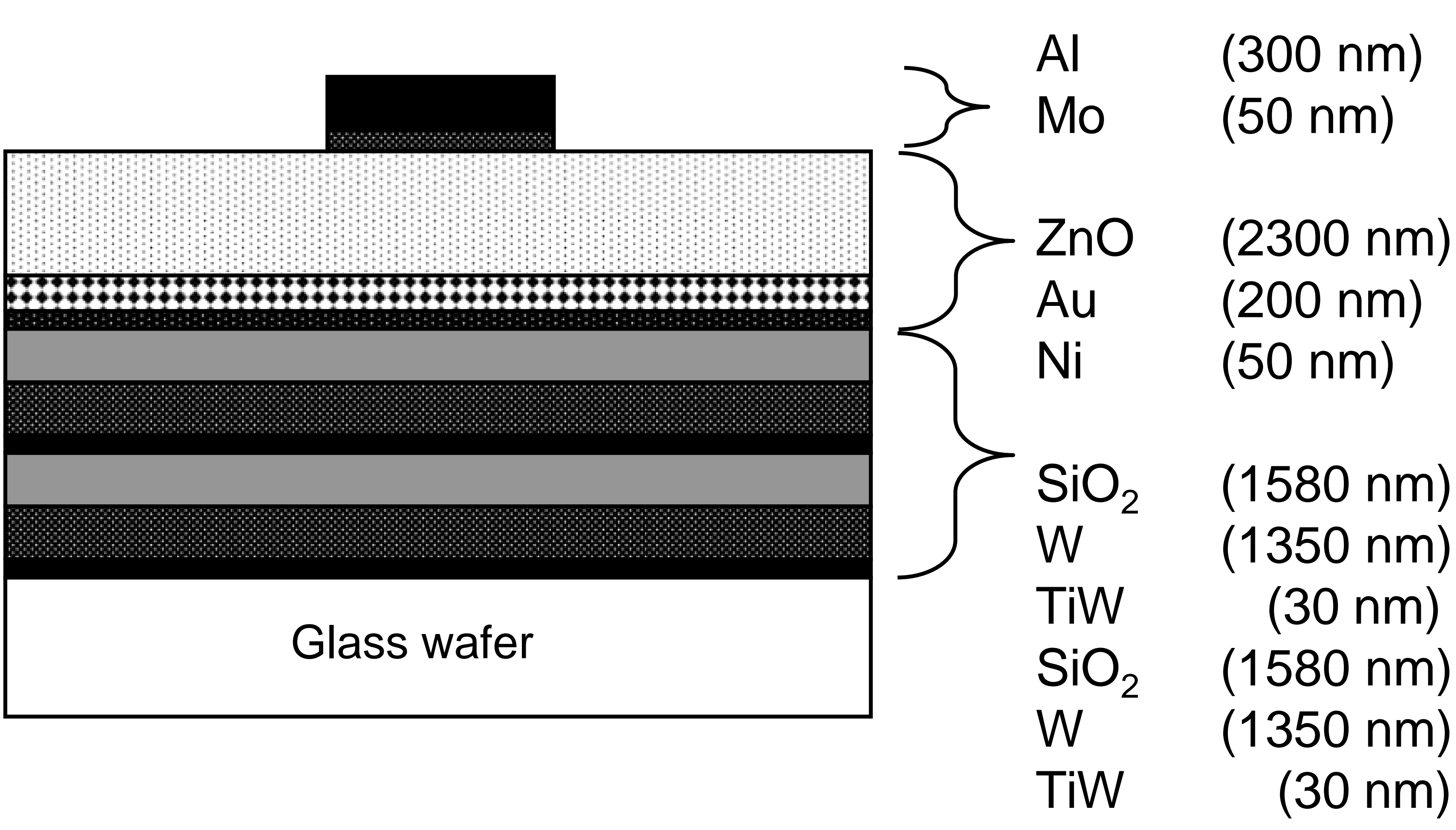
2nd deposition:
Dielectric: 500 nm
SiO_2 /SiN_x both 250 nm

3rd deposition:
Ti/TiN
20 nm/50 nm

4th deposition: W 500 nm

5th deposition:
Ti/TiN/Al
20/50/1000 nm

Acoustic multilayers

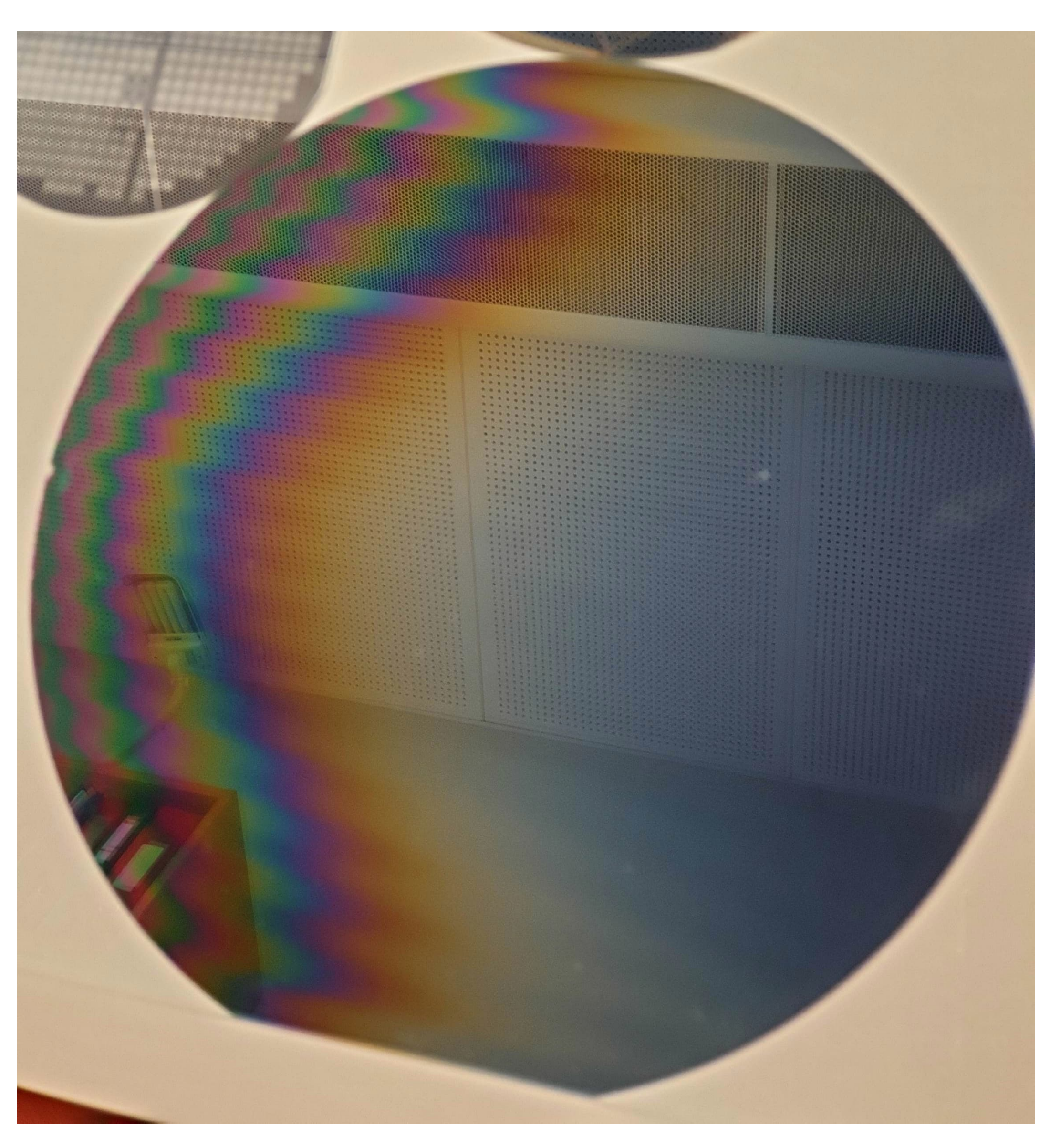


Film quality

Uniformity:
across-the-sample uniformity of thickness, resistivity, refractive index…
Usually given as
U = (max-min):(2*ave), 1-10% typical

Homogeneity:
film has same structure and composition all over, e.g. grain size or dopant concentration is independent of position, no directionality of crystals, no stress gradient, no interfacial layer, …

Why rainbow colors ?



To sum up:

- Typically 100 nm – 2 µm thick
- In modern CMOS many films in range 2 nm-100 nm
- If you have no idea, assume 1 µm !!
- But below 1 µm LW, assume aspect ratio is 1:1

- PVD for metals
- CVD for dielectrics
- (PE)CVD for polysilicon, a-Si, SiO_2, SiN_x @300^oC
- Electroplating for thick metals (Cu, Ni) up to 100 µm
- ALD for special cases:
  - very thin films (<100 nm);
  - 100% step coverage