Thermal oxidation of silicon

sami.franssila@aalto.fi

Thermal oxidation (at ~1000°C)

Dry oxidation:

$Si\ (s) + O_2\ (g) \rightarrow SiO_2\ (s)$

Wet oxidation:

$Si\ (s) + 2\ H_2O\ (g) \rightarrow SiO_2\ (s) + 2\ H_2\ (g)$

What happens to materials in oxygen at 1000^{o}C ?

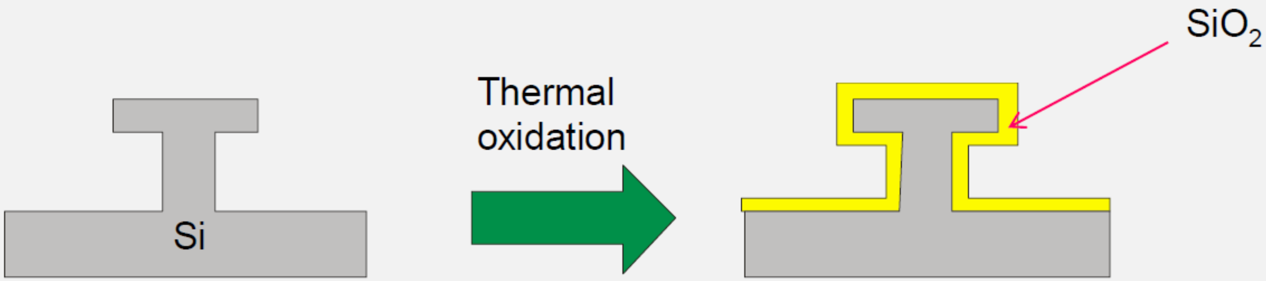
-silicon
-epitaxial silicon
-polysilicon
-amorphous silicon

oxidized into SiO_2

-silicon nitride: not affected
-metals: melted (Al m.p. 653°C)
-metals: oxidized (e.g. CuO)
(==> not conductive any more)
-metals: reacted with silicon (e.g. $TiSi_2$, conductor)
-polymers (e.g. resist): burned (CO_2; H_2O)

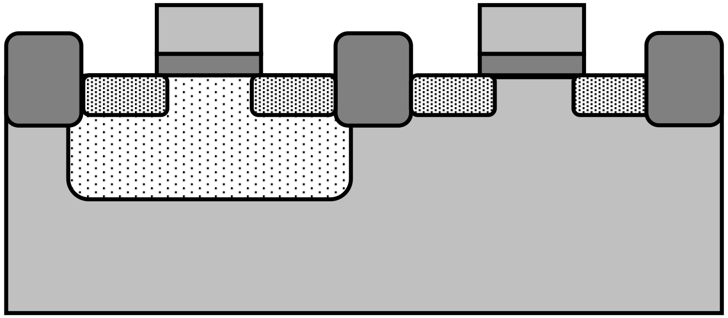
Thermal SiO_2 properties

- Excellent electrical insulator - high breakdown electric field
- Stable and reproducible Si/SiO_2 interface
- Selective oxidation with corresponding mask, e.g. Si_3N_4 (not PR)
- Good diffusion mask for common dopants
- Very good etching selectivity between Si and SiO_2
- Conformal oxide growth on exposed Si surface



Roles of silicon dioxide

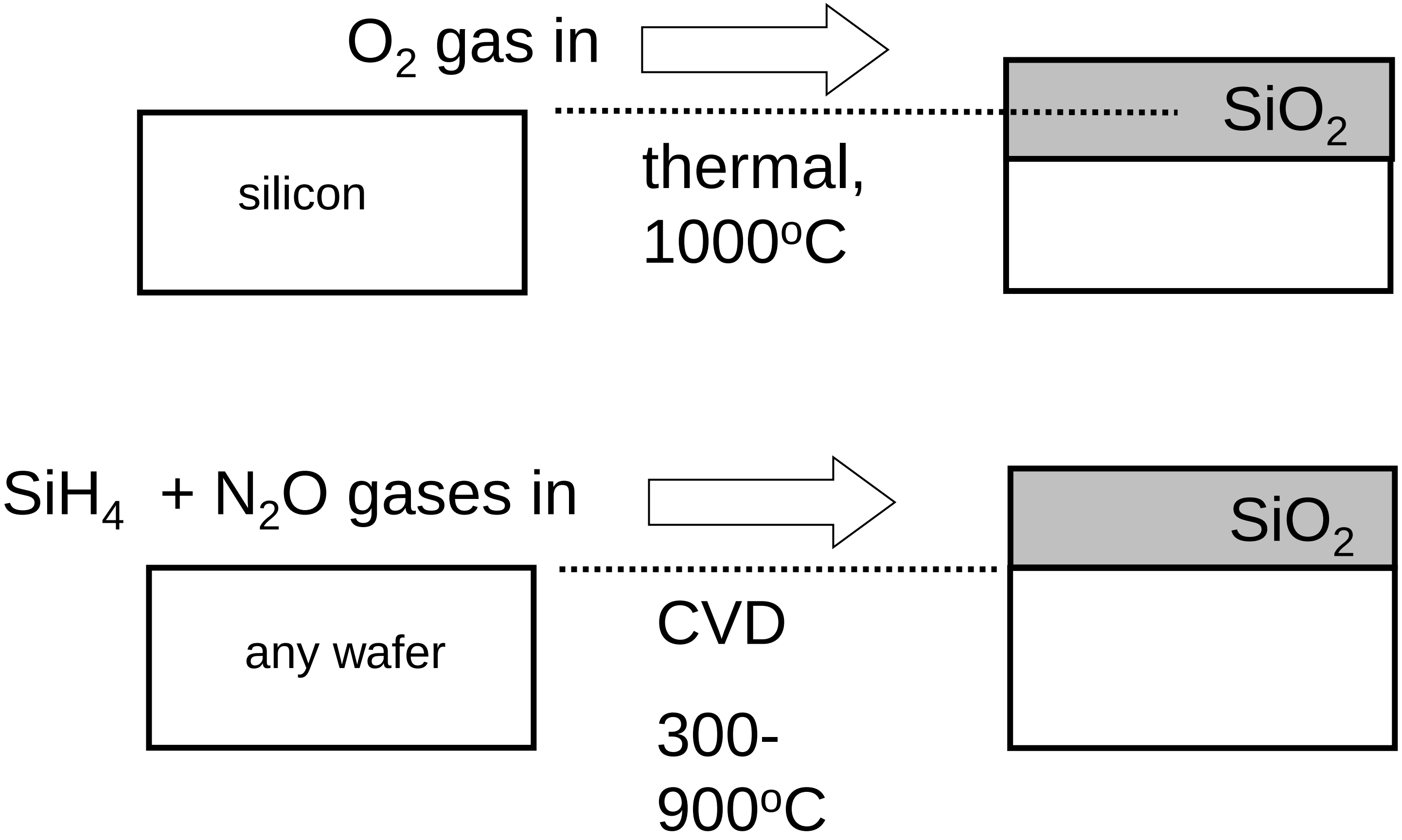
1. diffusion/implant mask (~1 µm)
2. surface passivation (a few nanometers and up)
3. transistor isolation (up to 1 µm)
4. gate oxide in MOS structures (5-25 nm)
5. structural and sacrificial layer in MEMS (~1 µm)



Videos

- Thermal oxidation
- https://www.youtube.com/watch?v=nzF8f6ocqXo

Thermal oxide vs. CVD oxide



O_2 gas in

silicon

thermal, 1000°C

SiO_2

Compressive stress always, silicon consumed

SiH_4 + N_2O gases in

any wafer

CVD

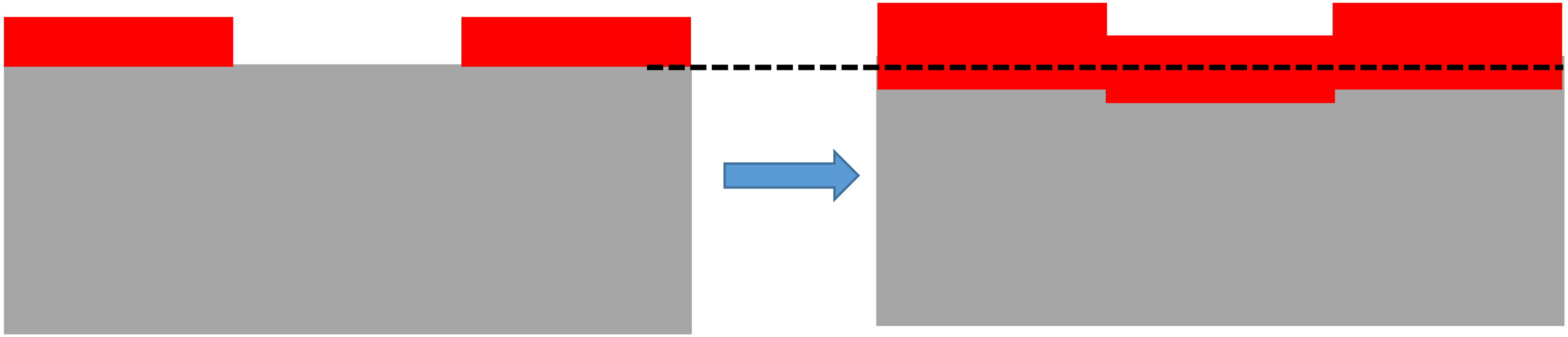
300-900°C

SiO_2

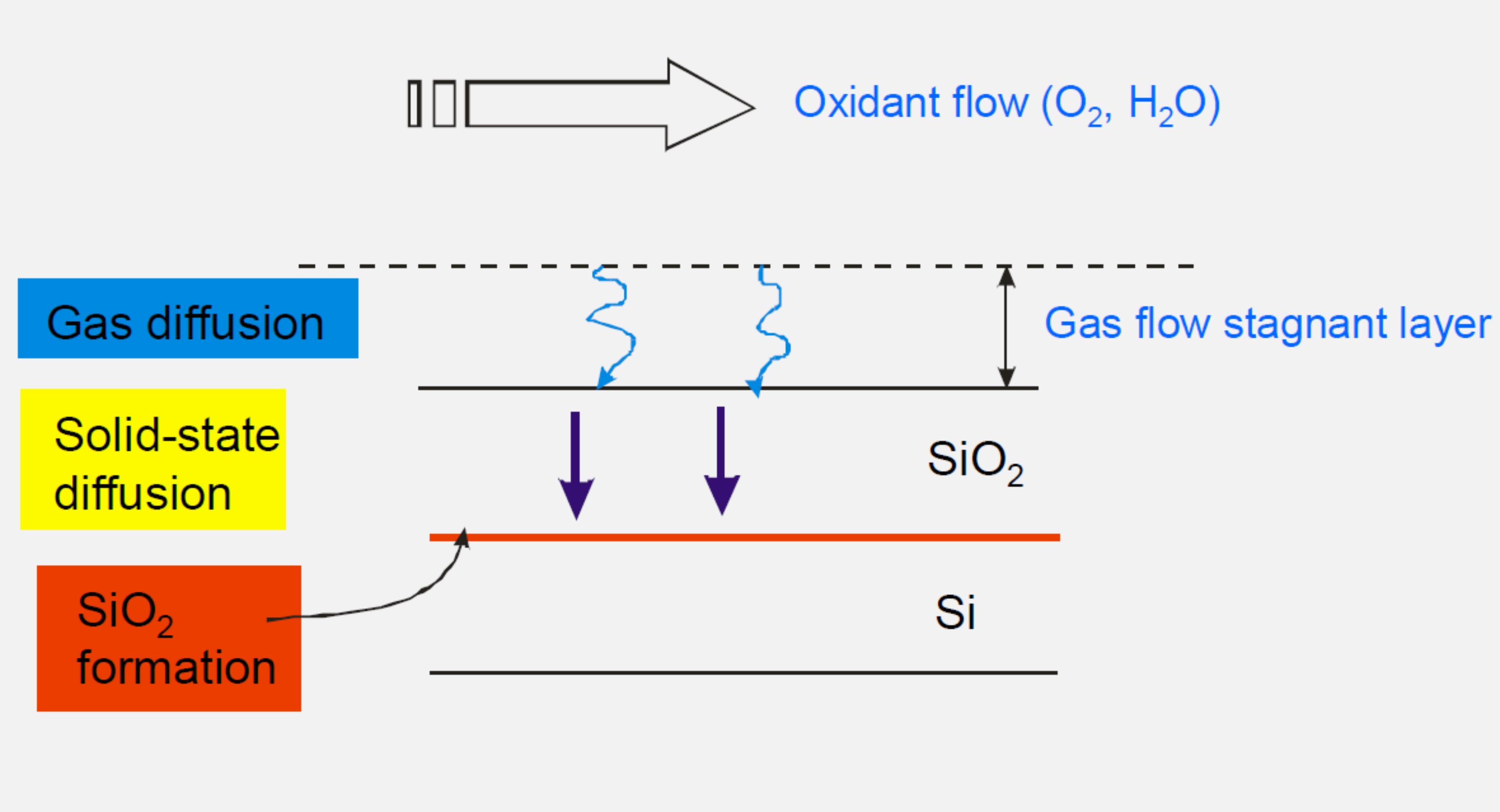
Stress can be tailored tensile or compressive, deposition also on metals

More thermal oxide

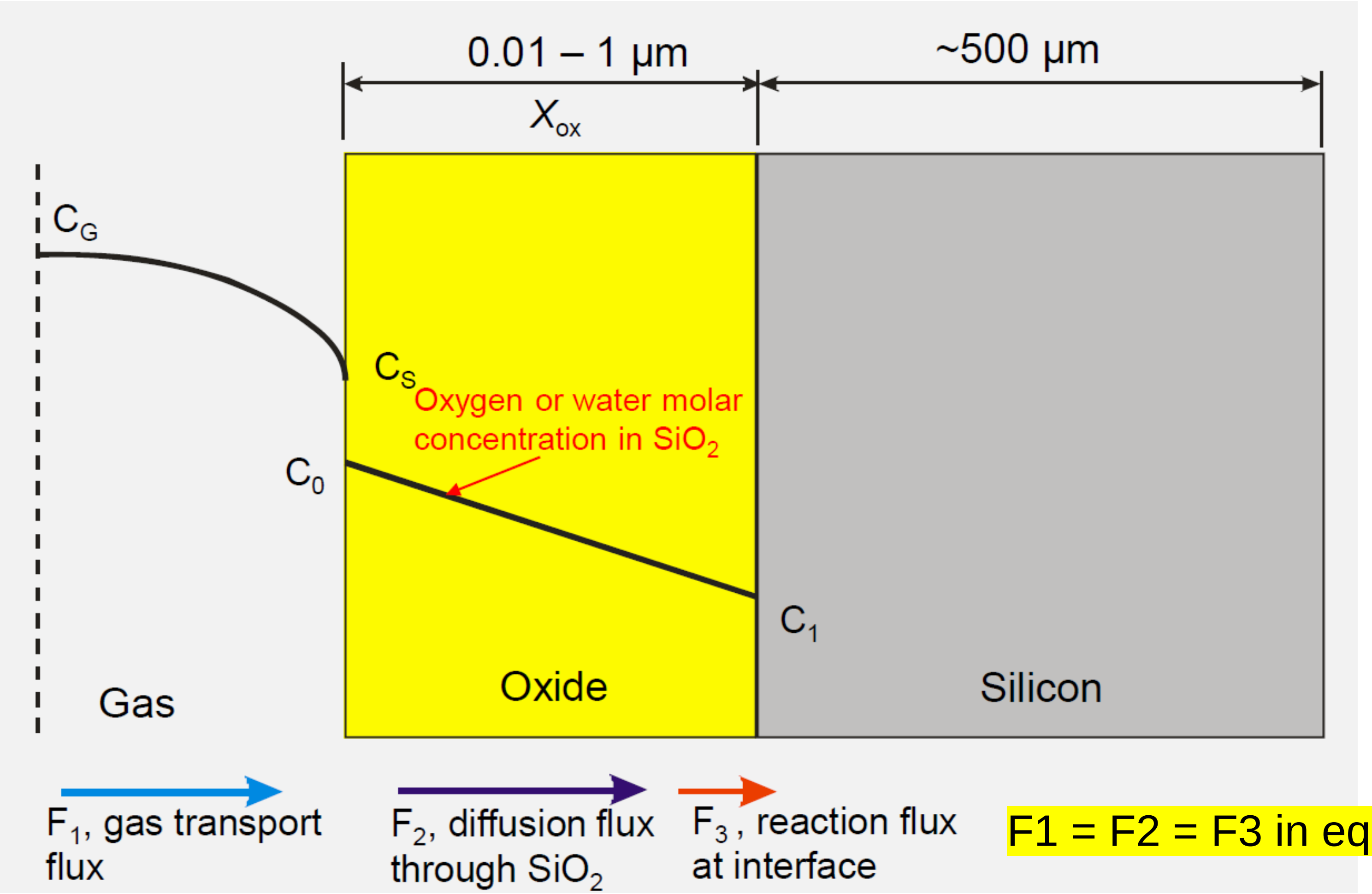
If there are both silicon and oxide areas exposed, oxidation will occur on both !



Oxidation overview



Deal-Grove oxidation model



F1 = F2 = F3 in equilibrium

Deal-Grove growth rates

General solution:

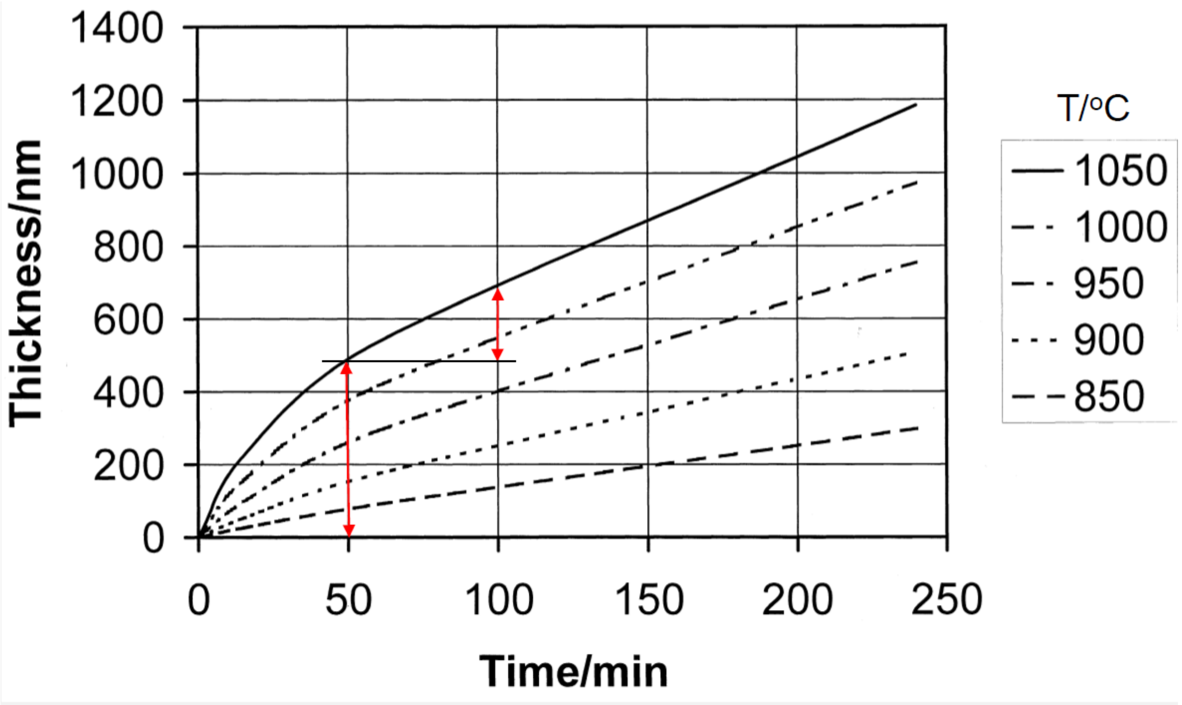
$$t = \frac{x}{kC_s v} + \frac{x^2}{2DC_s v}$$

Two useful approximations:

$$x = kC_s vt \qquad x < 100nm$$

$$x = \sqrt{2DC_s t} \qquad x > 100nm$$

Parabolic rate law: SQRT dependence

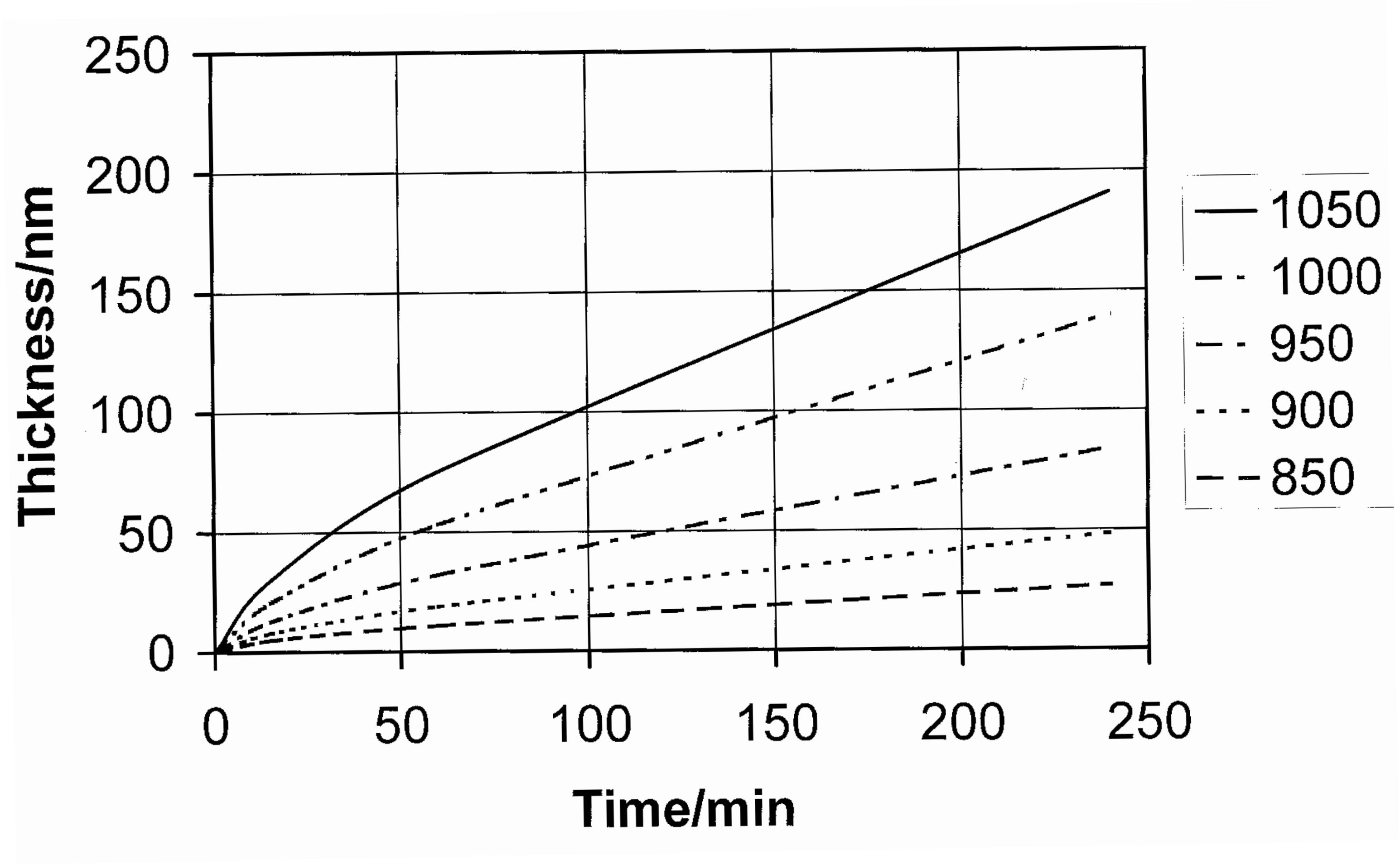


Simulator results, not very accurate.

Double thickness requires quadruple time !

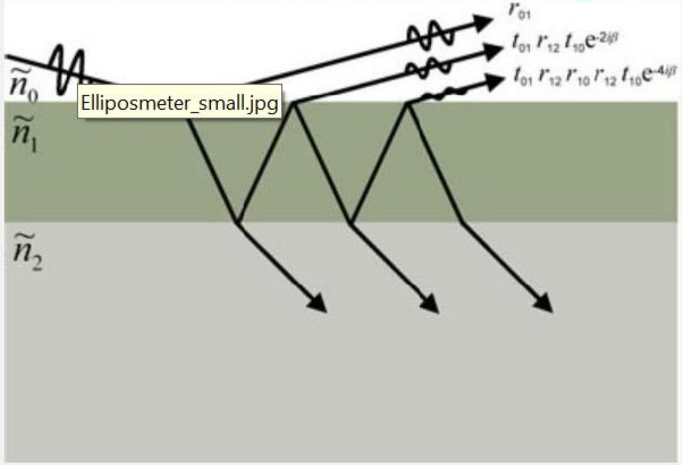
Doubling time only increases thickness by $\sqrt{2}$, or 50 min to 100 min ➔ 500 nm to 700 nm.

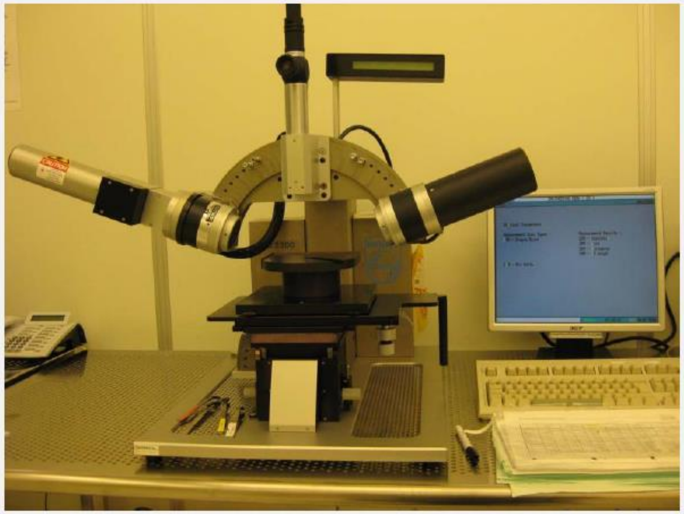
Dry oxidation is slower

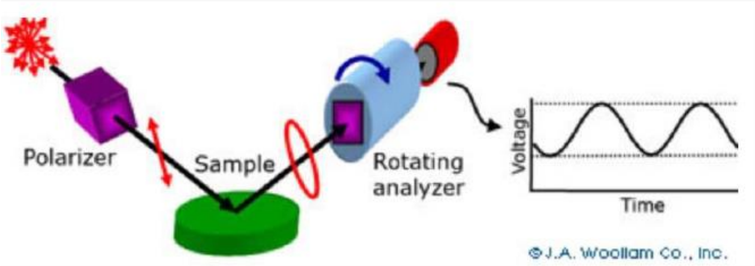


Oxide thickness measurement: ellipsometry

Interference is a reason of SiO_2 colour







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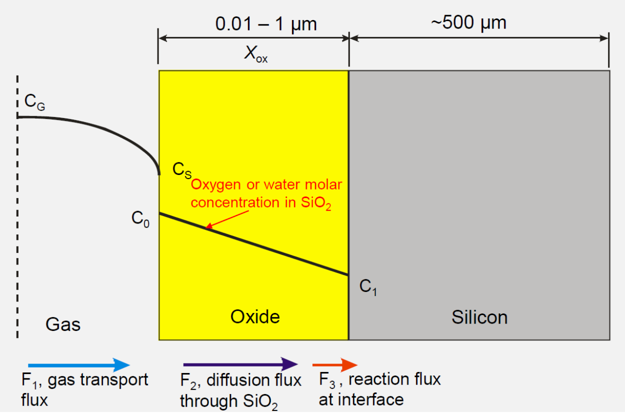
Best accuracy 0.1nm
Transparent films 10 – 1000 nm

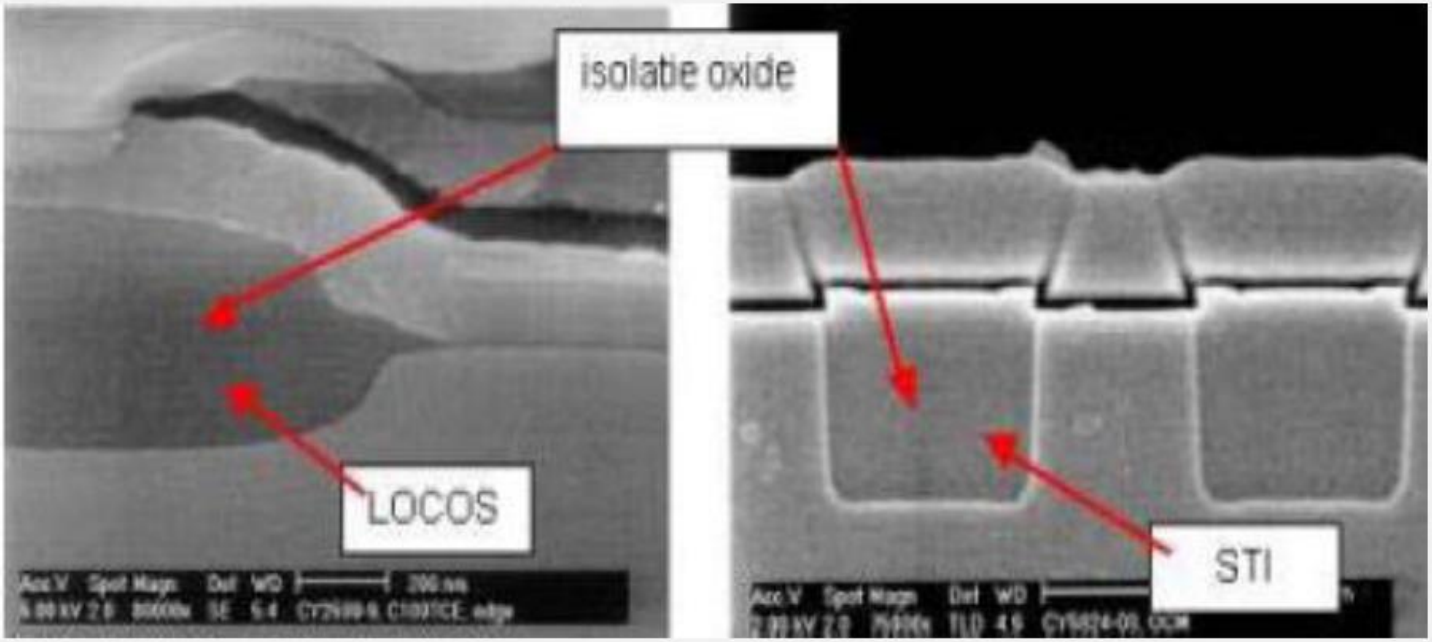
Wet vs dry



Oxygen diffusion thru oxide is faster than diffusion of H_2O ➔ you might think that dry oxidation is faster.

But water solubility in oxide is 1000X higher than soluibility of oxygen ➔ wet oxidation is faster even though individual molecules diffuse slower.

Device isolation: LOCOS vs. STI



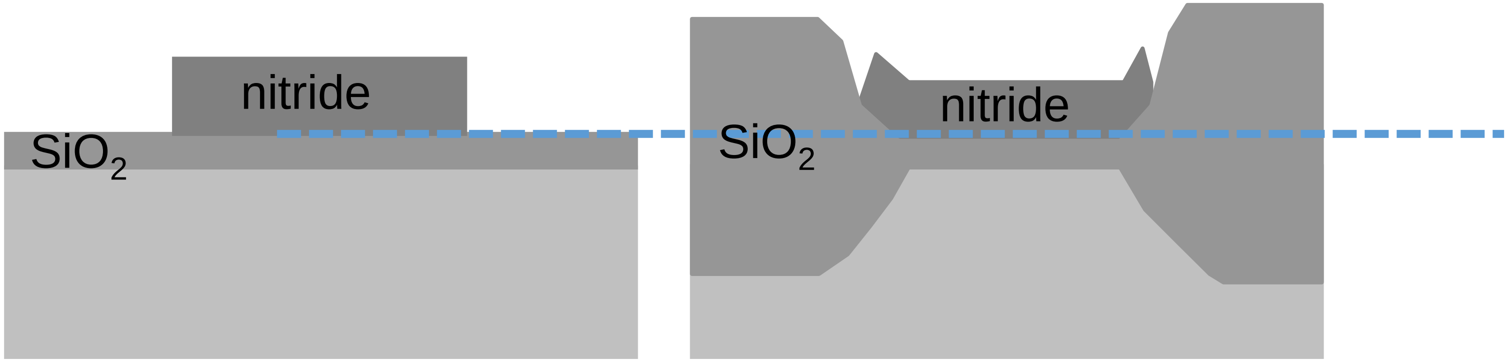
STI – shallow trench isolation

Thermal oxide

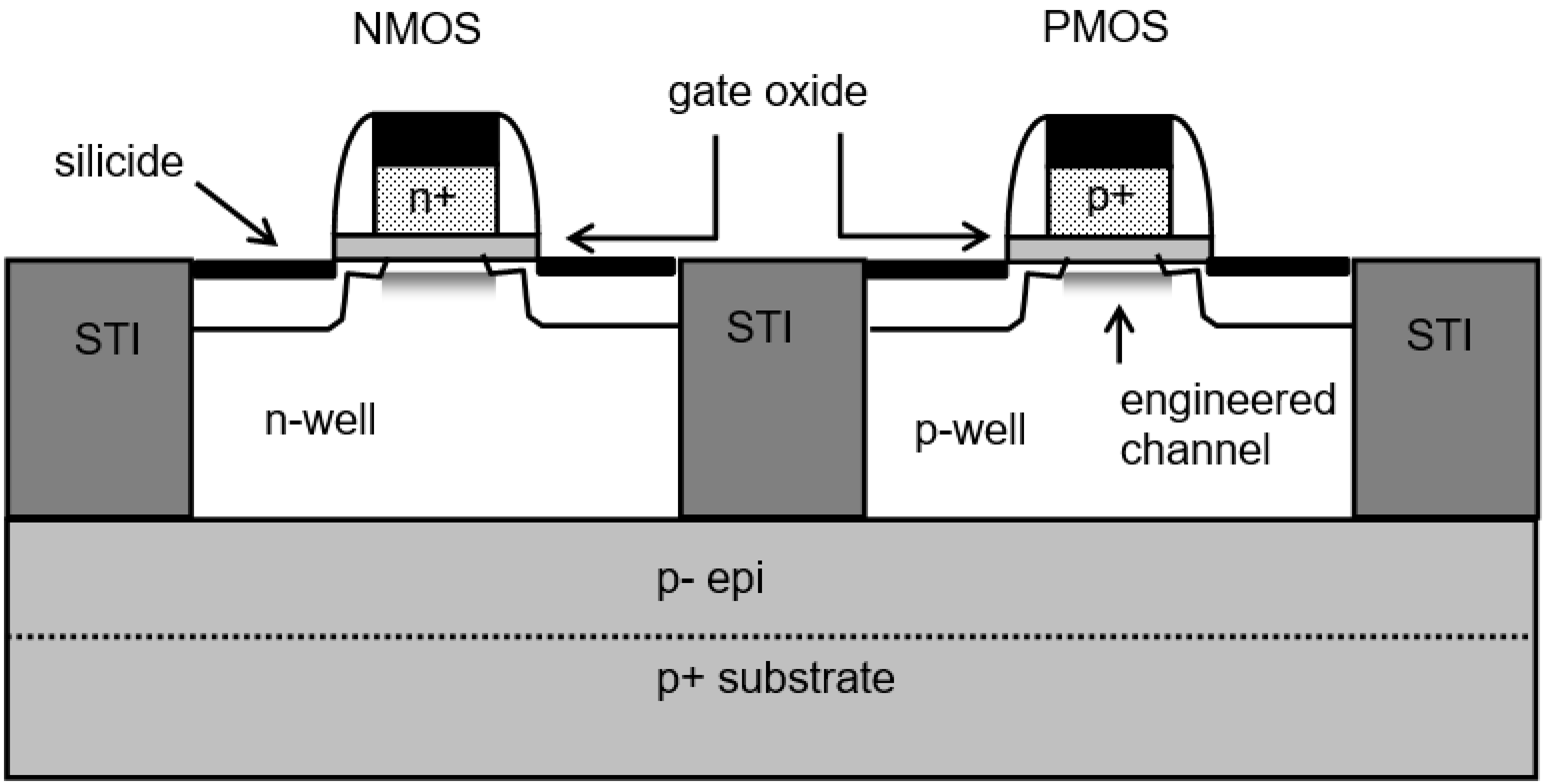
Thermal + deposited oxides

Local oxidation of silicon (LOCOS)

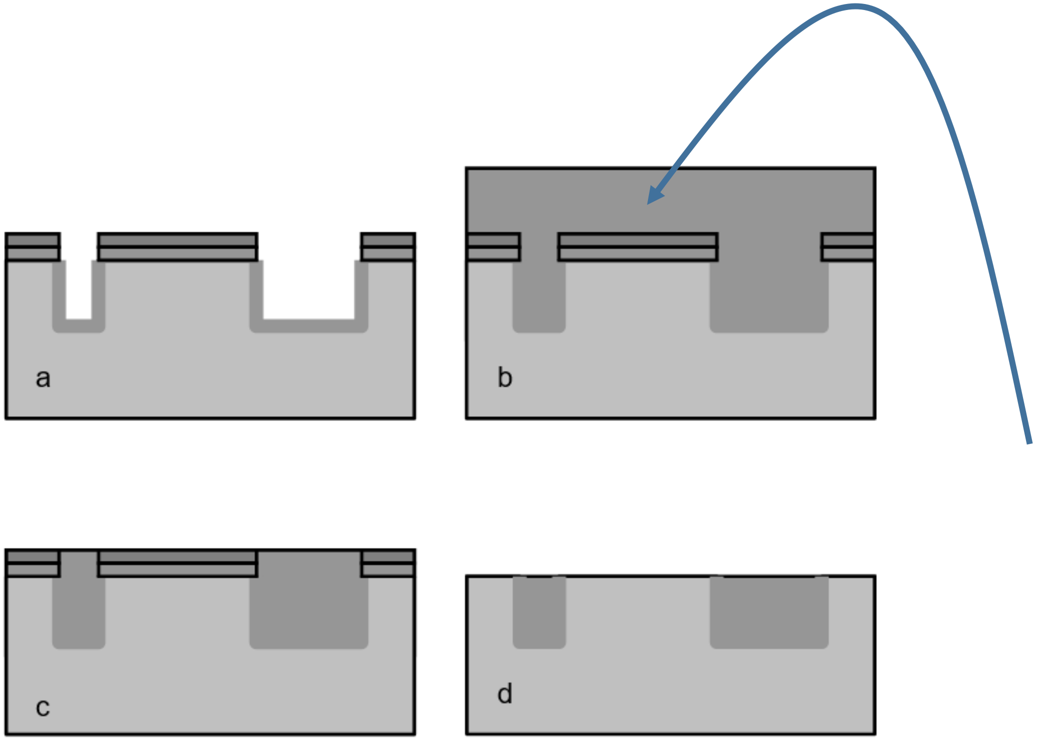
- Nitride prevents oxygen diffusion ➔ oxidation areas defined by nitride lithography & etching



STI: Shallow trench isolation

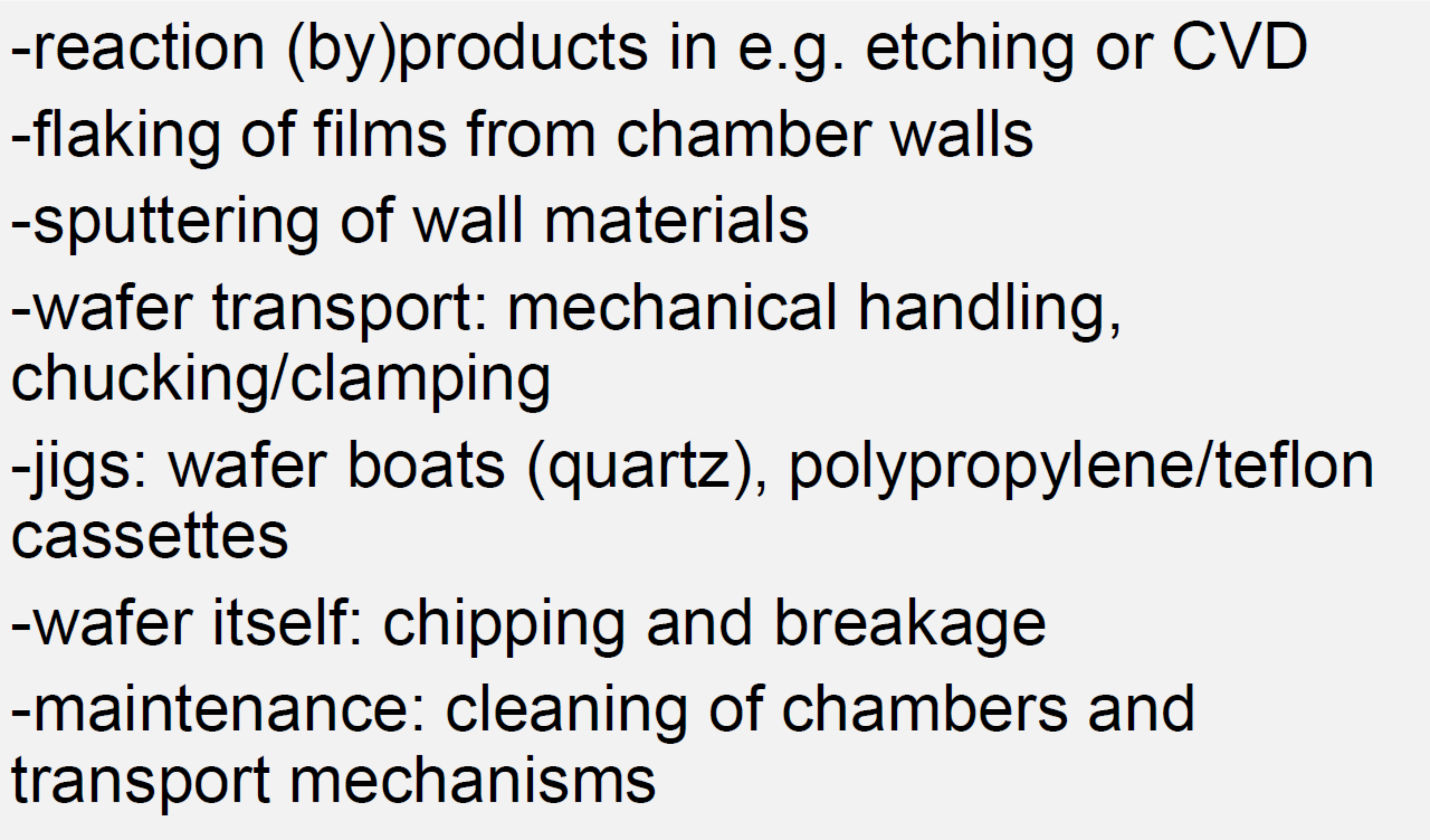


STI process



pad oxide (thermal)
pad nitride (LPCVD)
lithography
etching nitride/oxide/silicon
resist strip and cleaning
liner oxide (thermal)
CVD oxide deposition
CMP planarization of the oxide
Nitride etching
Oxide etching

Contamination sources



-reaction (by)products in e.g. etching or CVD

-flaking of films from chamber walls

-sputtering of wall materials

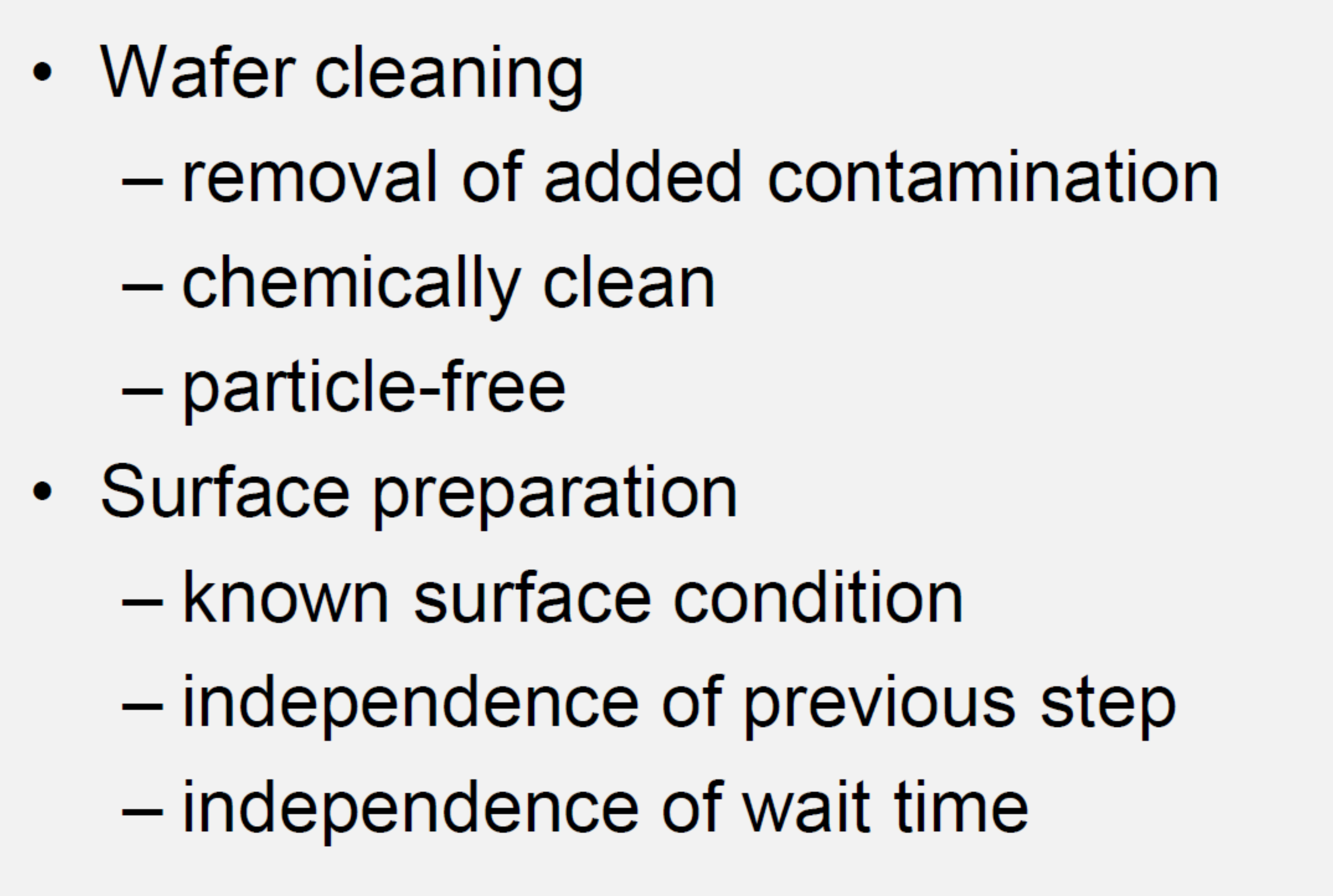
-wafer transport: mechanical handling, chucking/clamping

-jigs: wafer boats (quartz), polypropylene/teflon cassettes

-wafer itself: chipping and breakage

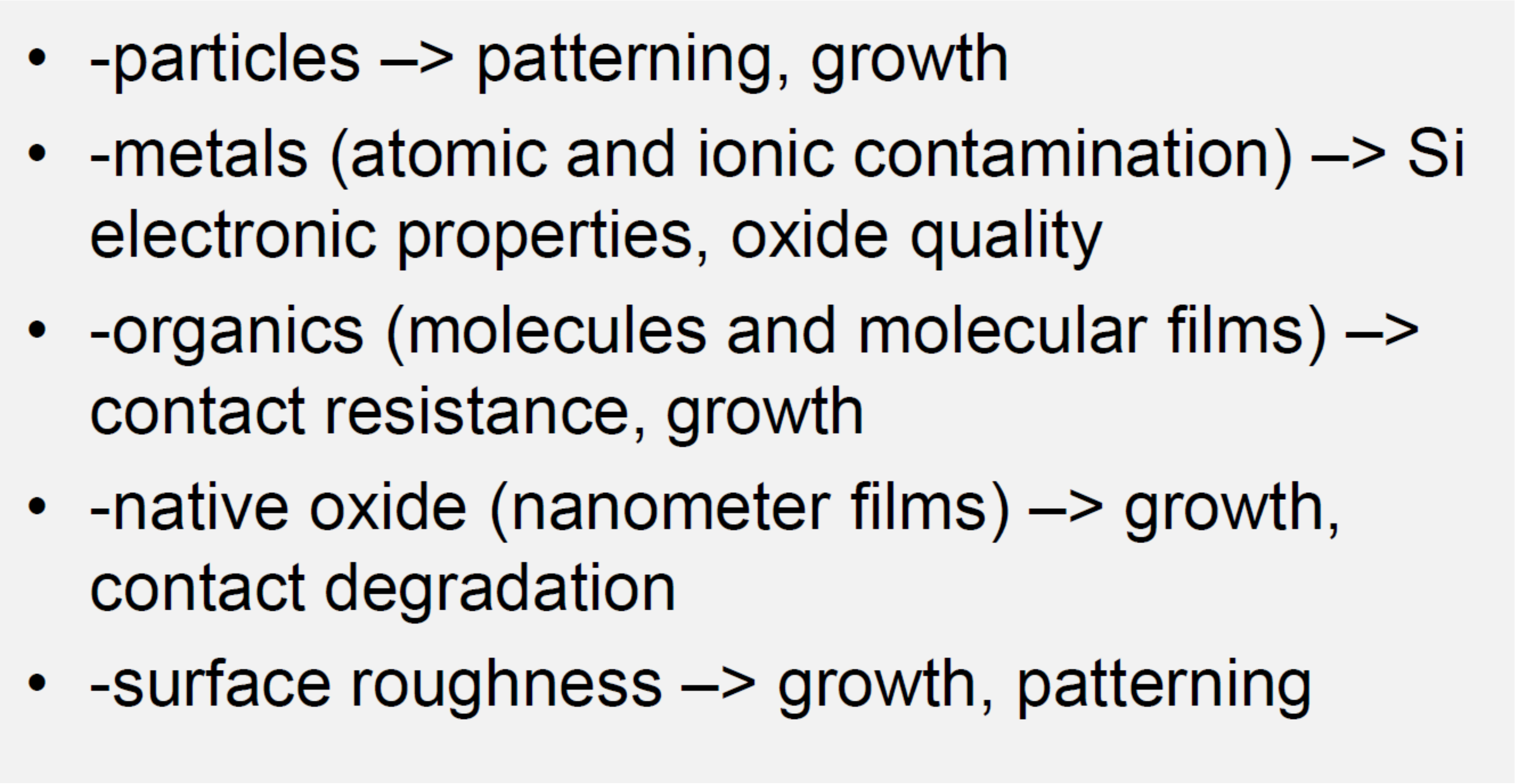
-maintenance: cleaning of chambers and transport mechanisms

Cleaning vs. surface preparation



- Wafer cleaning
  - removal of added contamination
  - chemically clean
  - particle-free
- Surface preparation
  - known surface condition
  - independence of previous step
  - independence of wait time

Contamination effects

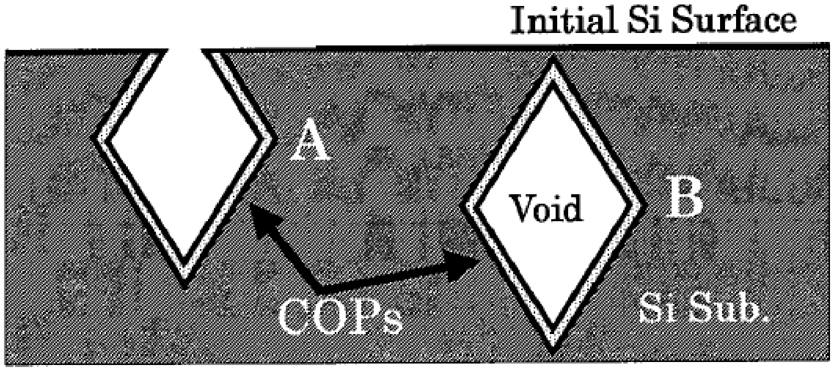


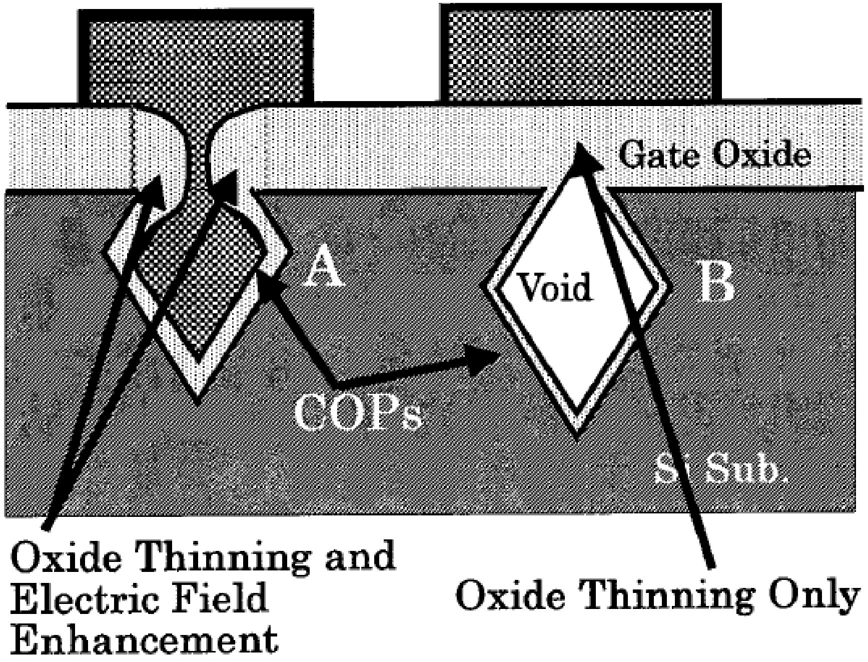
- -particles –> patterning, growth
- -metals (atomic and ionic contamination) –> Si electronic properties, oxide quality
- -organics (molecules and molecular films) –> contact resistance, growth
- -native oxide (nanometer films) –> growth, contact degradation
- -surface roughness –> growth, patterning

Oxide defects

COP defects (pits)

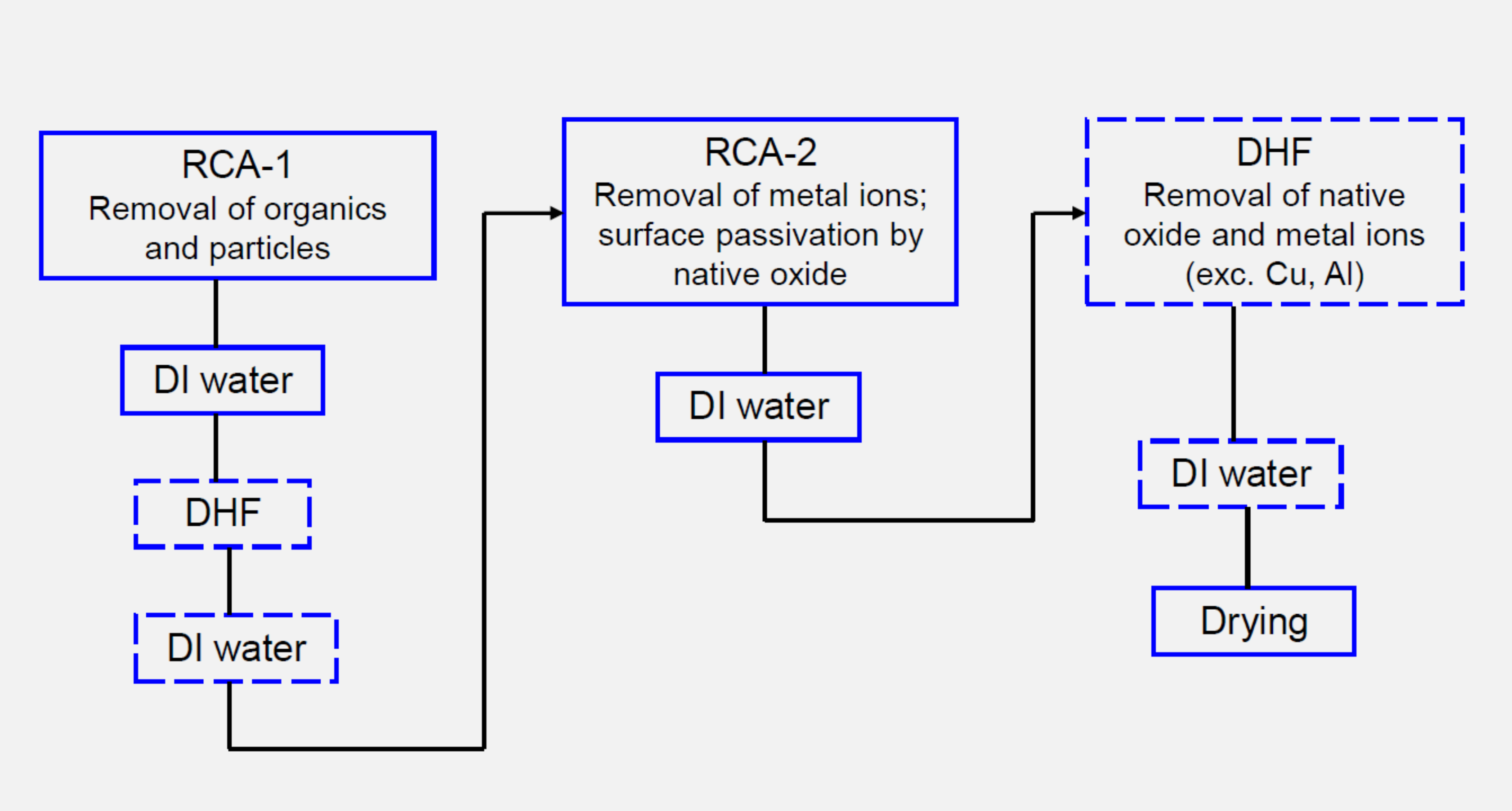
After thermal oxidation and polysilicon capacitor electrodes





Yamabe et al: Journal of The Electrochemical Society, 150 ~3! F42-F46 ~2003!

Pre-oxidation cleaning



RCA-1
Removal of organics and particles

DI water

DHF

DI water

RCA-2
Removal of metal ions; surface passivation by native oxide

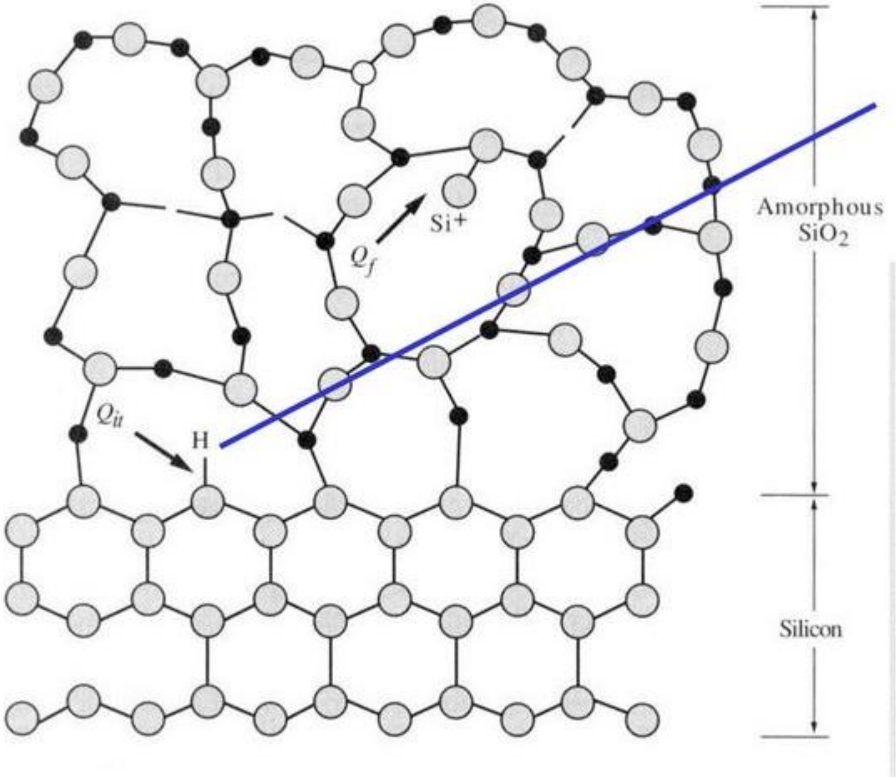
DI water

DHF
Removal of native oxide and metal ions (exc. Cu, Al)

DI water

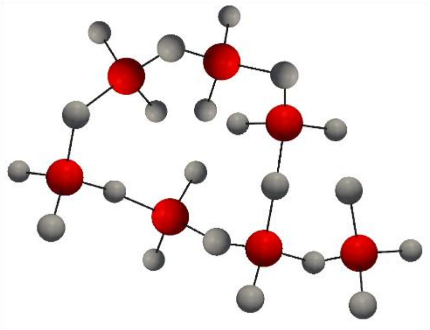
Drying

Defects at Si/SiO_2 interface



Dangling bonds create havoc by allowing charge to stick

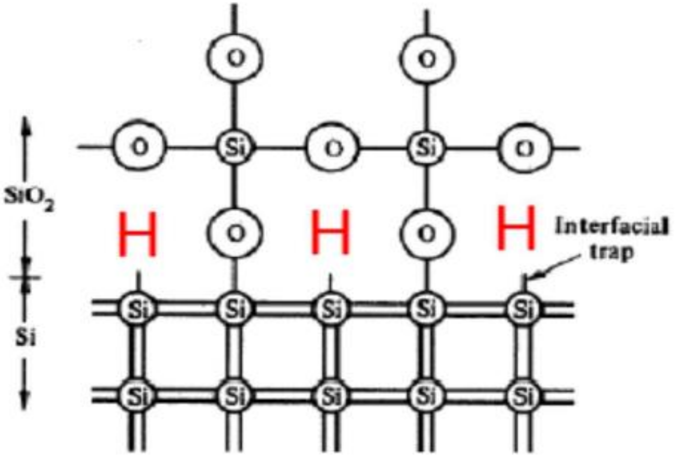
Amorphous and crystalline material cannot match exactly ➔ defects at interface



Six silicon atoms in a ring formation is the basic element of oxide

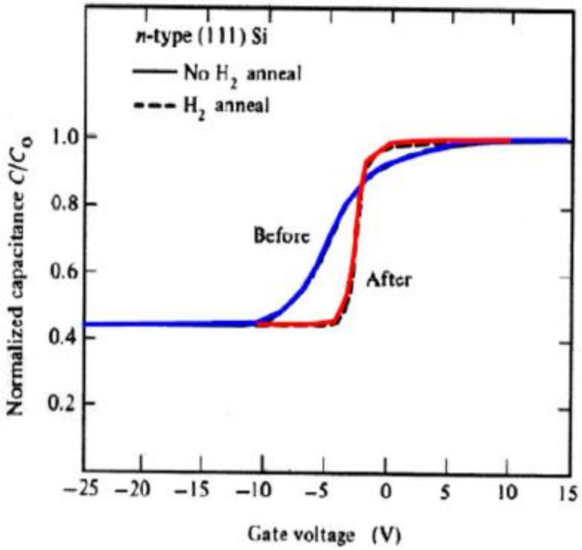
Plummer, Deal, Griffen: VLSI

Interface (in)stability



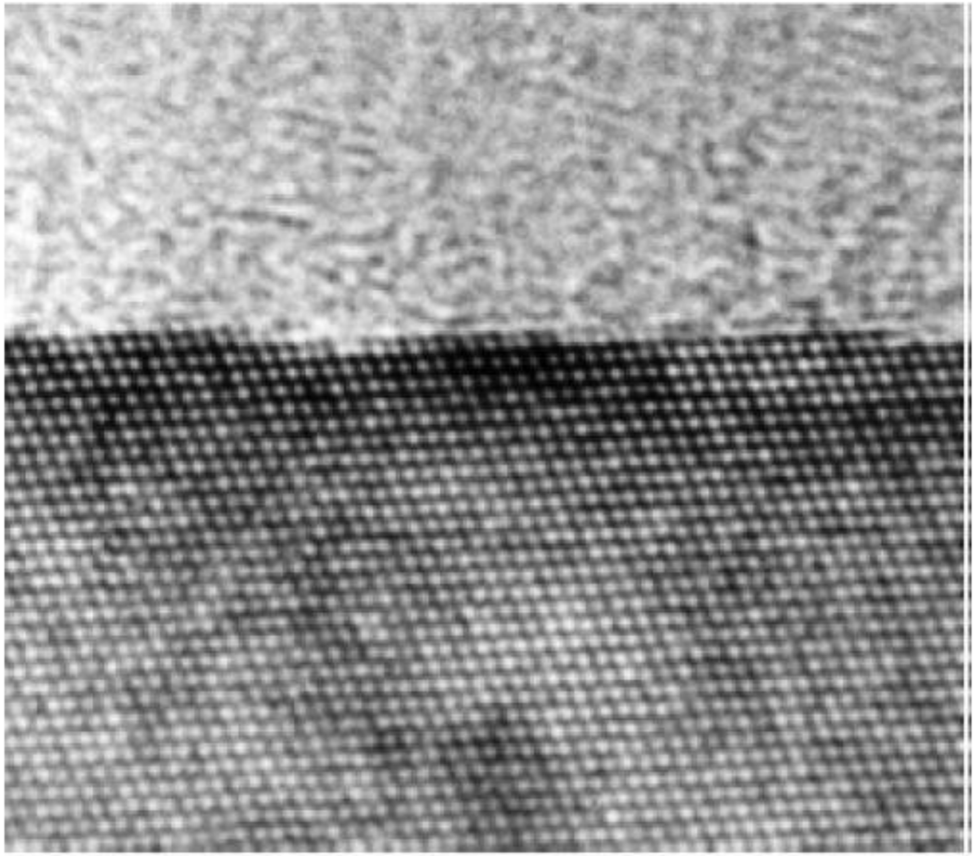
Dangling bonds can be stabilized by hydrogen treatment.

But hydrogen easily diffuses away at elevated temperatures.



CV-measurement: Broad if dangling bonds present; narrow if bonds terminated by H.

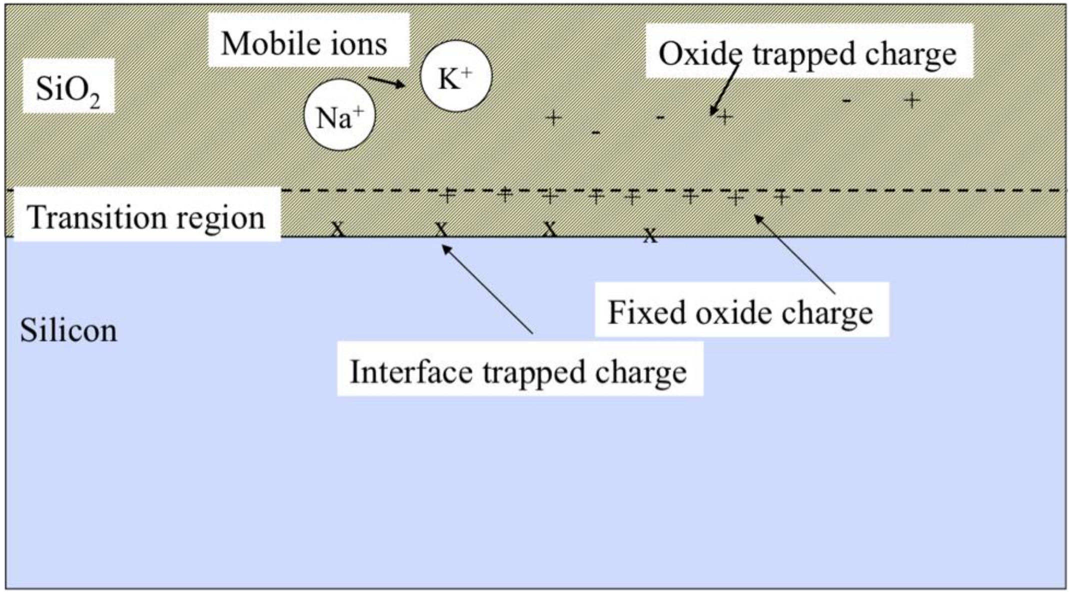
The Si/SiO$_2$ interface



(Photo courtesy of J. Bravman.)

In HRTEM we can see atoms but not dangling bonds.

Oxide microdefects



Dangling bonds at interface

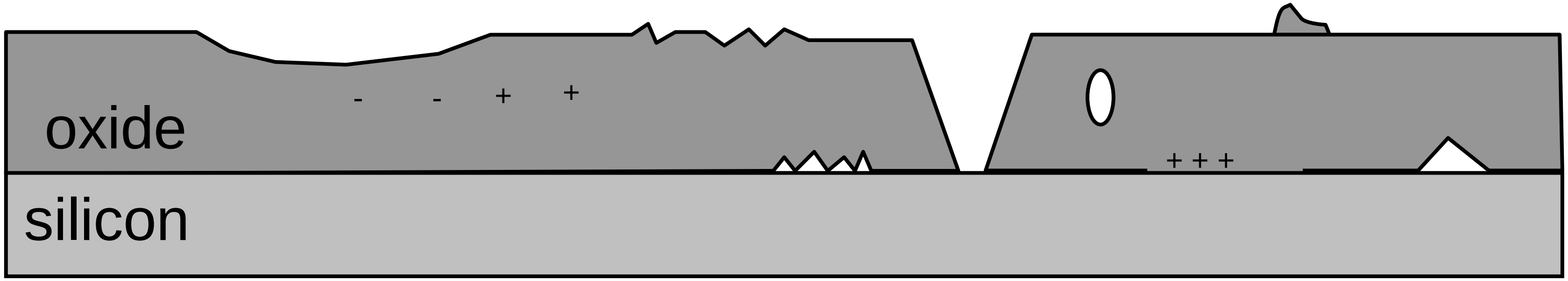
Fixed charge at interface.

Charged defects in oxide bulk

Impurity atoms/ions: Na & K mobile

https://www.semitracks.com/newsletters/april/2015-april-newsletter.php

Gross oxide defects



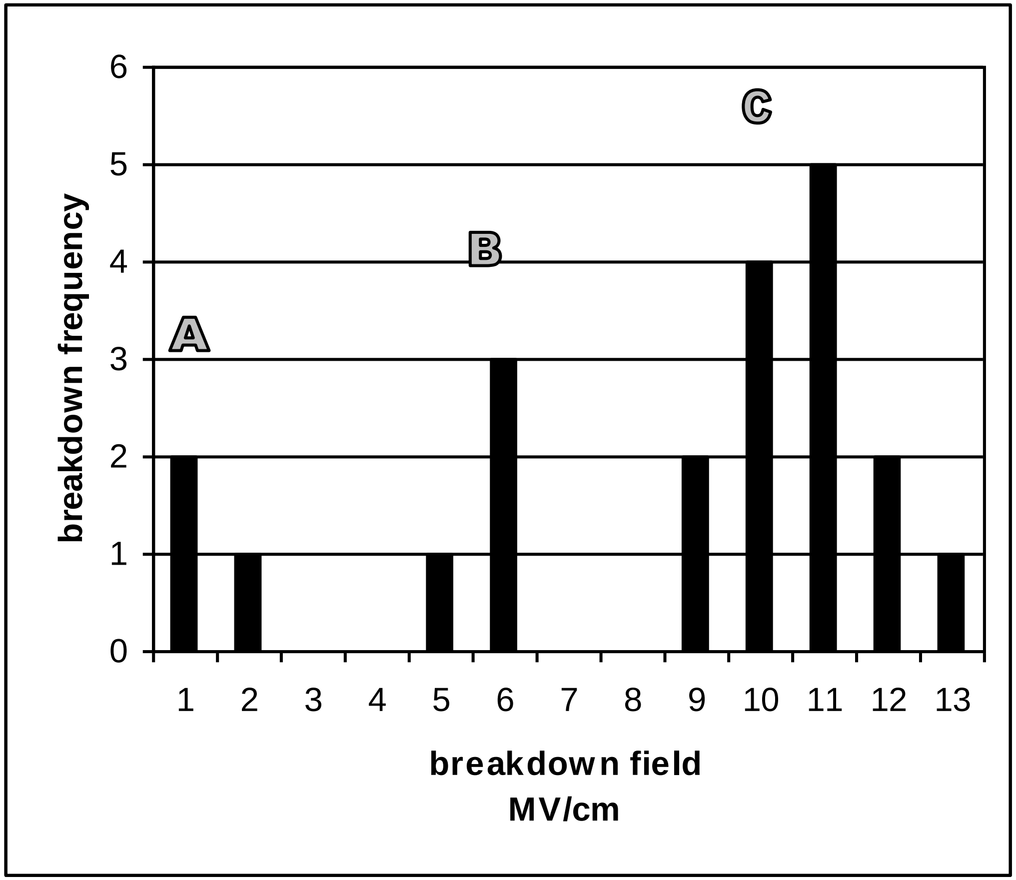
- thinning
- roughness
- pinholes

Something has prevented oxidation locally

- voids
- particles
- stacking faults

Failure in surface prep: not good enough starting surface, or particles have prevented growth

Oxide electrical quality



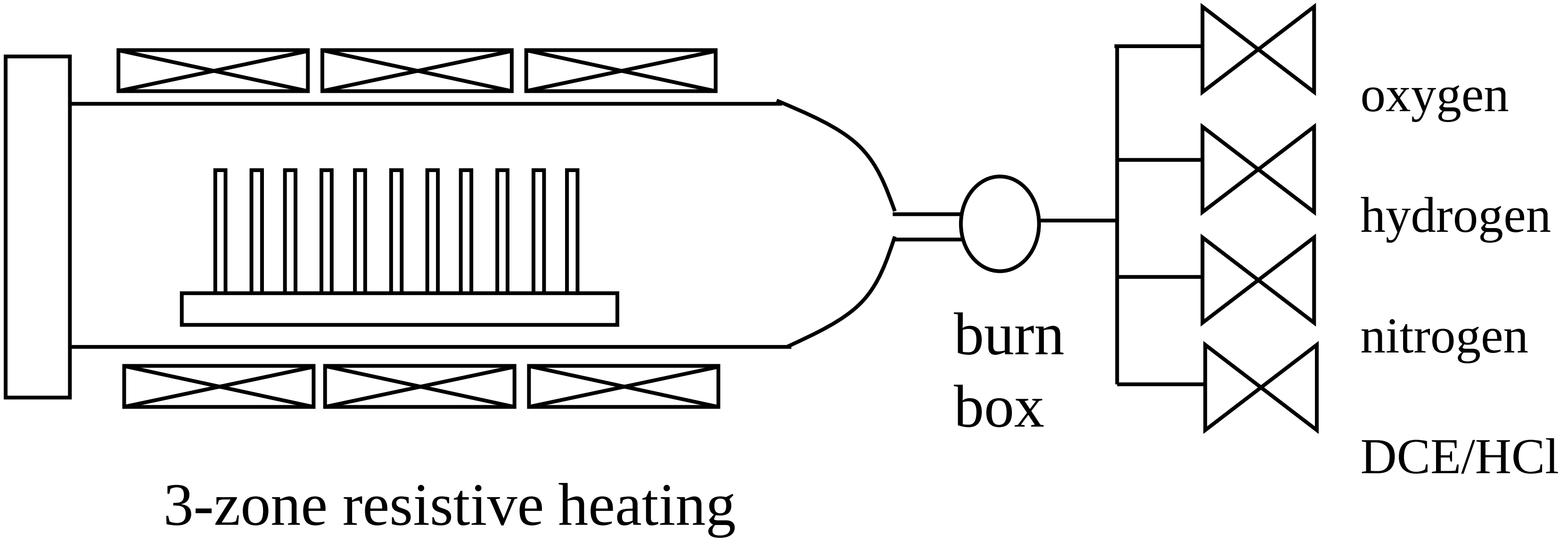
A-mode defects:
Big problems, e.g. voids.

B-mode defects:
Small problems: thinning, roughnening, impurity atoms, …

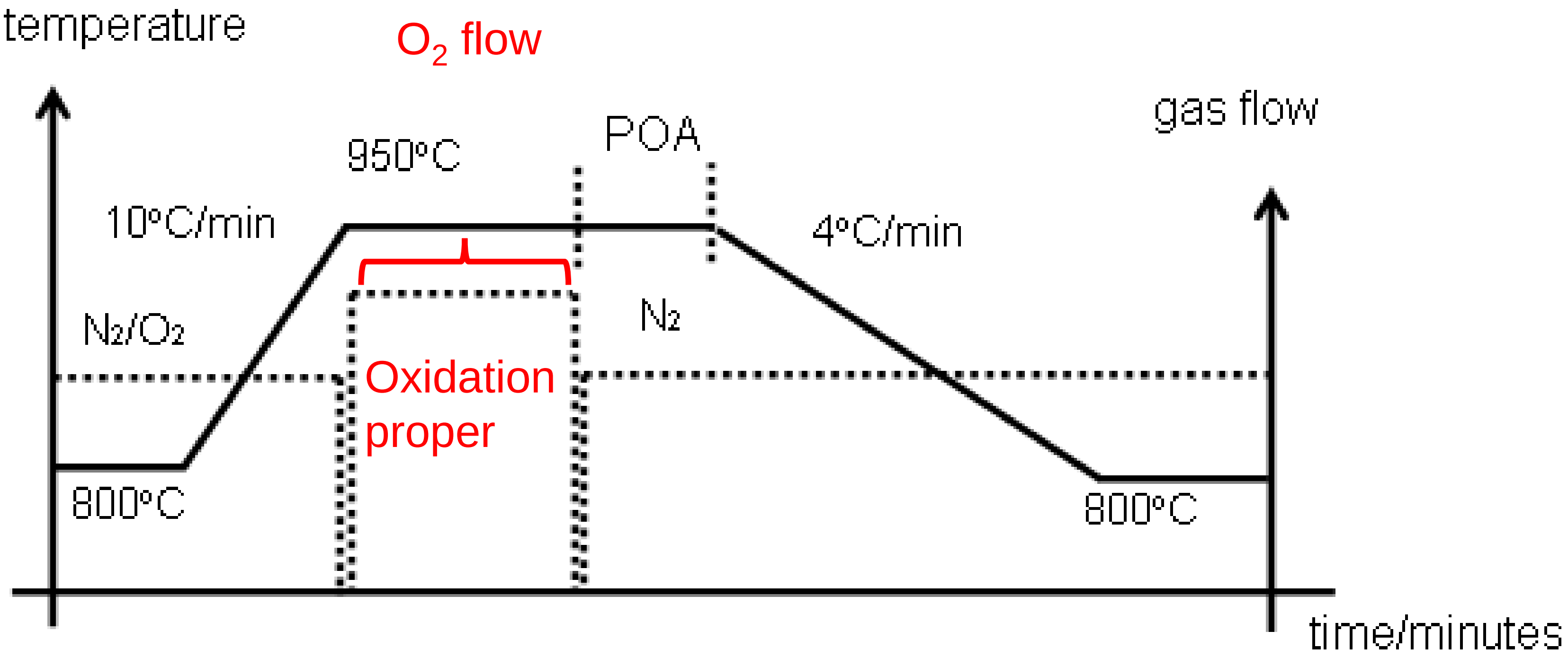
C-mode defects:
Fundamental oxide quality, strength of chemical bonds and uniformity of oxide

Breakdown field: $E = V/d$; $E_{BD} = V_{max}/d$

Oxidation furnace



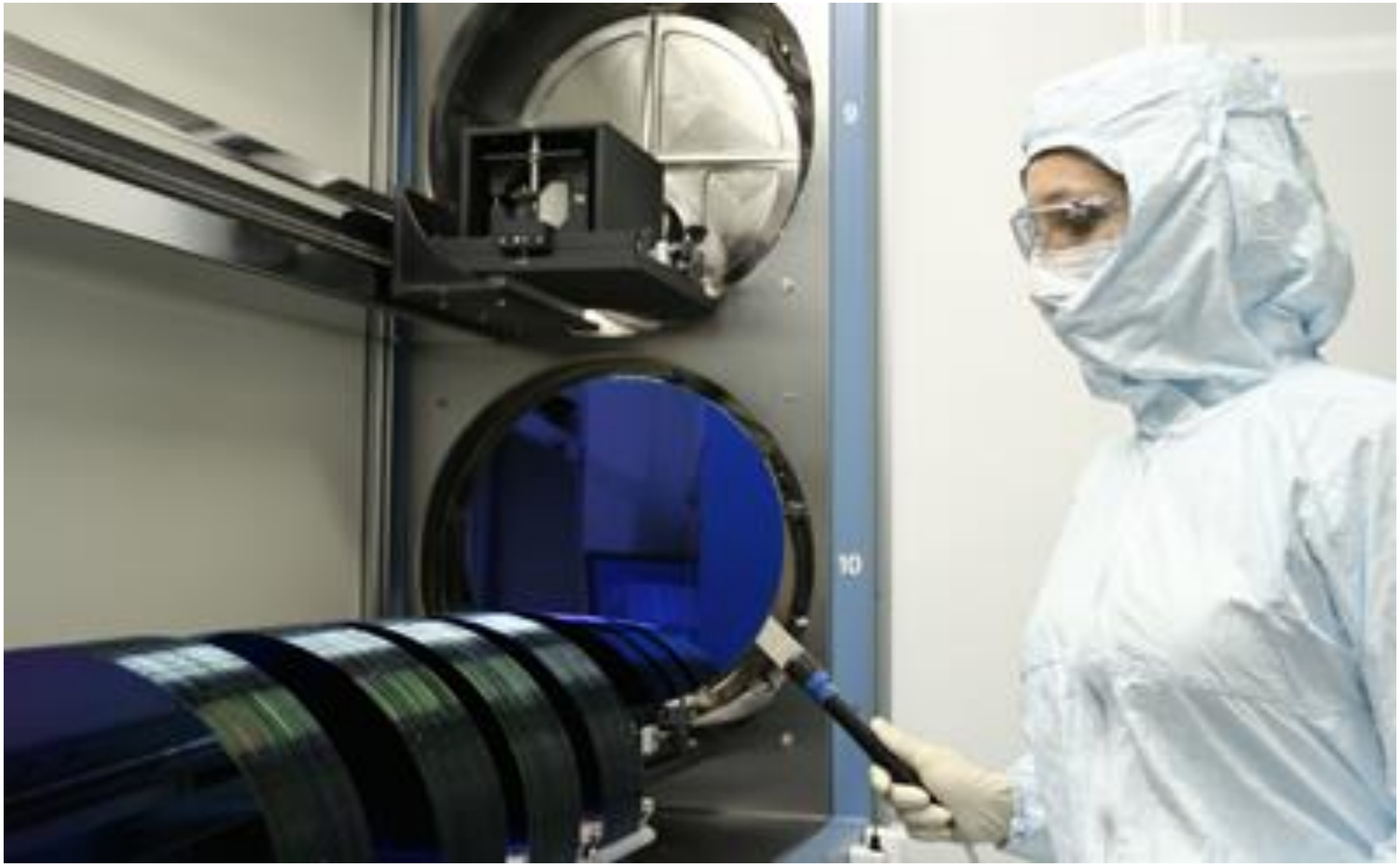
Practical oxidation



POA: post oxidation anneal. Oxide thickness unchanged but densification and some defect elimination.

Franssila: Introduction to Microfabrication

Furnace for 300 mm wafers



Oxidation of polysilicon

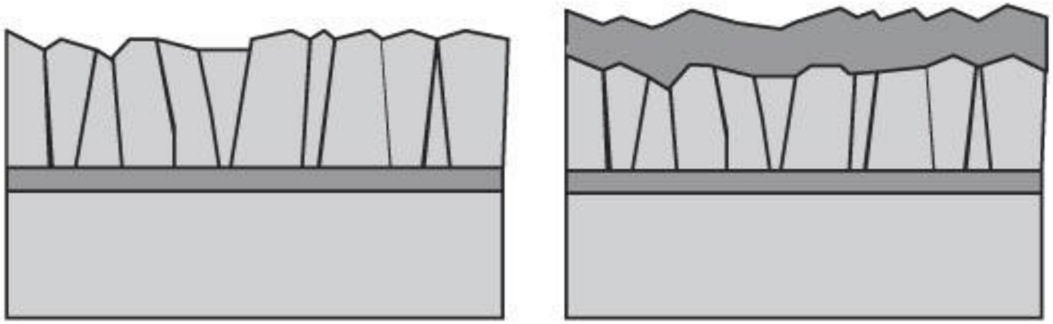
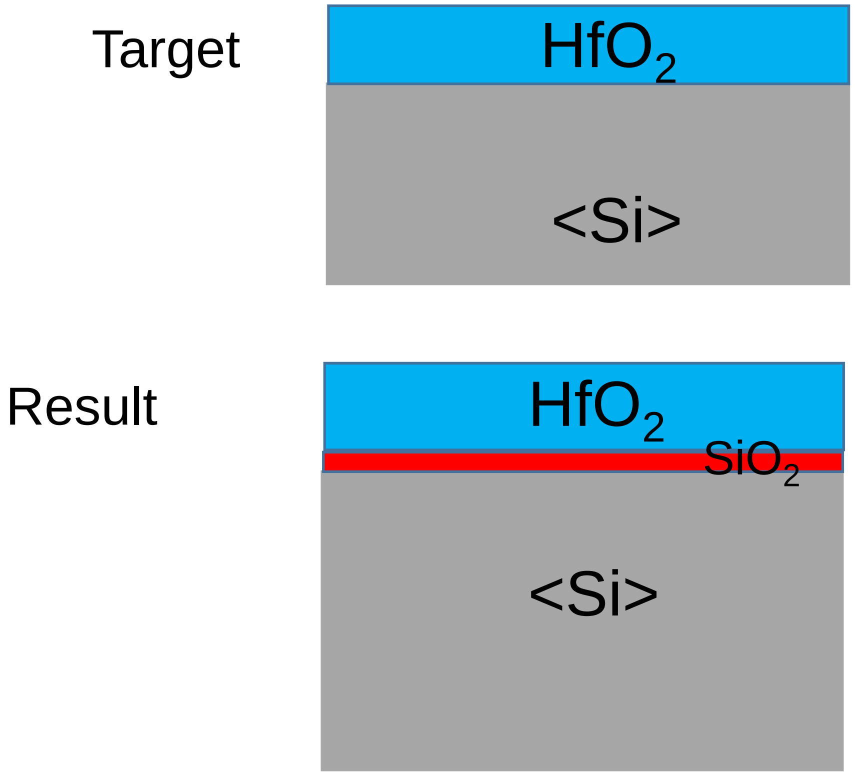


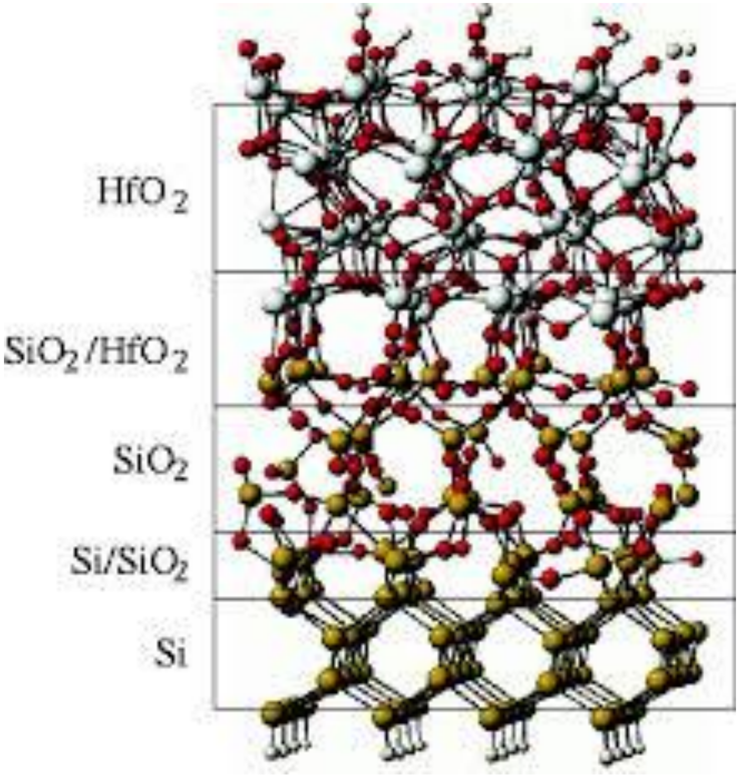
Figure 13-5

Polysilicon is rough and consists of grains of different orientations, which oxidize at slightly different rates, leading to rough oxide with non-uniform thickness.

$$Si\ (s) + O_2\ (g) \Longrightarrow SiO_2\ (s)$$

ALD HfO_2/Si interface

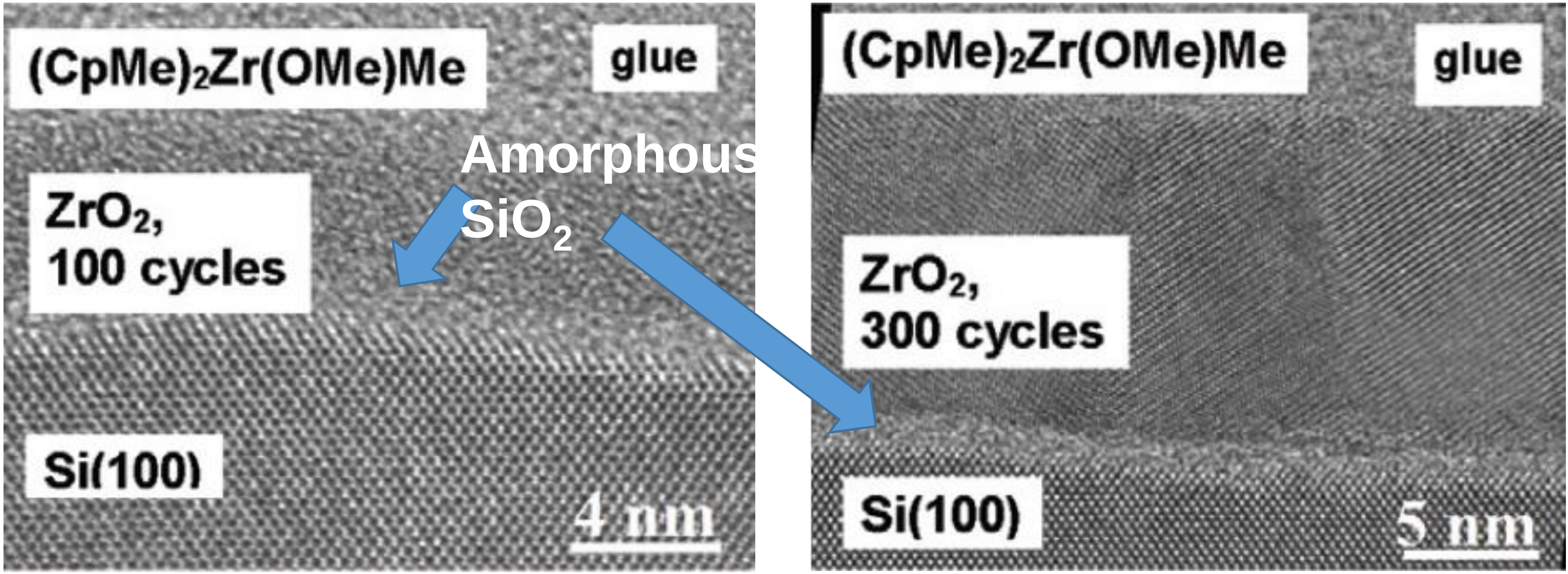




Silicon is easily oxidized, and when we introduce oxygen to deposit HfO_2, silicon turns to SiO_2.

Gavartin: Modeling HfO2/SiO2/Si interface, 2007

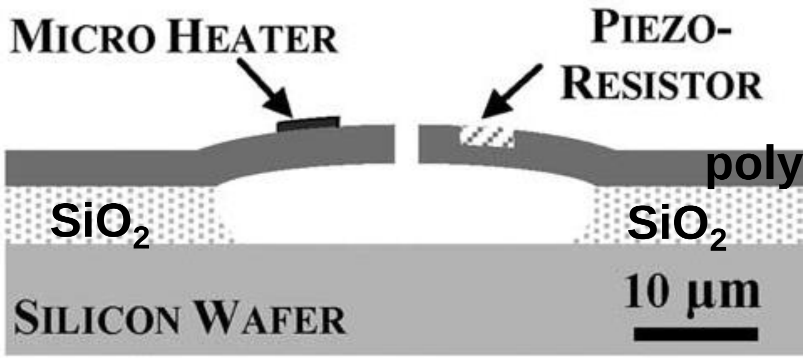
When depositing ALD oxides ➔ thermal SiO_2

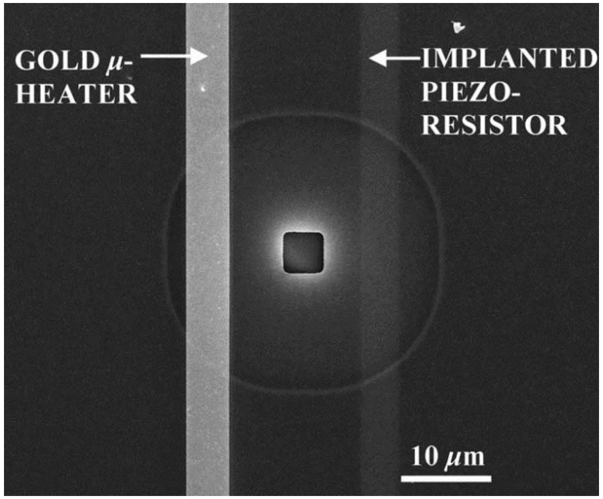


Amorphous SiO_2

ref. Kukli 2007.

Oxide as sacrificial material



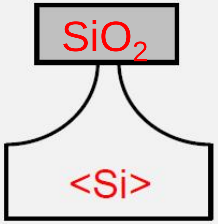


Isotropic HF wet etching of oxide under polysilicon
➔ Membrane is released and can move (=vibrate according to cyclic thermal expansion induced by cyclic heating the gold wire)

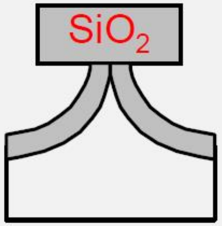
H. G. Craighead

Oxidation for silicon tip fabrication

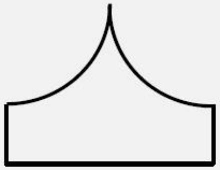
Isotropic Si etching

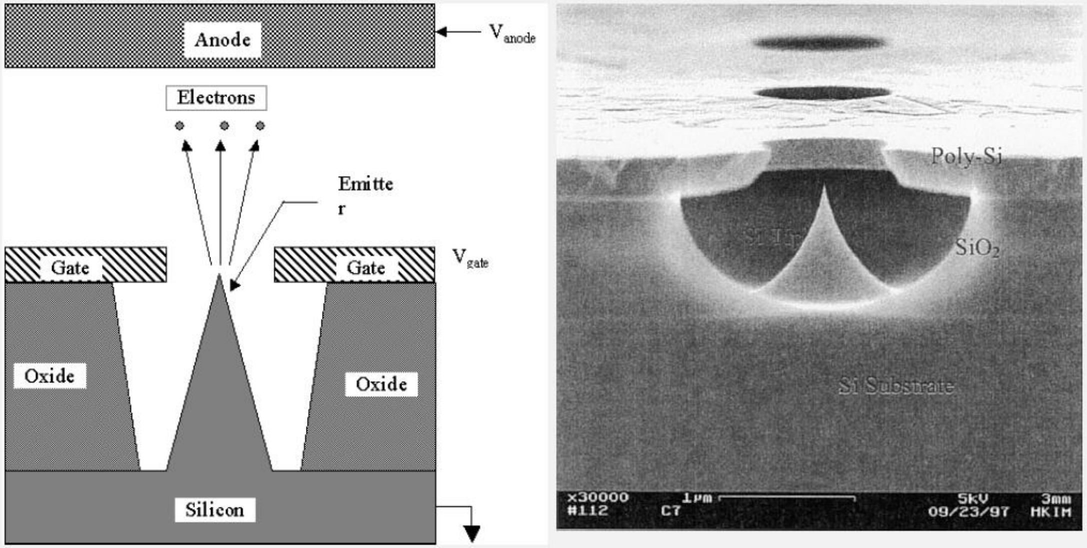


Thermal oxidation



SiO_2 etching

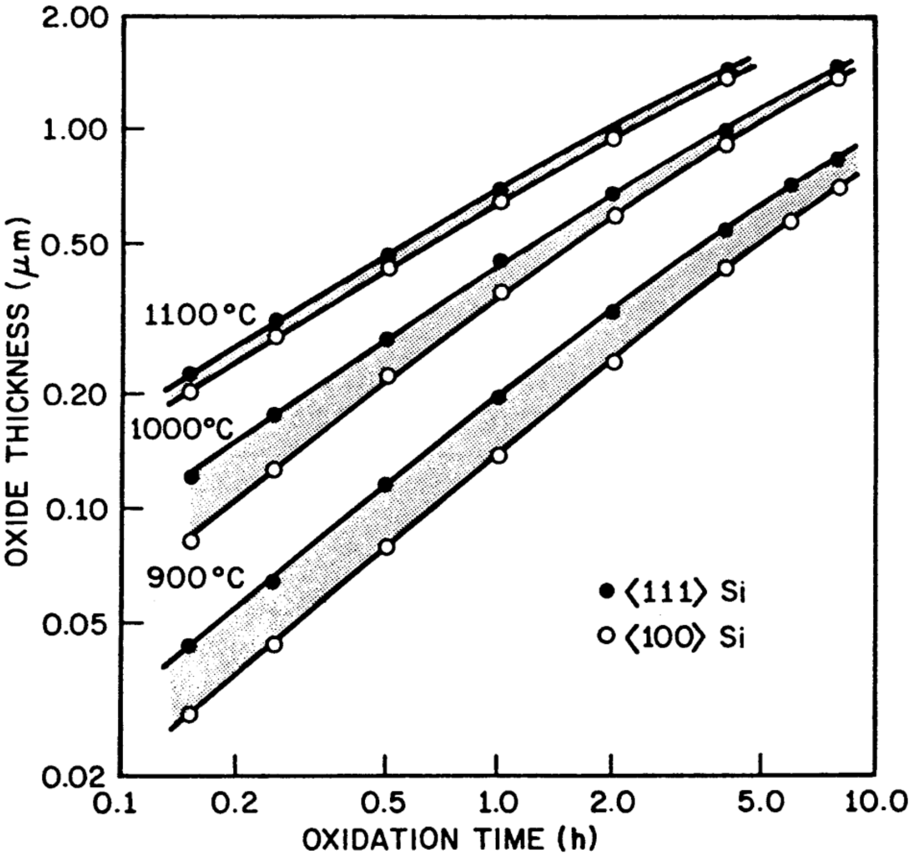




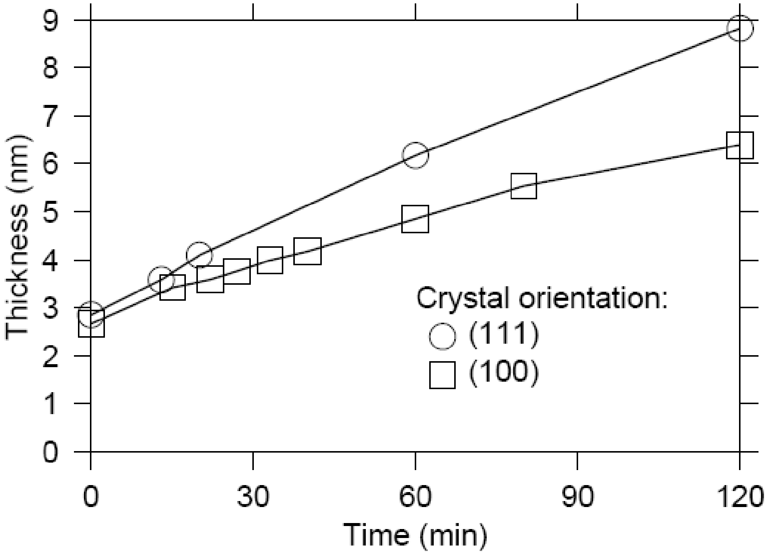
Field emission display (FED)

Ding, "Silicon Field Emission Arrays With Atomically Sharp Tips: Turn-On Voltage and the Effect of Tip Radius Distribution", 2002.

<111> vs. <100> oxidation



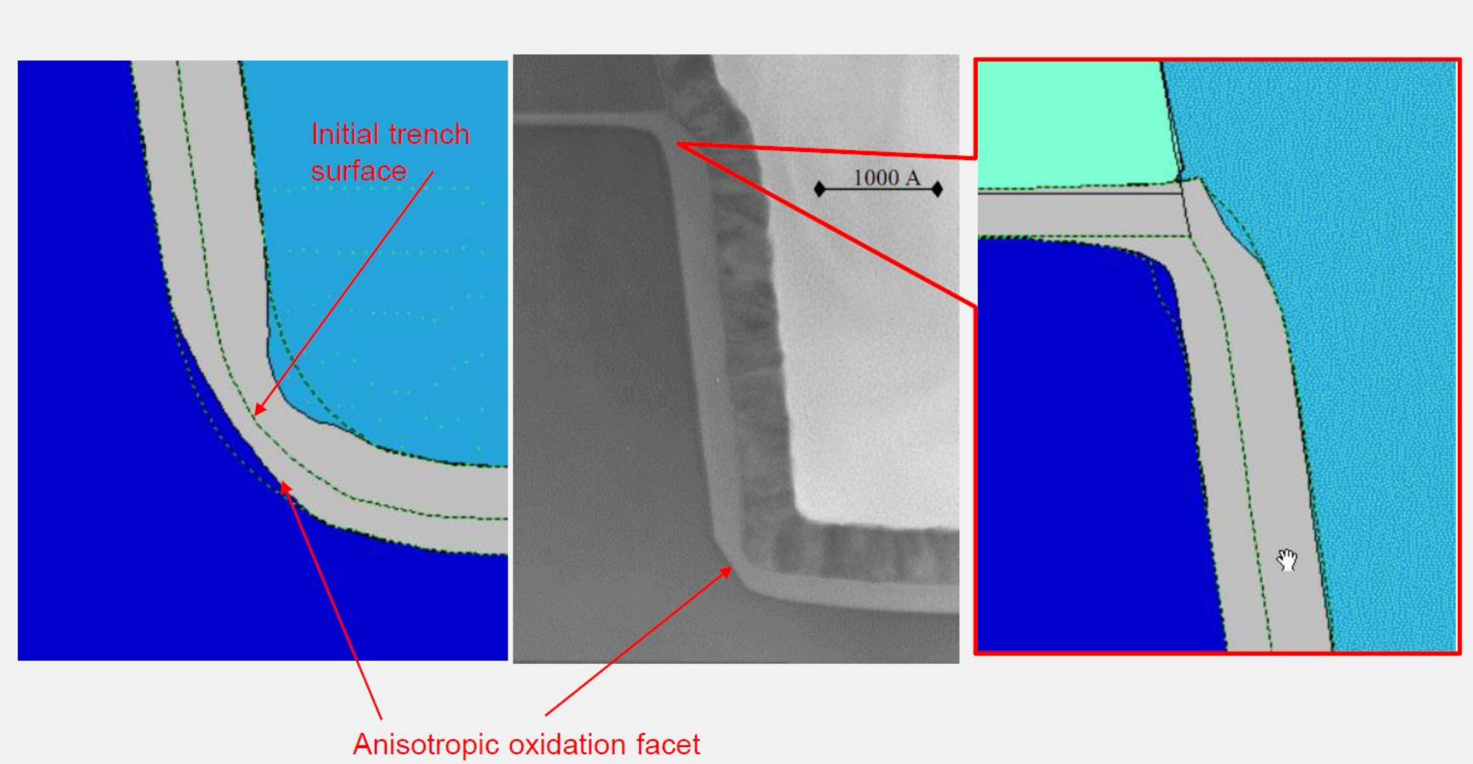
City University of Hongkong, Ch 4



For very thin oxides

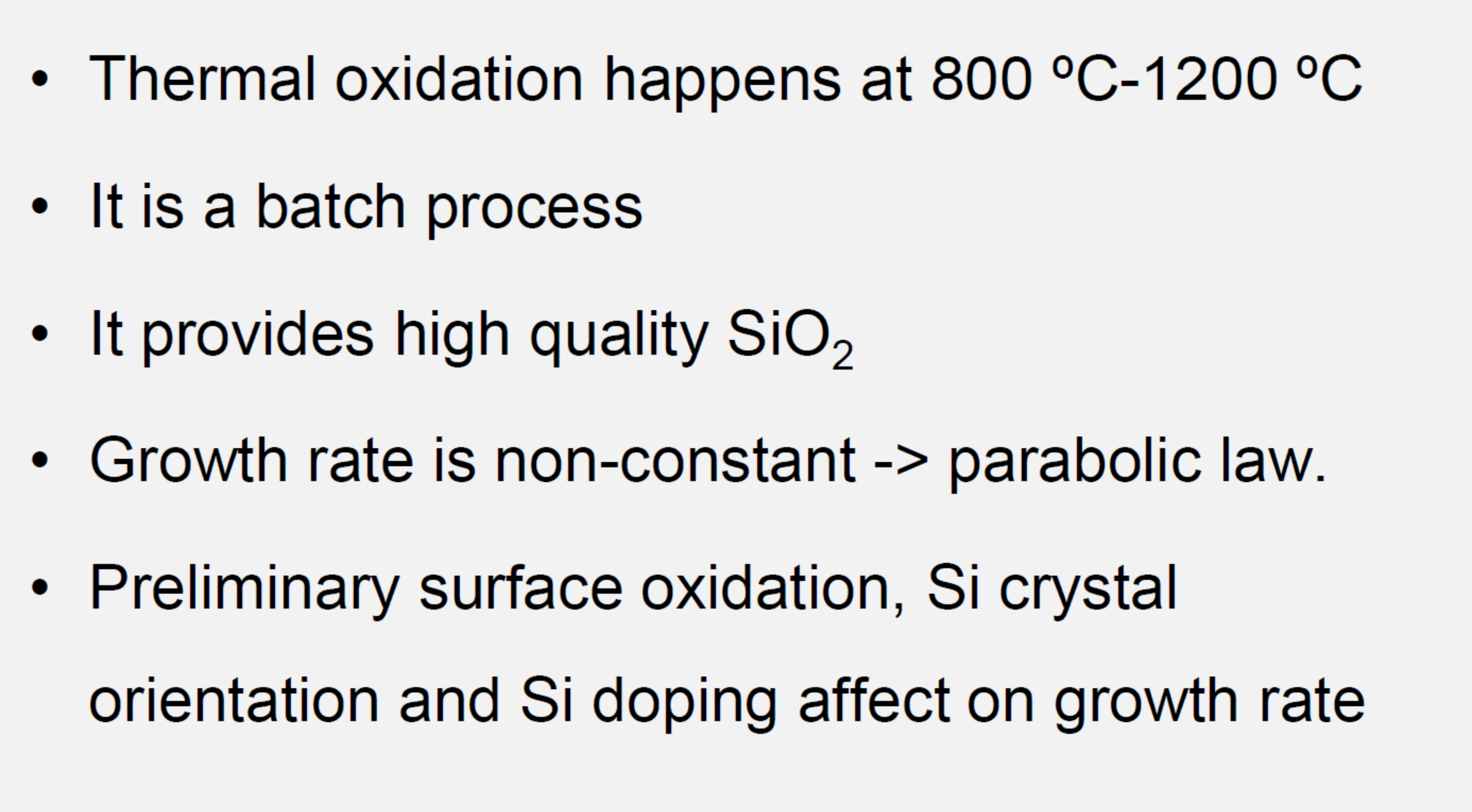
Antti J. Niskanen, PhD thesis, Aalto 2012

Oxidation of corners



Both crystal orientation effects and stresses affect oxidation in corners.

Summary



- Thermal oxidation happens at 800 ºC-1200 ºC
- It is a batch process
- It provides high quality SiO_2
- Growth rate is non-constant -> parabolic law.
- Preliminary surface oxidation, Si crystal orientation and Si doping affect on growth rate