Process integration
General topics
(CMOS and MEMS process integration later on)
2023

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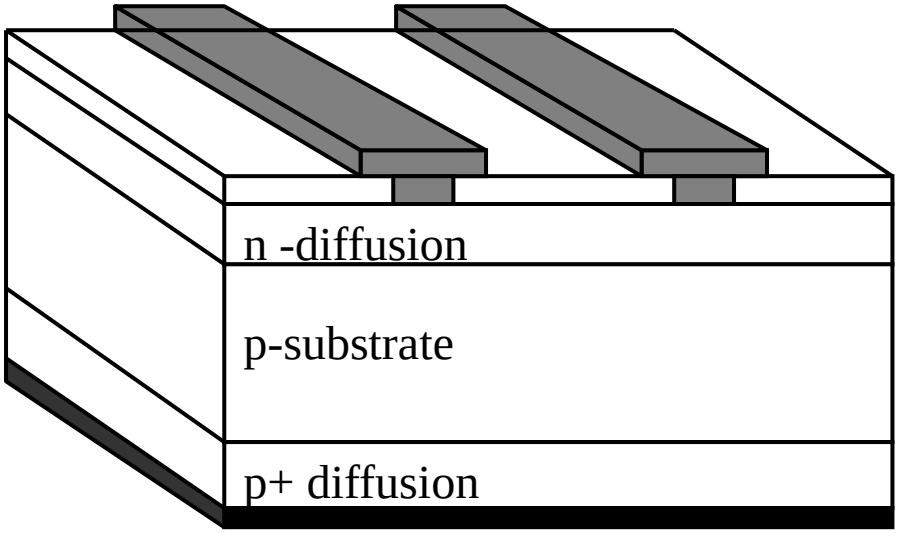
Integration: solar cell process



top metallization

anti-reflective coating (ARC)

backside metallization

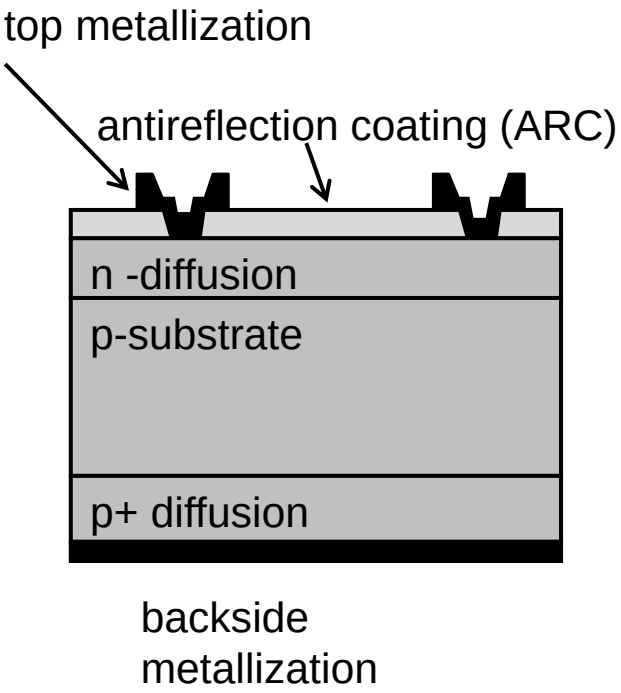
The contact holes in anti-reflective coating are non-critical

The metallization alignment to contact holes is critical

(in case of misalignment, metal does not fully cover holes, and gases, liquids, dirt can penetrate into silicon)

Front end processing

- wafer selection (thin p-type)
- wafer cleaning
- thermal oxidation
- photoresist spinning on front
- backside oxide etching
- resist stripping
- wafer cleaning
- p+ back diffusion (boron 10^{19} cm^{-3})
- front side oxide etching
- wafer cleaning
- n-diffusion (phosphorous 10^{17} cm^{-3})

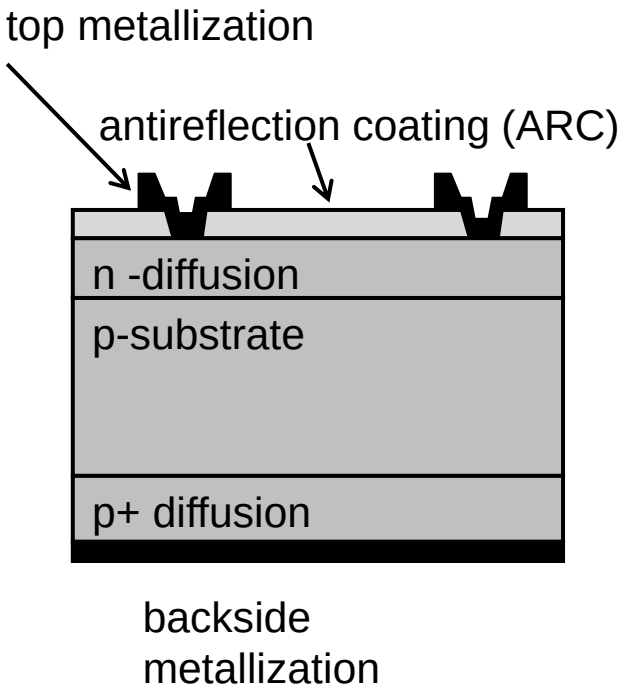


FRONT END = STEPS BEFORE METALLIZATION

High temperature compatible steps: oxi, epi, diff, implant

Backend processing

- resist spinning on front
- metal sputtering on back side
- resist stripping
- wafer cleaning (acetone + IPA)
- PECVD nitride deposition (ARC)
- lithography for contact holes
- etching of nitride
- resist stripping
- wafer cleaning
- metal deposition on front side
- lithography of front metal
- metal etching
- photoresist stripping
- contact improvement anneal



BACKEND = PROCESS AFTER FIRST METAL DEPOSITION

Limited by Si/metal interface <450^{o}C

Materials stability at high temperatures

- high temperature (>900°C; diffusion fast)

  really only Si, SiO_2, Si_3N_4, SiC
- intermediate temperature (450-900 °C)

  refractory metals not in contact with Si
- metal compatible temperature (<450 °C)

  Si/metal interface stable, glass wafers
- polymer compatible (<120 °C)

  evaporation, sputtering (lift-off resist)

Thermal budget

Time-temperature limits that the device can endure.
Thermal budget = f (t,T)

High temperature causes:

- -diffusion (in all atmospheres)
- -oxidation (in oxidative atmosphere)
- -damage recovery
- -grain growth

Some of these are wanted effects, some are problems:

- -implantation damage removed
- -dopants driven deeper
- -silicon oxidation competes with diffusion

Examples of thermal budget

Implant damage recovery anneal:

Either

950^{o}C, 30 min in furnace

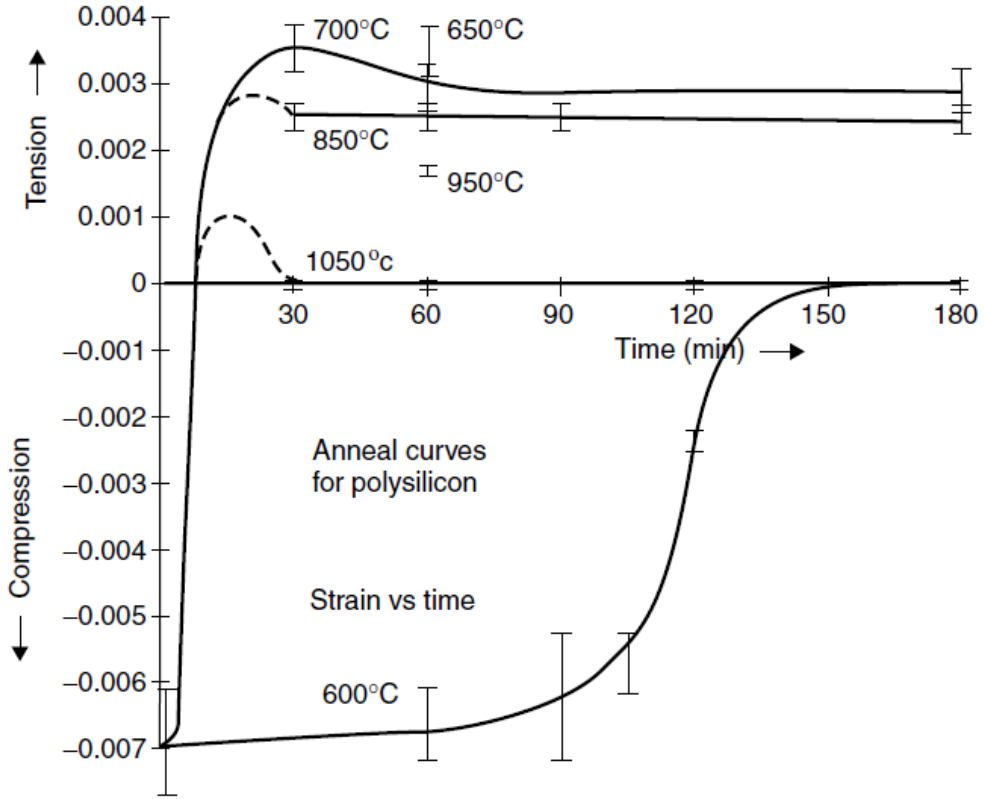
or

1100^{o}C, 15 secs in RTA (Rapid Thermal Anneal)

Aluminum contact improvement anneal:

Either 450^{o}C, 30 min ***or*** 425^{o}C 60 min

Anneal to modify stress



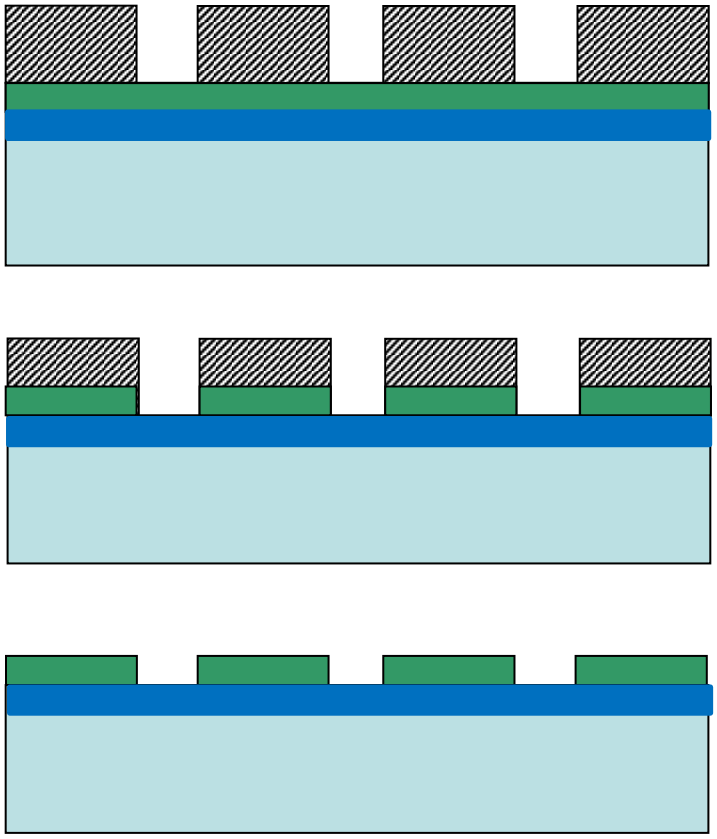
LPCVD 580°C deposition, i.e. amorphous silicon initially

Stress reduction is anneal temperature ***and*** time dependent !

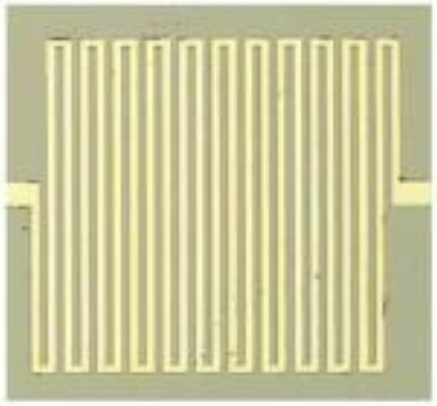
Thermal budget
= f (t,T)

Compare English vs. French roast beef:
175°C & 1 h
vs. 125°C & 3 h

Metal resistor processing

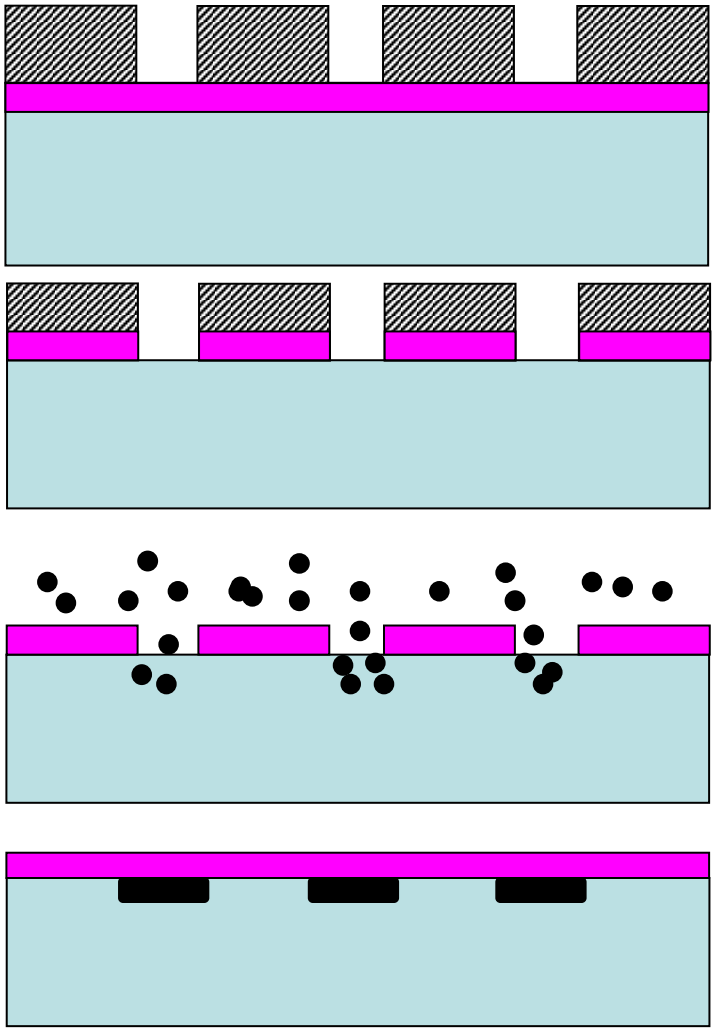


1. Silicon wafer, no specific specs
2. Insulator deposition
3. Metal sputtering (or evaporation)
4. Lithography with resistor mask



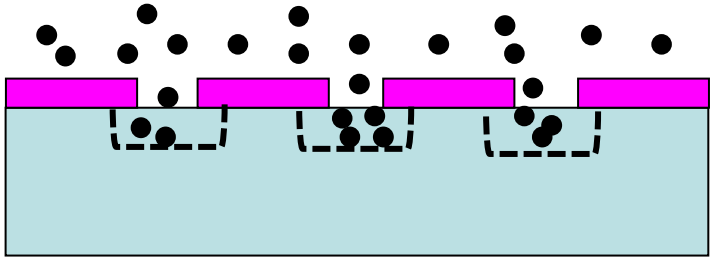
5. Metal etching & resist stripping

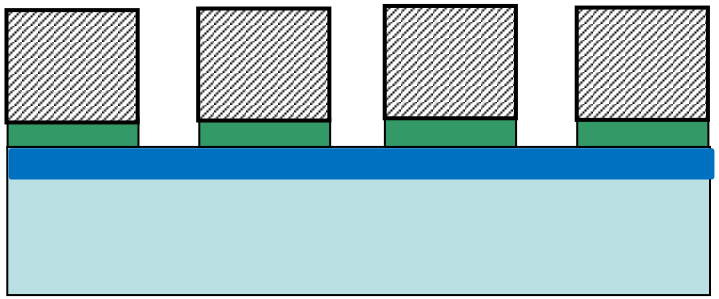
Diffused resistor processing



1. ***Cleaning***
2. Thermal oxidation
3. Lithography with heater mask
4. Oxide etching + resist strip
5. ***Cleaning***
6. Diffusion (in furnace)
7. Oxide mask etched away
8. ***Cleaning***
9. New thermal oxidation !

Diffused vs. metal resistor





Size determined by:
Lithography + diffusion
➔ always spreading!!

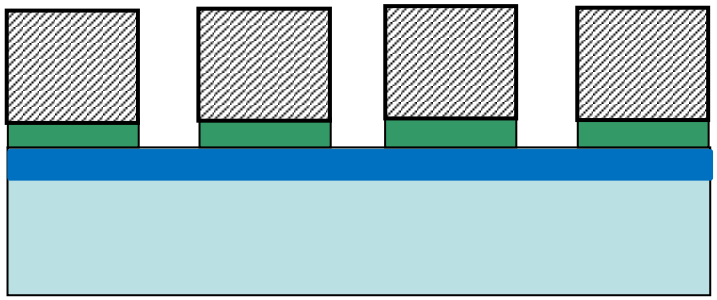
2 µm linewidth +
1 µm diffusion depth ➔
1 µm sideways diffusion
both left and right
➔ 4 µm wide resistor

Size determined by:
Lithography + etching

If etching is
anisotropic, then

2 µm linewidth ➔
2 µm wide resistor

3rd option: polysilicon resistor



1. Silicon wafer
2. Oxide (insulation)
3. Poly deposition
4. Poly doping
5. Lithography
6. Poly etching + strip PR

Many options for poly doping: ion implant (needs activation anneal), thermal diffusion, solid source diffusion from PSG (phoshorous doped silica glass). Difficult to dope during CVD growth, but possible.

Why is poly resistor option useful ?

Polysilicon resistivity can be tailored over a vast range.

Polysilicon can be thermally oxidized.

Design rules

Advice from process engineer to circuit designer of what the process is capable of.

For instance: what is the minimum feature size that can be used (different on different layers)

Some of these are mandatory ➔ if you break them, circuit will not work (e.g. transistor gate is so narrow that it does not control the current any more).

Some of these are recommendations of known good practices, e.g. make inductors octagons and not squares.

Mandatory line/space rules

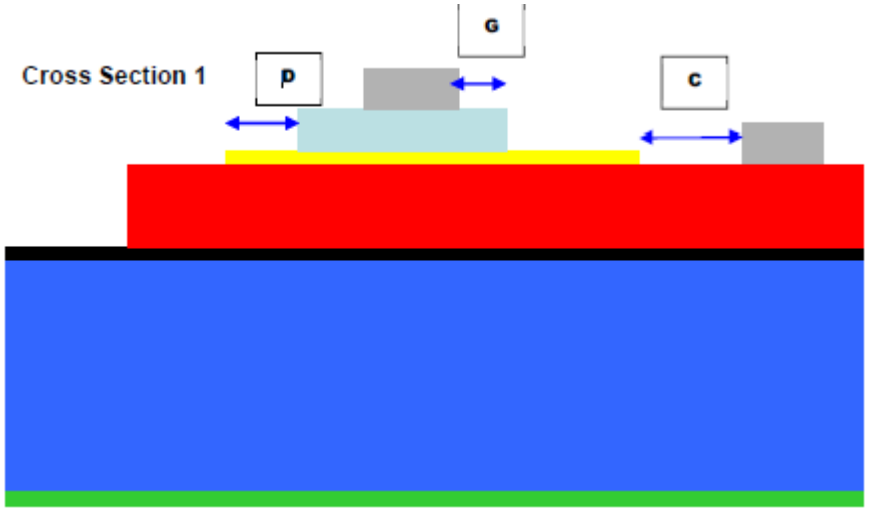
Lithography and etch related: on a planar surface litho is easier than on topography (depth of focus issue). On some layers plasma etching is used, but on some layers wet etching ➔ need to thick about line narrowing due to etch undercut)

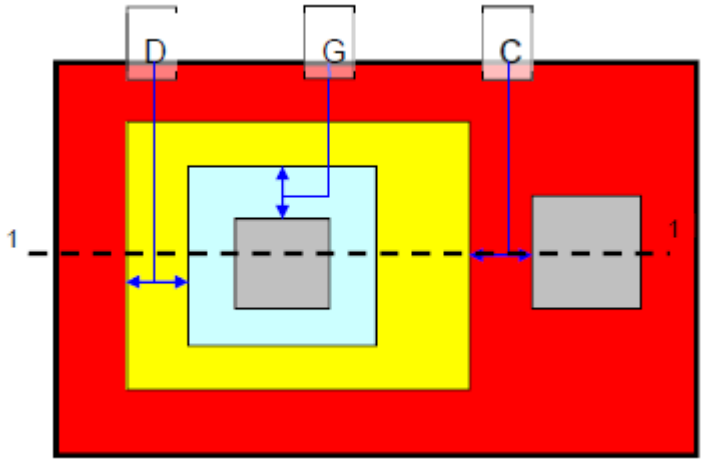
Mnemonic level name	Min. feature (µm)	Min. space (µm)
PADOXIDE	5	5
PZFILM	10	10
PADMETAL	3	3
SOI	2"	2"
SOIHOLE	3	3
TRENCH	200	200

MEMSCAP Inc.

Placement rules

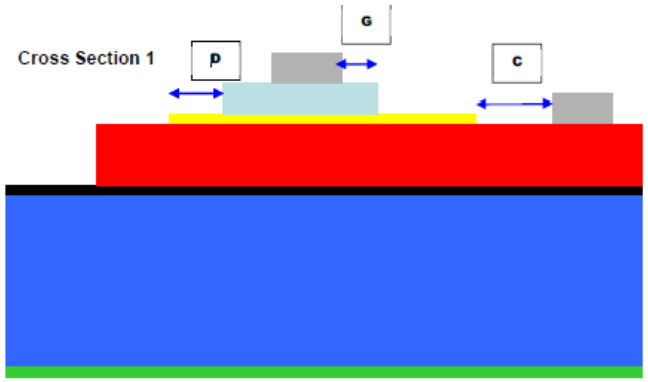
Structures either must make contact or avoid contact, and these rules tell what tolerances to use.

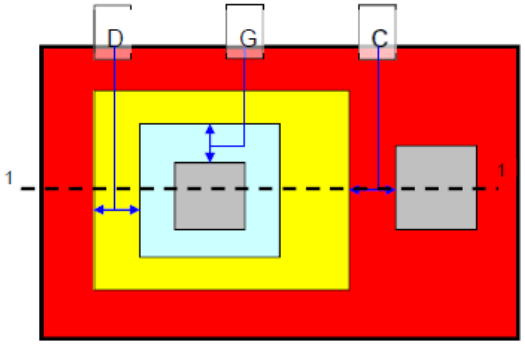




	Silicon		Substrate		Bottom Oxide		Pad Metal
	Oxide		PiezoMaterial		Pad Oxide		Frontside Protection Material

Placement rules (2)





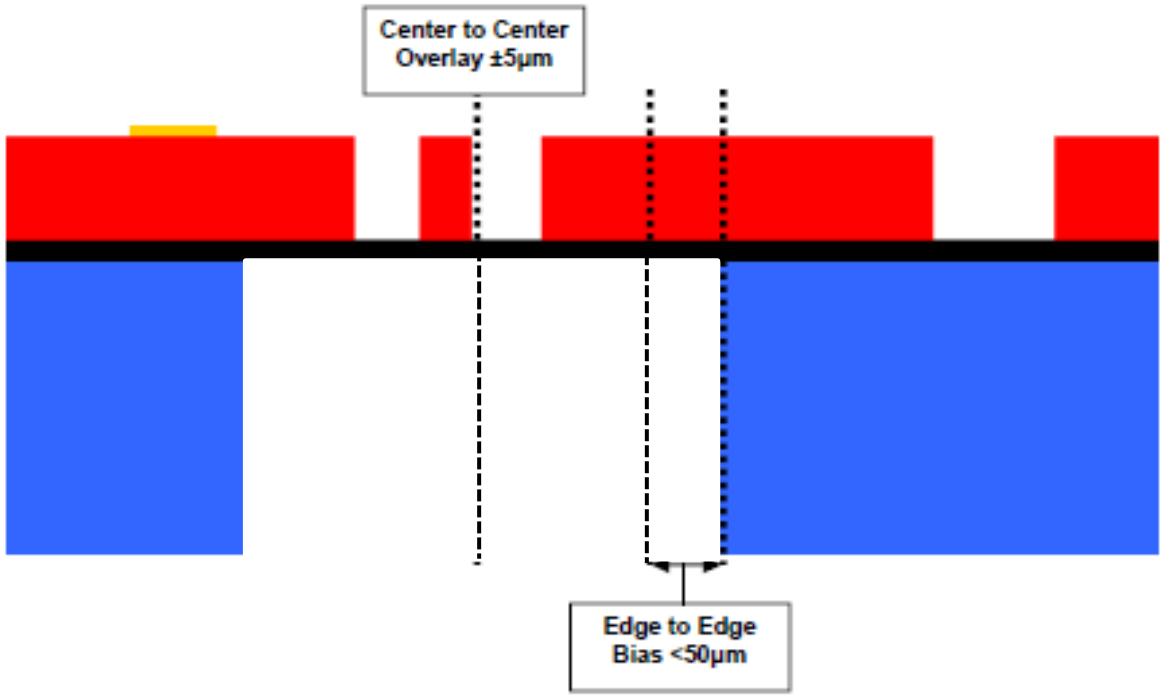
C: PADOX space to PADMETAL > 5.0µm to ensure the Pad Metal layer **does not** interact with the PADOXIDE.

D: PADOX enclose PZFILM > 5.0µm to ensure the piezoelectric layer **is not** in electrical contact with SOI device layer.

G: PZFILM enclose PADMETAL > 4.0µm. The distance PZFILM must extend beyond the edge of PADMETAL to **ensure complete coverage** of PADMETAL.

	Silicon		Substrate		Bottom Oxide		Pad Metal
	Oxide		PiezoMaterial		Pad Oxide		Frontside Protection Material

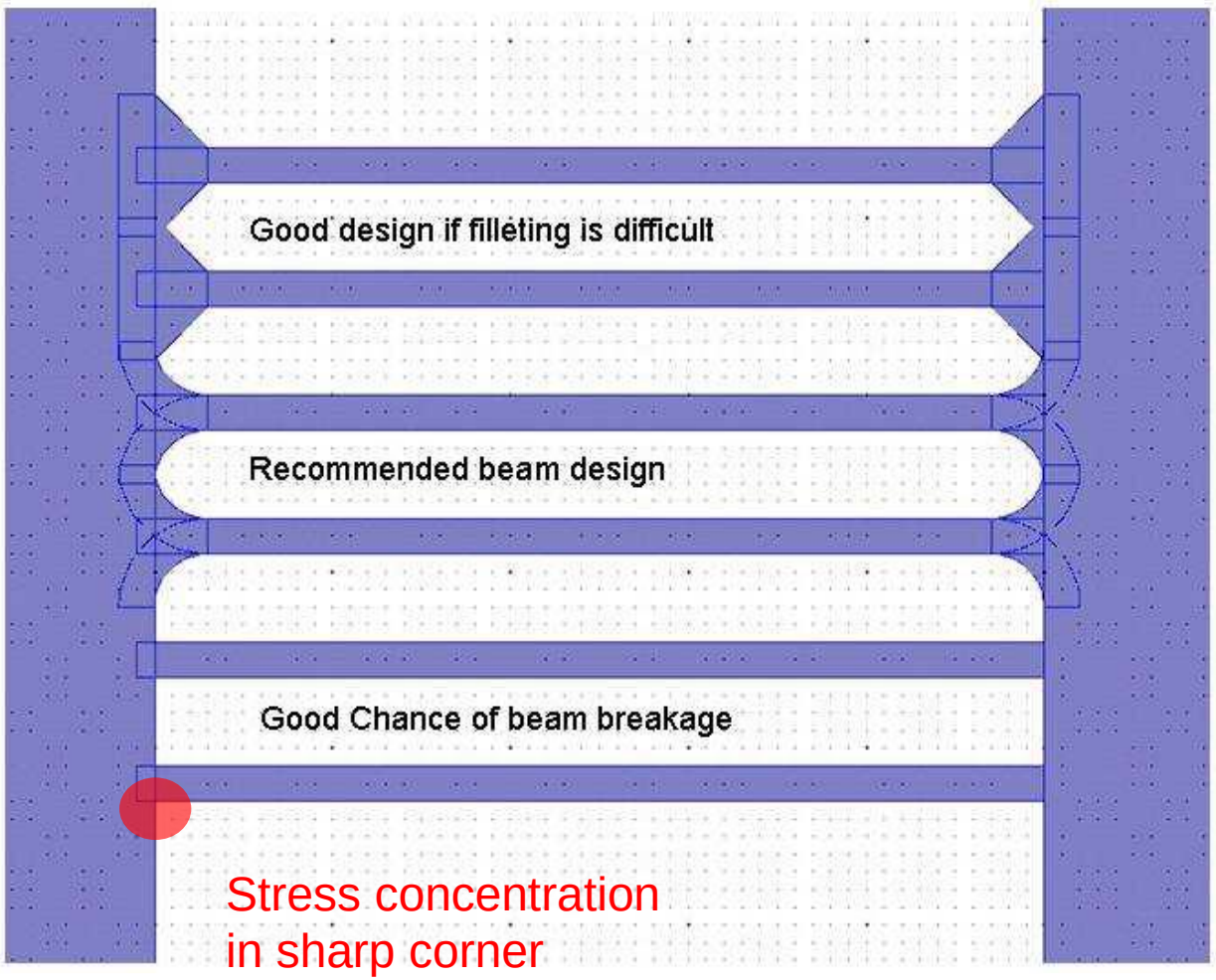
Front-to-back rules



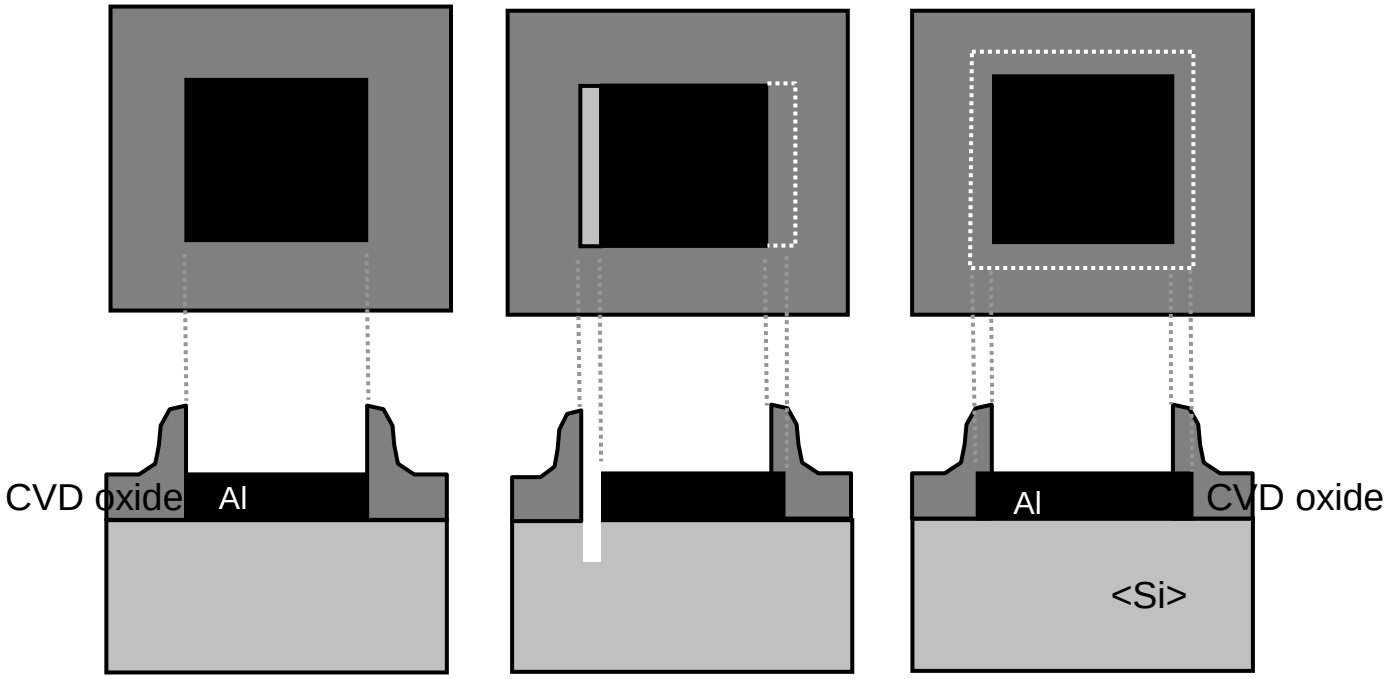
These are most often rather relaxed.

Alignment front-to-back not as good as front-to-front alignment.

Recommendation rule



Alignment of contact hole

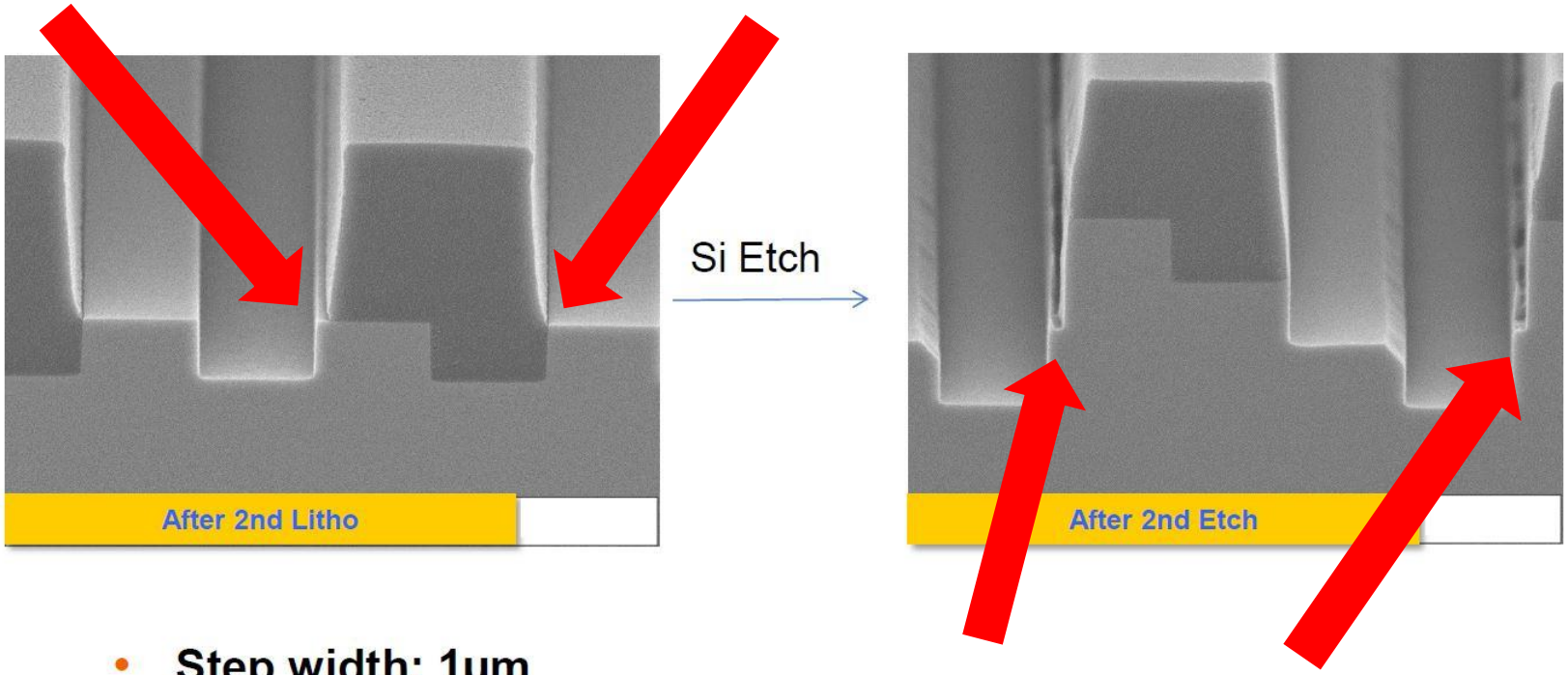


There is no perfect alignment ➔ overlap must be designed:
Coinciding structures must overlap by e.g. ~LW/3

Alignment error + etching

Not perfect here

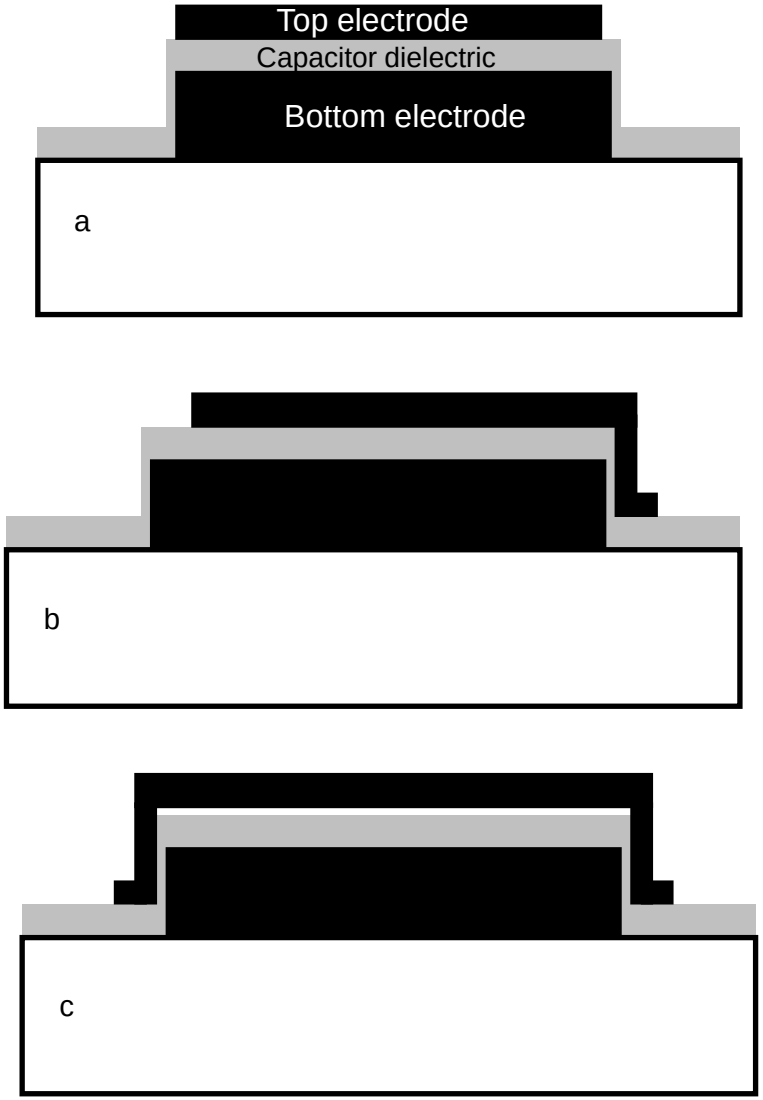
As good as it gets



- **Step width: 1µm**
- **Step height 0.5 µm**
- **Overlay error <100nm**

This is not what you want: depends too much on alignment success.

Design rules: capacitor

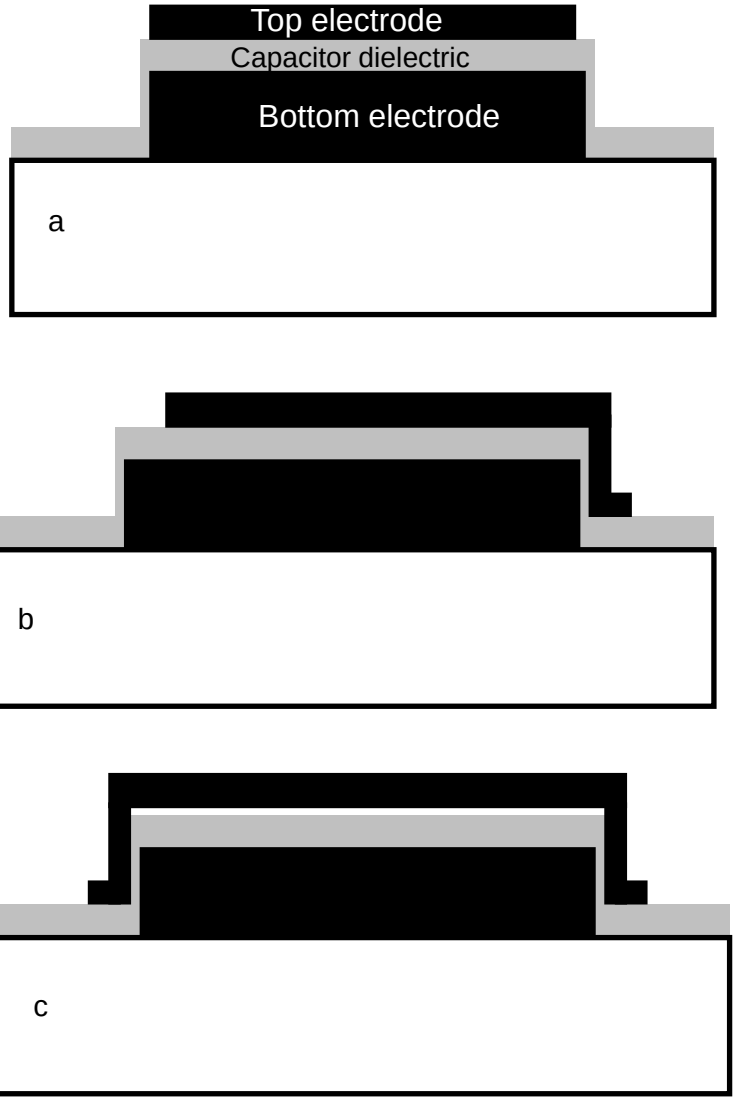


a) Top electrode size correct when perfect alignment

b) Correct top electrode size but top electrode misaligned to right

c) Correct alignment but top electrode mask too big ➔ unknown capacitance from sidewalls

Capacitor problems



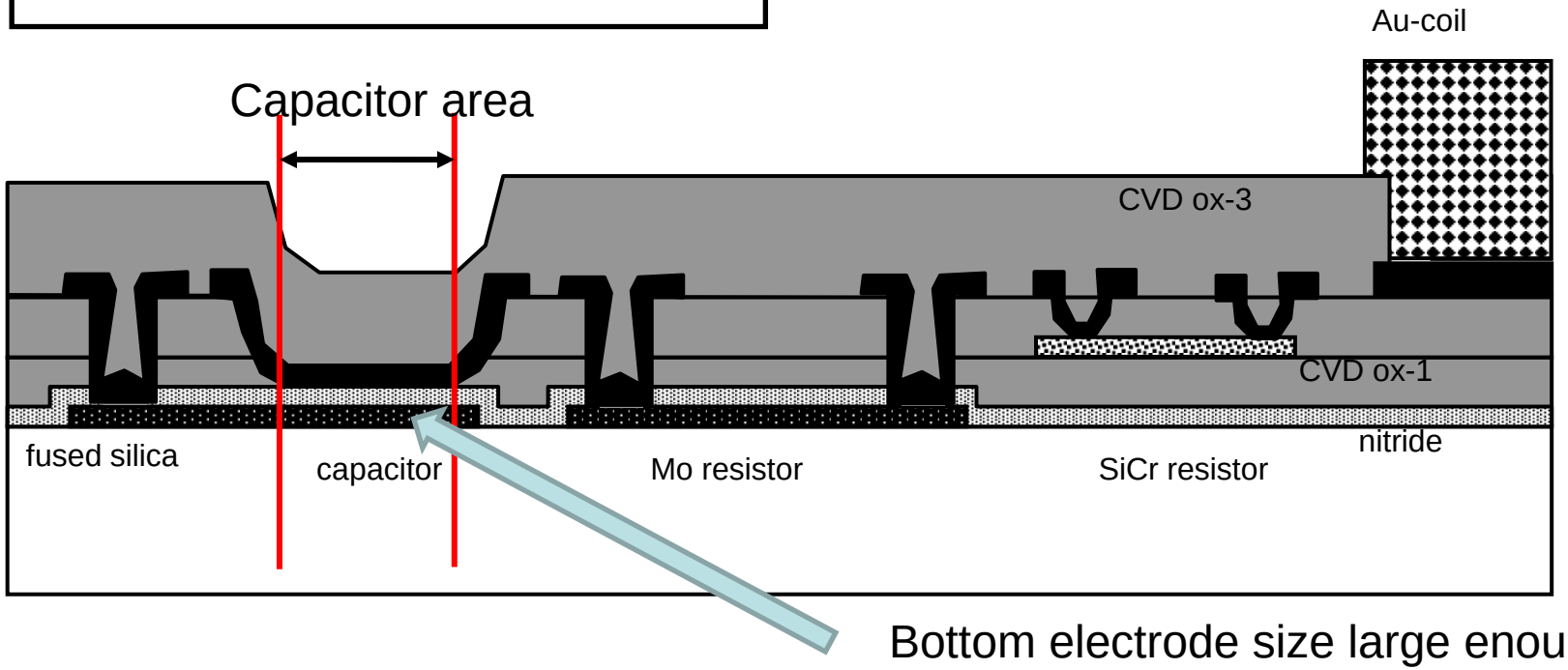
a) As it should be

b) Capacitor dielectric on the sidewall is not the same thickness as on horizontal surfaces ➔ incorrect capacitance, and potentially a weak point in system

c) Too big capacitance because area error

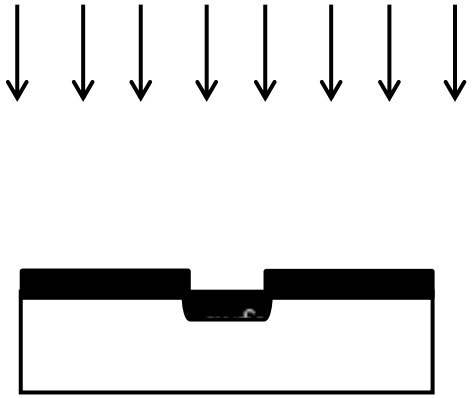
Solution to capacitor

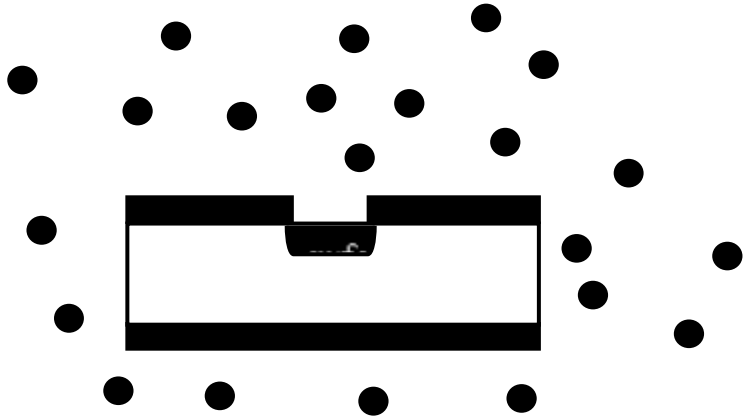
Top electrode is made smaller than bottom electrode, to make sure that it lands on capacitor dielectric on planar area.



Bottom electrode size large enough
➔ easy alignment

Equipment: 1- or 2-sided processing





Beam processes 1-sided

Immersion processes 2-sided

-photon beams (=lithography)

-atom beams (=evaporation)

-ion beams (=implantation)

-mixture of beams (=plasmas)

-liquids (=wet etching)

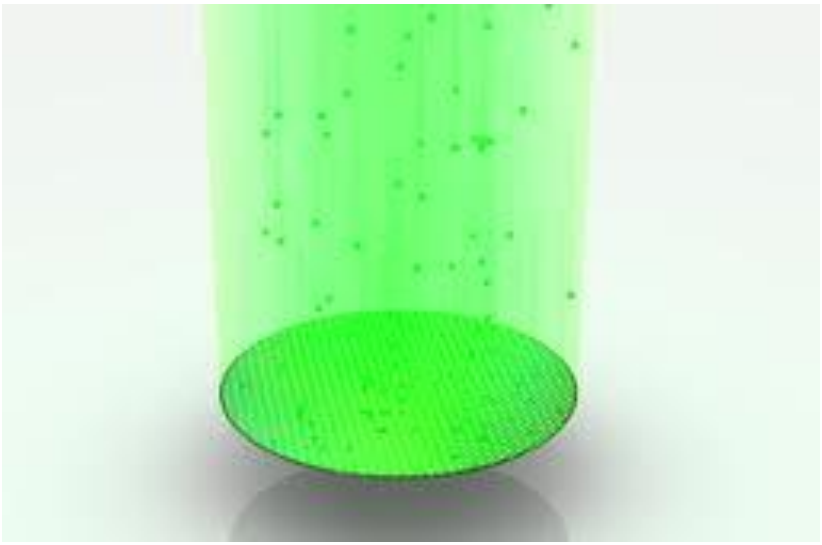
-liquids (=cleaning)

-gases (= oxidation, diffusion)

-gases (=thermal CVD, ALD)

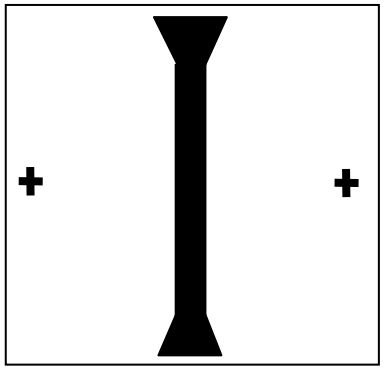
Single side processes

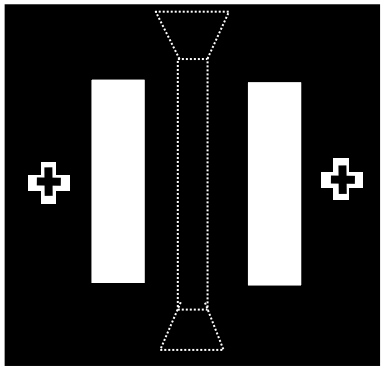
PECVD,
RIE,
sputtering,
evaporation



Ion implantation
Photolithography

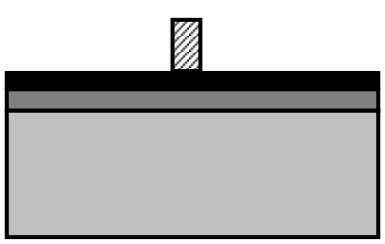
Bolometer single sided process

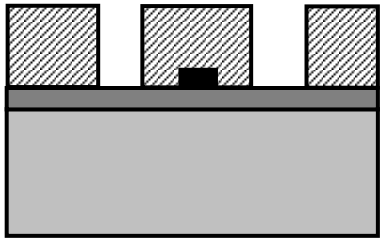




Bolometer mask view

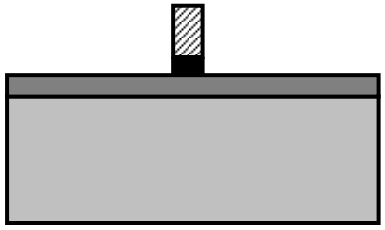
1) Thermal ox
2) Metal deposition
3) Lithography

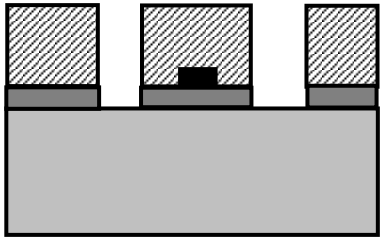




6) 2nd lithography

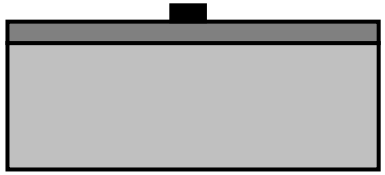
4) Metal etching

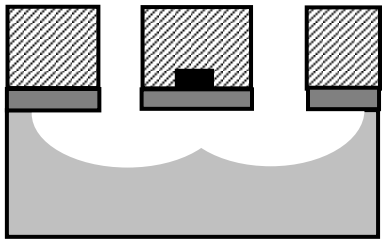




7) Oxide etch

5) Resist strip





8) Silicon isotropic etch

Thermal oxide grows on both sides, but all processing is on front only.

Bolometer in SEM

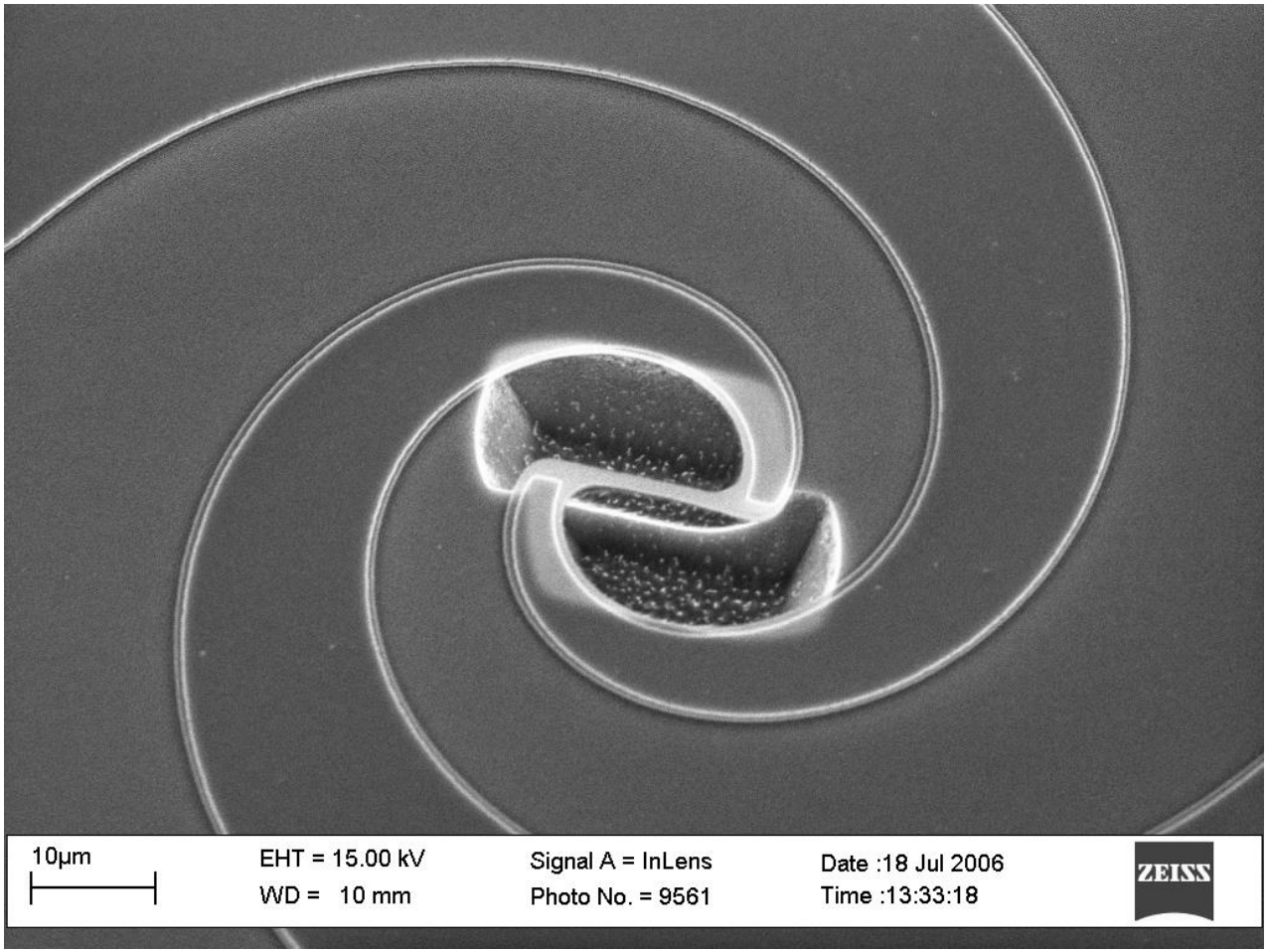
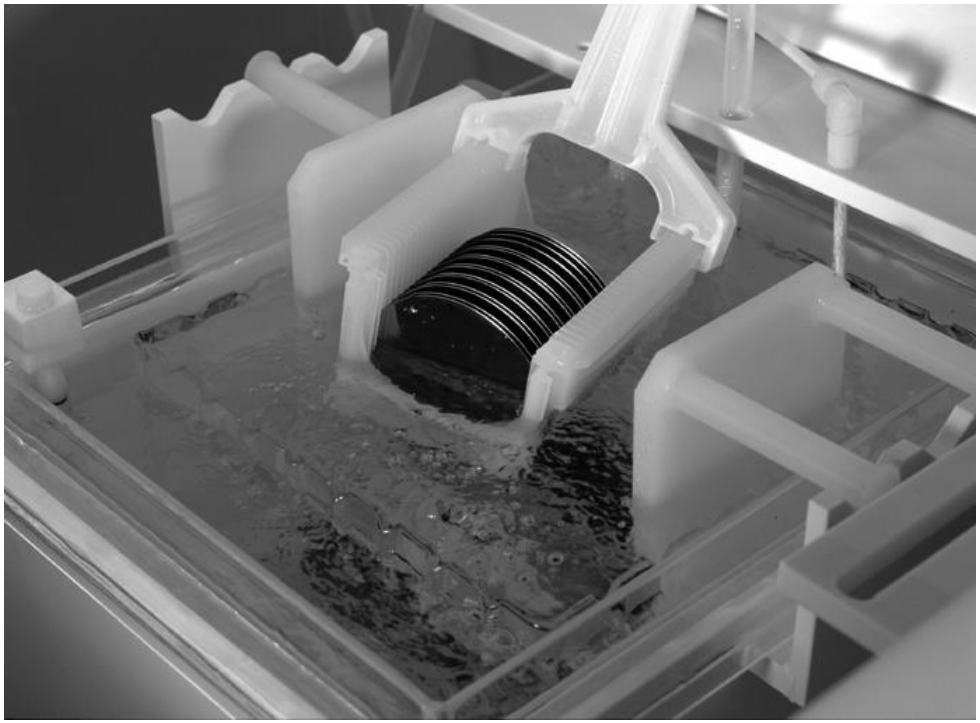


Figure courtesy Leif Grönberg, VTT

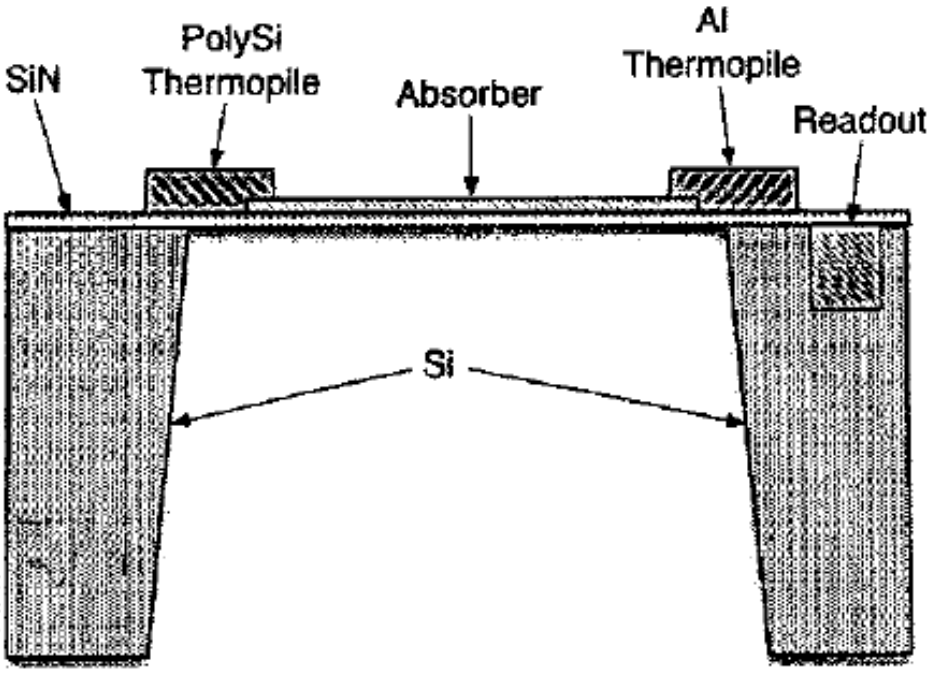
Double-sided processes



Thermal oxidation
Thermal CVD

Wet etching
Wet cleaning

Bolometer double sided



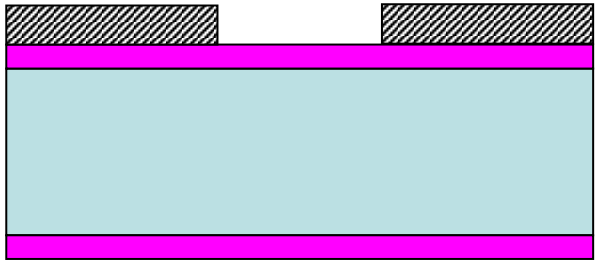
Adam, Sarro, IEEE 2004

Need alignment of backside etching to front side structures.

Need to protect front side during backside etching.

(It is not a good idea to etch backside first and then do frontside processing because SiN membrabe is thin and fragile)

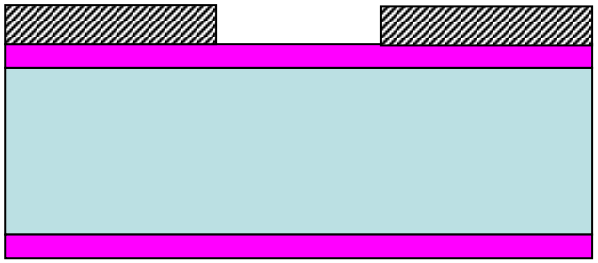
Wet vs. plasma



Oxide wet etch in HF

Undercut, isotropic

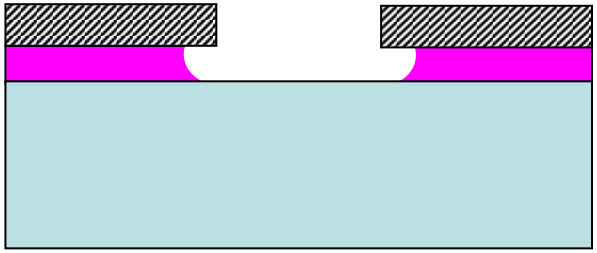
High selectivity



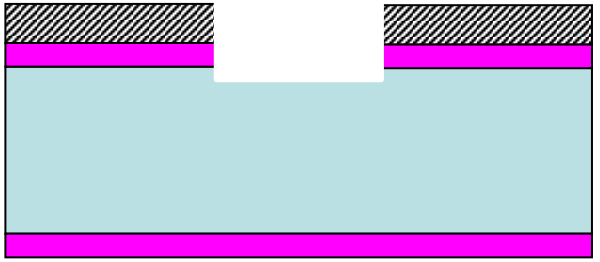
Oxide plasma etch in CHF_3

Vertical walls, no undercut

Not so good selectivity

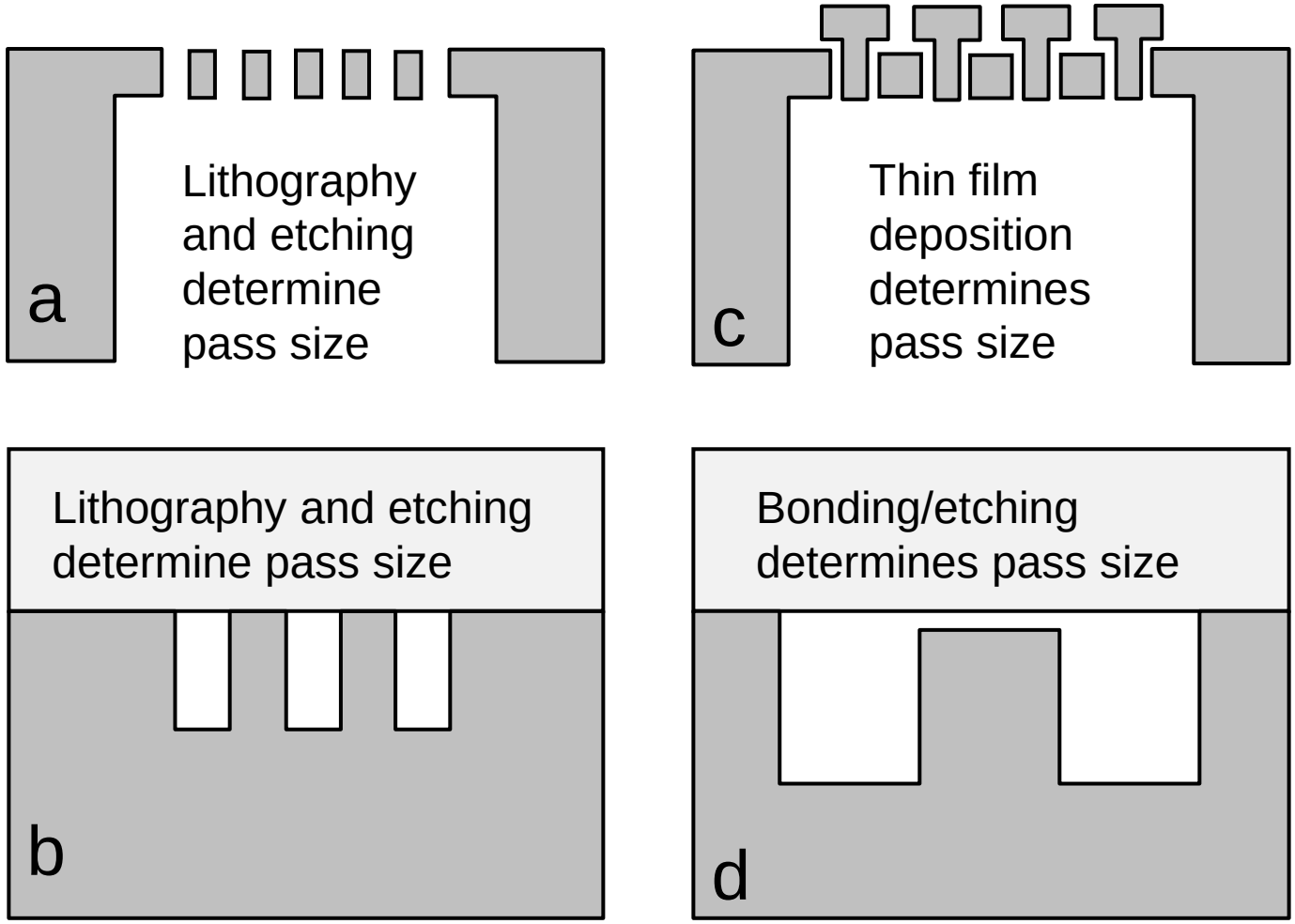


Film removed from backside

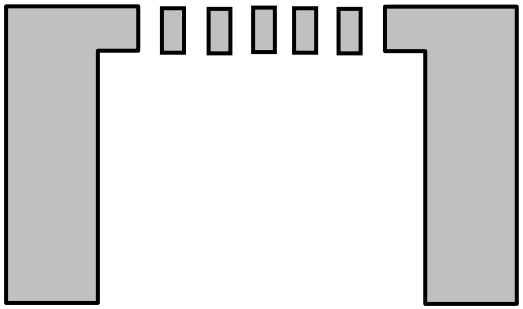


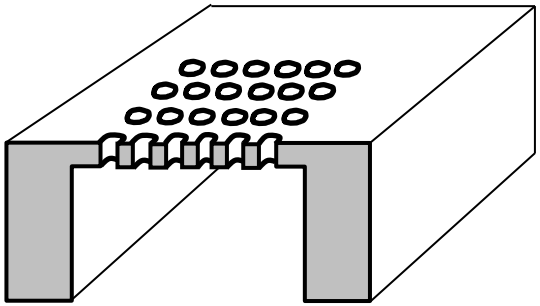
Film remains on backside

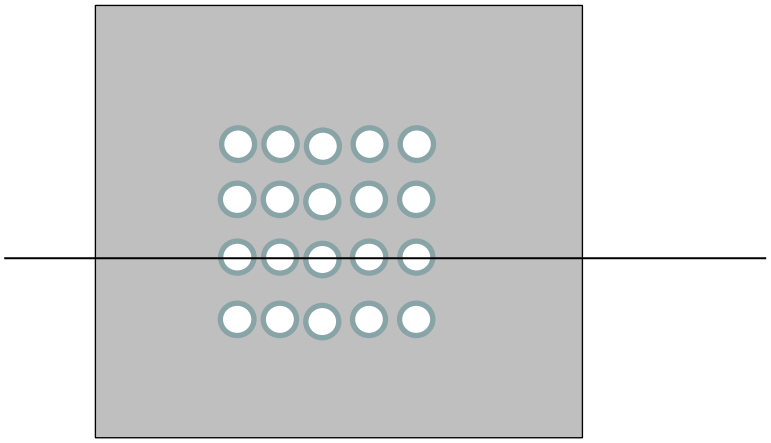
Fluidic filters

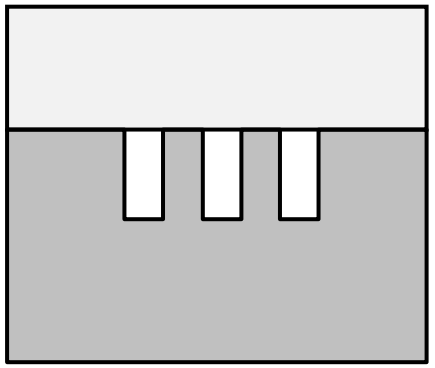


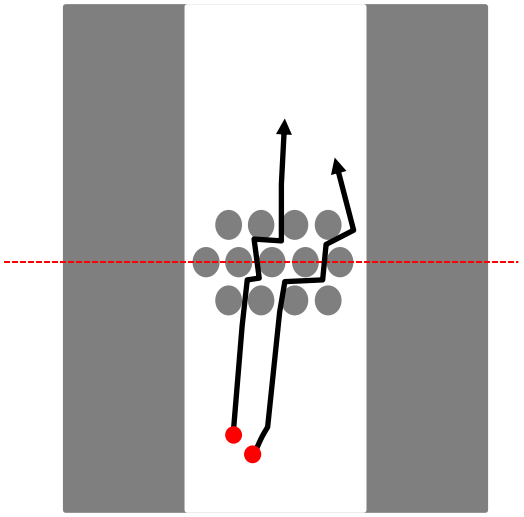
Cross section vs. layout view











Fluidic filters (2)

Criteria:

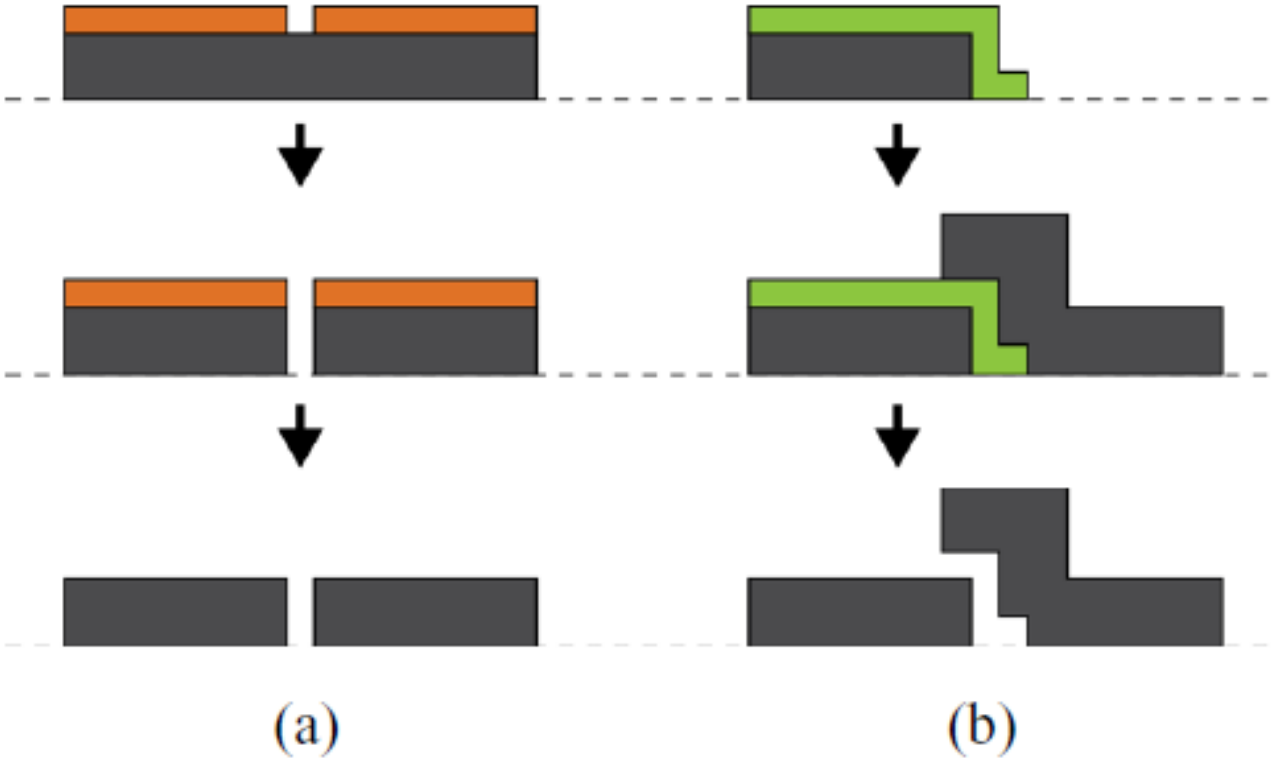
Need one or two wafers ? Cost, bonding...

Pass size determined by litho ? Bonding ?

Flow resistance ? Aperture ratio.

Clogging ? Active cleaning ?

Litho vs. depo



Lithography capability (+etching) determine size

Thin film deposition thickness control determines gap size

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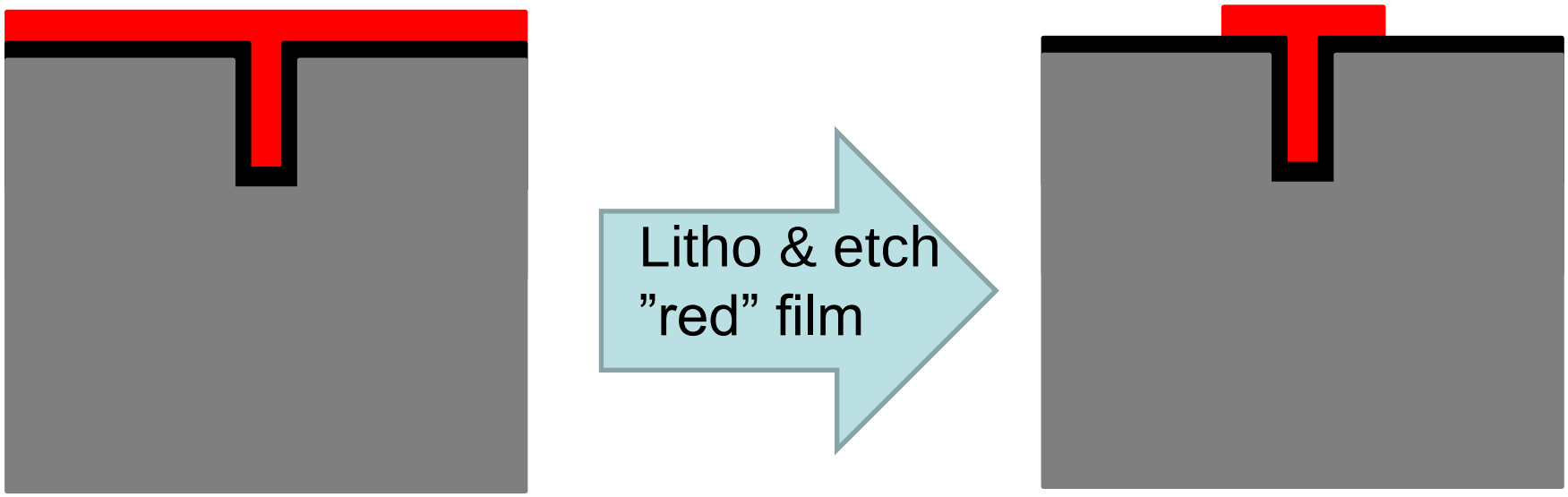
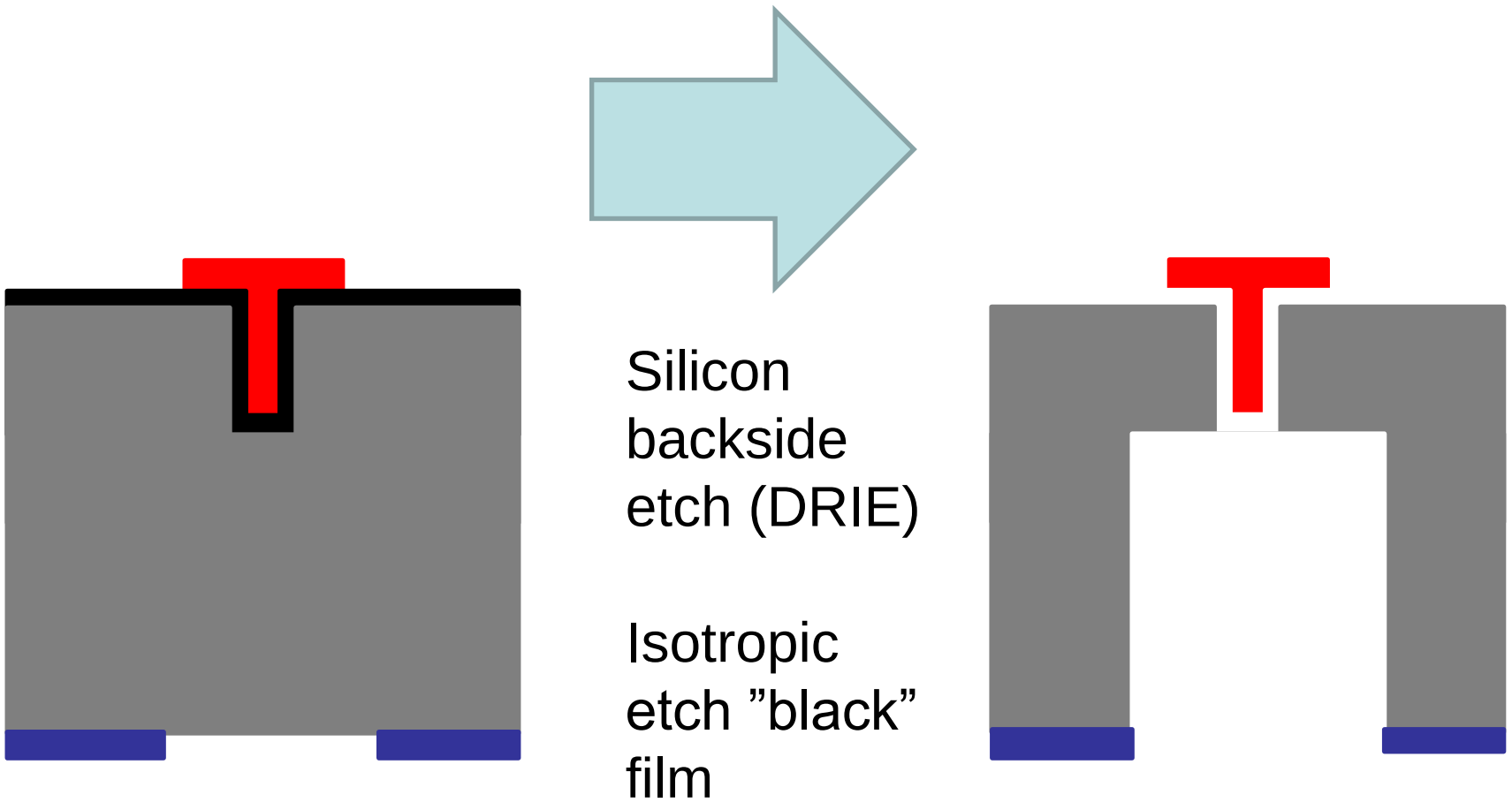
Pass size by thin film deposition





More realistically: black film has to be patterned, too: there have to be anchor points where the red film is securely attached to the wafer.

Etch deeper…

We will encounter a lot more process integration issues in forthcoming lectures, for example:

-front side and backside: how to align ?
-difficulty of doing litho on deep etched structures (because photoresist spinning into deep holes and trenches is nigh impossible)
-alternative hard masks: Al, Al_2O_3, AlN, Cr
-step coverage in deep structures
-…