Bonding and CMP

Victor Ovchinnikov

Chapters 16, 17

Previous lecture

- Selective doping:
  - diffusion
  - ion implantation
- Epitaxy

Next lecture

- Integration

Outlook

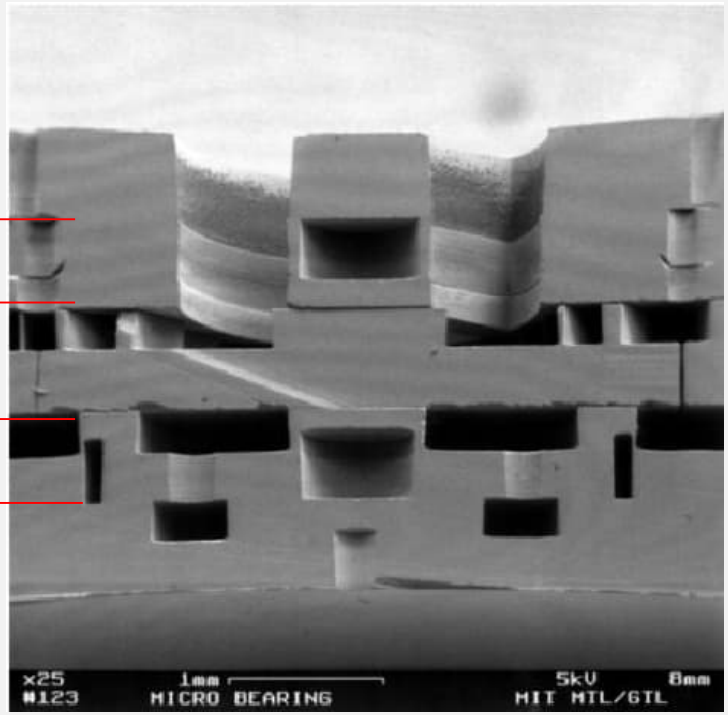
- Bonding in general
- Bonding methods
- CMP
- Etching vs. CMP

Wafer bonding

- It is wafer-level permanent connection technology, ensuring mechanically stable and hermetically sealed assembling
- Bonding of blank and patterned wafers
- Wafer size 100 – 300 mm
- Back end of line (BEOL) process

Wafer bonding applications

- Advanced substrates - SOI
- Packaging
- Capping/Encapsulation
- Multi layer devices
- 3D structures
- Layer transfer



5 wafers, 380 µm each
No wafer thinning
Bonding – one at a time

Wire bonding
Flip chip bonding

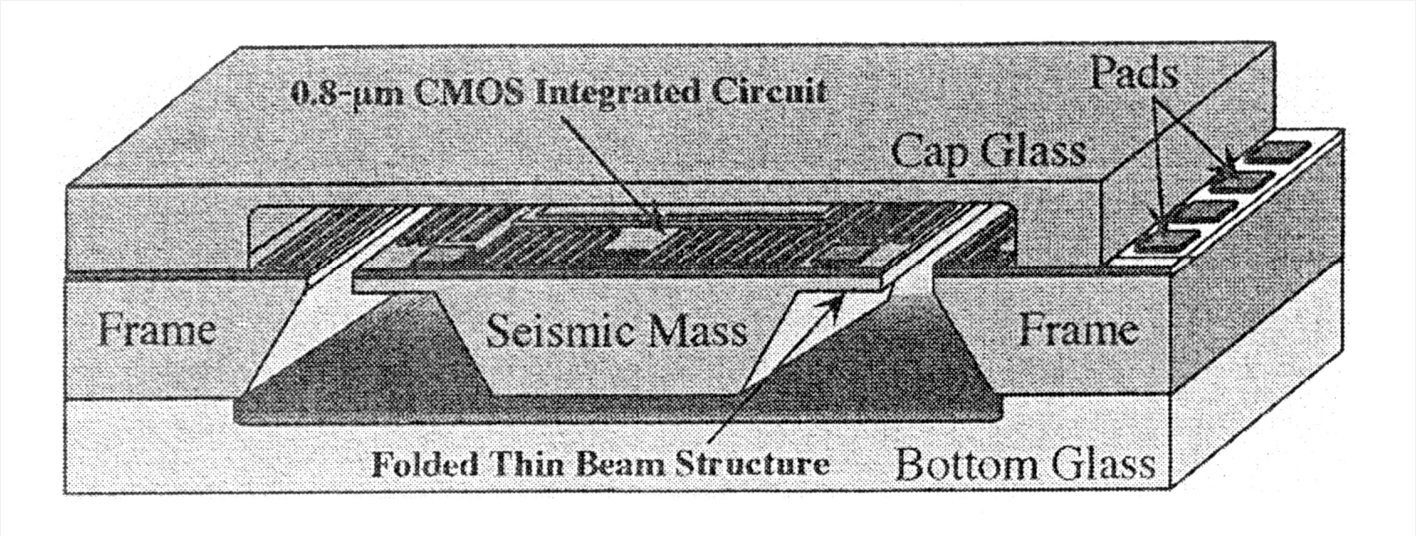
} Not part of this course

Accelerometer (glass-Si-glass)

Capping/Encapsulation application

Anodic bonding: silicon-to-glass. Twice

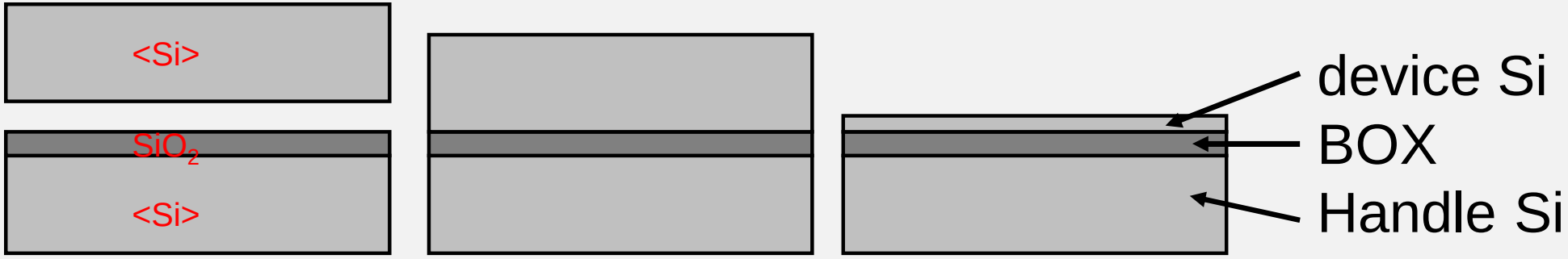
Hermetic cavity (vacuum)



SOI wafer fabrication

Advanced substrates application

Surface preparation **RT joining. Anneal (bonding)** **Thinning**



BOX= buried oxide

Basic requirements for bonding

Wafers are flat (no centimeter scale wavyness)

Wafers are smooth (atomic/micrometer scale), RMS=0.5 nm

Materials form chemical bonds across the interface

No high stress

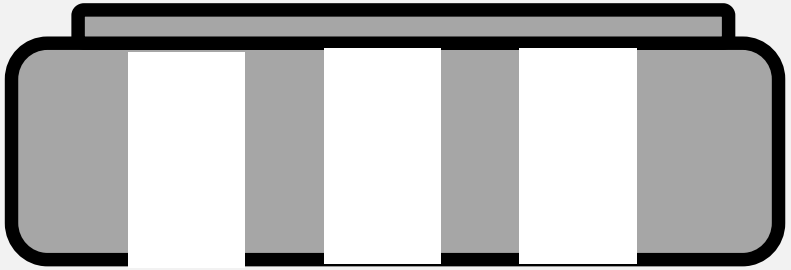
No interface bubbles

Why SOI wafers ?

CMOS

-easy isolation of transistors
-fewer process steps
-elimination of substrate effects
➔ faster transistors

MEMS



-easy etch stop
-single crystal material superior
-device and handle silicon optimized separately

Why not SOI ? -> Expensive

Bonding process steps

-particle removal

-chemical surface modification

-(optional) vacuum pumping

-(optional) wafer alignment

-room temperature joining

-application of force/heat/voltage

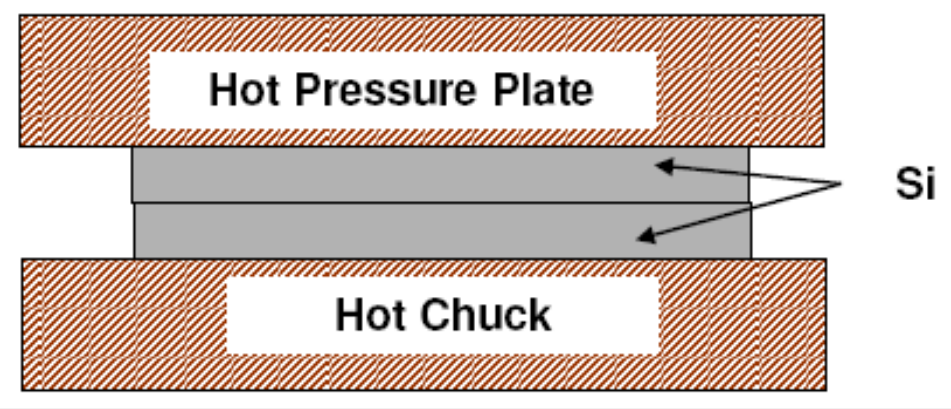
-(optional) wafer thinning

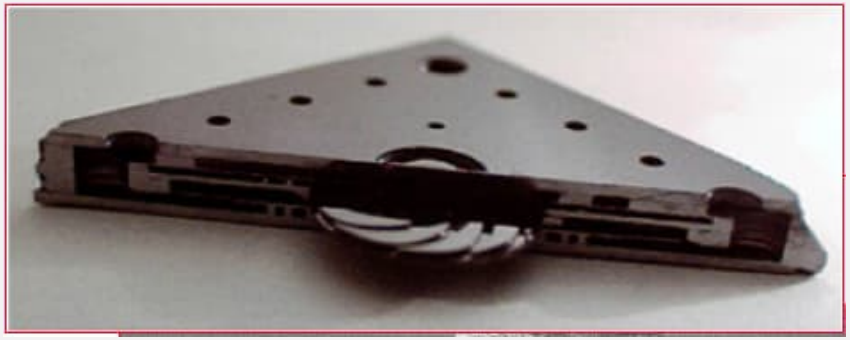
Bonding techniques

- silicon direct bonding (SDB) = fusion bonding (FB):
  (Si/Si or SiO_2/Si or SiO_2/SiO_2)
- anodic bonding (AB) = field assisted thermal bonding (FATB):
  Si/glass, glass/Si/glass
- thermo-compression bonding (TCB):
  Au-Au
- eutectic bonding:
  Si/Au (363 ^oC)
- adhesive bonding, “glueing”:
  Si/polymer/Si
- glass frit bonding:
  Si, glass,SiO_2, Al, Ti

Direct (fusion) bonding

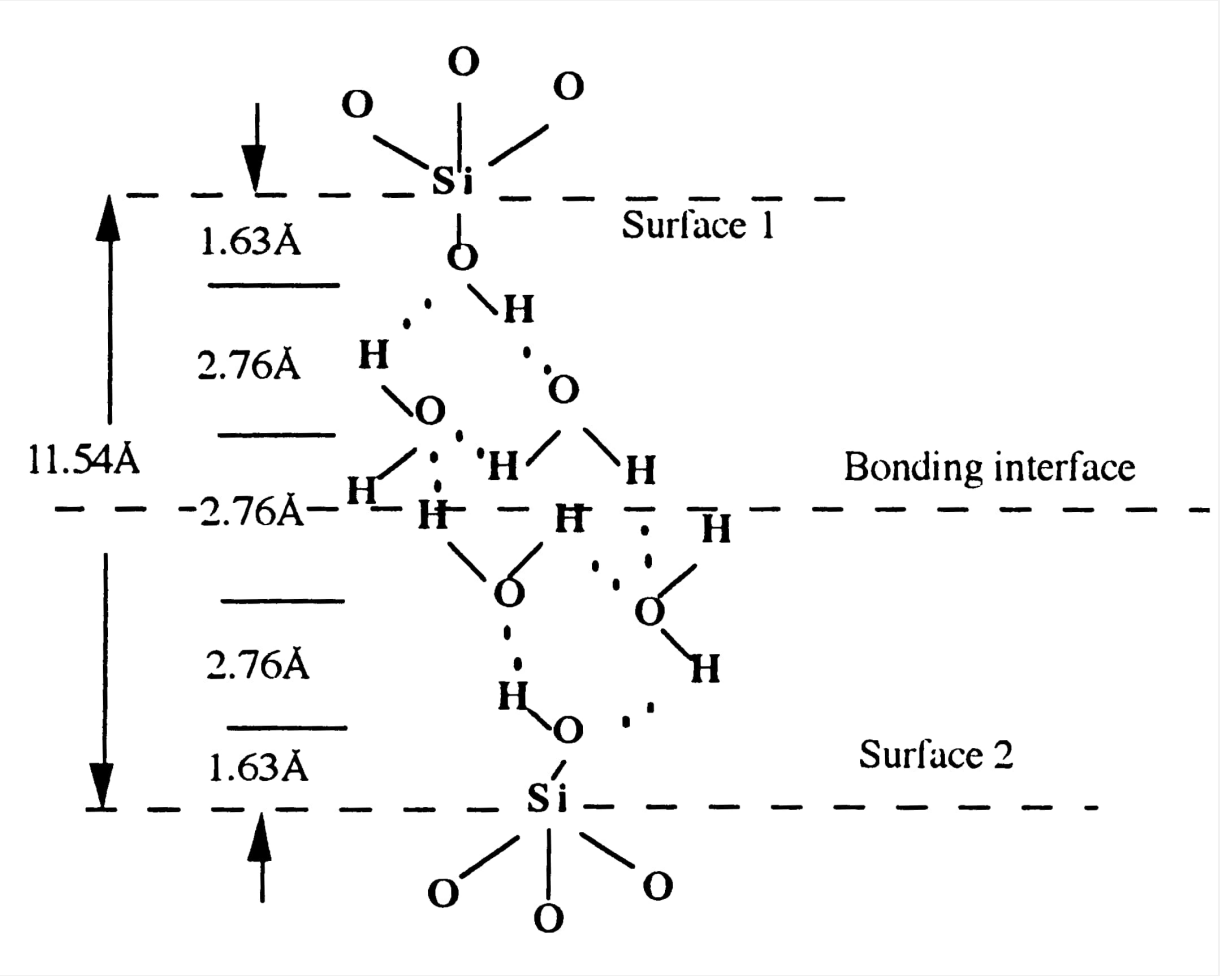
- surface cleaning in RCA-1 (NH_4OH-H_2O_2)->Si-OH
- room temperature joining
- initiation of bonding at centre or wafer flat
- anneal for bond energy improvement 1000ºC or 400ºC
- further processing with some limitations:
  - gases in cavities expand
  - thin membranes bend
  - bonded wafer stack is thicker than usual





M.Schmidt, MIT

Bonding of hydrophylic Si surfaces: low temperature, low strength



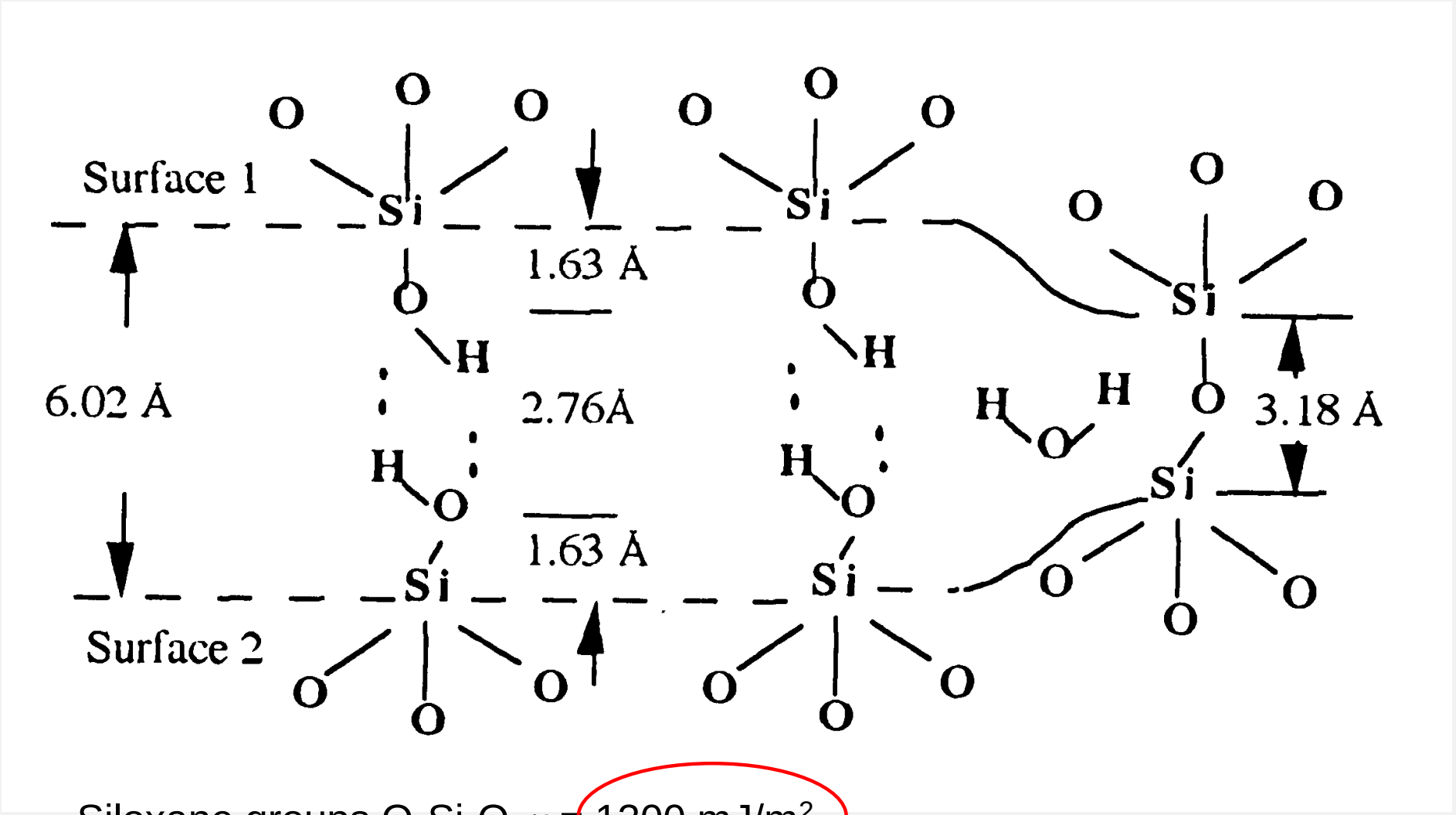
Surface energy

$\gamma = (1/2)\, E_{bond}\, d_{bond}$,

E_{bond} - bond strength
d_{bond} - bond density

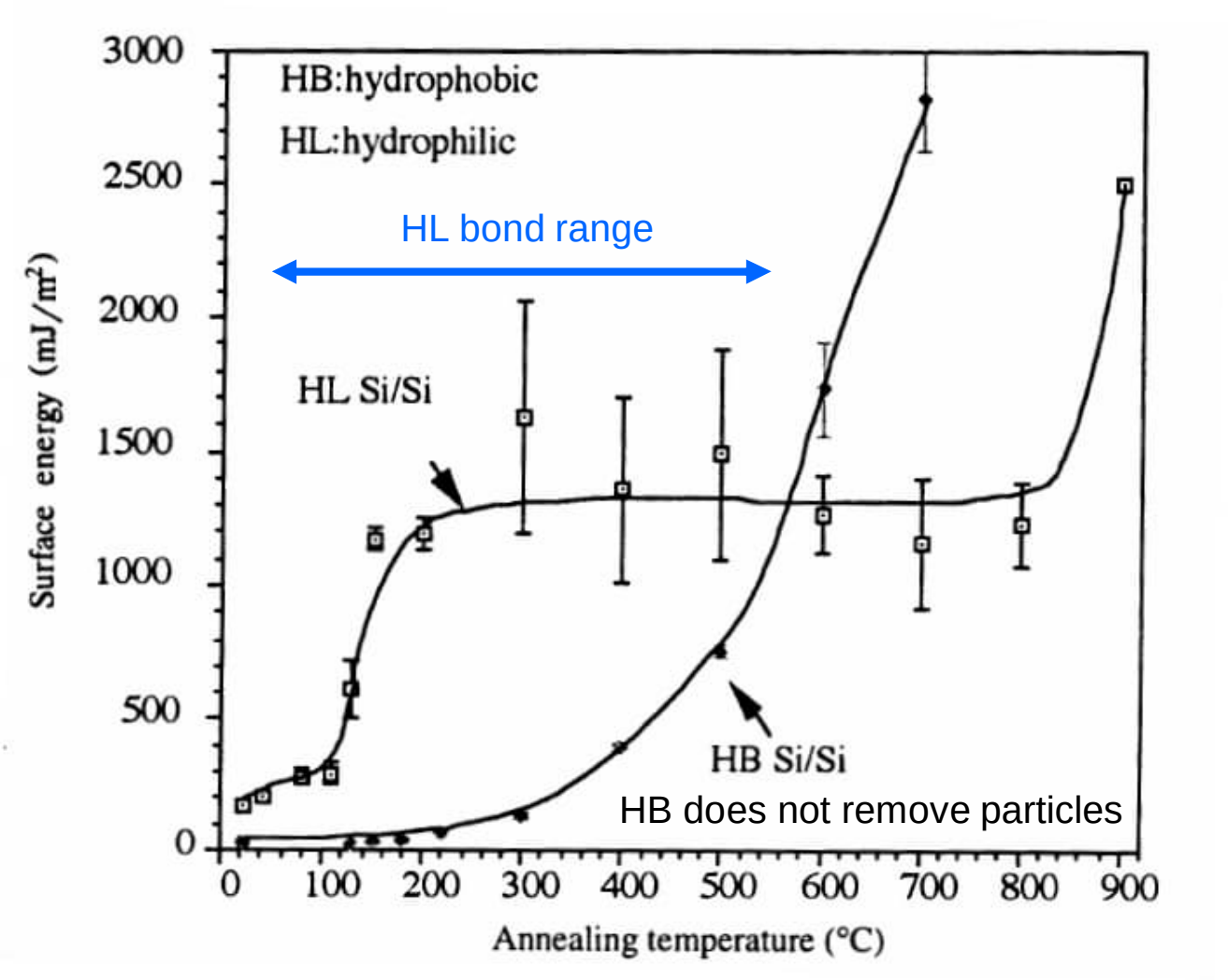
Silanol groups Si-OH
γ = 200 mJ/m^2

H_2O removing and siloxane bond formation: high temperature, high strength



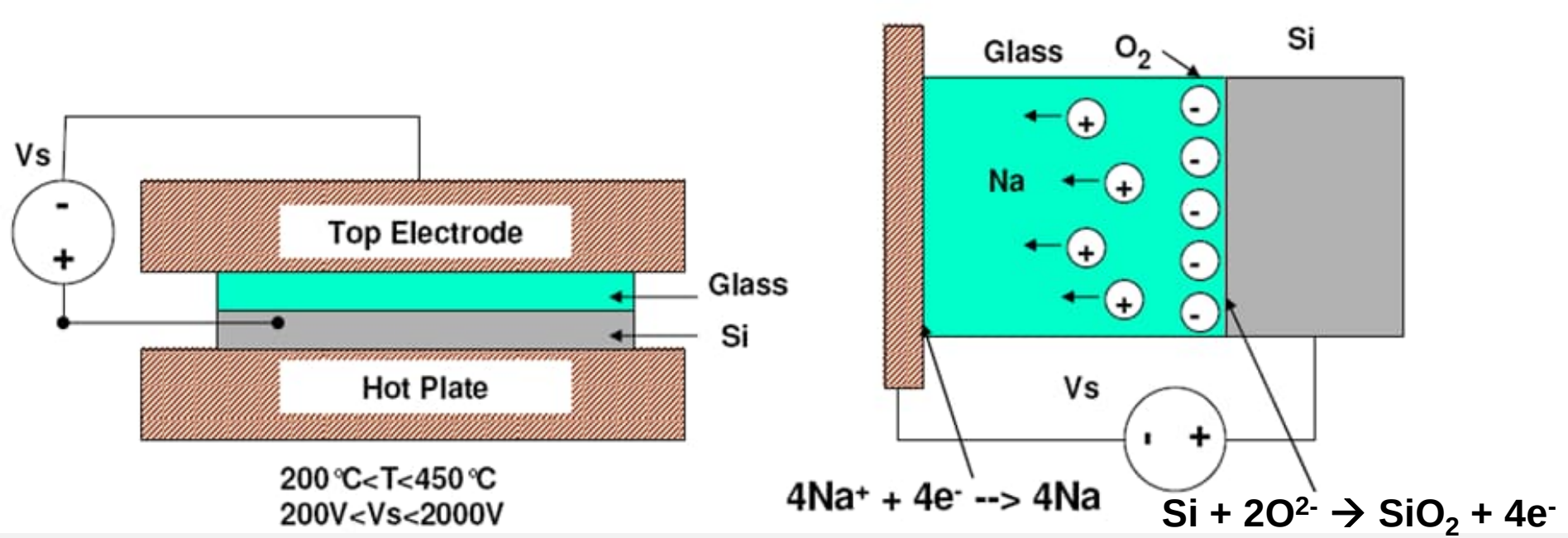
Siloxane groups O-Si-O γ = 1300 mJ/m^2

Bond strength



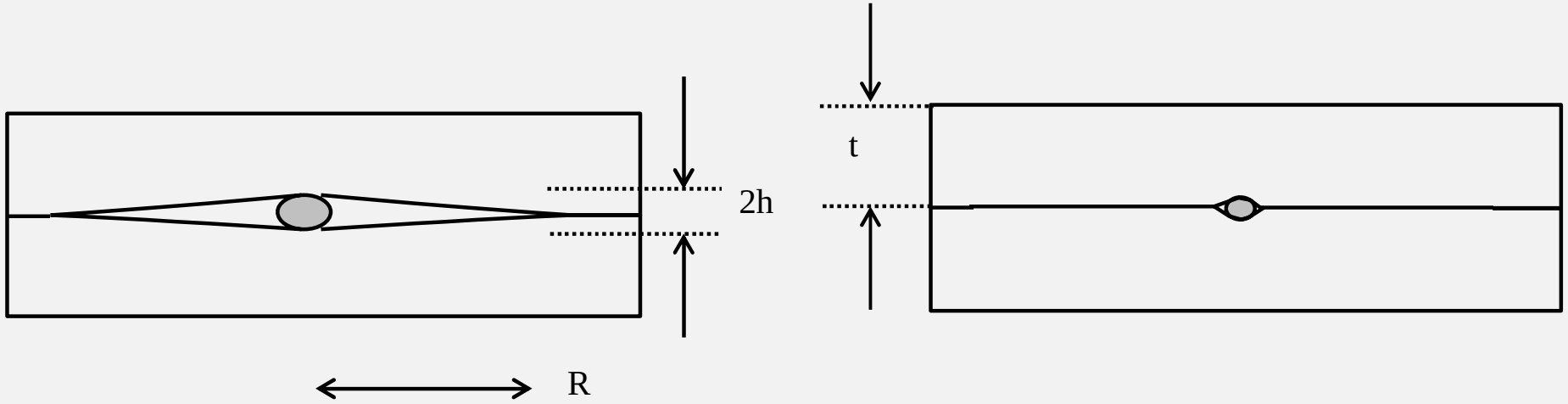
Tong & Gösele: Semiconductor wafer bonding

Anodic bonding



1. Limited number of glasses can be used (CTE problem), e.g. Pyrex 7740
2. Surface cleaning to remove particles. Native oxide, thin metal are not a problem
3. Pump to vacuum, heating, alignment
4. Mechanical contact and applying voltage
5. Electrostatic force pull wafers together and SiO_2 bonds are created

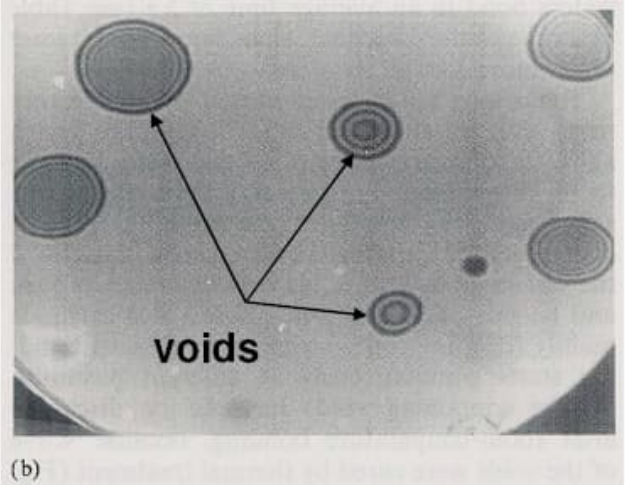
Interface particles and bubbles



Voids created by particles are very large compared to particles themselves because silicon is rigid material

Silicon can conform only to very small particles, < 100 nm

Problems with trapped gas

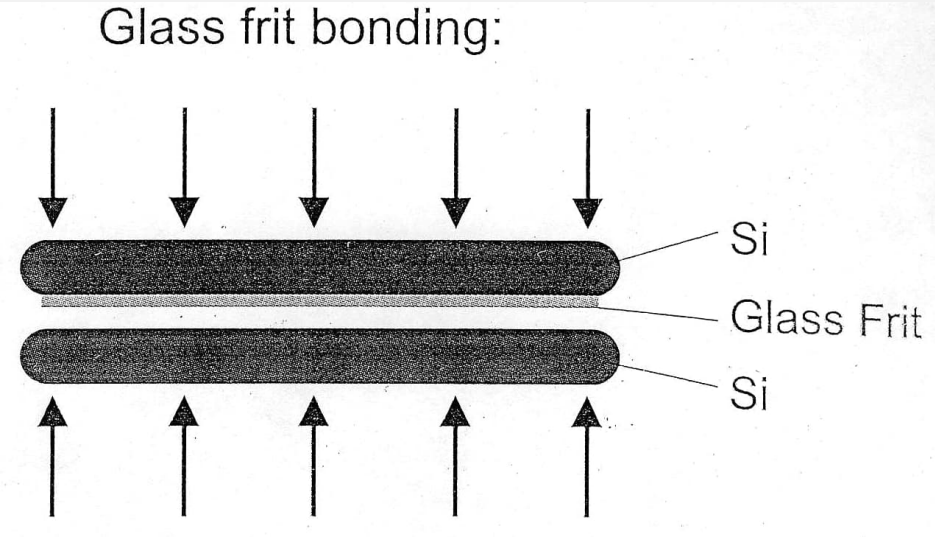


Some of voids due to trapped gas

S. Franssila presentation, Microsyste tech., 2006

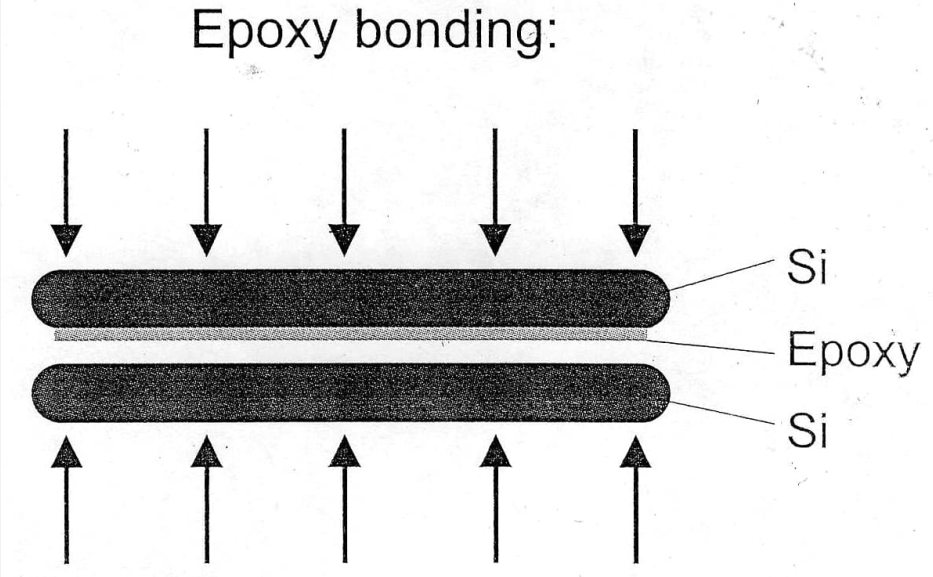
Glass frit and adhesive bonding

Rough surfaces
High strength
No outgassing
Si, SiO_2, Si_3N_4, Al, Ti, glass
Pattern by screen printing



450ºC

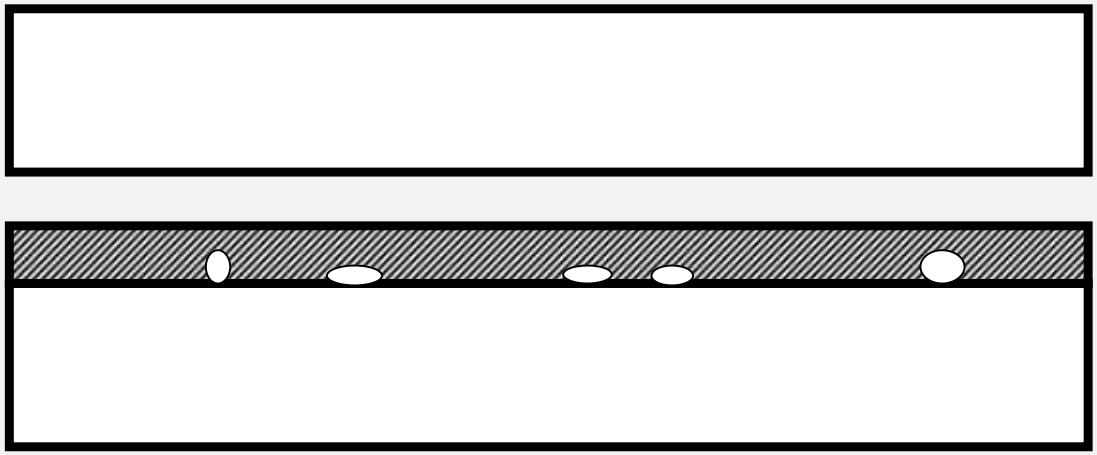
Rough surfaces
Low temperature
Outgassing
Pattern by screen printing



200ºC

Adhesive bonding

Deposit adhesive polymer on wafer



Any materials

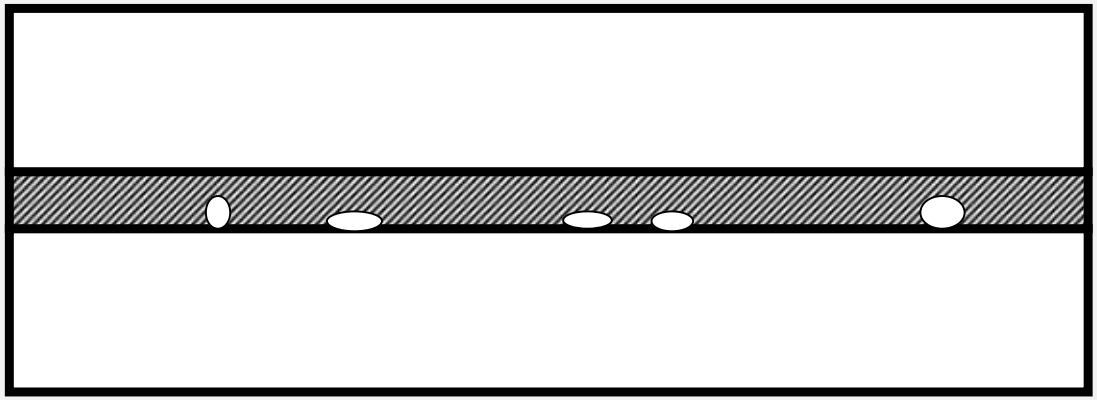
Low temperature <200C

Tolerant to particles

Structured wafers

Low cost

Bring to contact at T>Tg and bake



Instability

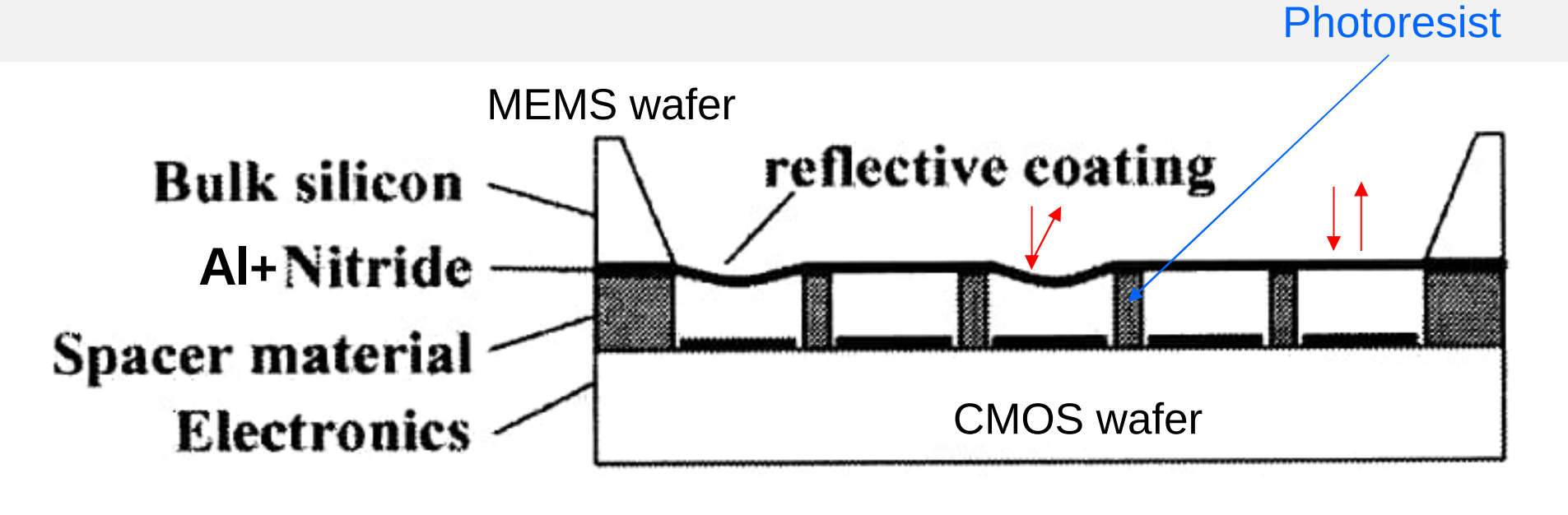
Outgassing

Moisture penetration

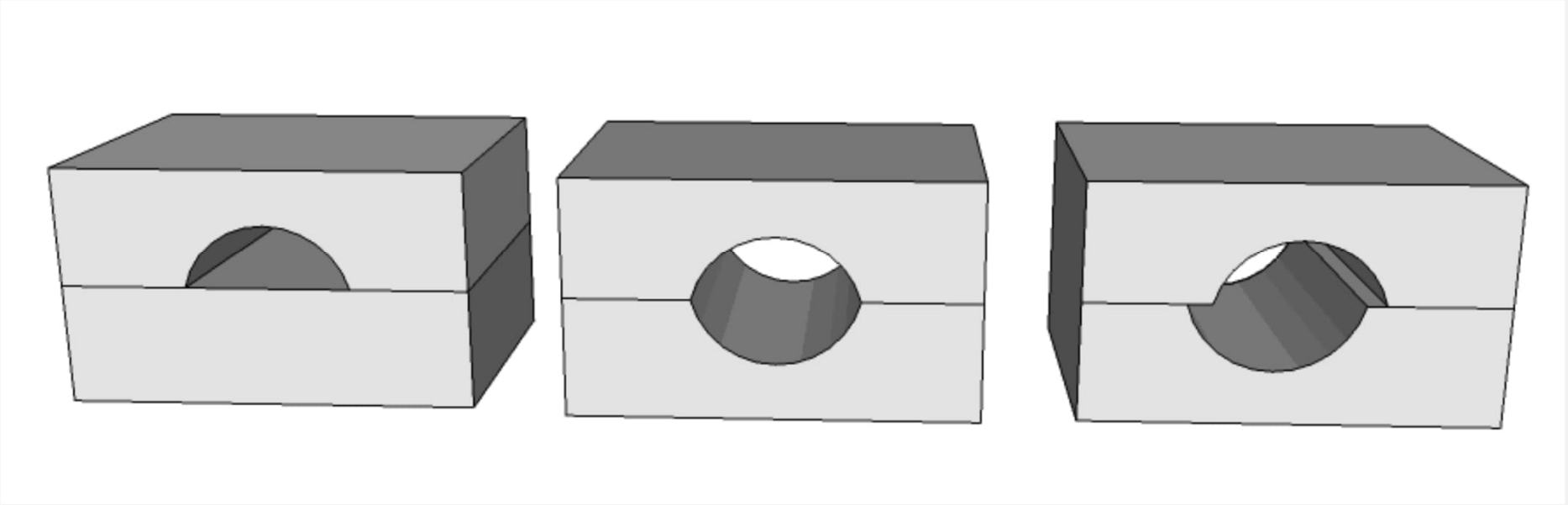
Low temp. processing

Adhesive bonding of patterned wafers

Aluminium mirror on nitride membrane



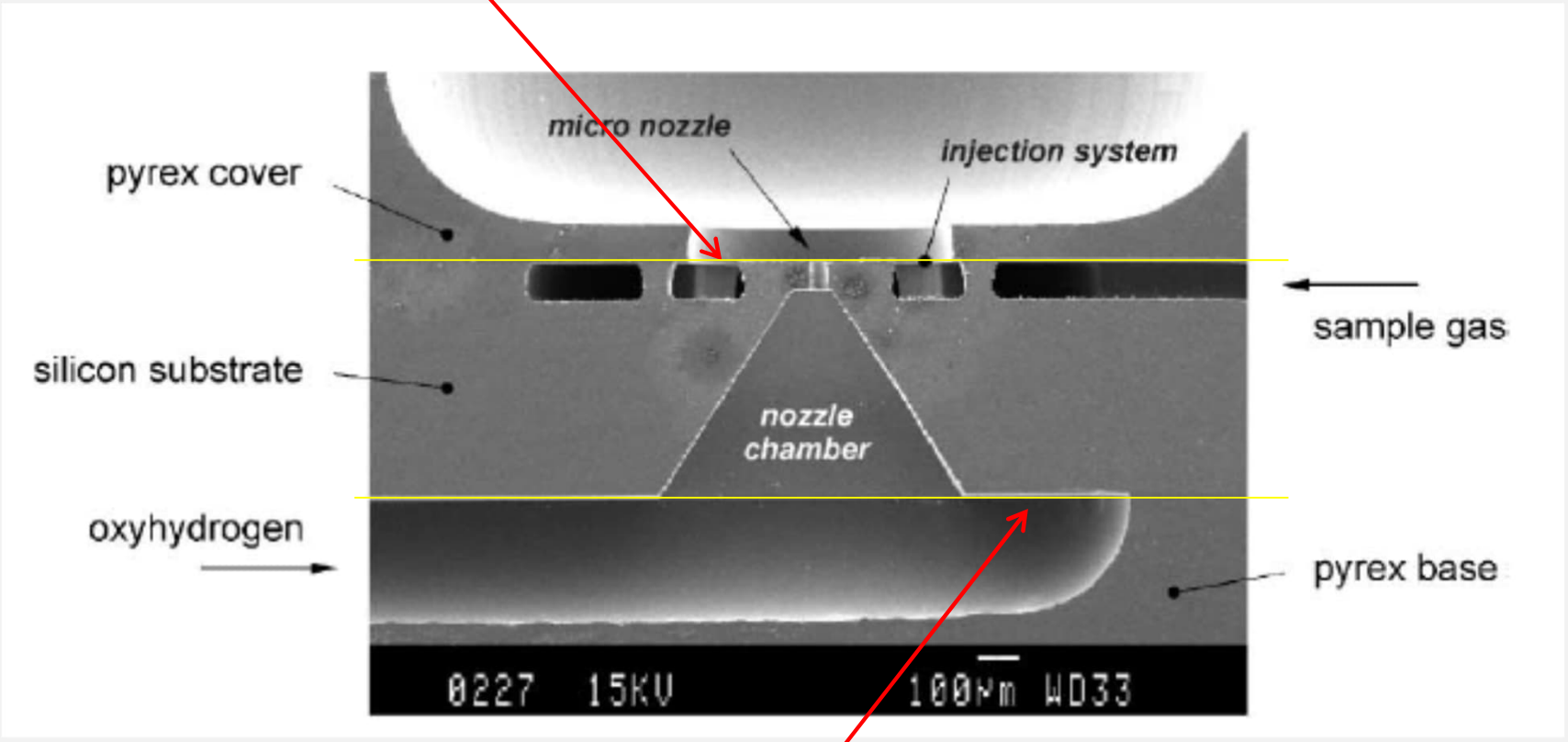
Bond alignment I



None	Perfect	Misaligned
Simple equipment enough	Requires advanced tools	Some devices more sensitive to misalignment than others.

Bond alignment II

Critical alignment



Non-critical alignment

Summary I

- Bonding provides vertical integration of separately processed substrates
- High quality bonding can be done for limited range of materials and at elevated temperature
- Bonding is VERY sensitive to surface preparation – particles, chemical bonds etc

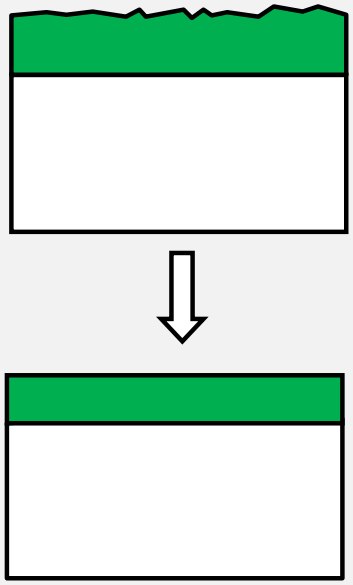
Chemical mechanical planarization

- Chemical Mechanical Planarization (CMP) combines chemical action with mechanical abrasion to achieve selective material removal through polishing

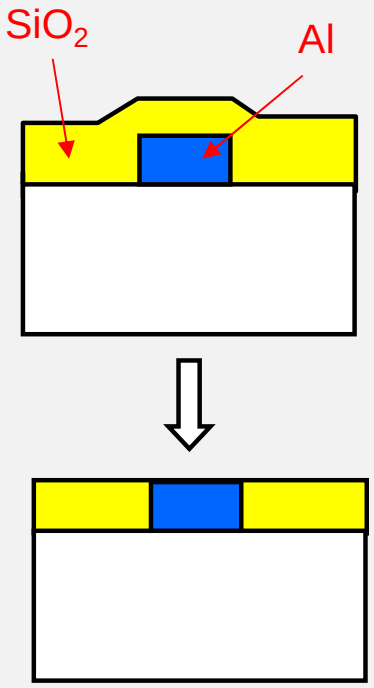
- CMP achieves the greatest degree of planarization of any currently known technique

Applications of CMP

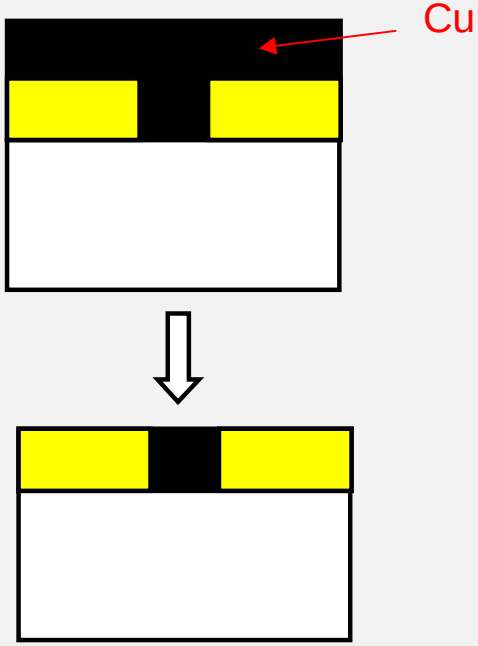
Smoothing



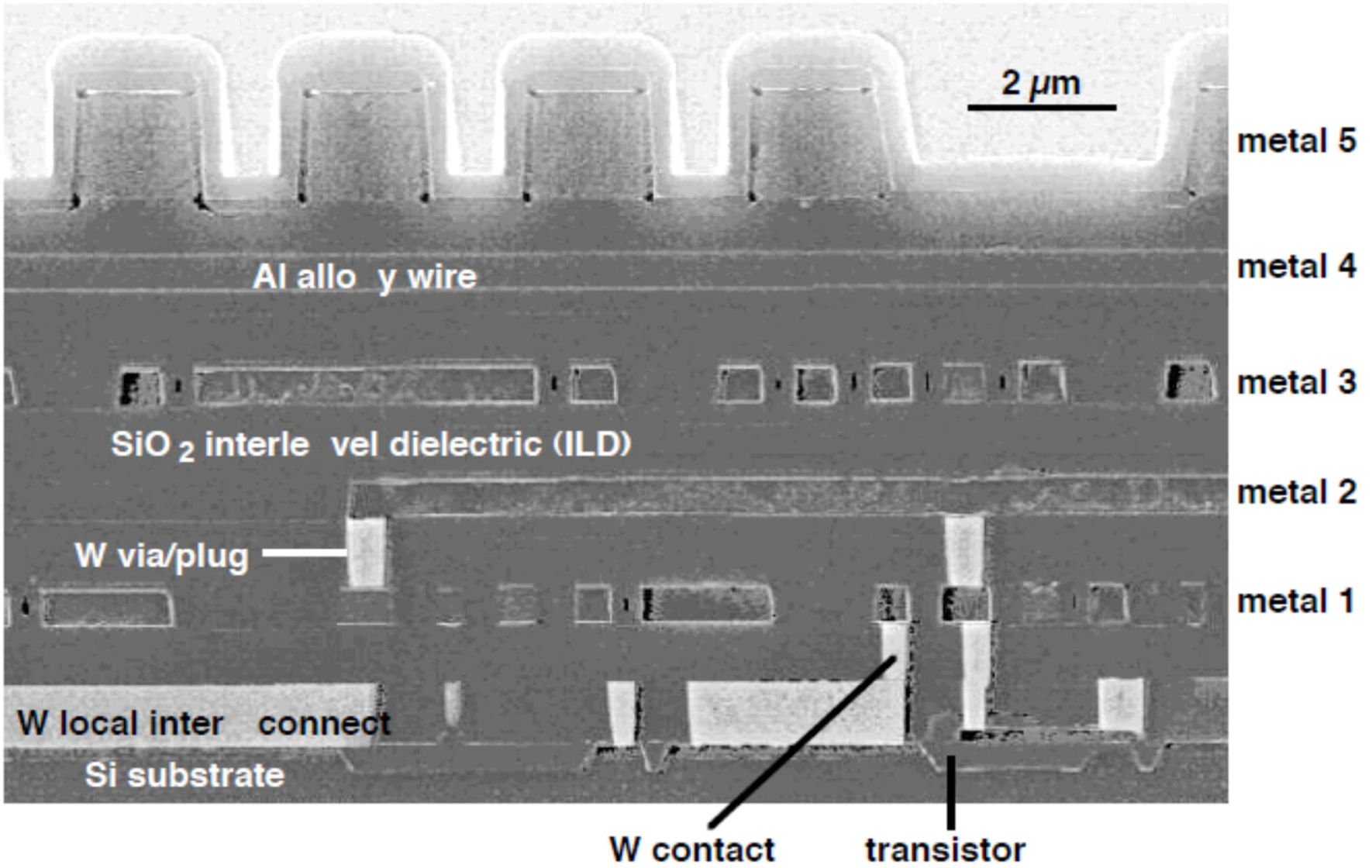
Planarization



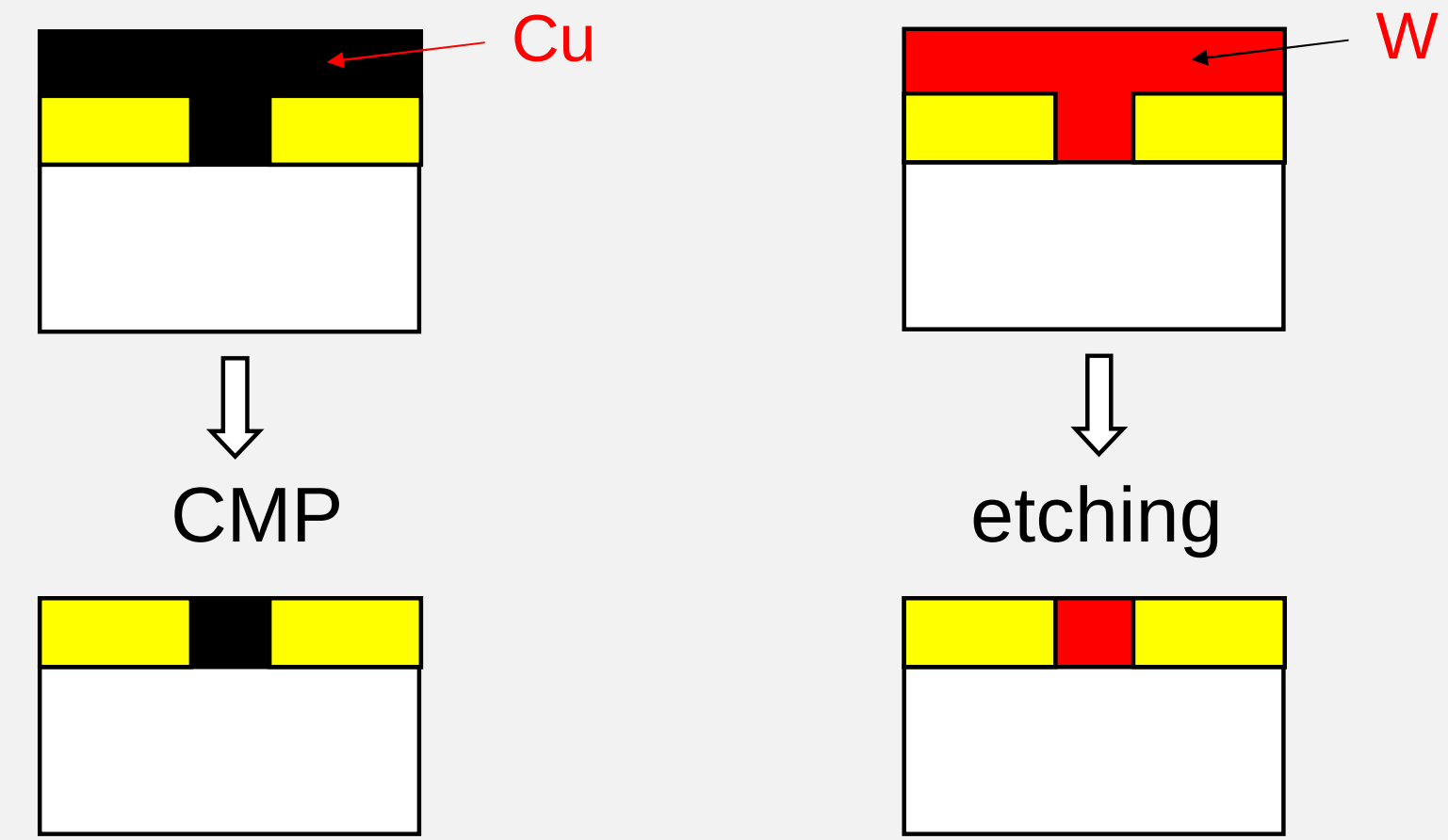
Damascene or patterning



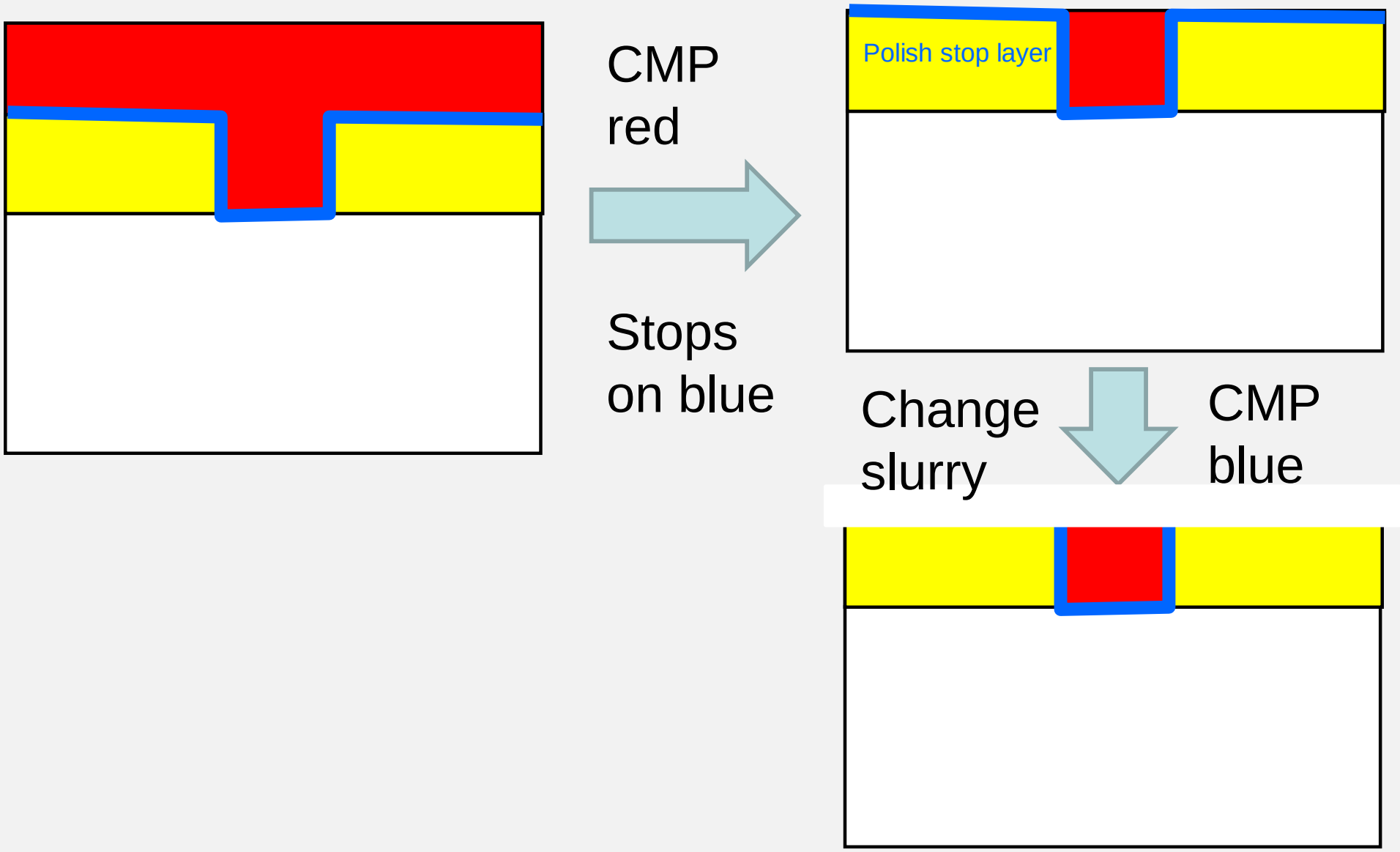
A Motorola μprocessor with 5 Al layers



Cu damascene vs. W etchback ?



Multilayer processing by CMP



Polish selectivity & polish stop

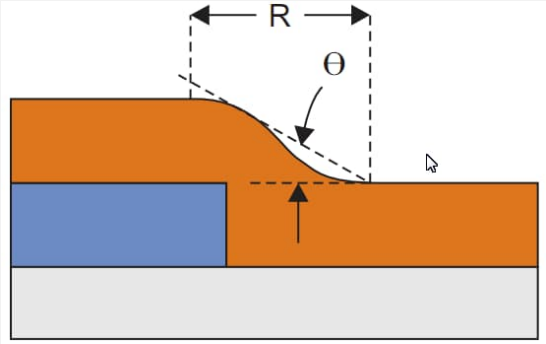
Polish selectivity:

Polishing rate of material 1 / polishing rate of material 2

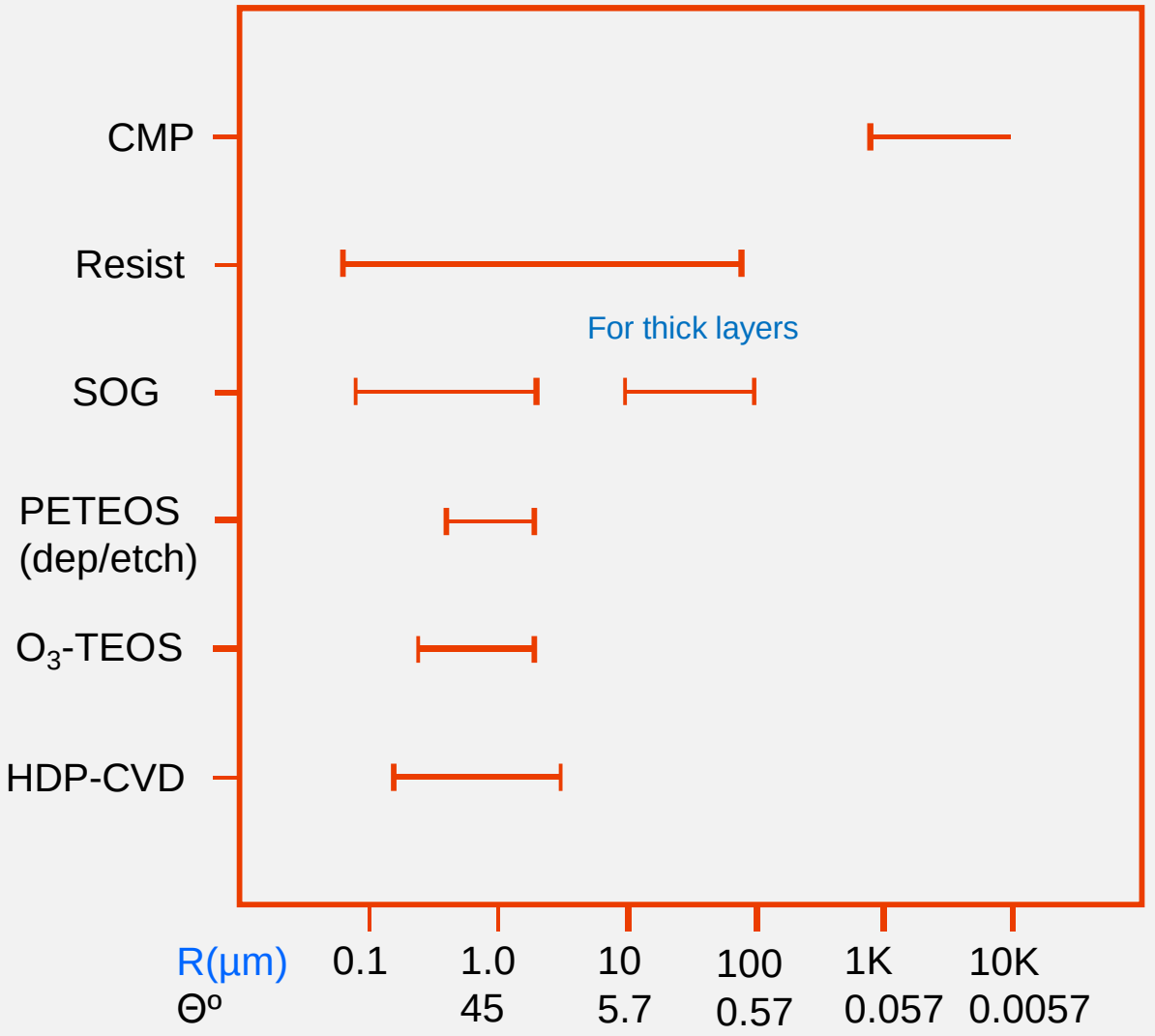
e.g. Copper 400 nm/min Oxide 40 nm/min ➔ 10:1
e.g. Copper 400 nm/min TaN 10 nm/min ➔ 40:1

Polish stop: if selectivity is very high, we call it polish stop (even though some underlying material is removed)

Planarization



R – planarization length



TEOS - Tetraethyl orthosilicate, 600C

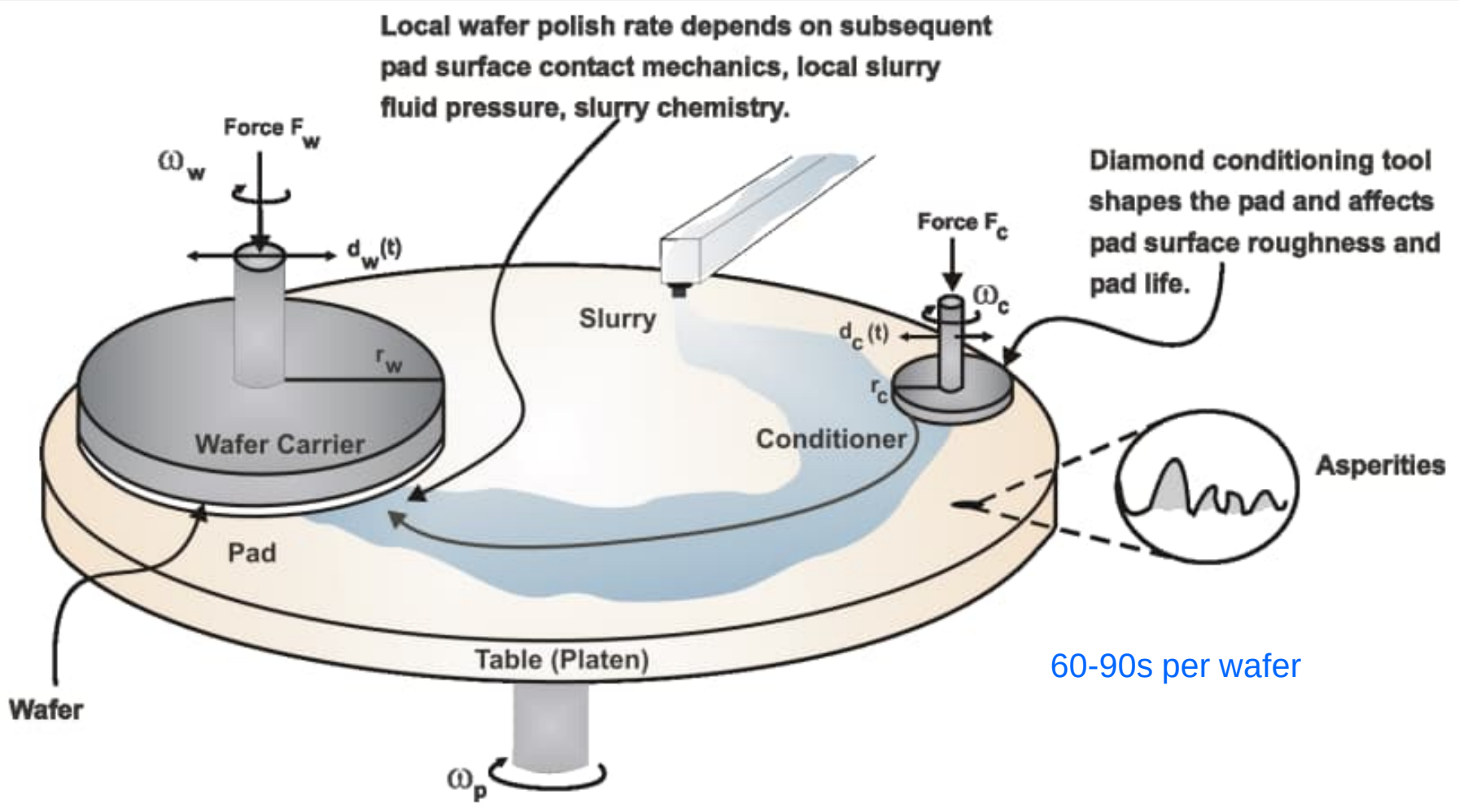
PETEOS – plasma enhanced TEOS, 400C

O_3-TEOS – TEOS plus O_3 CVD, 400C

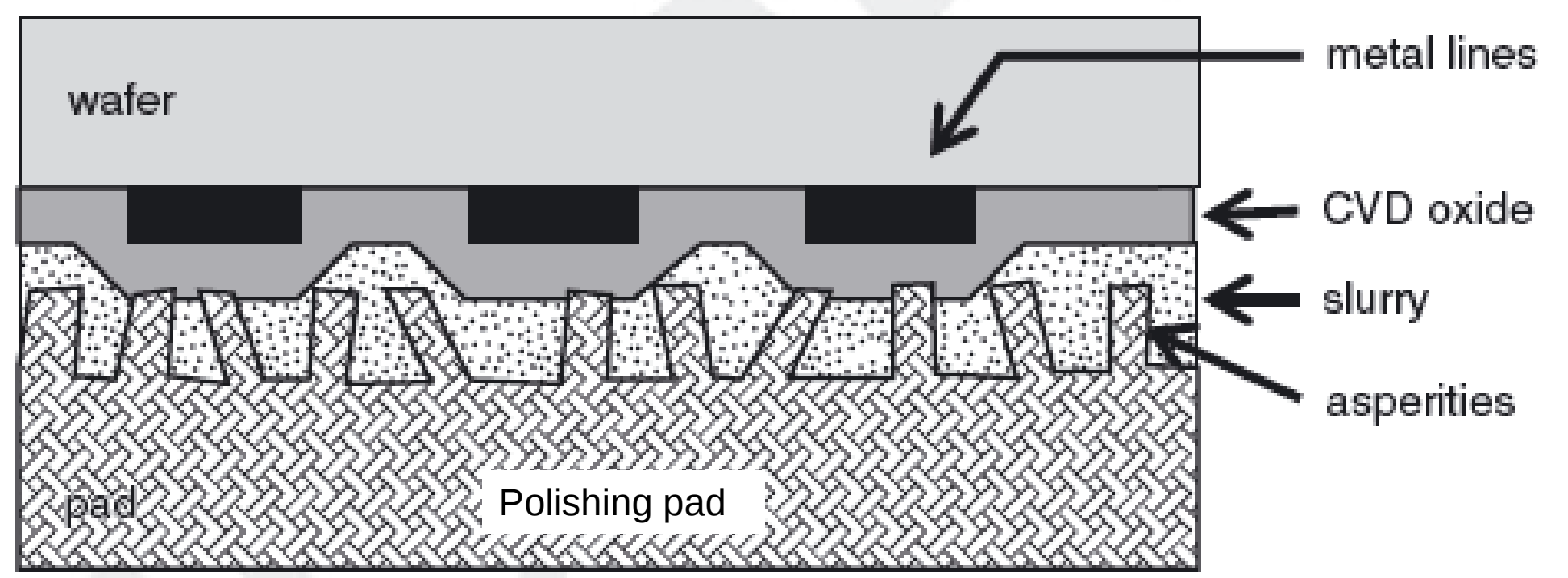
SOG – spin on glass

HDP-CVD – high density plasma CVD, 100C

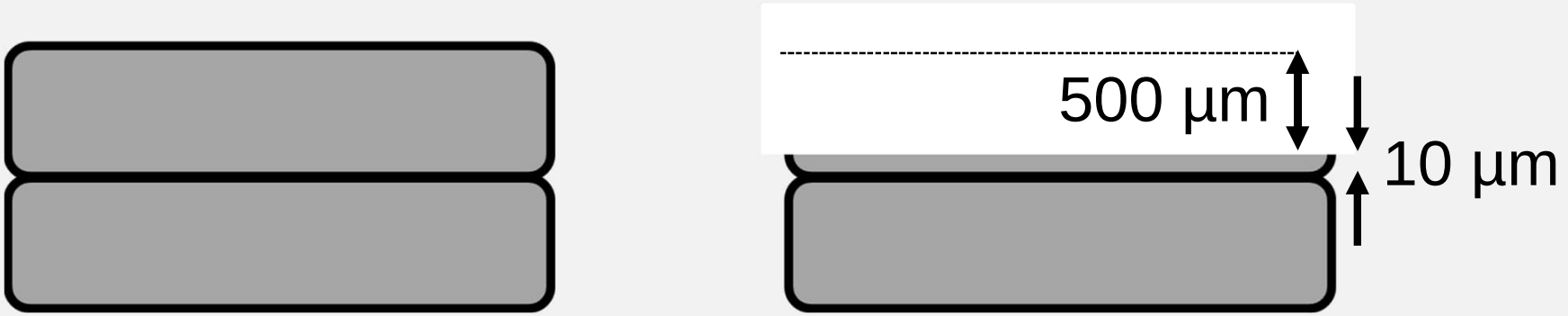
Rotary CMP tool



Polishing in action



Grinding vs. polishing

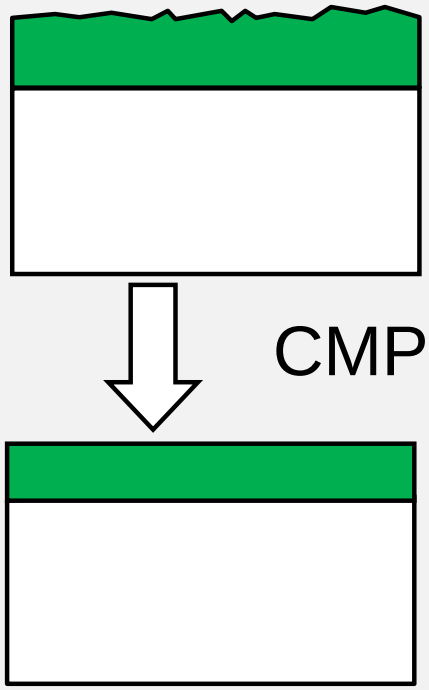


Both use abrasive particles, but:

Grinding removes 10 µm/min in large chunks because large particles
Grinding results in very rough surface because very large chunks
Grinding leaves mechanical damage due to large chunks being torn off

Polishing uses nanoparticles to achieve smooth surfaces
Polishing removes 0.1 µm/min because small particles, small forces
Mechanism of removal is chemical and mechanical (CMP !)

Polishing is needed after grinding !

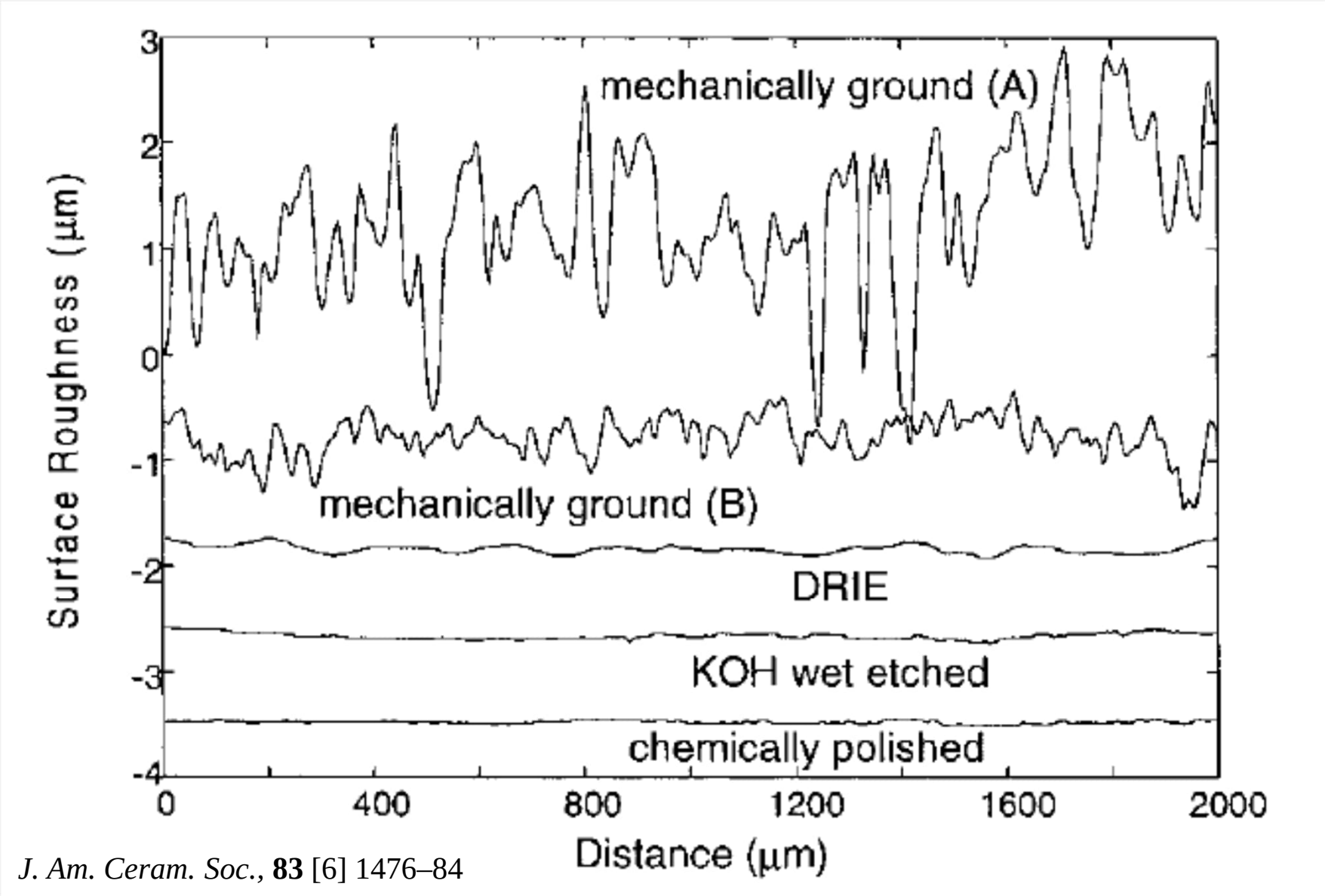


Surface roughness e.g. 200 nm

Surface roughness e.g. 1 nm

Surface roughness

Log scale



J. Am. Ceram. Soc., **83** [6] 1476–84

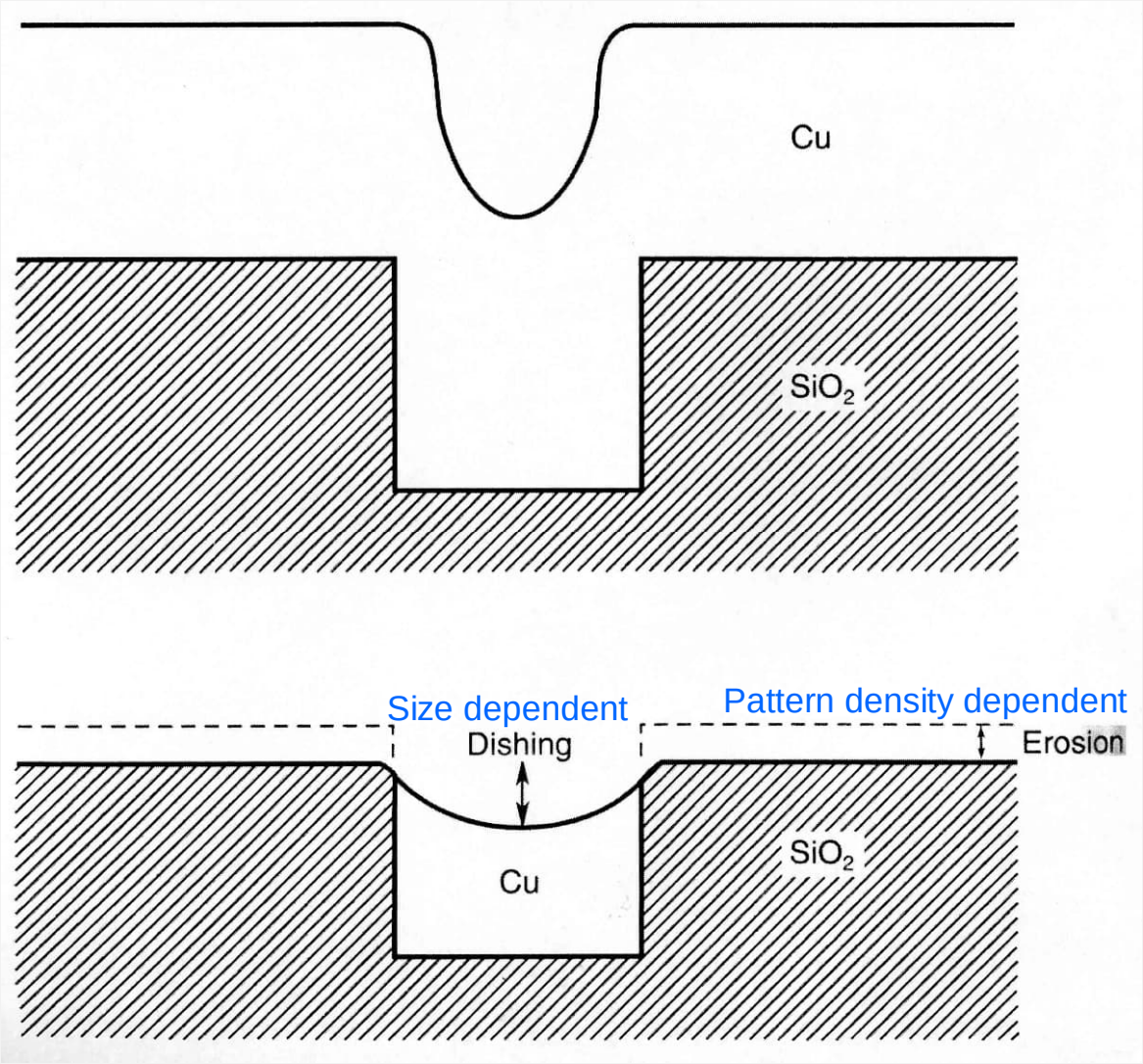
CMP tool input variables

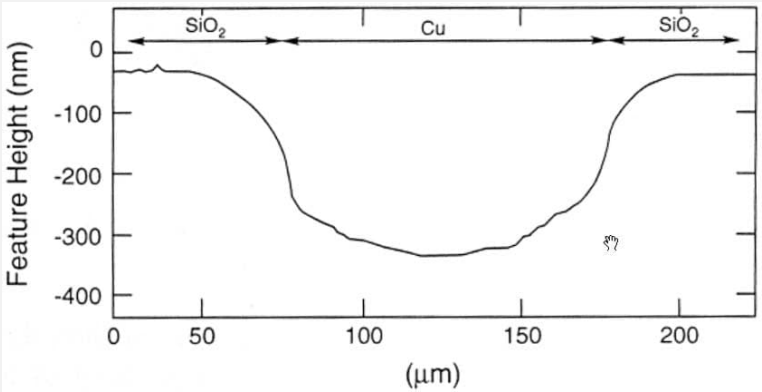
- -platen rotation 10-100 rpm
- -velocity 10-100 cm/s
- -applied pressure (load) 10-50 kPa
- -slurry supply rate 50-500 ml/min
- -slurry chemicals (pH, conc., viscosity,...)
- -pad (material, porosity, hardness,...)
- -abrasives (size, type, hardness, conc.,...)
- -wafer (curvature, mounting, backpressure)
- -patterns (size, density, ...)
- -films (hardness, μ-structure, stress, ...)

Process outputs resemble etching ones

- -polish rate, 100-500 nm/min
- -selectivity 1:1 – 100:1
  (blind polishing and stopped polishing)
- -overpolish time
- -pattern density effects
- -uniformity across wafer, 10%
- -wafer-to-wafer repeatability, 10%

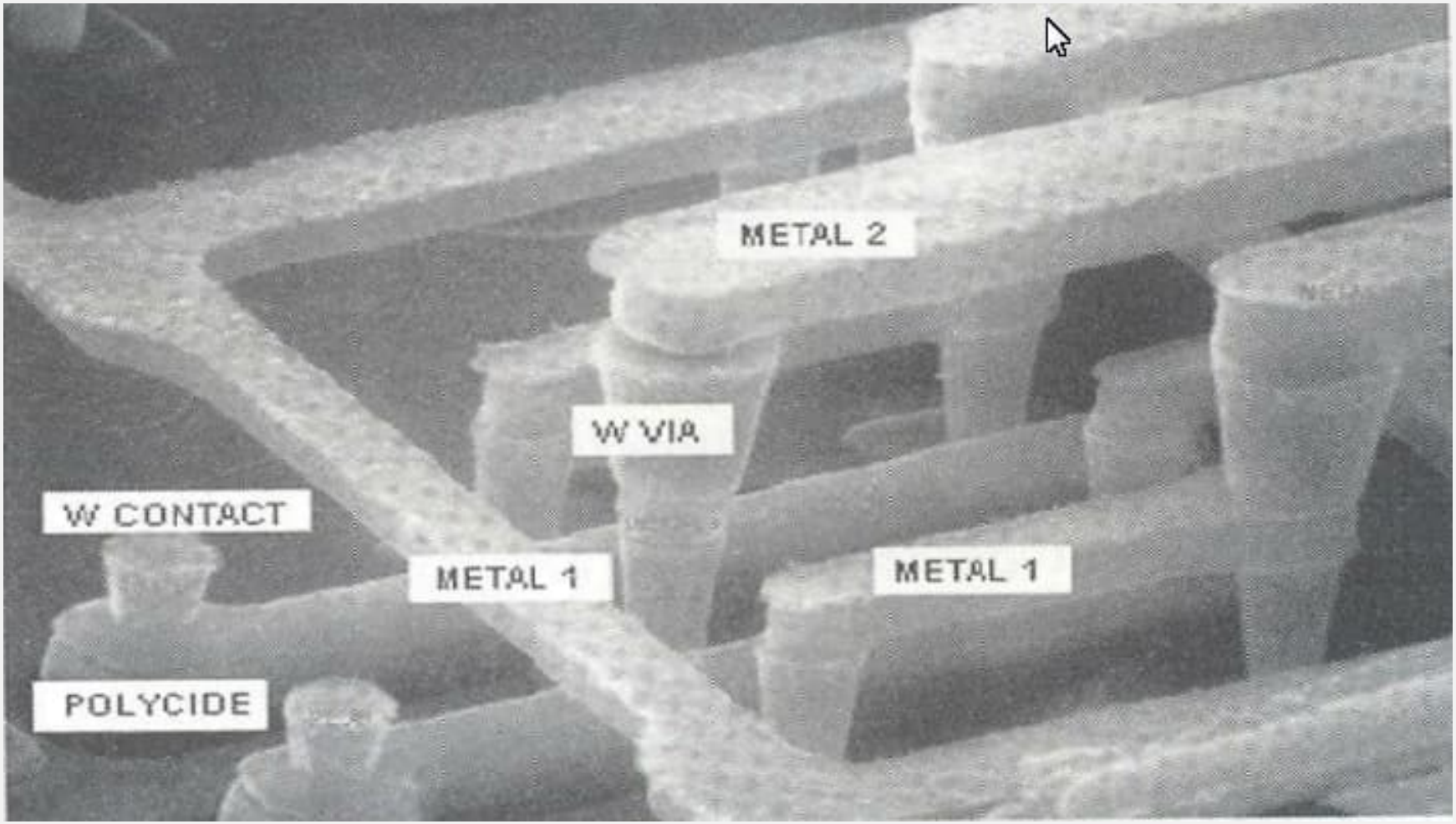
Erosion and dishing in CMP





Plug recess – pure chemical etching of metal

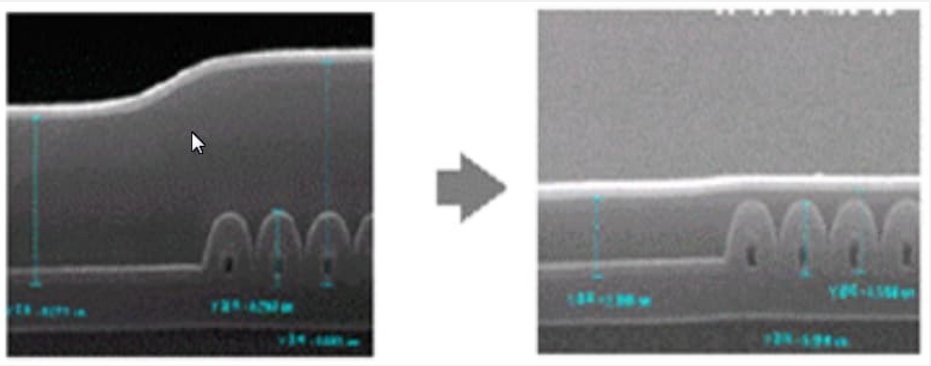
Planarization in multilevel metallization



Silicon VLSI Technology by Plummer et al.

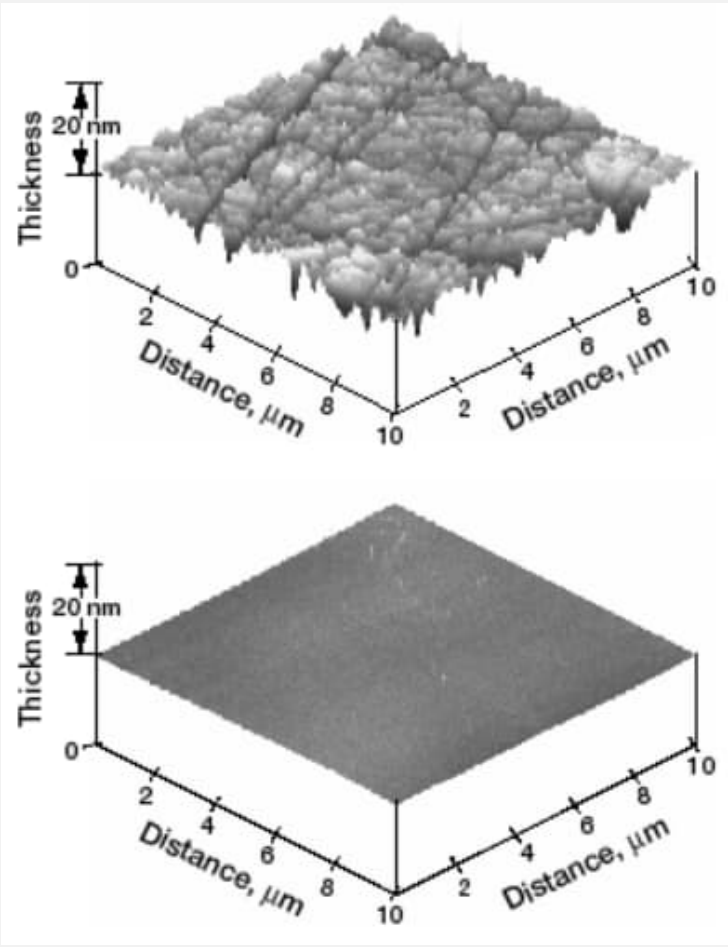
Results of CMP

CMP of SiO_2



Planarization

SiC wafer before and after CMP



Polishing →

Etching and CMP

- The same rate 100 – 1000 nm/min
- Surface/transport limitation of reactions
- Pattern dependency is the same, but pattern size effect is opposite
- Chemical and physical effects – ions in RIE and mechanical force in CMP
- Preferred directions/planes – verticlal in RIE and horizontal in CMP
- Post-CMP cleaning is more chanllenging than post-etching one