Etching for MEMS (based on chapters 11,20,21)

sami.franssila@aalto.fi

Etching in MEMS

Silicon etching in focus.

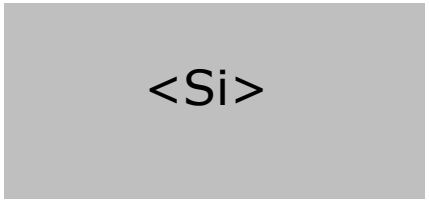
Need to etch deep, even thru the wafer, 500 µm.

So far we have mostly talked about etching thin films, 100 nm - 1 µm thick

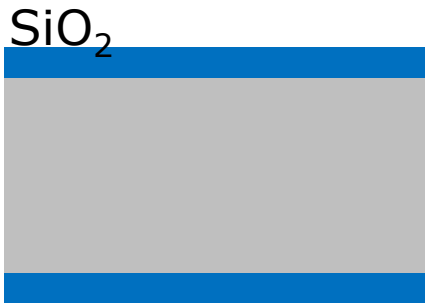
Photoresist does not tolerate long, aggressive etches ➔ hard masks.

This applies to both wet etching and DRIE.

Hard mask

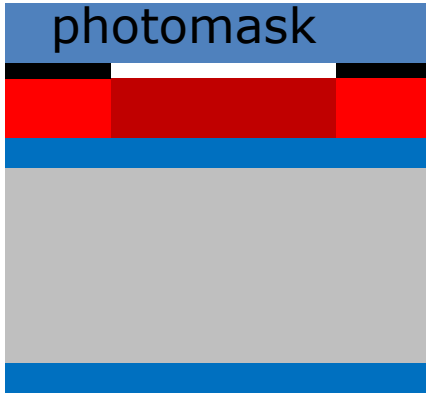


Cleaned silicon wafer



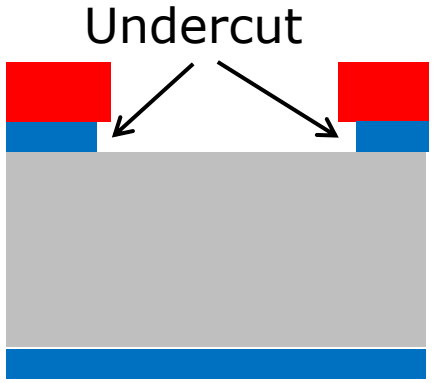
Thermal oxidation @ 1100 °C

Lithography: Photoresist spinning



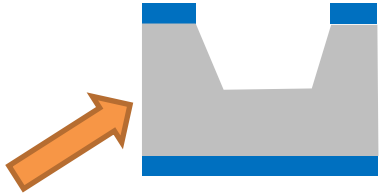
Lithography: UV-exposure

Photoresist development

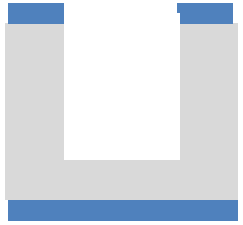


HF etching of SiO_2

Photoresist removal



KOH etch silicon



DRIE silicon

Why hard mask ?

Resists do not tolerate hot acids and bases

e.g. KOH 80^{o}C or aqua regia (HNO_3-HCl) are detrimental to resists

Resist selectivity is limited in plasma:

e.g. 100:1 resist selectivity and 1 µm thick resist only allows max. 100 µm depth, in practice ca. 50-80 µm

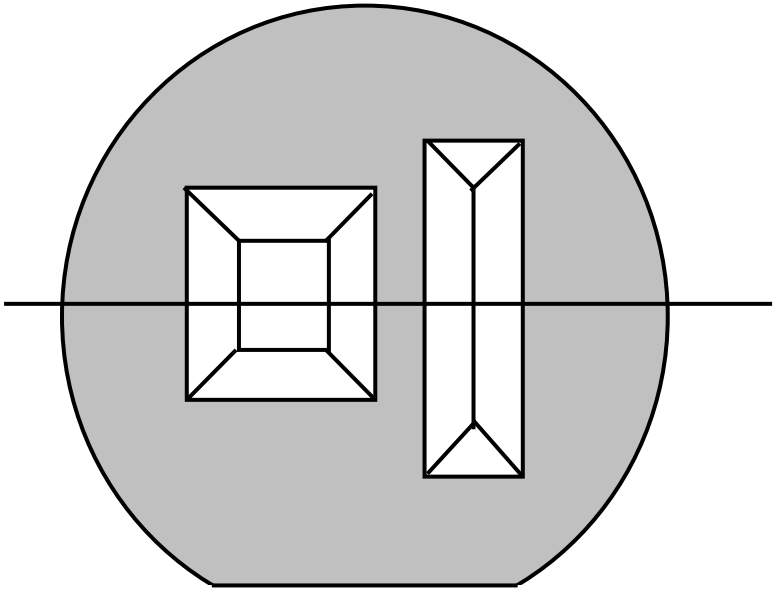
Plasmas heat resist and it will flow if $T>T_g$.

Resist also carbonizes, which makes removal difficult.

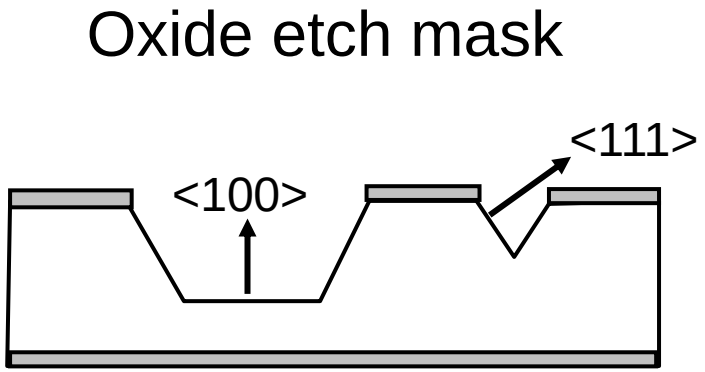
The more aggressive and/or long etches more difficult

➔ DRIE thru-wafer requires a hard mask

Anisotropic wet etching of silicon, a.k.a. crystal-plane dependent etching



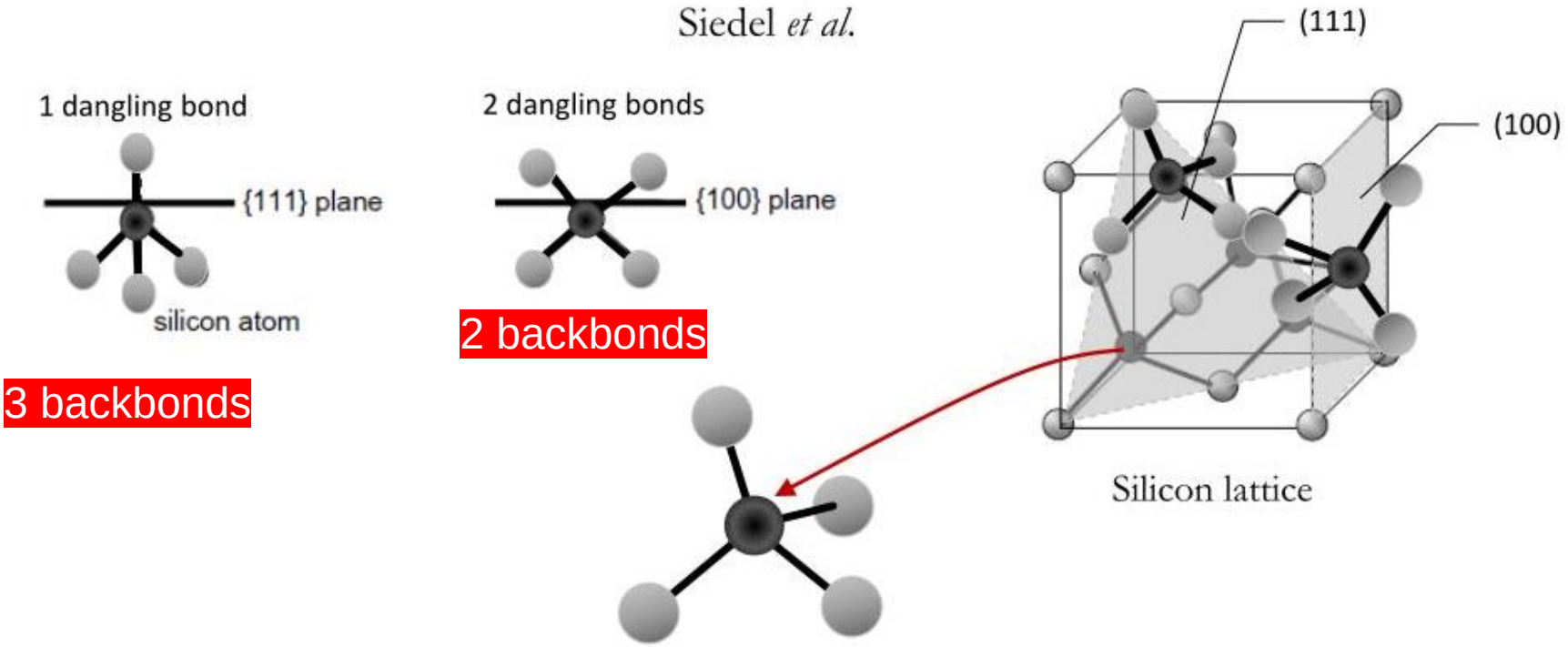
Top view (mask layout)



Cross sectional view

<100> silicon etch rate is faster (by a factor of 30 or 100) than <111> silicon

<100> vs. <111> etching

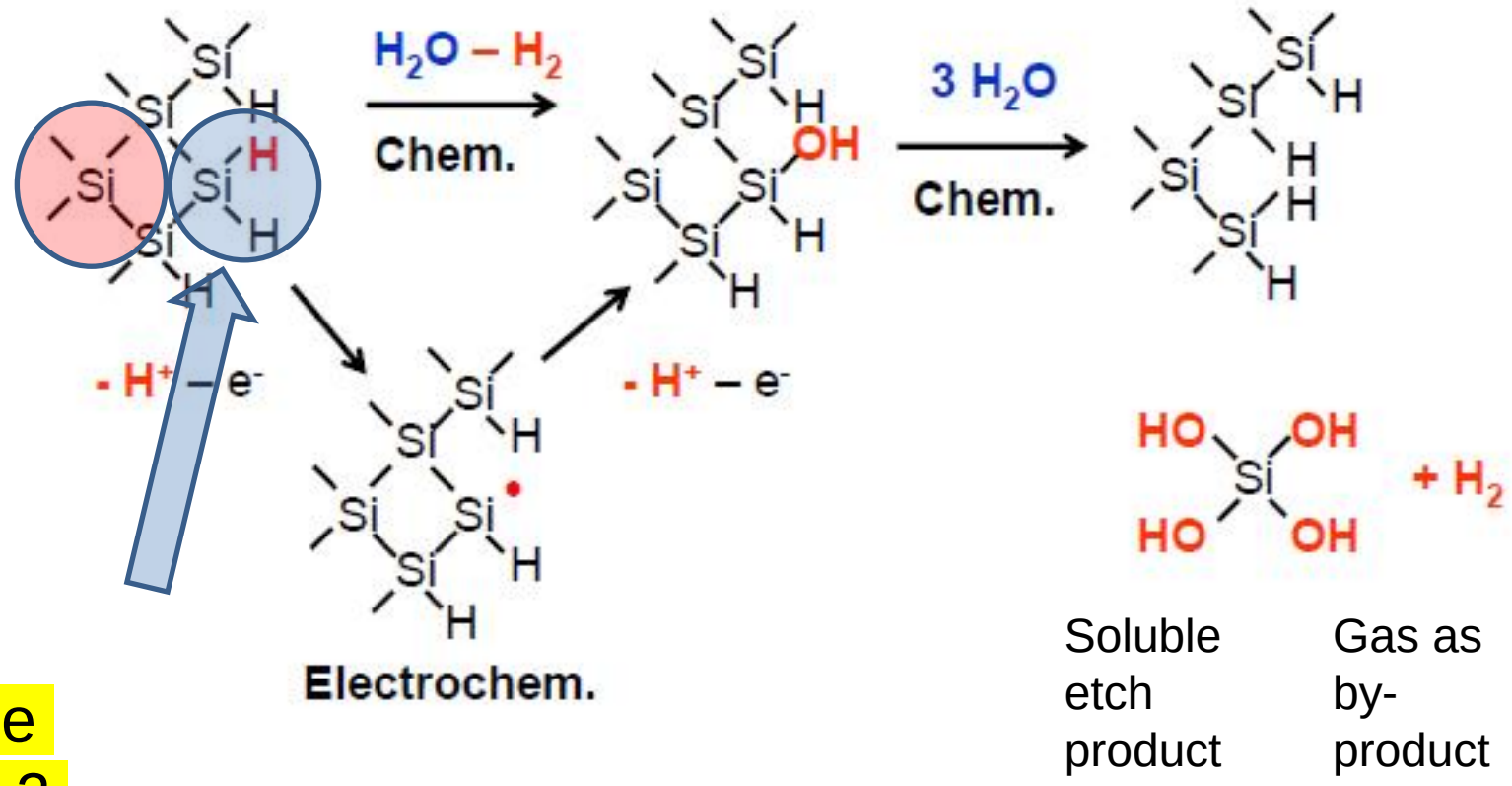


The lower reaction rate for the {111} planes is caused by the larger **activation energy** required to break bonds behind the etch plane. This is due to the larger bond density of silicon atoms behind the {111} plane.

https://www.slideserve.com/eljah/bulk-micromachining

Mechanism of KOH etching

Bulk silicon atom has 4 neighbors



Surface atoms on (100) plane bonded to 2 neighbors only

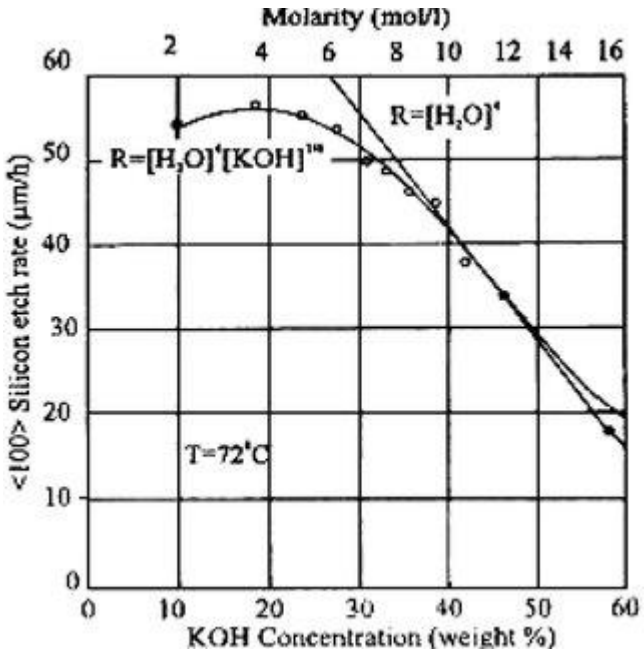
https://pmc.polytechnique.fr/spip.php?article580&lang=fr

Reaction

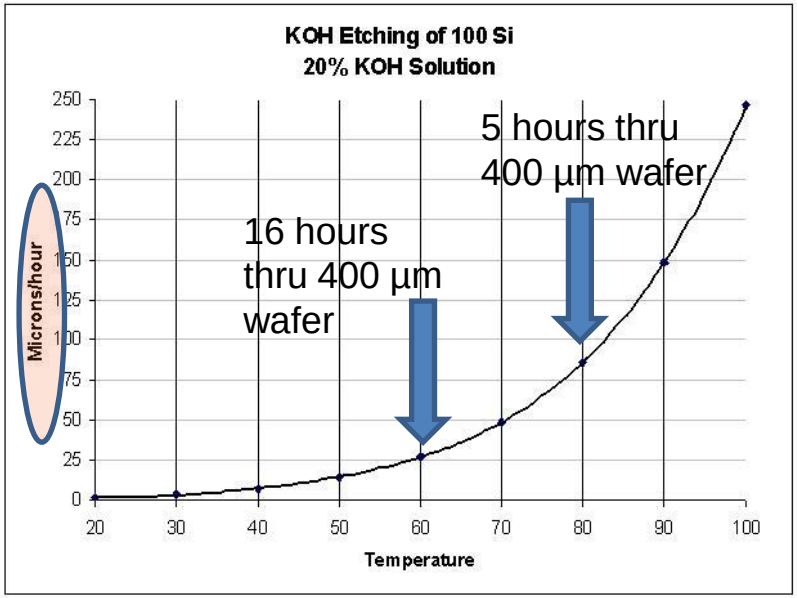
$$Si + 2OH^- \rightarrow SiOH_2^{++} + 4\,e^- \qquad \text{(oxidation step)}$$

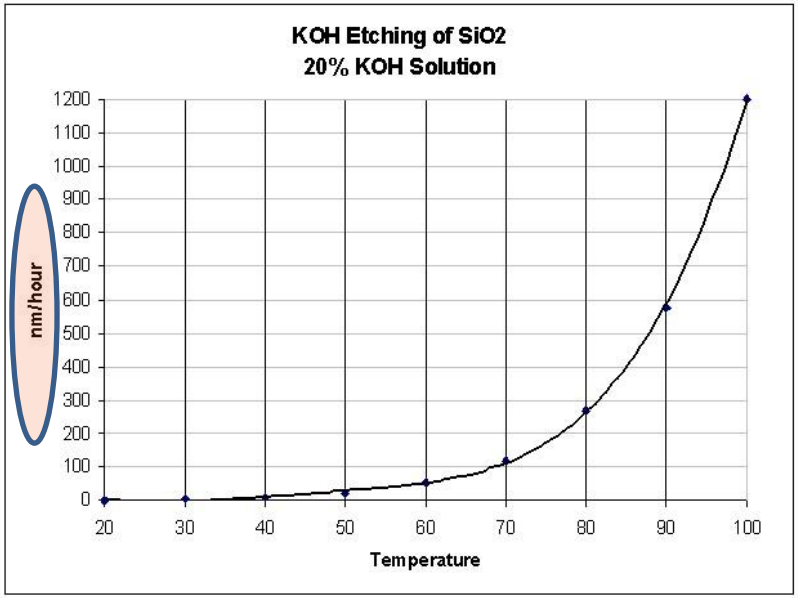
$$SiOH_2^{++} + 4\,e^- + 4\,H_2O \rightarrow Si(OH)_6^{--} + 2\,H_2 \qquad \text{(reduction step)}$$

Because both H_2O and OH^- are required by the reaction, we can expect the etch rate to be lower when either H_2O or OH^- is in short supply and the rate has maximum in the middle concentrations.



Rate and selectivity





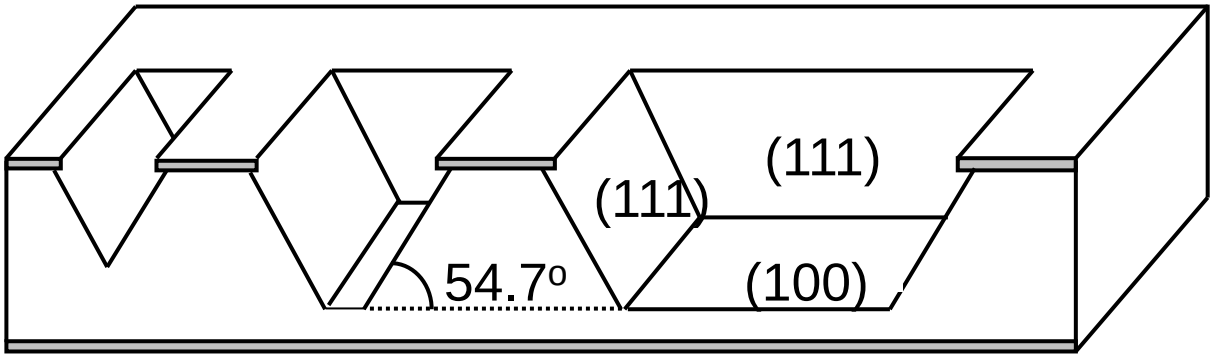
https://cleanroom.byu.edu/KOH

Both silicon and oxide etch rates show Arrhenius-behavior

Other etch criteria:
-surface quality
-uniformity (good for surface controlled)

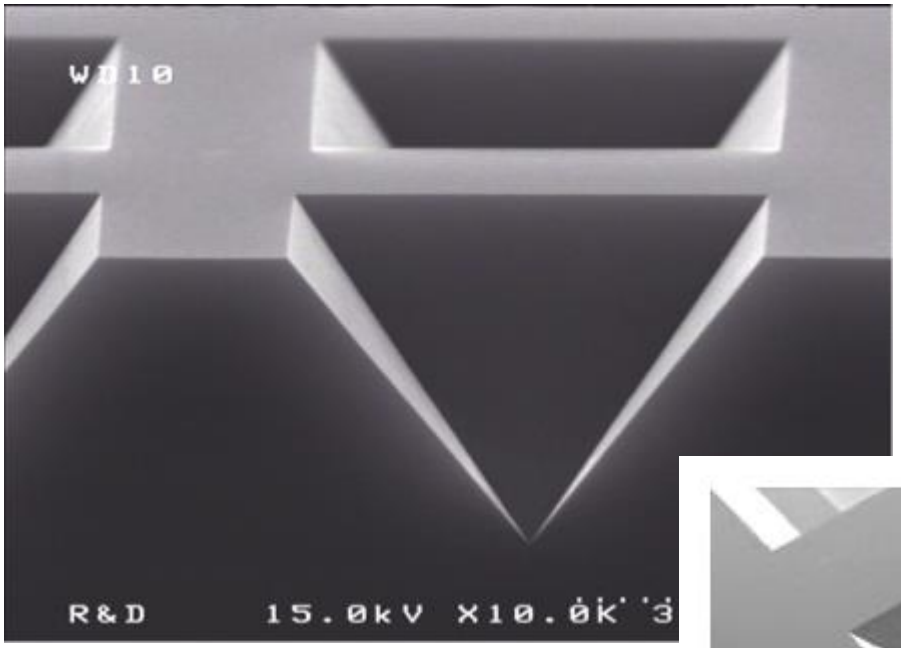
60°C: 500:1
70°C: 450:1
80°C: 300:1
90°C: 250:1

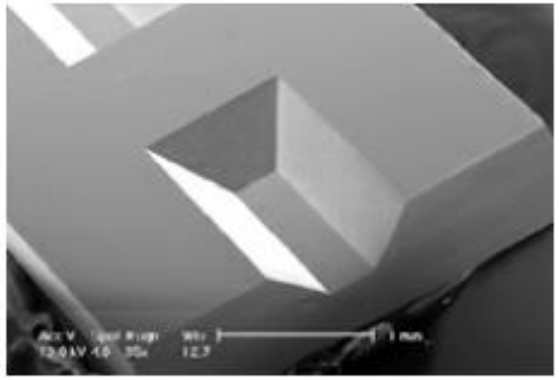
Anisotropic wet etching of silicon

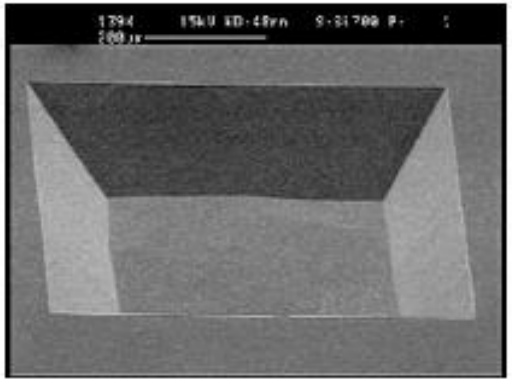


- Because <100> and <111> planes meet at 54.7° angle ➔ narrow structures form a V-goove (self-limiting)
- The sloped sidewalls are the slow etching (111) planes; the horizontal planes are fast etching (100) planes.
- Etching will terminate if the slow etching (111) planes meet.

Anisotropic wet etched profiles







http://greman.univ-tours.fr/axis-3/development-of-anisotropic-structures-by-electrochemical-etching-for-3d-devices-276485.kjsp

https://www.mems-exchange.org/MEMS/fabrication.html

Mask shape and orientation

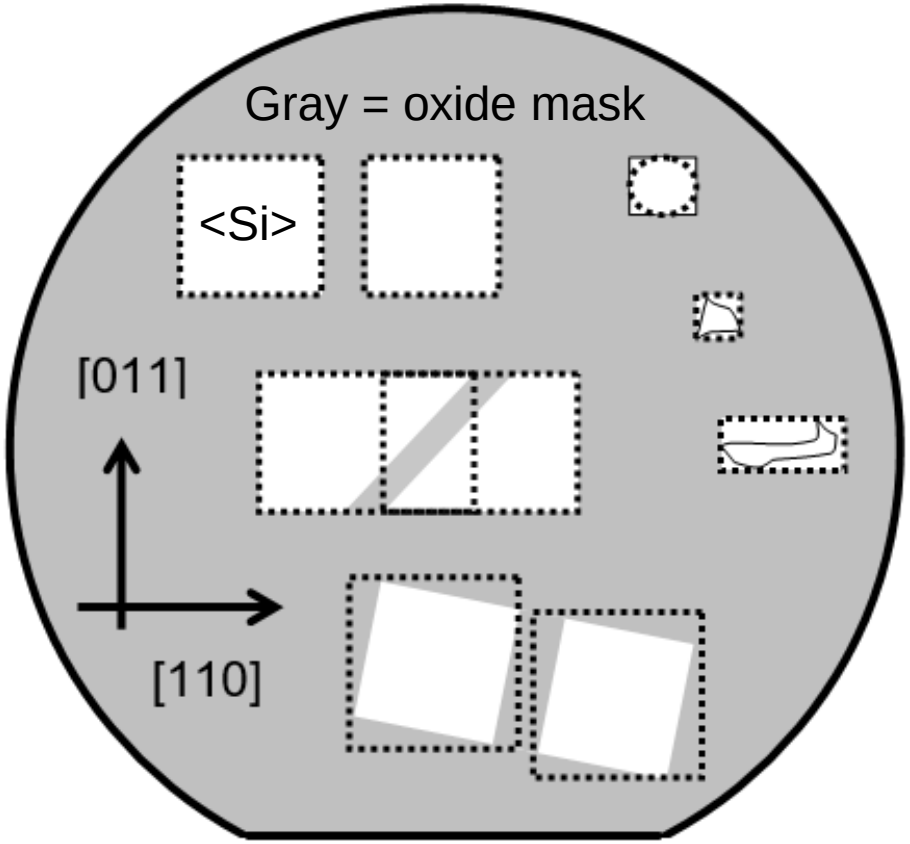


Fig. 20.9

Slow-etching <111> crystal planes define the final structures.

Irregular shapes will become rectangles, limited by <111> planes.

If structures are misaligned relative to crystal axes, ***structures will span the largest rectangle defined by the mask.***

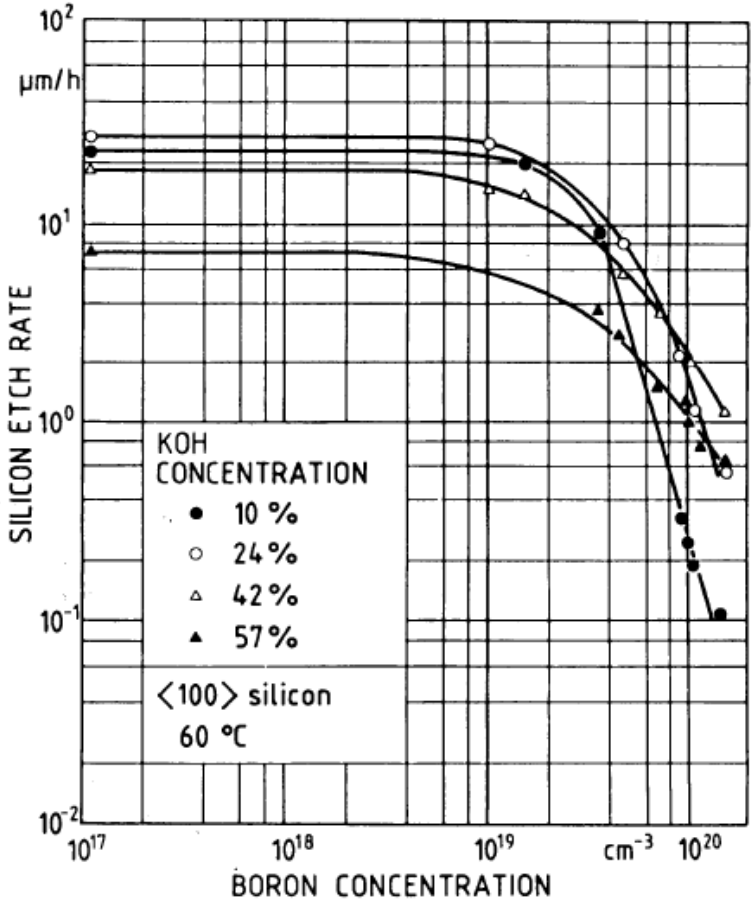
Defects of any shape will also end up as rectangles if we etch long enough.

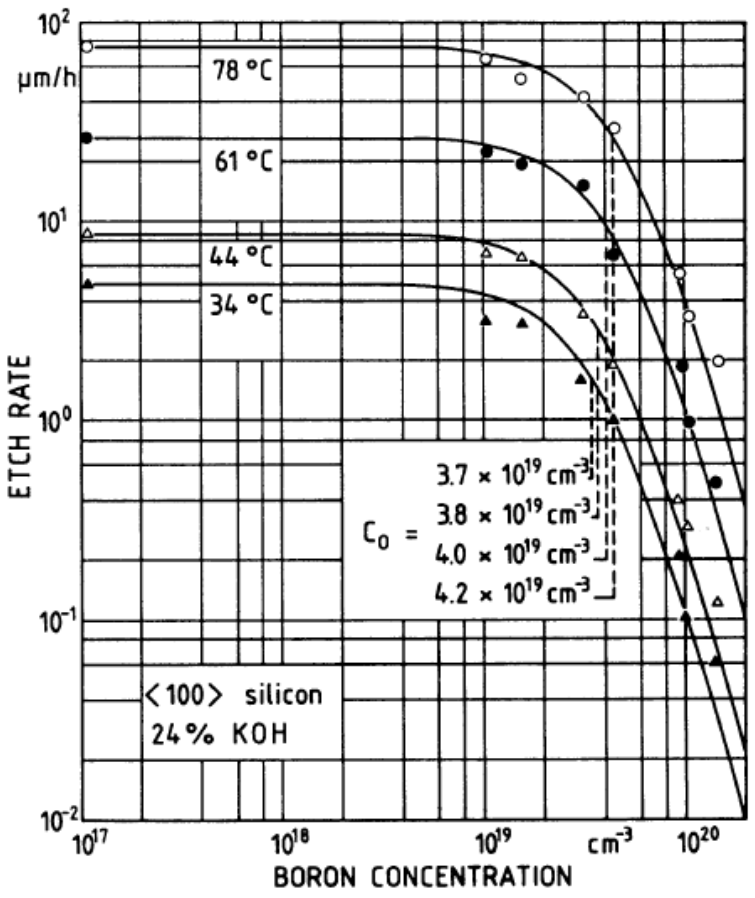
Oxide bridge can be formed by undercut etching, as shown in middle.

Alkaline anisotropic etchants: some main features

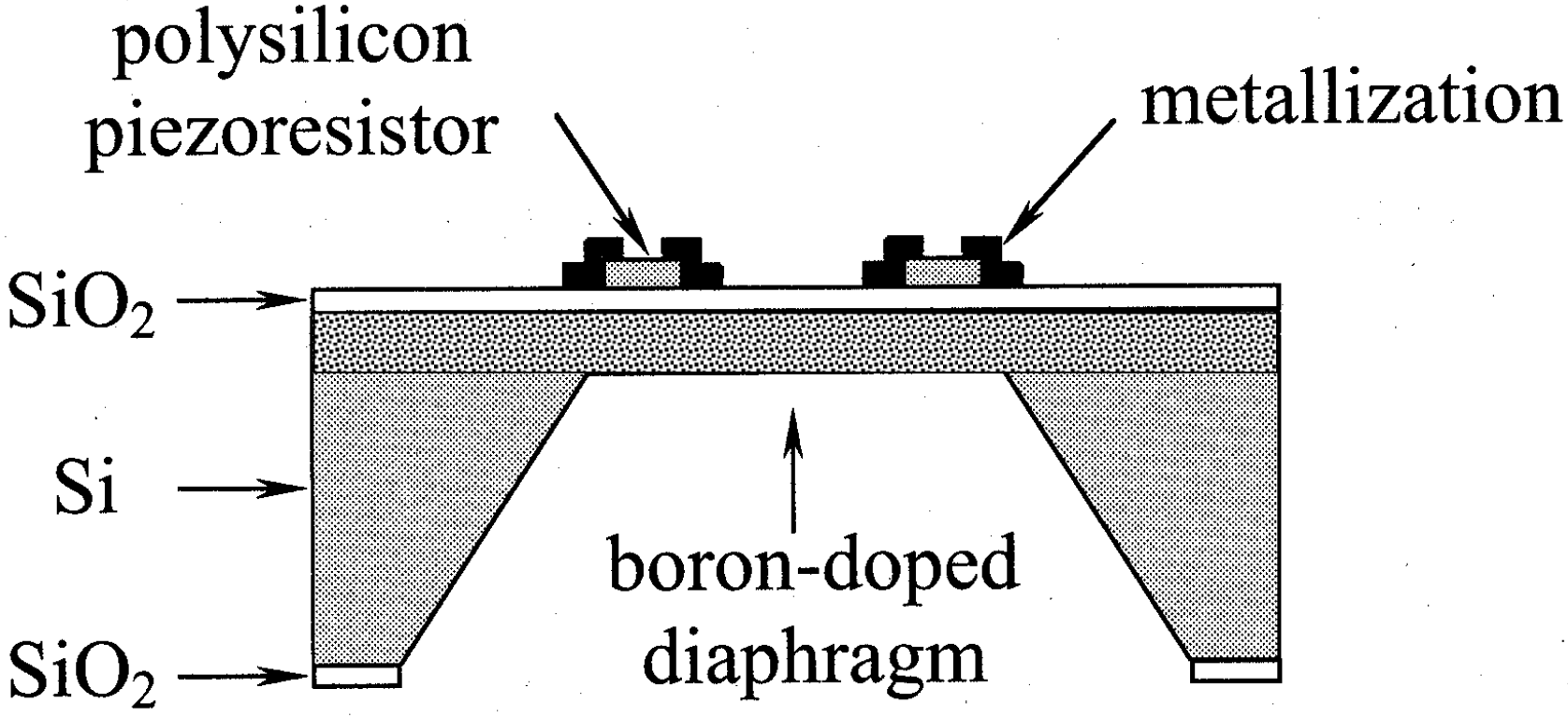
Etchant	KOH	TMAH
Concentration	40%	25%
Rate (at 80^{o}C)	1 µm/min	0.5 µm/min
Sel (100):(111)	200:1	30:1
Sel Si:SiO_2	200:1	2000:1
Sel Si:Si_3N_4	2000:1	2000:1
Etch stop factor	10	100 (see next slide)

p++ etch stop
= highly doped <Si> etch rate slow





Piezoresistive pressure sensor



Boron doped p++ membrane is a passive structure ! Active elements consist of the deposited polysilicon resistors.

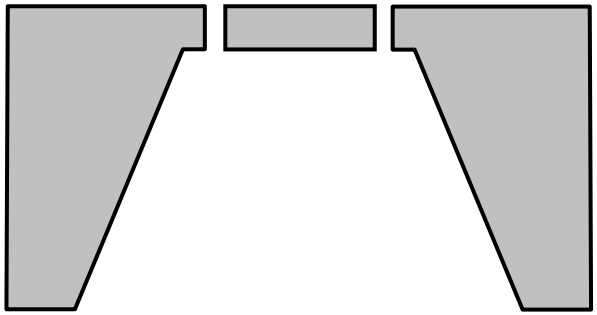
p++ etch stop limitations

- p++ doping level very high (>10^{19} cm^{-3})

➔ no electronic devices can be made on it

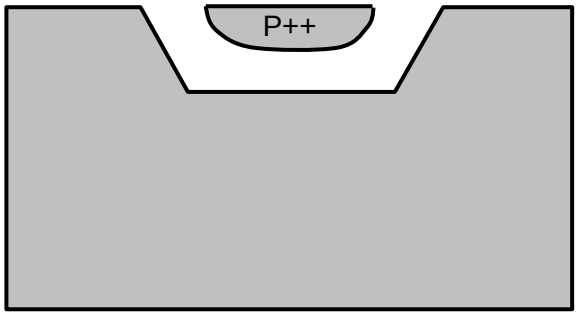
- only thin p++ can be made by diffusion
- thick epitaxy is expensive
- p++ mechanically inferior (dislocations)
- bonding to p++ material difficult (dislocations)
- best etch stop with 10^{20} cm^{-3} ; corresponds to 0.2% foreign atoms, or every 8^{th} atom in linear chain is a boron atom)

<Si> microbridges



Backside micromachining

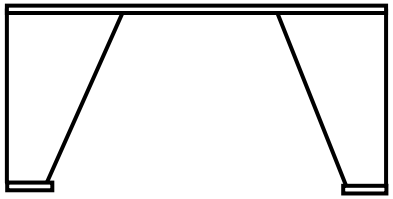
Need front-to-back alignment
Bridge thickness free variable
May use p++ etch stop
May use KOH and/or DRIE



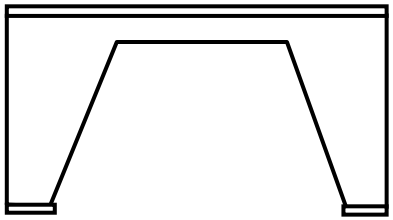
Front side micromachining

Alignment on front only
Needs p++ etch stop
Depends on p++ etch selectivity
Needs epi for thick bridge
Wider bridge ➔ depth under bridge larger

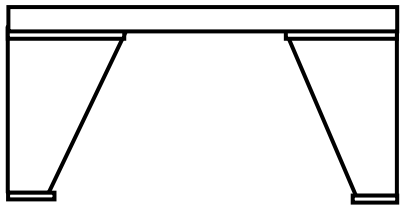
Membrane formation



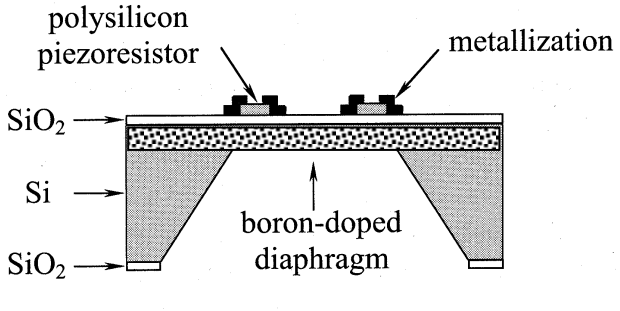
Nitride membrane; no timing needed



Timed silicon membrane; thickness depends on etch rate control and wafer thickness control.

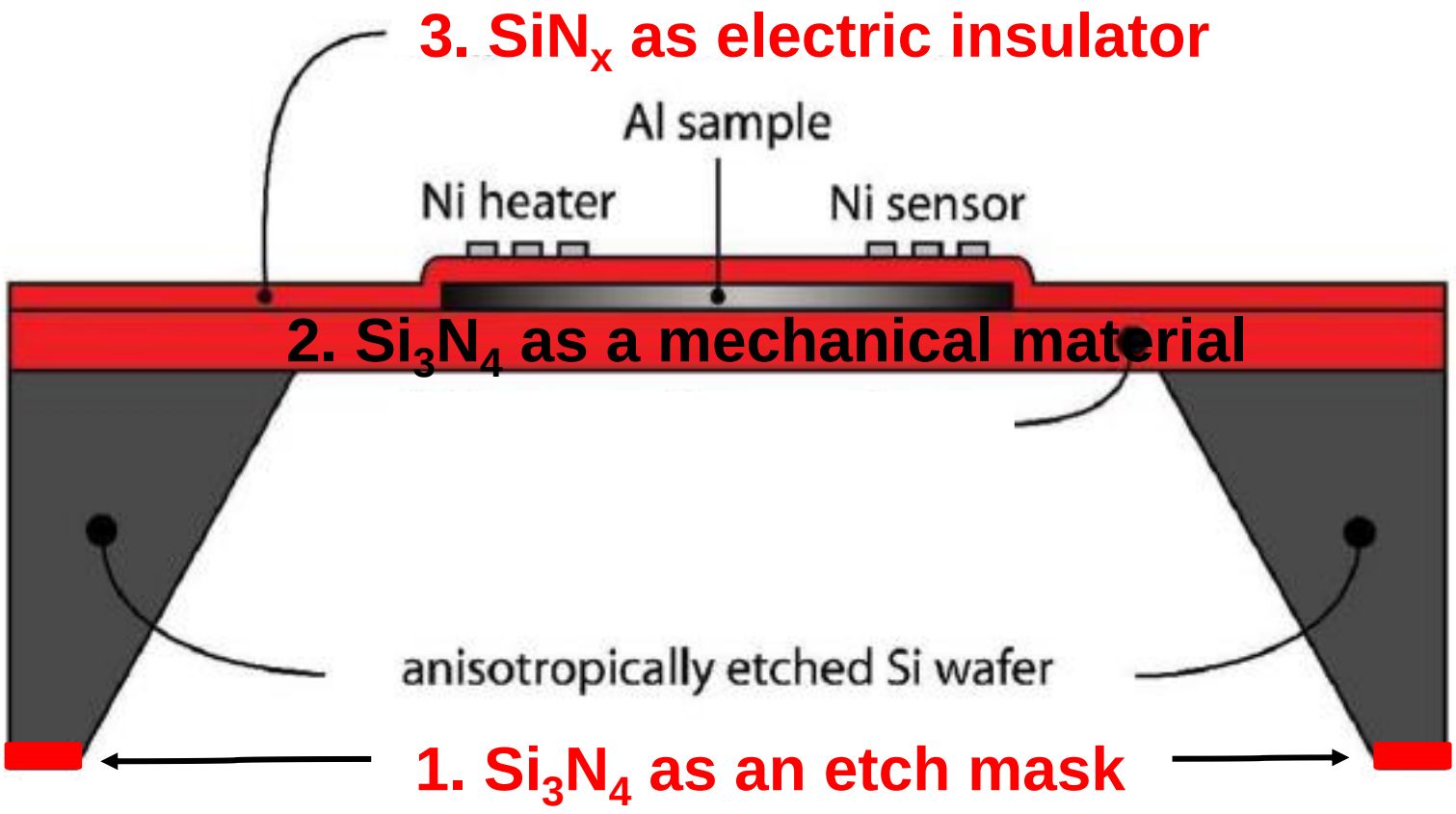


SOI wafer, membrane thickness determined by SOI device layer thickness. Excellent, but expensive.



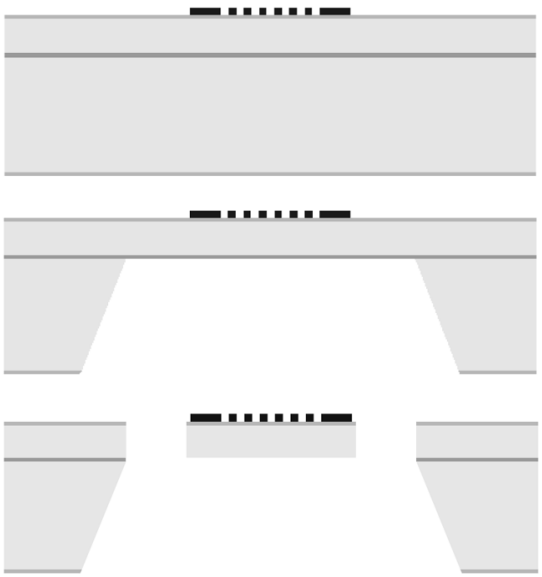
p++ membrane

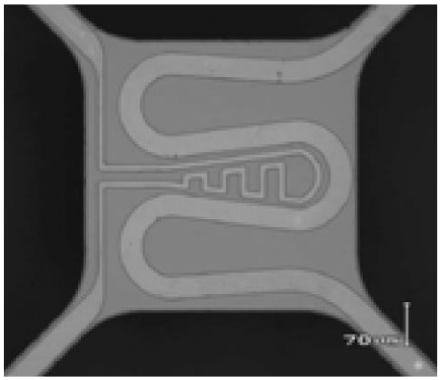
Different roles of nitride



JMEMS VOL. 16, NO. 5, OCTOBER 2007, p.1269

SOI heat spreader hot plate





SOI-substrate: 380µm handle silicon, 1µm SiO_2 and 15µm device silicon.

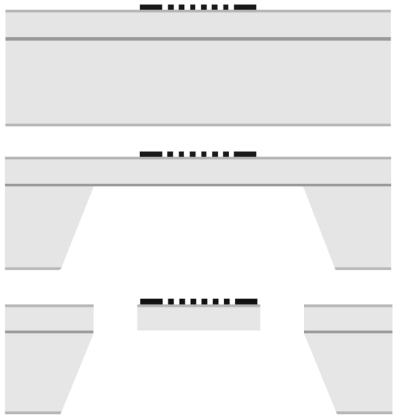
Both side deposited with a SiN layer. Pt-heater and Pt-T-sensor elements on the top side.

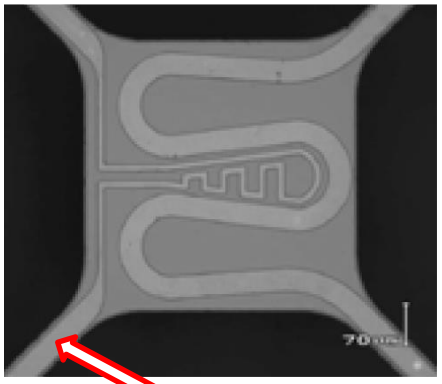
Bottom side KOH-etch.

Top side structuring of the suspension bars: litho & DRIE.

Hildenbrand et al: IEEE SENSORS JOURNAL, VOL. 10, NO. 2, FEBRUARY 2010 353

SOI hot plate process





1. SOI wafer (backside always polished)
2. LPCVD nitride @850^{o}C, both sides
3. Lithography of heater
4. Ti/Pt (20 nm/200 nm) by evaporation
5. Lift-off (Why not sputter-litho-etch ?)
6. Litho on backside
7. Plasma etch nitride (why not wet etch ?)+strip
8. Protect front side (jig or wax)
9. Silicon handle wafer etch by KOH (backside)
10. Litho on front side (suspension bars)
11. DRIE of nitride and SOI device silicon (can they be etched in the same step ?)
12. Strip resist
13. Etch buried oxide in HF

Are the suspension bars nitride/silicon/oxide stacks, or simply nitride bars ?

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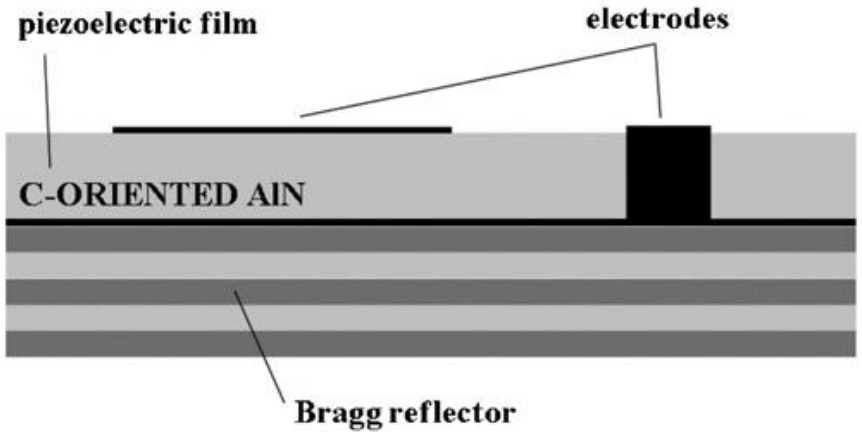
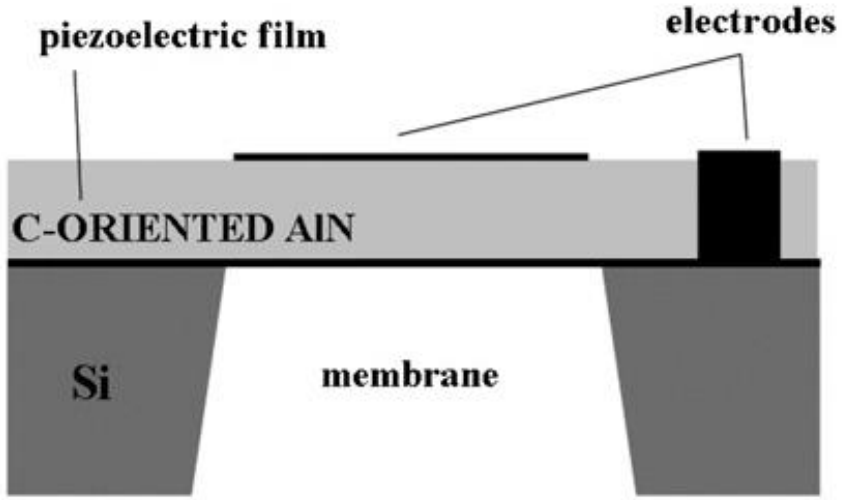
AlN as active material & membrane



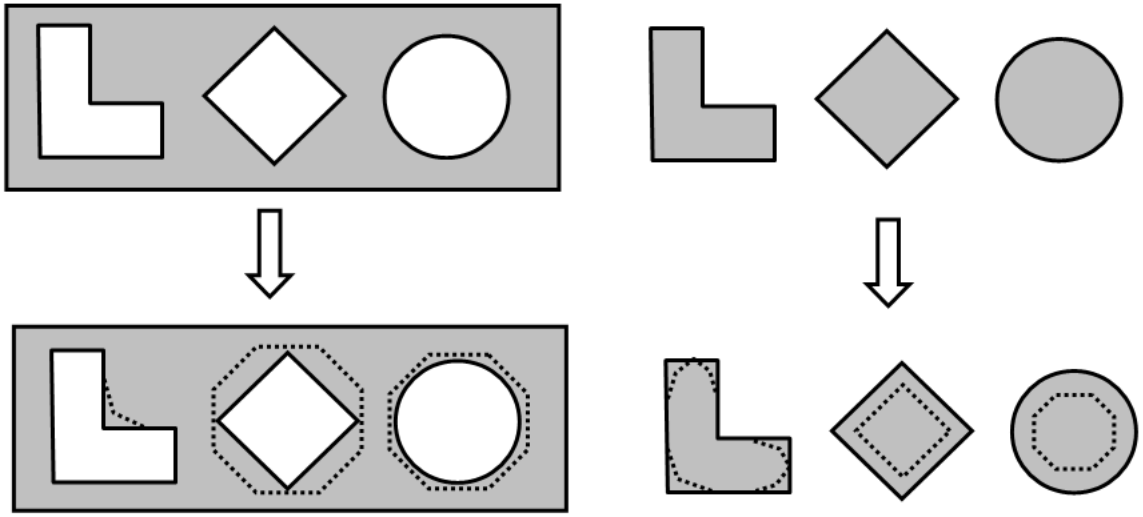
AlN as piezoelectric material
(grain orientation important)



Additionally, AlN as mechanical material
(stress control important)

D M Martin, V Yantchev and I Katardjiev, 2006

Mask polarity effects



Gray =
oxide mask

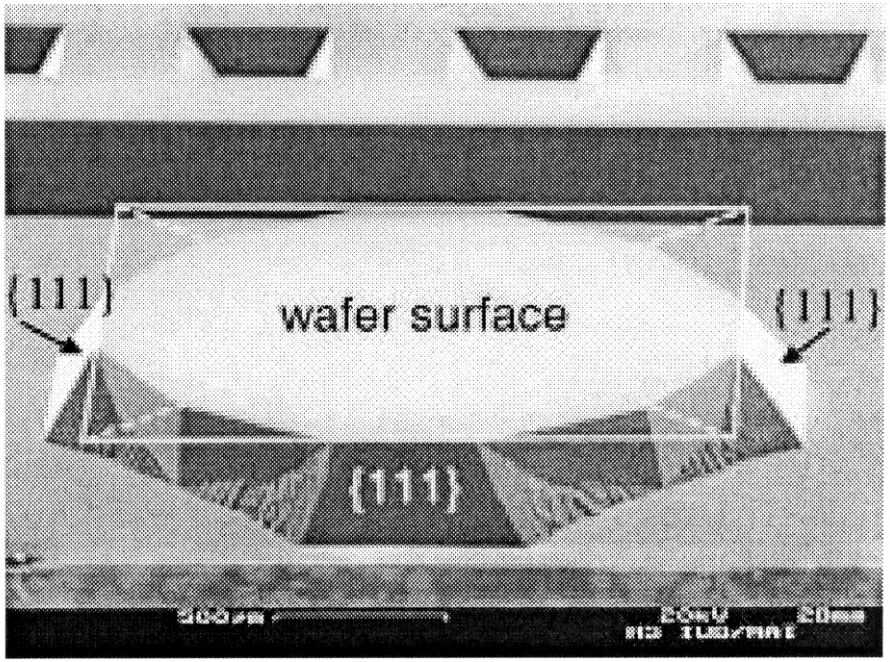
White =
open silicon

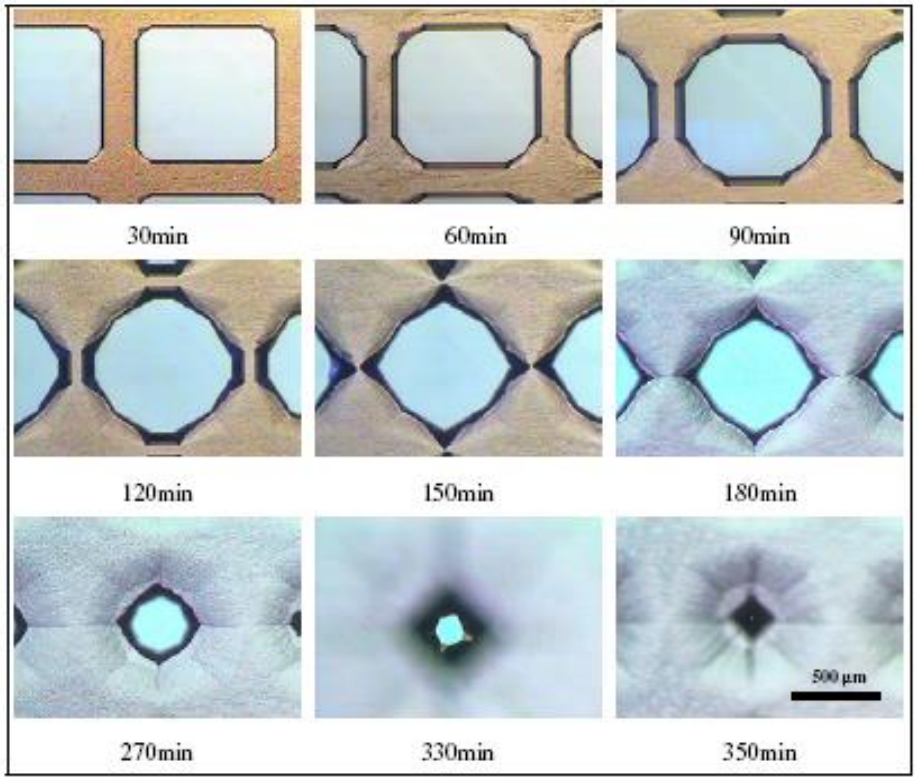
Openings in oxide will etch differently from oxide patches.

Oxide patches will result in mesas or peaks if etching continues long enough.

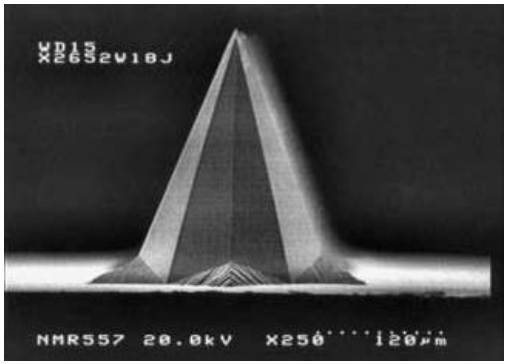
Fig. 20.11

Etching mesas and pyramids



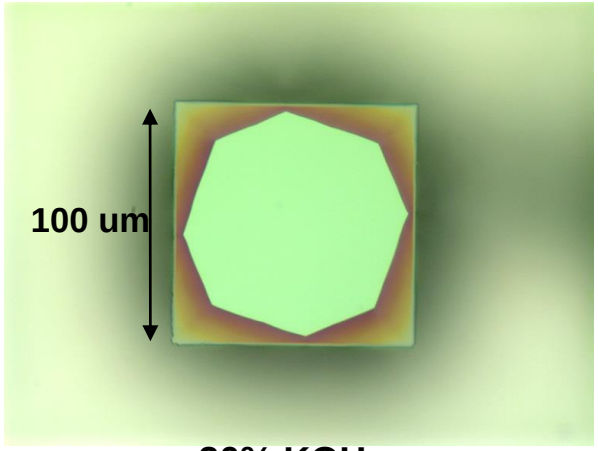


Mask undercut will lead eventually to a pyramid



H.Schröder, E. Obermeier, A. Horn, G. Wachutka, Convex Corner Undercutting of {100} Silicon in Anisotropic KOH Etching, J. Microelectromechanical Systems, v. 10 (1) March 2001, p.88

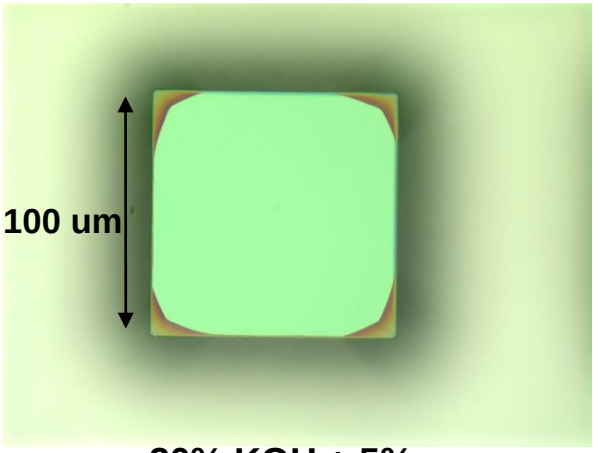
Undercutting depends on exact etch chemistry and conditions



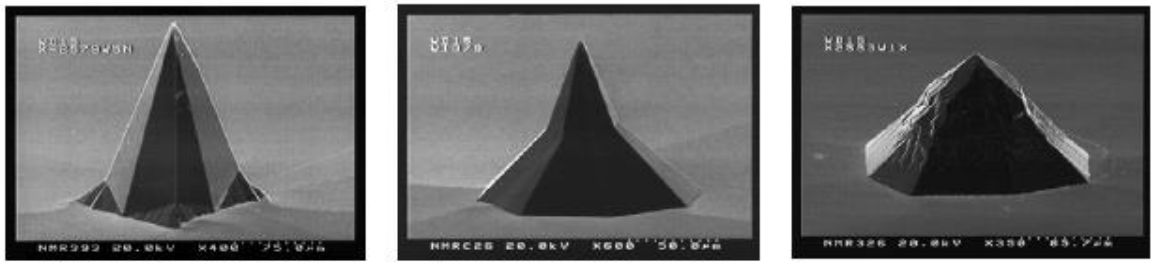
20% KOH

Adding IPA (isopropyl alcohol) to KOH reduces the underetch, and changes crystal plane selectivity.

Kestas Grigoras,
Aalto University



20% KOH + 5% IPA

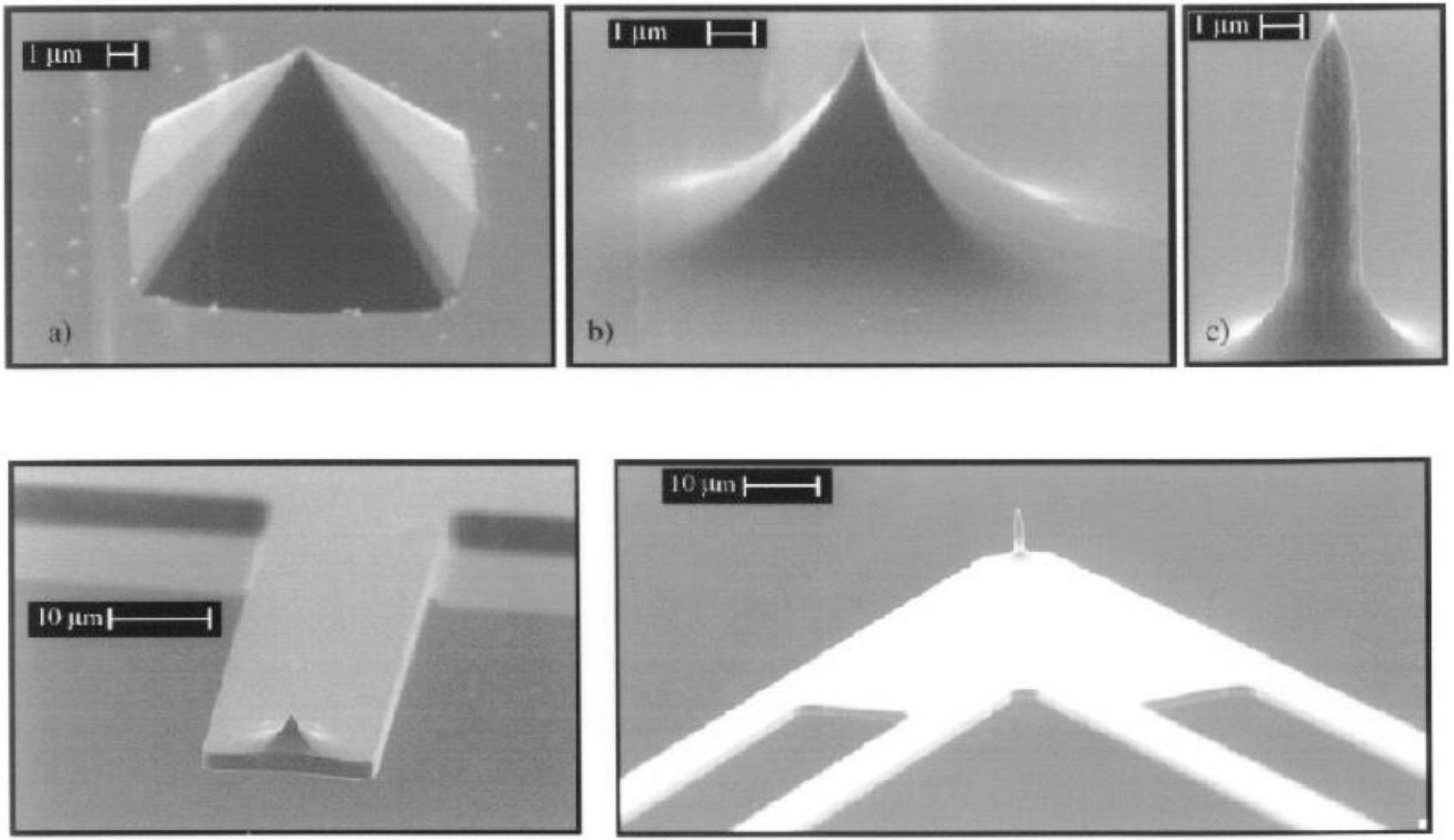


(a) (b) (c)

Figure 13. Influence of bath age: (*a*) fresh bath, (*b*) bath about 15 h used, (*c*) bath over 40 h used.

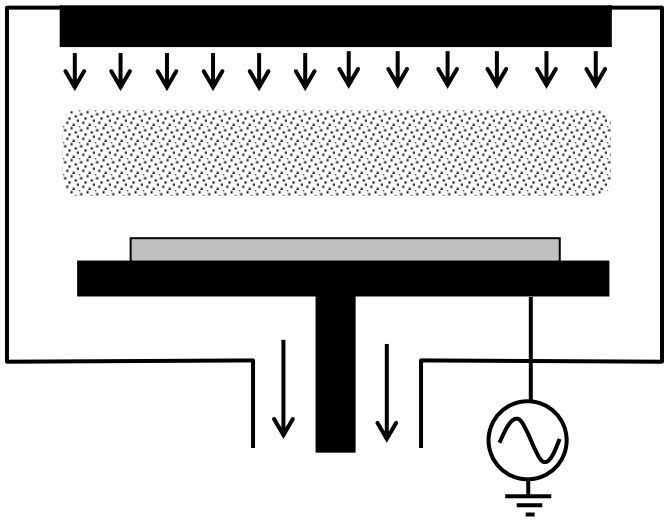
N Wilke *et al* J. Micromech. Microeng. **16** (2006) 808–814

AFM tips and cantilevers



A Boisen *et al* J. Micromech. Microeng. **6** (1996) 58–62.

Plasma/RIE



vacuum 1 mTorr -3 Torr

13.56 MHz RF

gas flow rates 10-1000 sccm

Reactions:

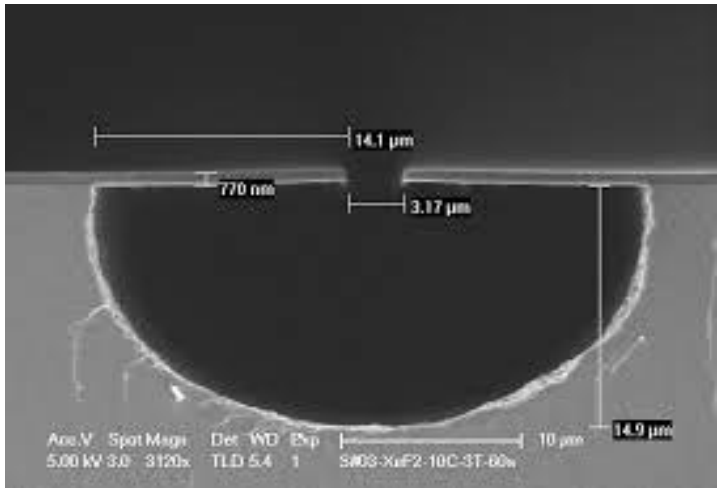
Ionization	e- + Ar ==> Ar+ + 2 e-
Excitation	e- + O_2 ==> O_2* + e-
Dissociation	e- + SF_6 ==> e- + SF_5* + F*

Note 1: RIE is synonym for plasma etching
Note 2: ions have minor role; excited neutrals major

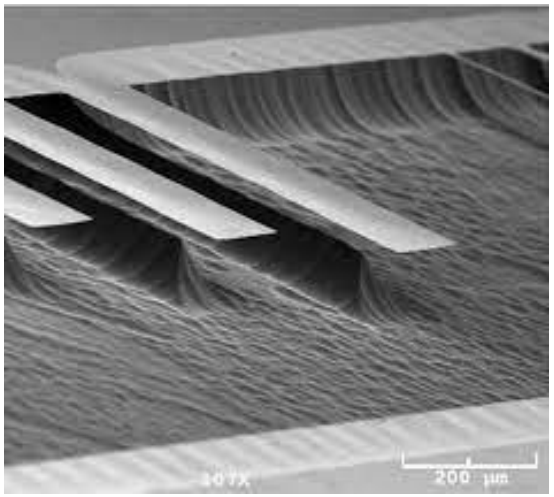
Dry etch

$2\ XeF_2\ (g) + Si\ (s) \rightarrow 2\ Xe\ (g) + SiF_4\ (g)$

This is dry etch (=uses gases, not liquids), but it is NOT plasma etch. No ion bombardment ➔ no directionality.

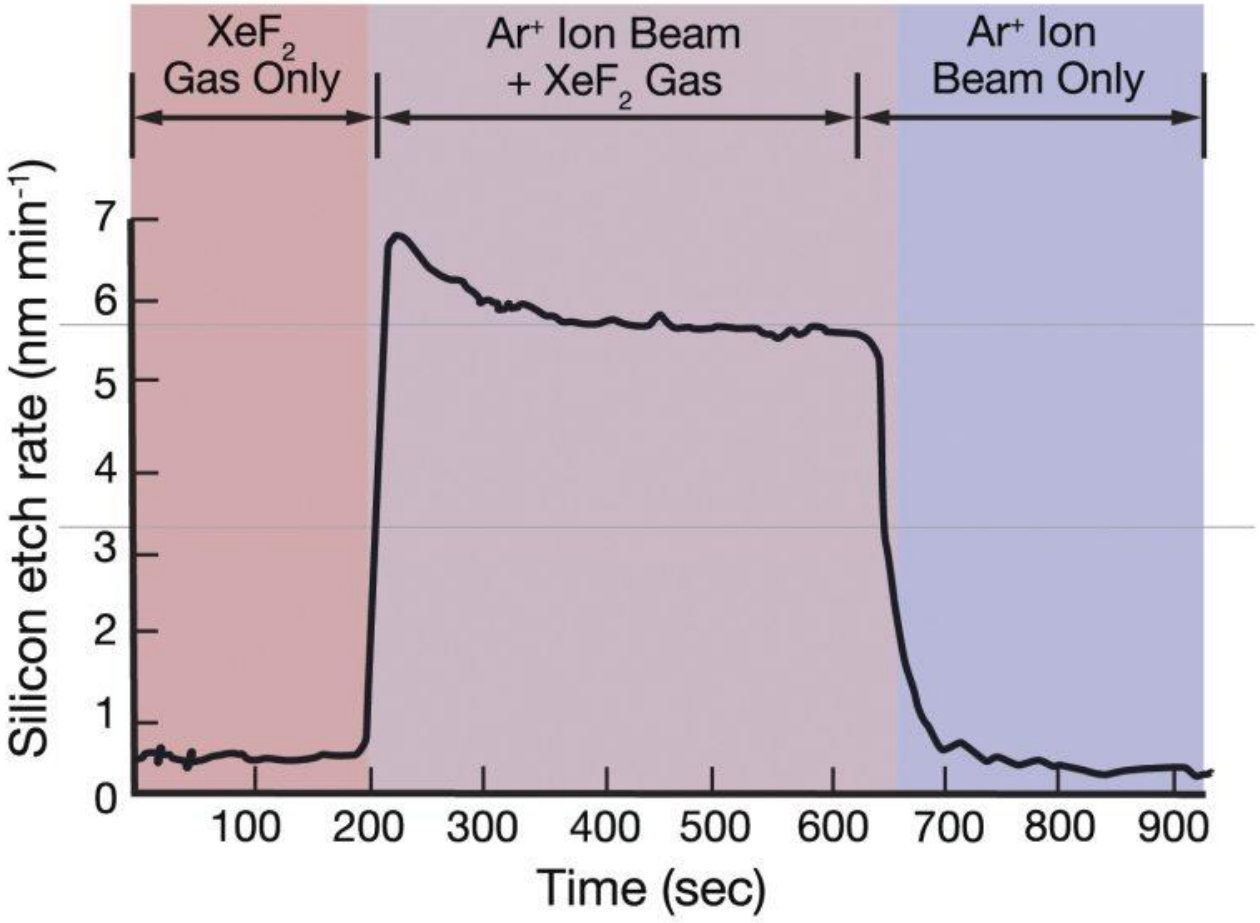


UCSB nanofab wiki



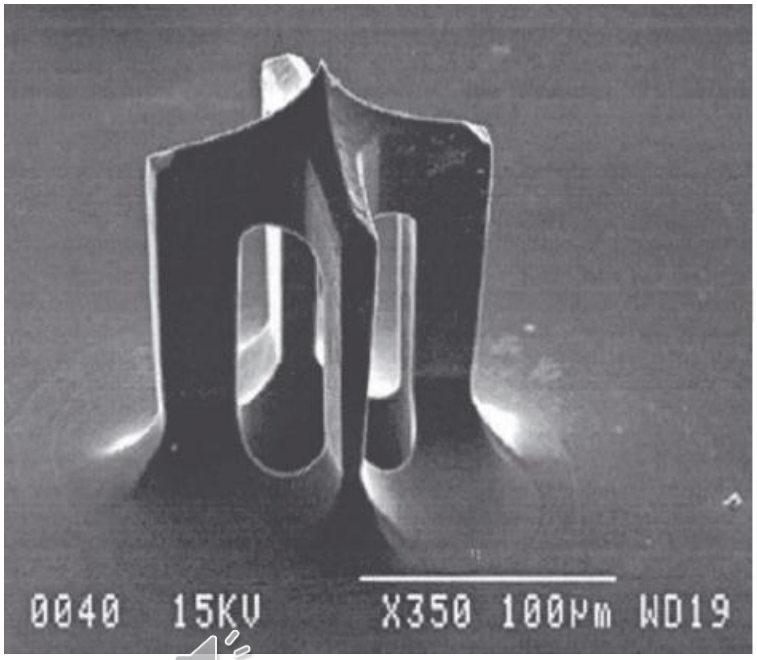
Orbotech

Plasma etch = physical+chemical

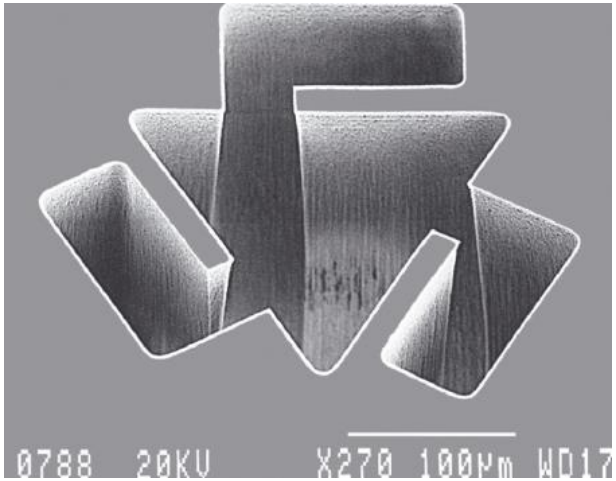


Coburn & Winters, JVST 1981

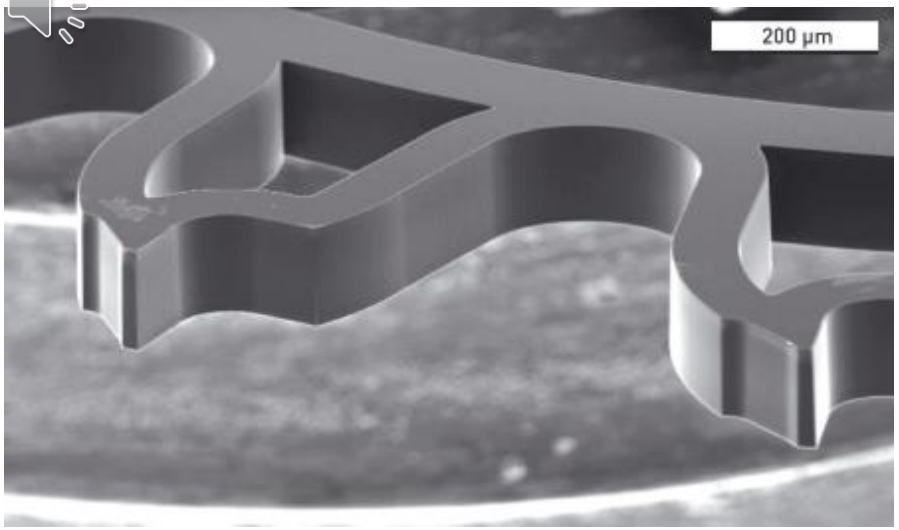
DRIE of silicon



Microfluidic needle for epidermal injection of drugs

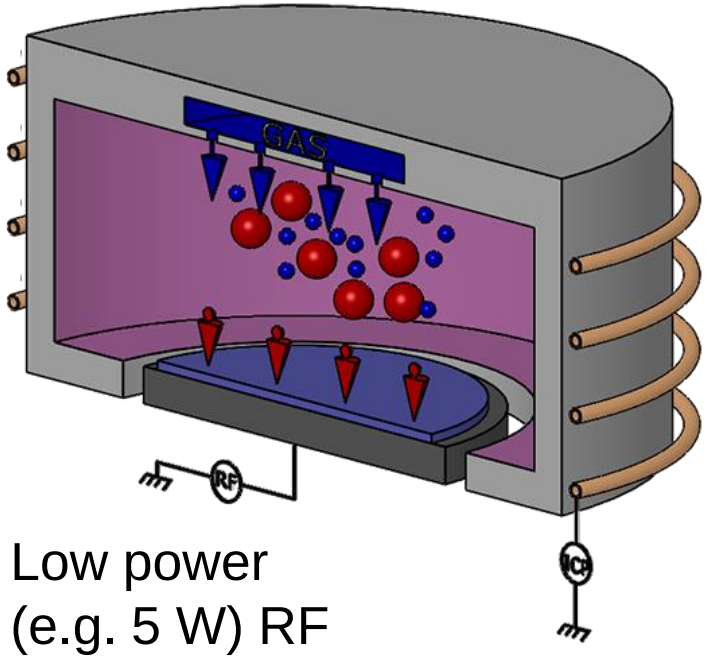


Optical fiber alignment fixture



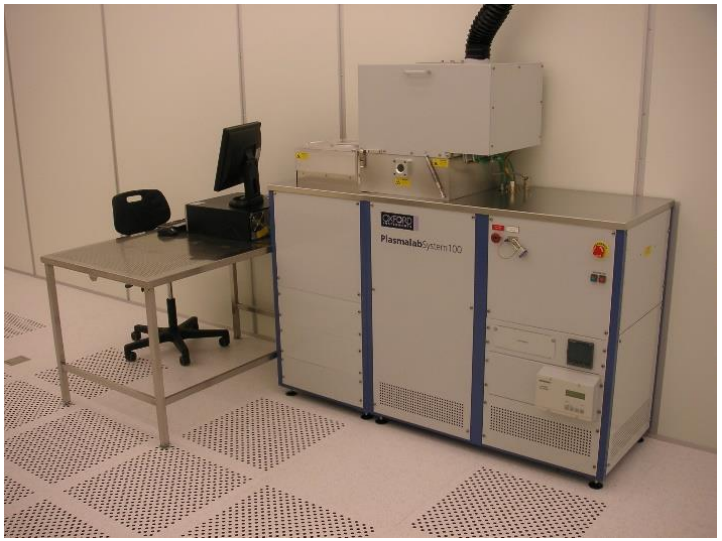
Mechanical spring for a (very expensive) watch

High density plasma (HDP)



Low power (e.g. 5 W) RF source to accelerate ions towards the wafer

High power inductive coil source (Inductive Coupled Plasma, ICP) of e.g. 2 kW generates intense plasma and excites molecules



Oxford ICP DRIE at Aalto

https://www.corial.com/en/technologies/icp-rie-inductively-coupled-plasma-reactive-ion-etching/

High density plasma (2)

- Two RF power sources do different things:
- ICP: plasma generation (high radical density)
- CCP: ion acceleration (tunable ion energy)

➔ radical concentration and energy decoupled
➔ high rate because high radical concentration
➔ high selectivity when low ion energy chosen

- Gas atoms at 20 mTorr pressure: 10^{15} cm^{-3}
- RIE: 10^{10} cm^{-3} ions (= 0.001 % ionized)
- HDP: 10^{11}-10^{13} cm^{-3} ions (=0.01% -1% ionized)

DRIE micromachining

- RIE = Reactive Ion Etching
- DRIE= Deep RIE
- but really HIGH RATE matters

- 1 µm/min OK for RIE in IC fabrication
- 10 µm/min needed for MEMS

because deeper structures are etched

(if 380 µm thick wafer ➔ 38 min for thru-wafer etching, still very slow !)

Bosch DRIE process

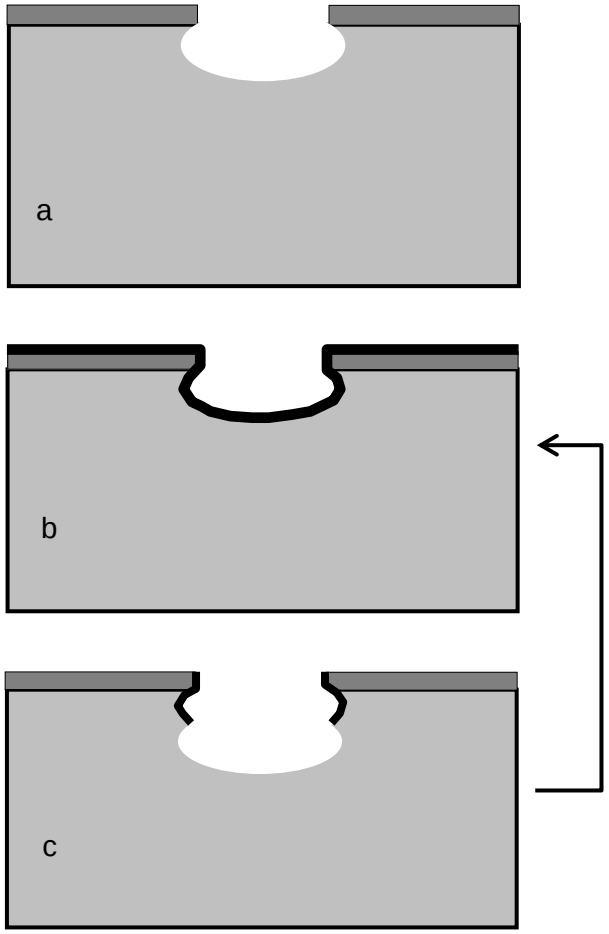


Fig. 21.8

Etch pulse of SF_6

Passivation pulse of C_4F_8

Etch pulse of SF_6: remove CF-polymer from bottom, then etch silicon

Sidewall is vertical,
but undulating (scalloping)

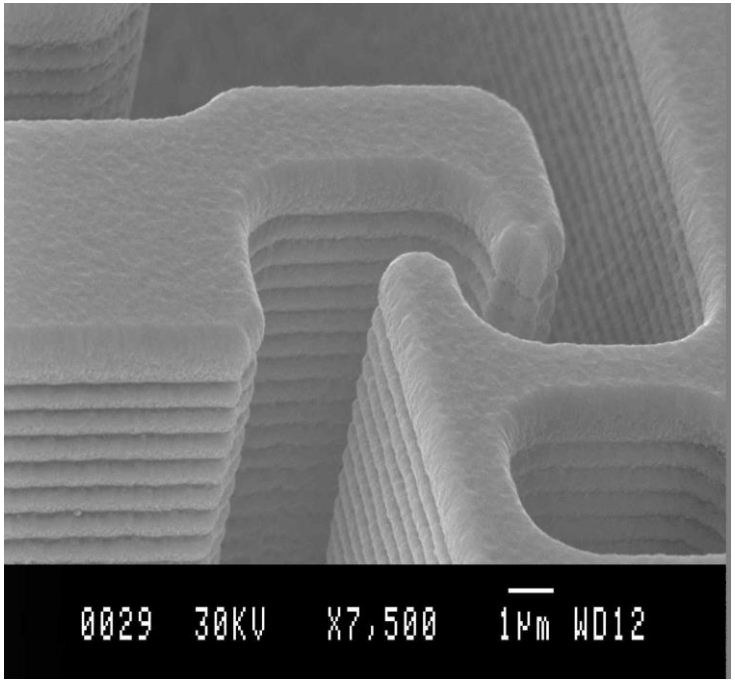
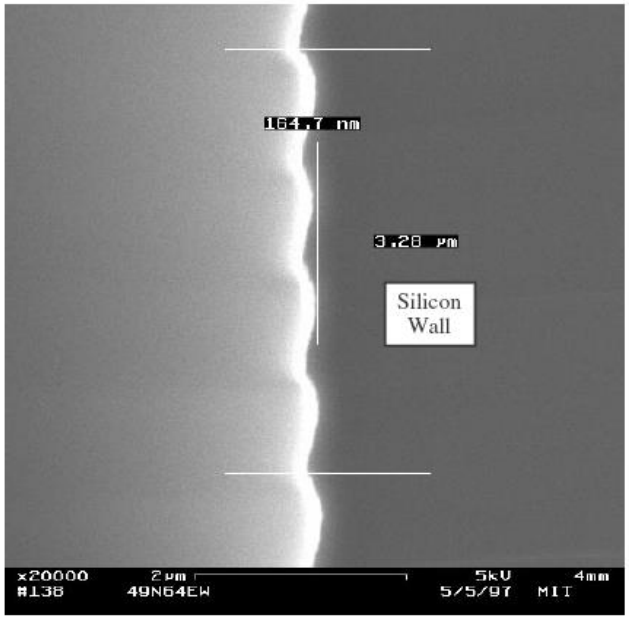


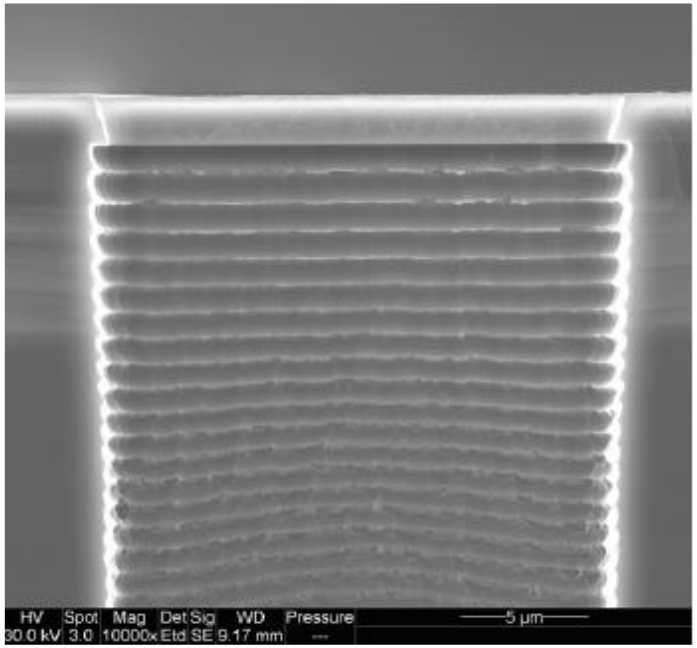
Fig. 21.9

Bosch-process (2): scallops

Because of the pulsed operation, sidewalls have undulation; a.k.a. scallops. If rate is 5 µm/min, and pulse lengths 13 s+ 5 s ➔ ca. 1.5 µm periodicity.

If perfectly smooth walls are needed, Bosch-process is not the right one. Cryo-process is better. Vertical walls are obtained in both.



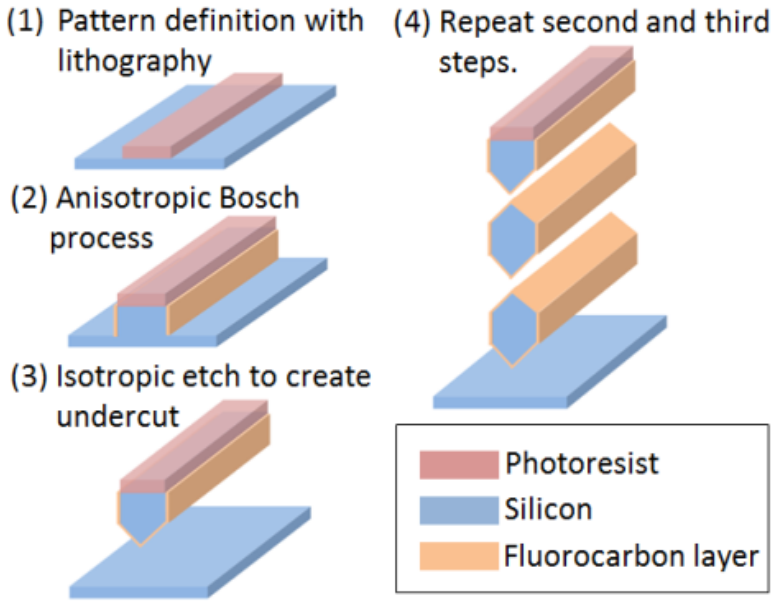


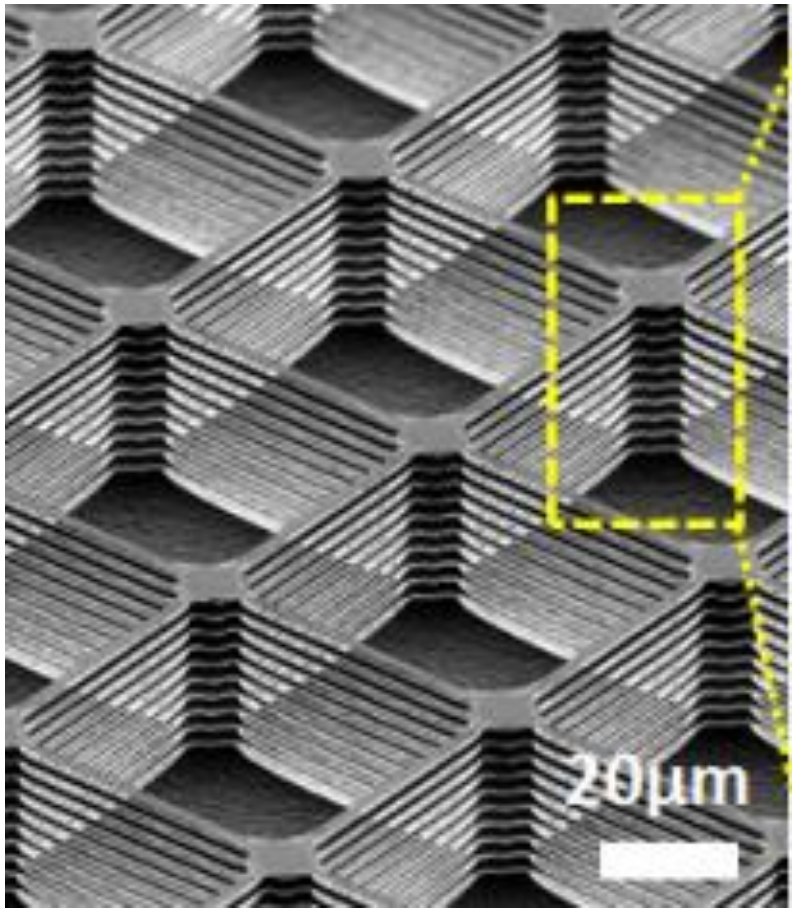
A A Ayón *et al* Smart Mater. Struct. **10** (2001) 1135–1144

J. Micromech. Microeng. **16** (2006) S29–S34

Bosch overdone

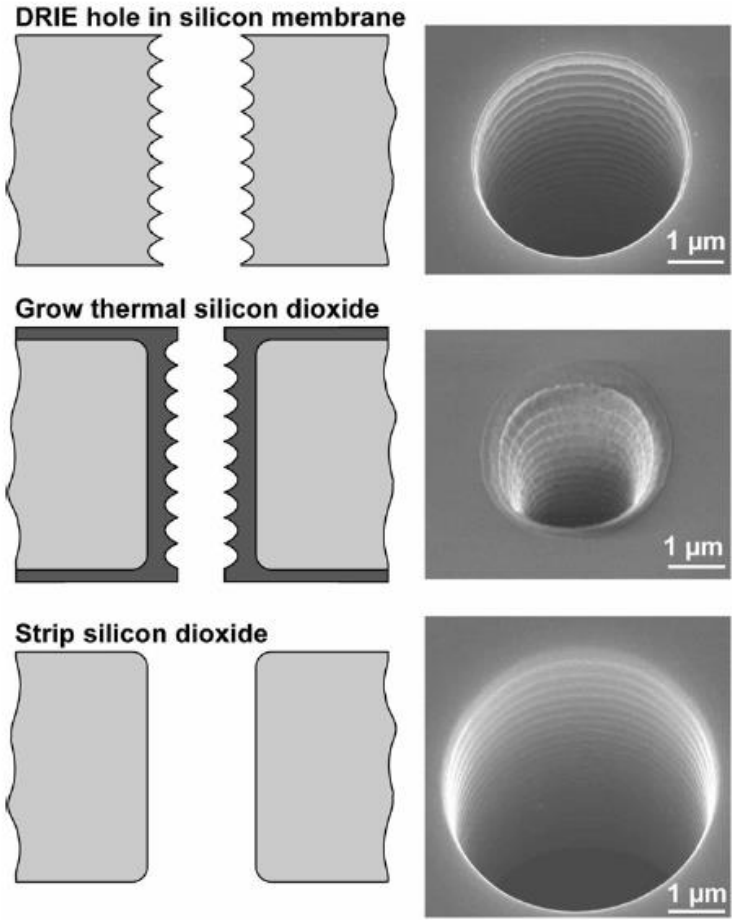
There is undercut in Bosch SF_6 etch step, and it can undercut and release structures, like other isotropic etch steps.



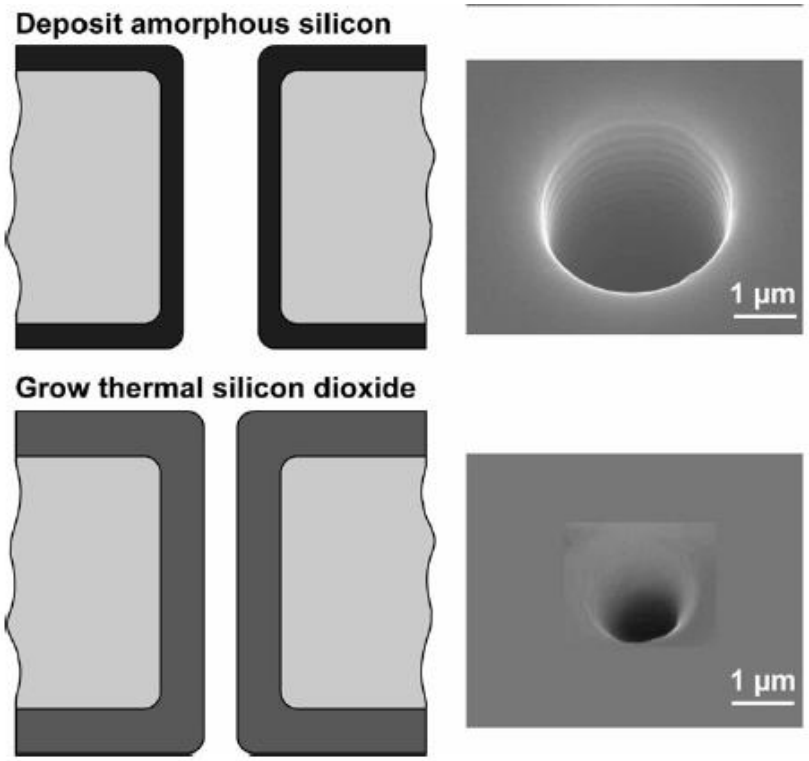


Chang: J. Micromech. Microeng. 28 (2018) 105012 (10pp)

Scallop/undulation reduction

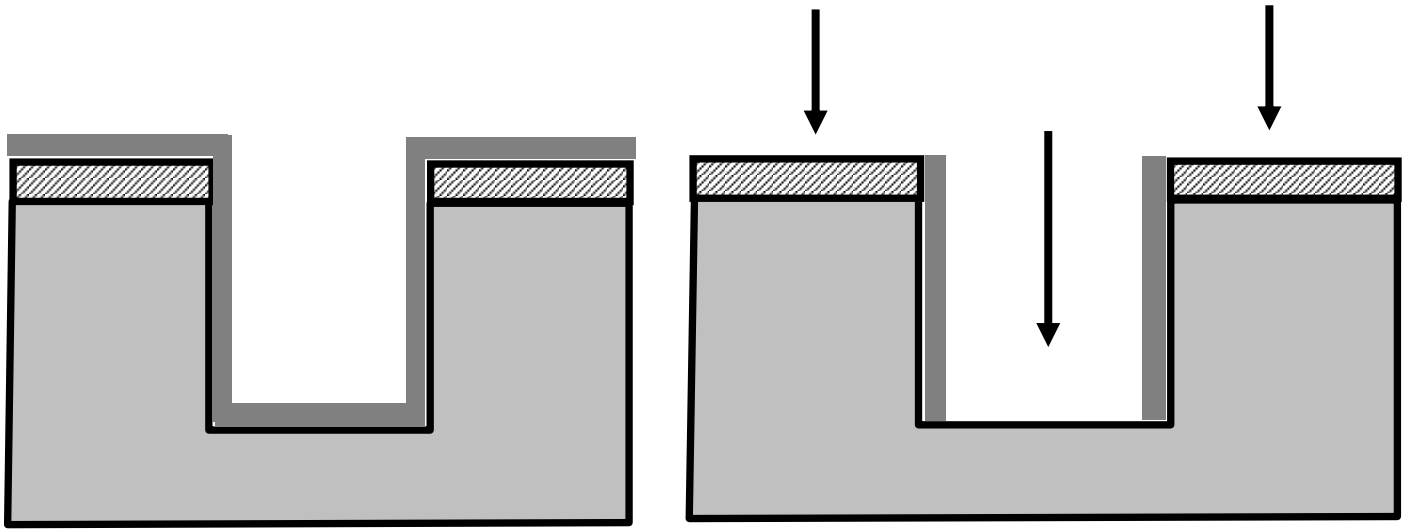


1. Thermal oxidation
2. Etching of oxide in HF
3. Deposition of a-Si
4. 2nd oxidation



Matthews & Judy, J.MEMS 15 2006, p.214

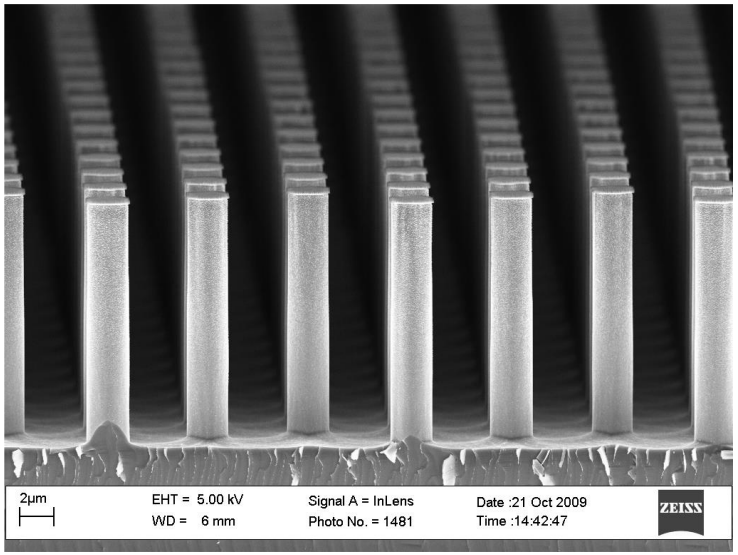
Cryogenic DRIE: SF_6+O_2 @ -120°C



A sideproduct from etching is SiO_xF_y (main product is SiF_4 gas)
SiO_xF_y is non-volatile at -120°C.
It condenses on the walls.
Ion bombardment removes it from “floor”, and etching can continue downwards.
Sidewalls are not etched because the SiO_xF_y protects them.

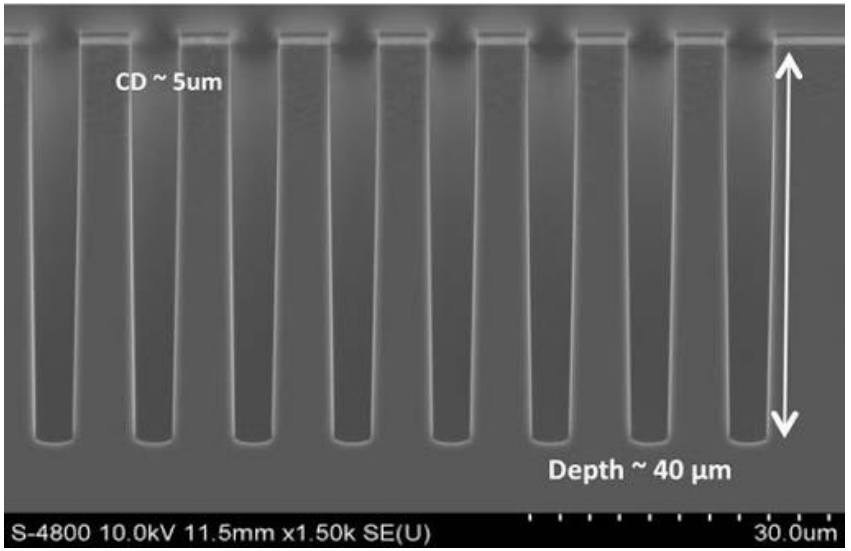
DRIE enables high aspect ratios

pillars



Lauri Sainiemi, Aalto University

trenches



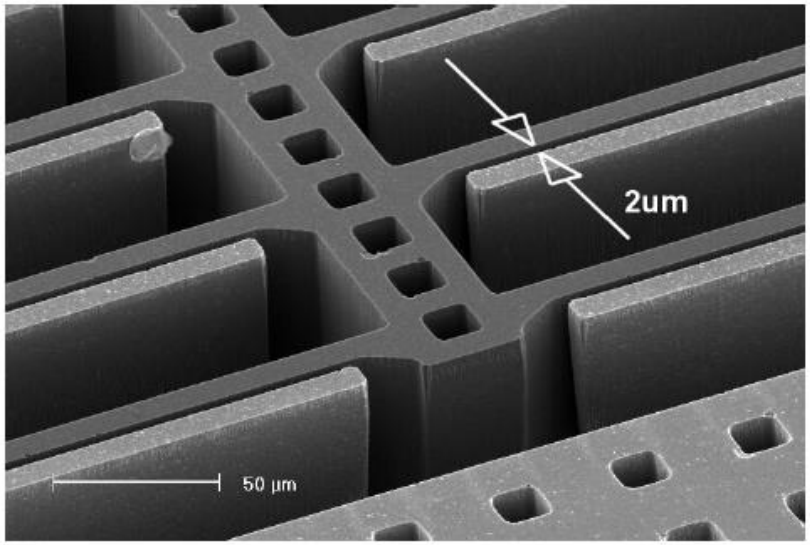
http://www.appliedmaterials.com/nanochip/nanochip-fab-solutions/december-2013/power-struggle

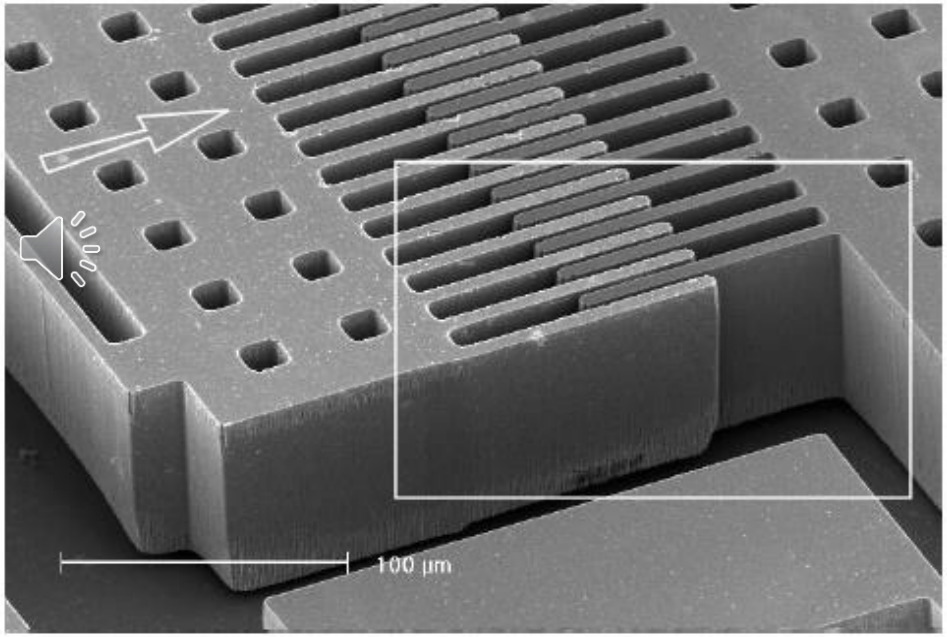
Aspect ratio: height:width

- 10:1 routine
- 20:1 optimized
- 40:1 in demos only
- 80:1 world record

Easier to etch trenches than pillars because etchable area is small, maybe 1-10%; while in pillar etching maybe 75-95% of silicon is etched (much more etch gas needed, which is difficult in low pressure).

DRIE enables closely spaced structures





Air gap capacitors, useful as sensors and actuators.

C Acar and A M Shkel J. Micromech. Microeng. **15** (2005) 1092–1101

Vertical DRIE mirrors

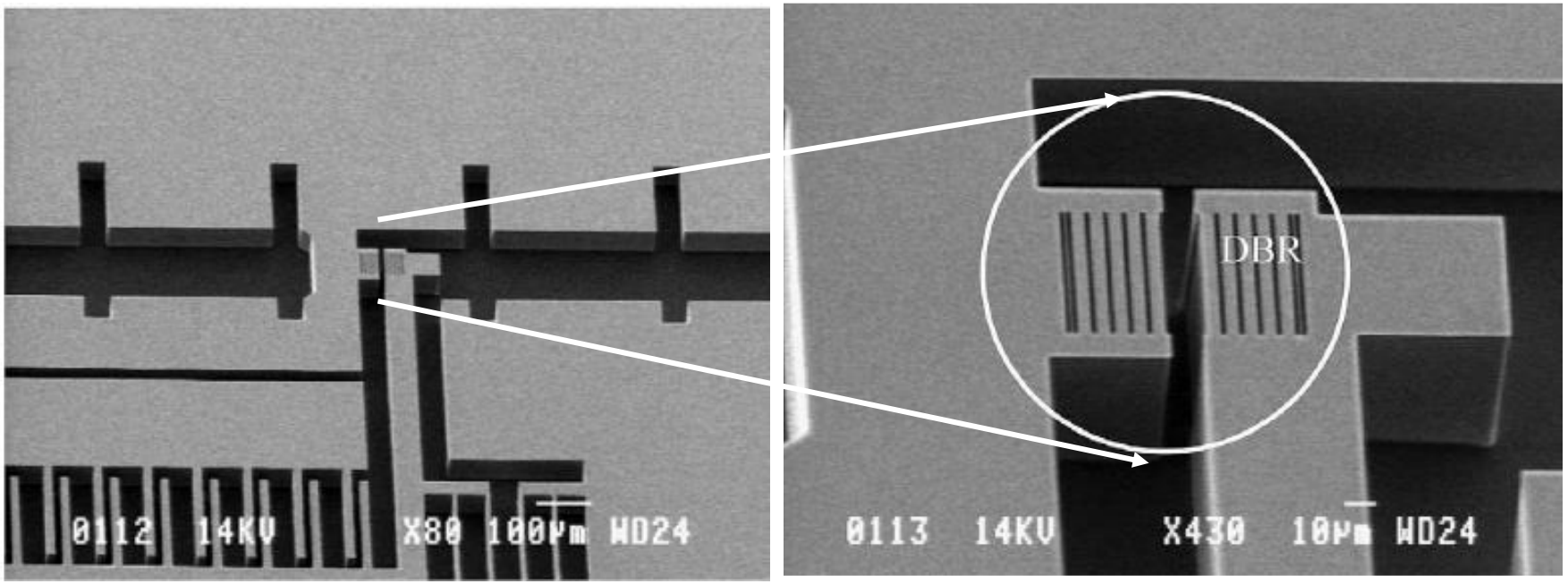
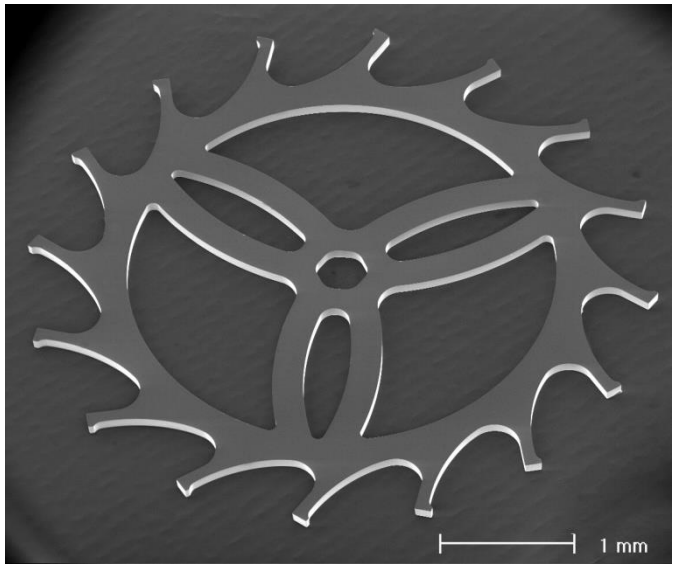


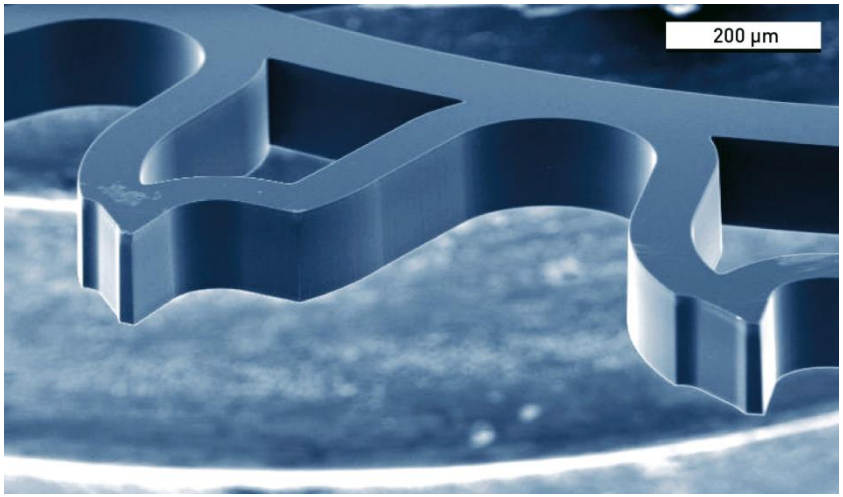
Fig. 3. (a) Tunable optical filter consisting of two freestanding vertical DBR mirrors. The air gap distance between the two mirrors is controllable using integrated electrostatic actuators. DRIE performed on SOI wafer. Detailed view.

Cryo-DRIE better than Bosch in this application.

F. Marty et al. / Microelectronics Journal 36 (2005) 673–677

DRIE strengths





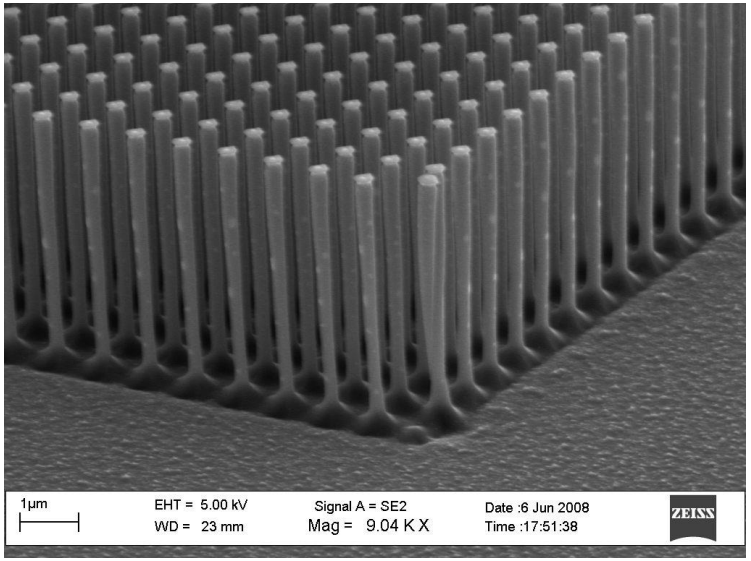
Courtesy CSEM

Any shape

Any size

Any crystal orientation

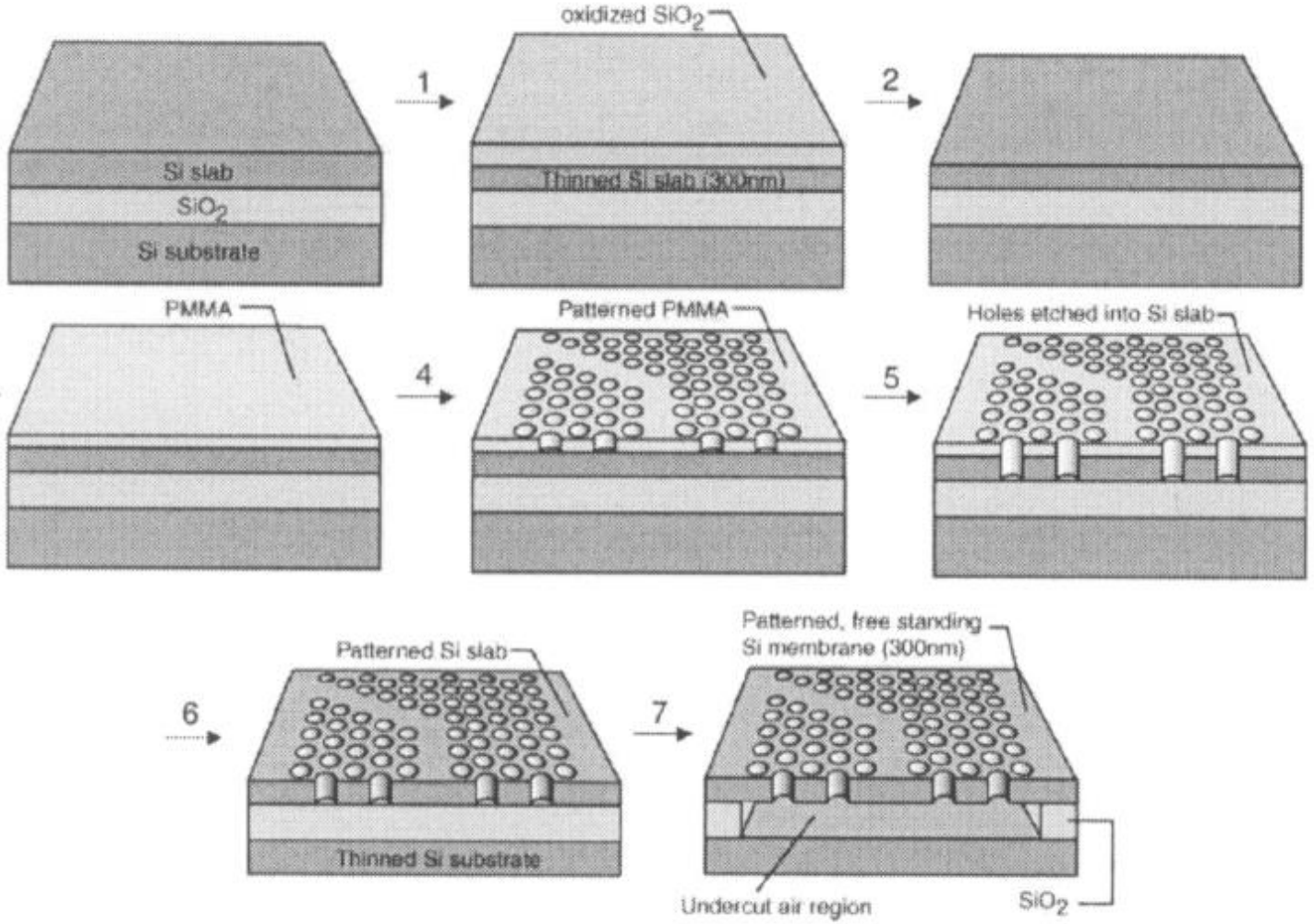
High aspect ratio



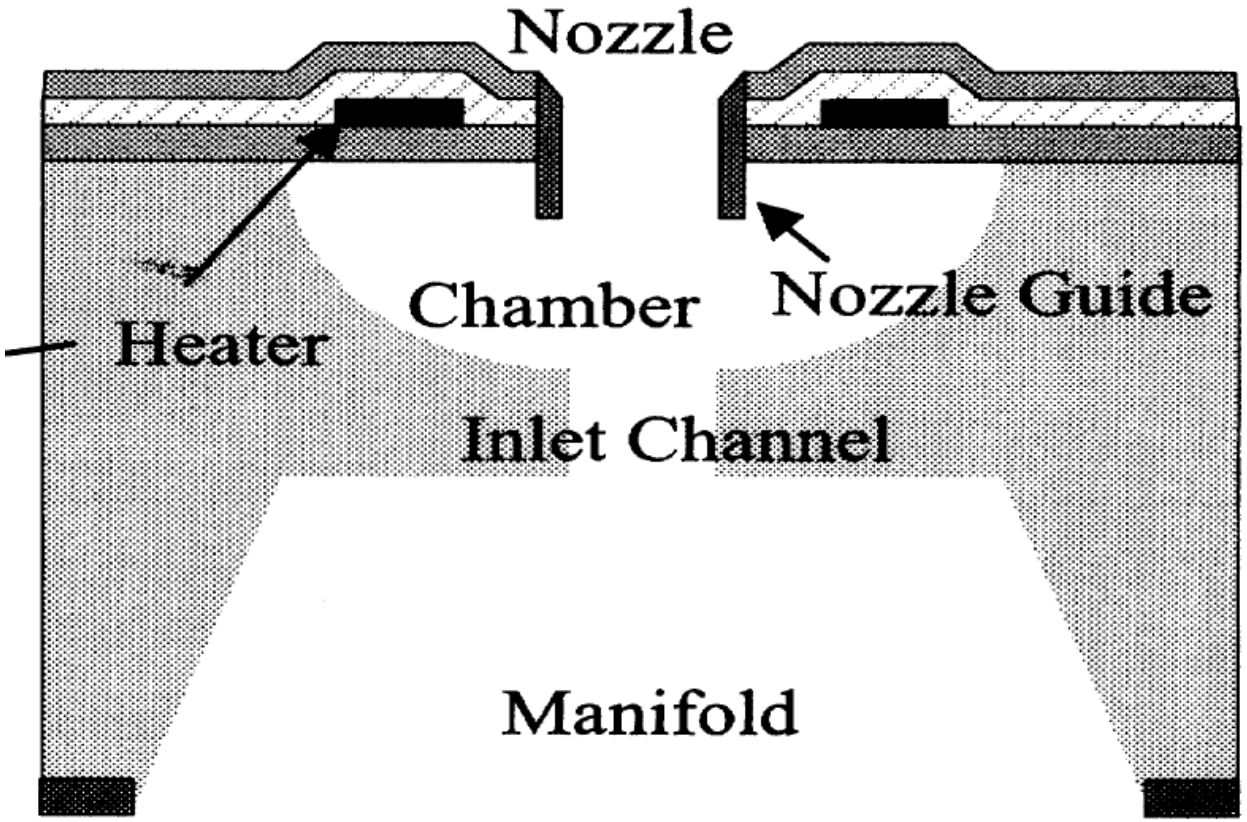
Nikolai Tsekurov, Aalto University

Photonic crystal on SOI: anisotropic + isotropic etching

PMMA is resist



RIE + isotropic+ anisotropic wet: ink jet nozzle: roof shooter



Shin, S.J. et al: Firing frequency improvement of back shooting inkjet printhead by thermal management, Transducers ’03, p. 380

MEMS continues

We will continue next week with bulk & SOI MEMS, where (thru-wafer) silicon etching is essential.

After that, we will discuss surface-MEMS, where etching of thin films is the key technology, and the starting wafer is not necessarily etched at all.