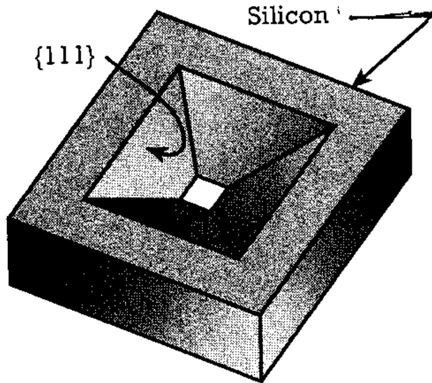
Spot 3
Etching for MEMS: solutions

Through-wafer square nozzle



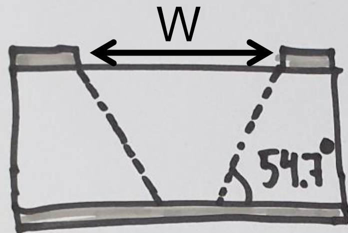
The red triangles depict dicing saw that will be used to detach the chips from each other.

Design a step-by-step process flow which creates a square hole.

Give your assessment what is the smallest practical nozzle size.

Simple square hole

- thermal oxidation happens on both sides simultaneously



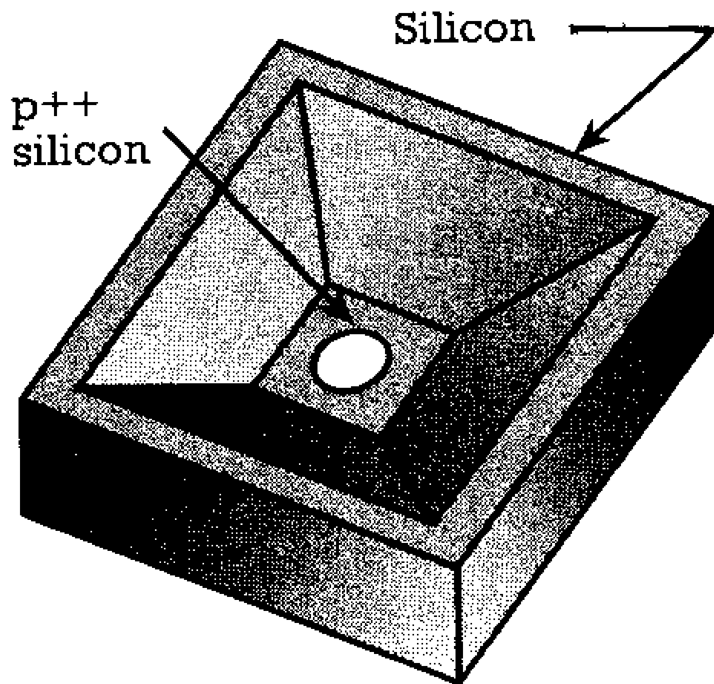
- lithography on front
- oxide etching
  (RIE etches only front; HF etches both sides, so backside needs resist for protection)
- *KOH etching*

For mask opening W, self-limiting depth is: $d = \frac{W}{\sqrt{2}}$

If we use 400 µm thick wafer, mask size $\sqrt{2} \cdot 400$ µm = 564 µm wide mask will result in zero-size opening.

If wafer thickness is 400 µm ± 10 µm
⇒ ca. 10 µm hole is formed, on the thinnest parts, and no holes on the thickest parts.

Through-wafer round nozzle



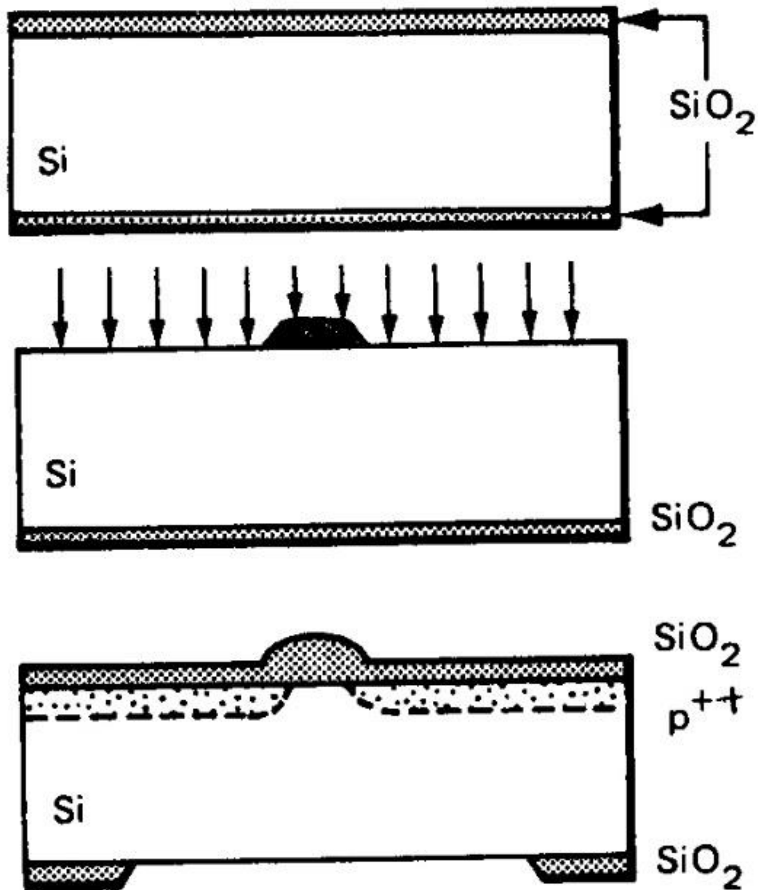
Design a step-by-step process flow which creates this nozzle.

Only wet etching process are used !

Thermal diffusion is used for doping.

Estimate which nozzle opening sizes are feasible with 3 µm litho available.

p++ etch stop: nozzle



<100> DSP wafer

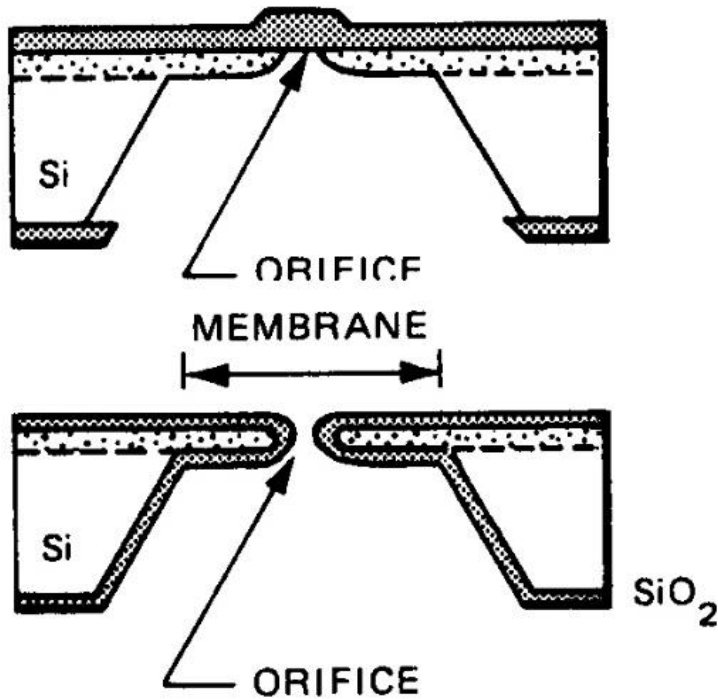
Thermal oxidation, both sides oxidized

Lithography on front
Oxide etching, front, RIE (ox back not)
Resist strip
Wafer cleaning
Boron diffusion

Oxide removal
Another thermal oxidation (p++ area oxidizes slower than standard doping silicon)

Lithography on back
Oxide RIE etching (oxide remains front)
Resist strip

p++ etch stop: round nozzle



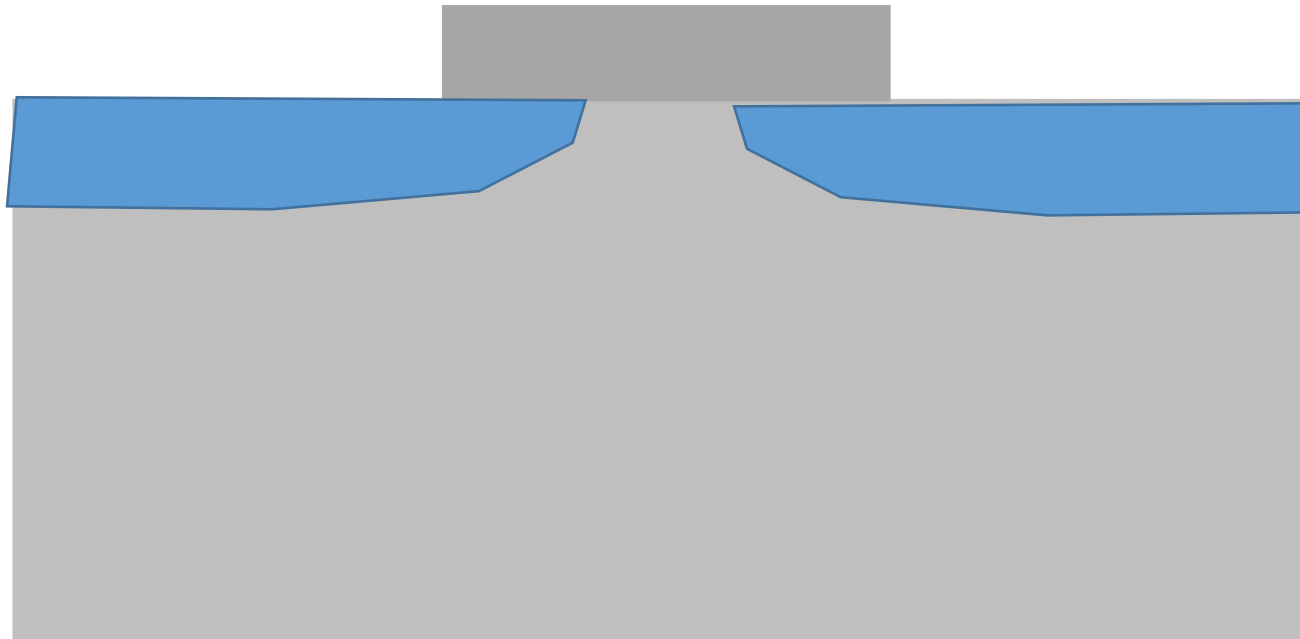
KOH etching from back (front protected by oxide)

P++ layer will stop etching elsewhere, but not in the round central spot.

Oxide is removed in HF

Another thermal oxidation to passivate all surfaces.

Round hole size

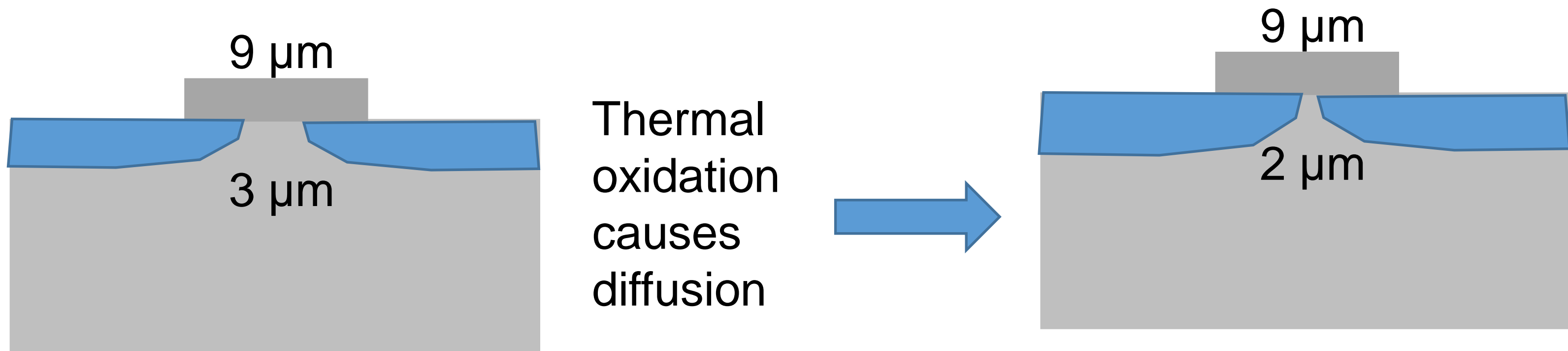


Round hole size

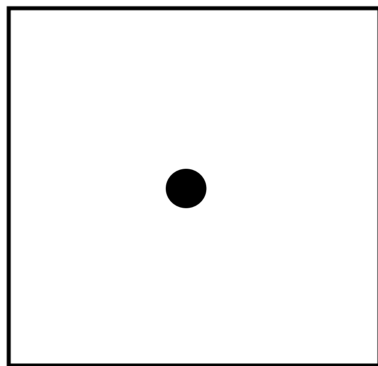
Lithography
Oxide etching These are well controlled, ±0.5 μm

Boron diffusion: need high concentration and deep (e.g. 3 μm)
➔ 3 μm sideways diffusion also

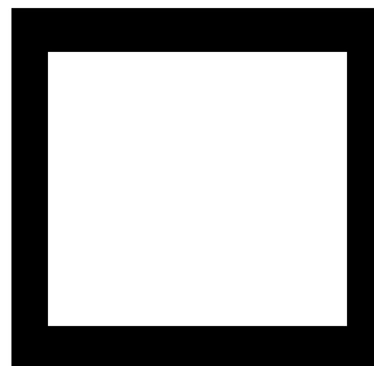
Final oxidation narrows the hole a bit: 500 nm thick oxide consumes ca. 250 nm of silicon ➔ narrowed from both sides ➔ 500 nm narrowing



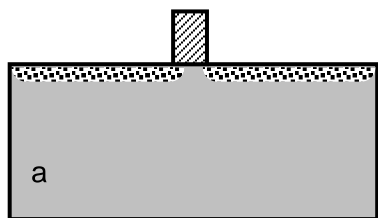
Critical vs. non-critical masks

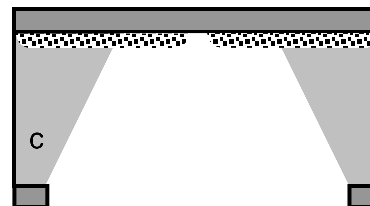


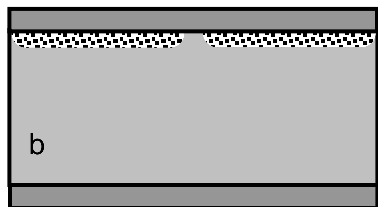
Mask #1



Mask #2

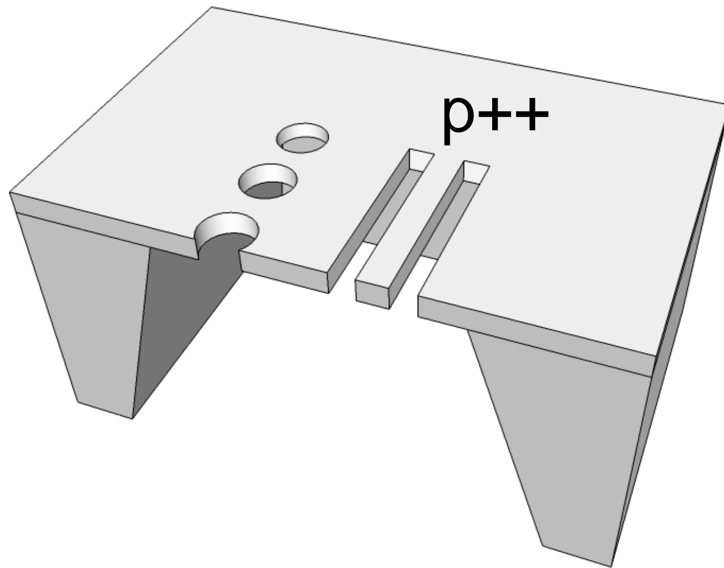






With DRIE

Simple blanket diffusion



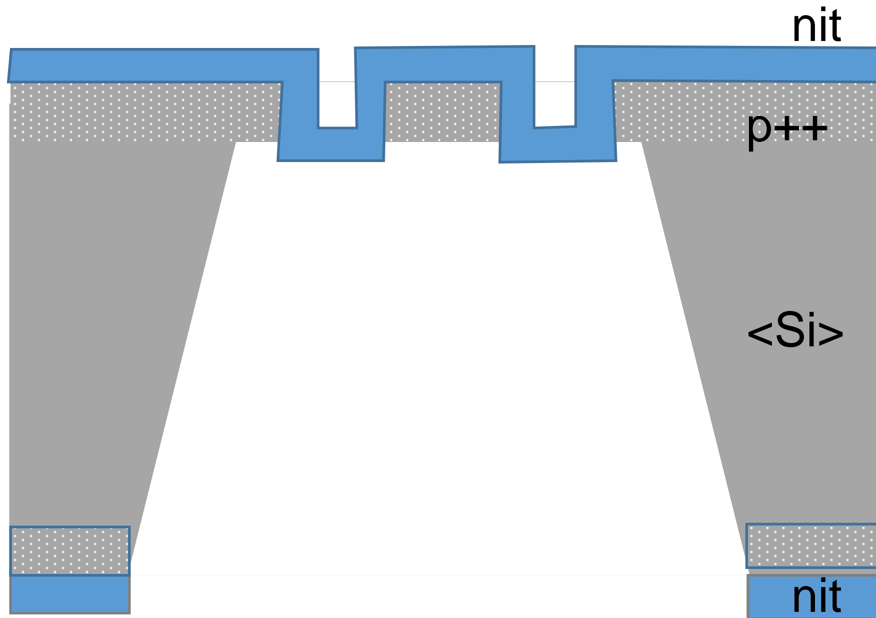
-eliminates diffusion narrowing

-allows narrow spaces, too (with p^{++} diffusion+wet etching process you can get small holes, but not closely spaced holes)

-DRIE enables any shape (difficult to make corners by diffusion) and is independent of doping level

Which is done first: KOH or DRIE ?

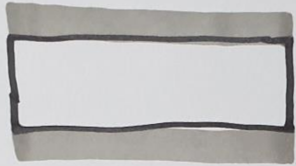
p^{++} & silicon DRIE

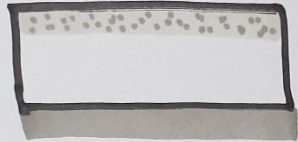


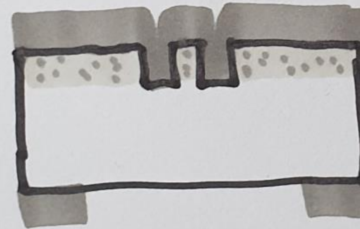
1. p++ diffusion on both sides
2. Top side litho (small holes)
3. Si DRIE + resist strip
4. LPCVD nitride (both sides coated)
5. Backside litho (large opening)
6. RIE nit/p++ Si + strip resist
7. Silicon KOH etch
8. Isotropic CF_4 etch of nitride

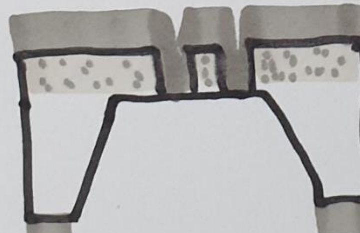
Why is resist mask enough in #3?

V 2.0: p++ & DRIE









V3.0: p++ & DRIE

1. p++ diffusion on both sides (3 μm deep)
2. Thermal oxidation (both sides, 1 μm deep)
3. Litho on bottom (large opening)
4. Oxide RIE + strip resist
5. KOH etch Si
6. Front side litho (round holes, 3 μm in diameter)
7. Oxide RIE + Si DRIE + strip resist