MOS basics

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Chapter 26, 38

Previous material

- All required process steps
- Integration, MEMS etching
- Next lecture
- Bulk MEMS

Outlook

- CMOS steps and doping units
- MOS (MOSFET) transistor
- Self-alignment concept
- 5 µm polysilicon gate CMOS transistors
- Advanced CMOS

CMOS steps

- Main process steps:
  - High temperature processing
    - Oxidation
    - Diffusion
    - Fusion bonding
  - Film deposition
  - Implantation
  - Lithography
  - Etching
  - CMP

  - Silicide formation

Doping levels and units

- Volume concentration, at/cm^3, ion/cm^3
  - Real doping
  - Atom self-concetration in *c*-Si is 4.5×10^{22} Si/cm^3
  - Semiconductor doping is always < 1 at%, i.e., < 4 x 10^{20} P/cm^3.
  - The highest doping takes place in poly-SI, 1 x 10^{20} at/cm^3
- Surface concetnration (dose), ion/cm^2
  - Technological approach, used in implantation
  - Surface concentration = (volume concentration)$^{2/3}$
  - Si atom surface concentration (4.5×10^{22})$^{2/3}$ = 1.3×10^{14} Si/cm^2
  - Implantation dose 10^{12}-10^{16} P$^+$/cm^2, energy 20-200 keV

LOCOS I

Was in use up to 2008

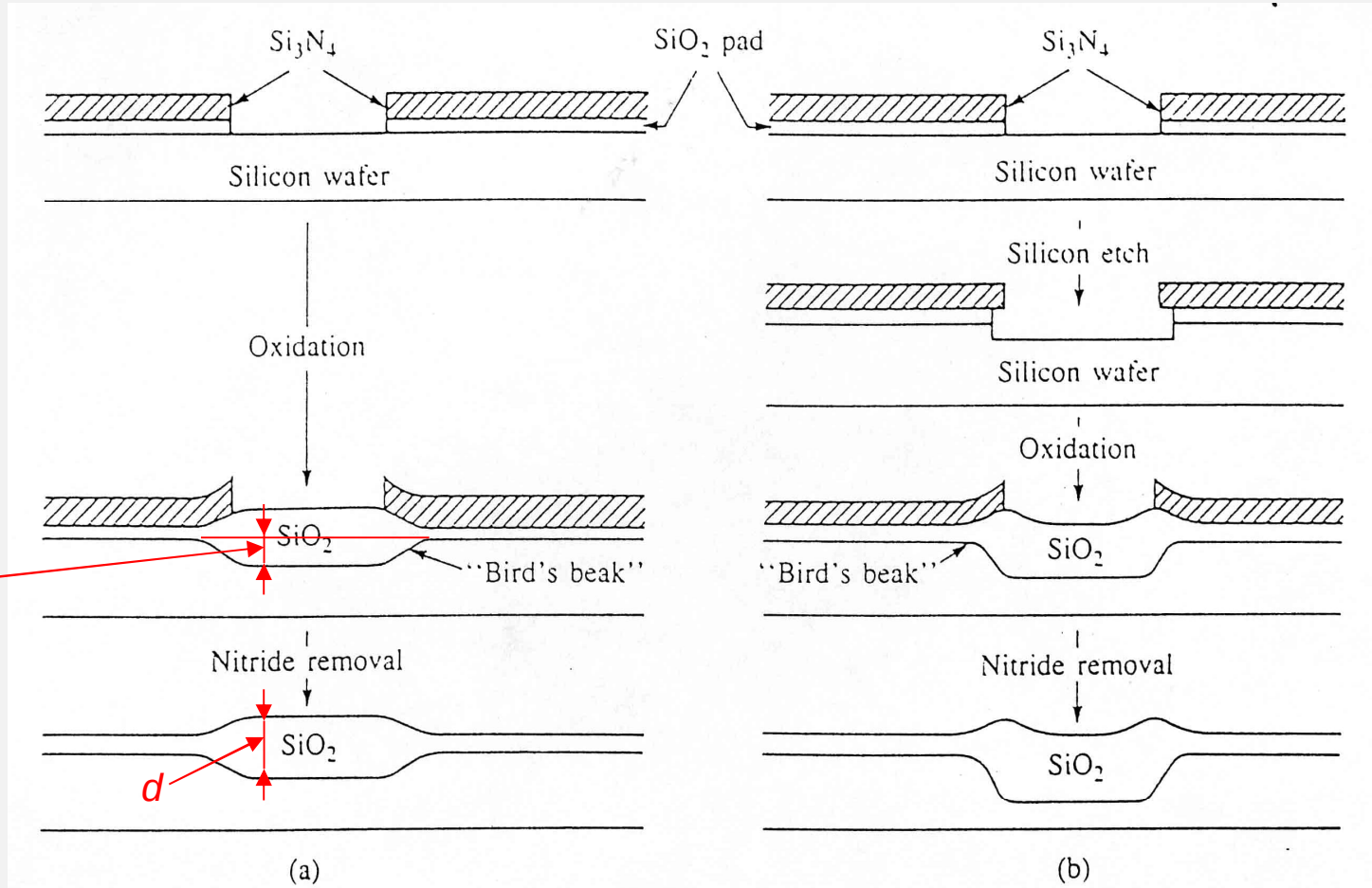
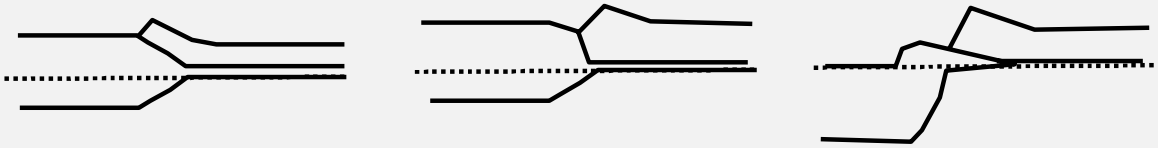
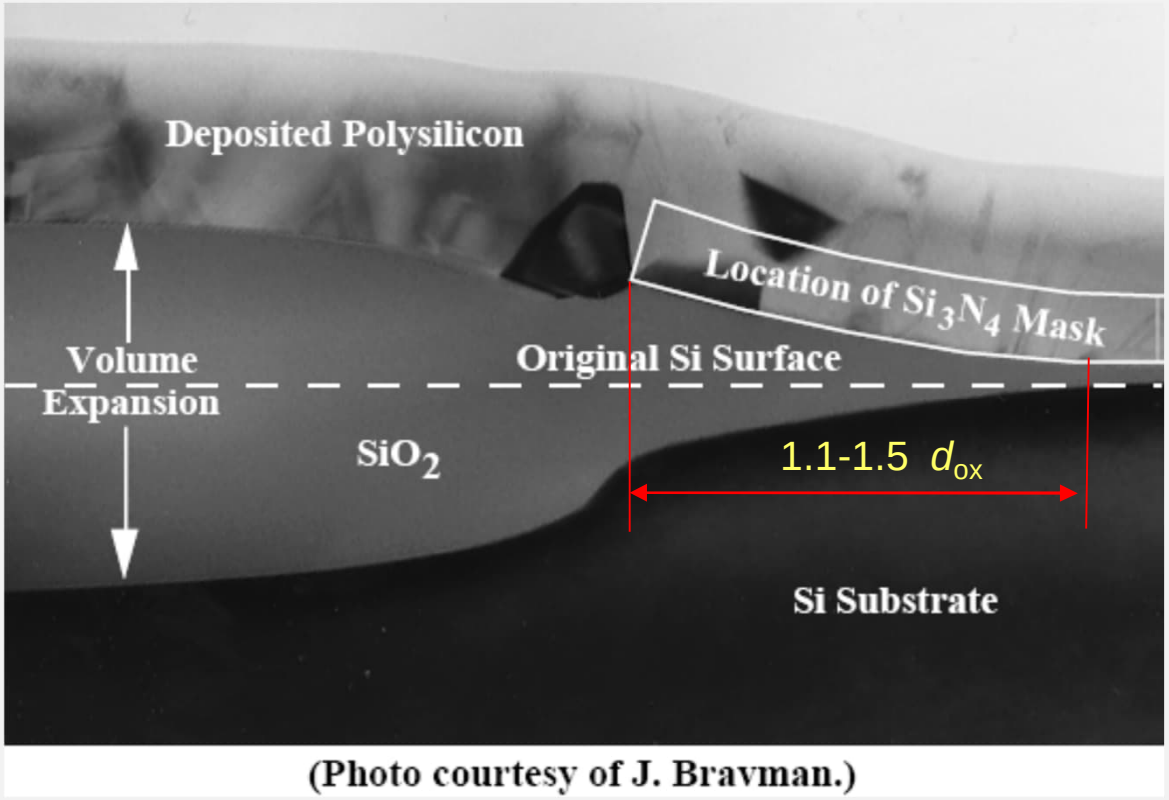


Fig. 3.12 Cross section depicting process sequence for (a) semirecessed and (b) fully recessed oxidations of silicon.

LOCOS II

thin nitride thick nitride recessed

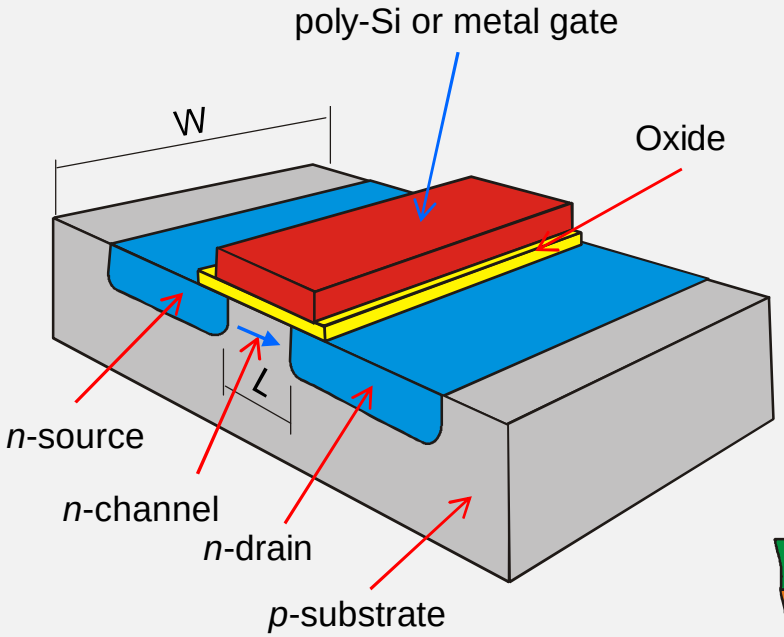




(Photo courtesy of J. Bravman.)

n-channel MOSFET

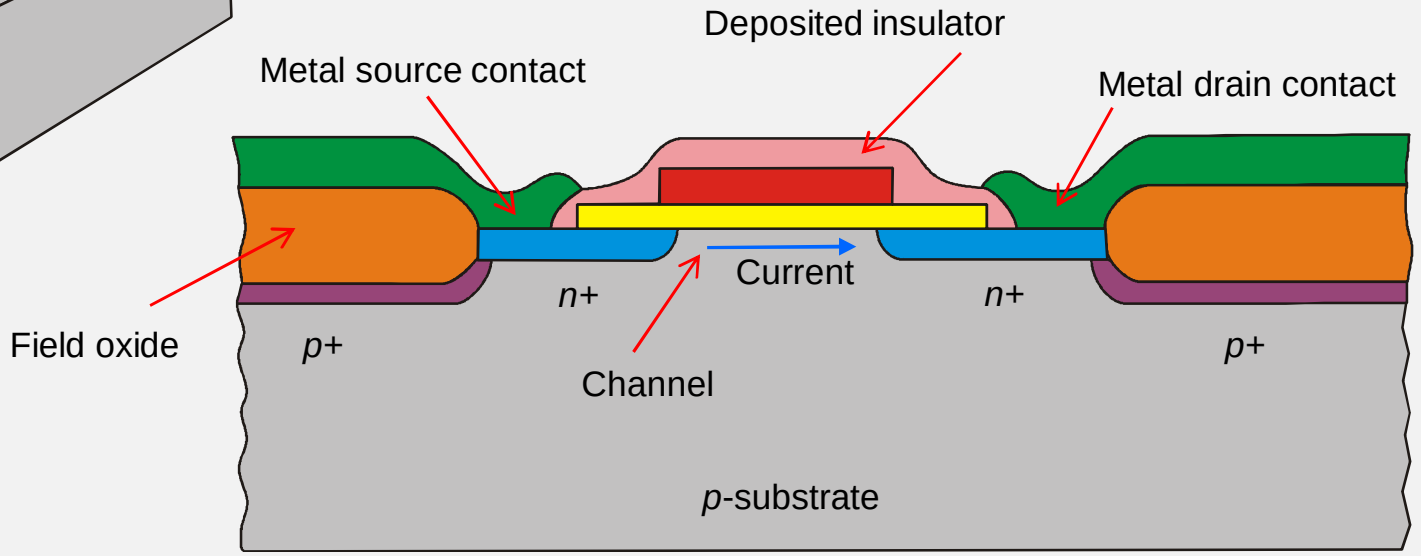
Theory



L – channel length

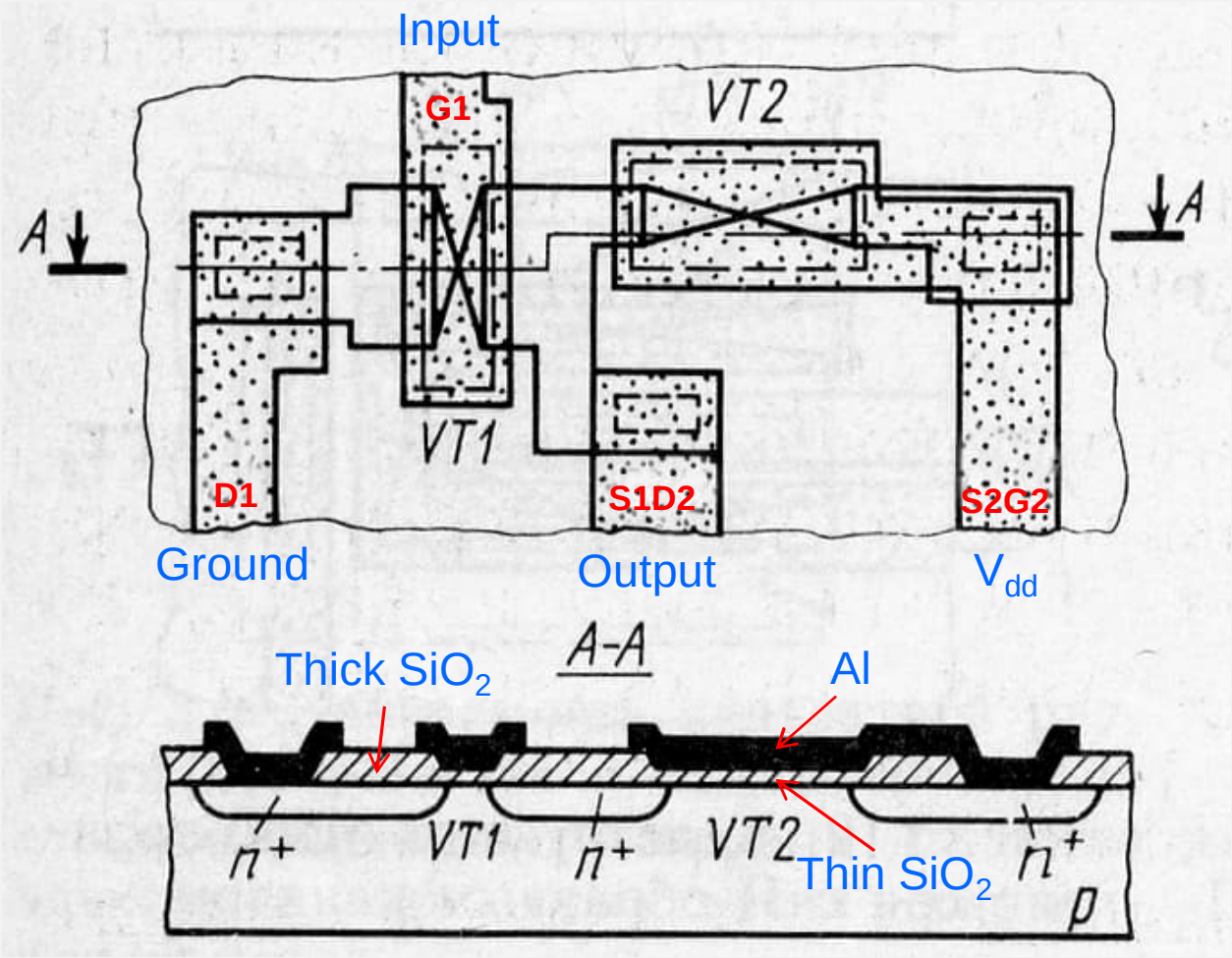
MOS – Metal Oxide Semiconductor
FET – Field Effect transistor

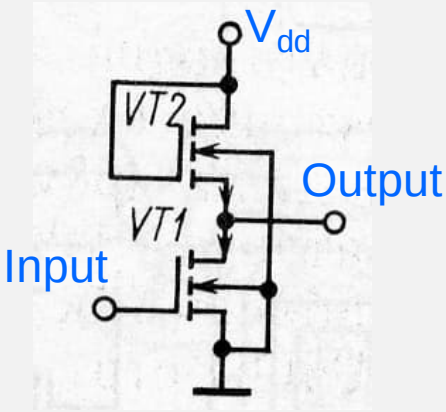
Real life



n-channel MOS inverter

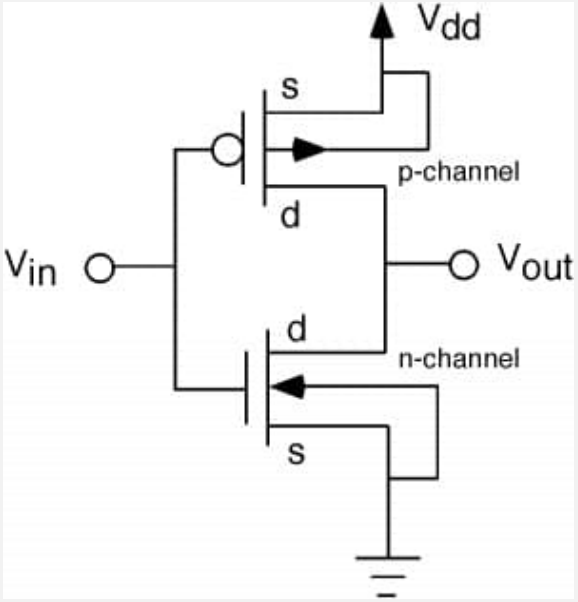
Used with Al gate, not poly-Si one!



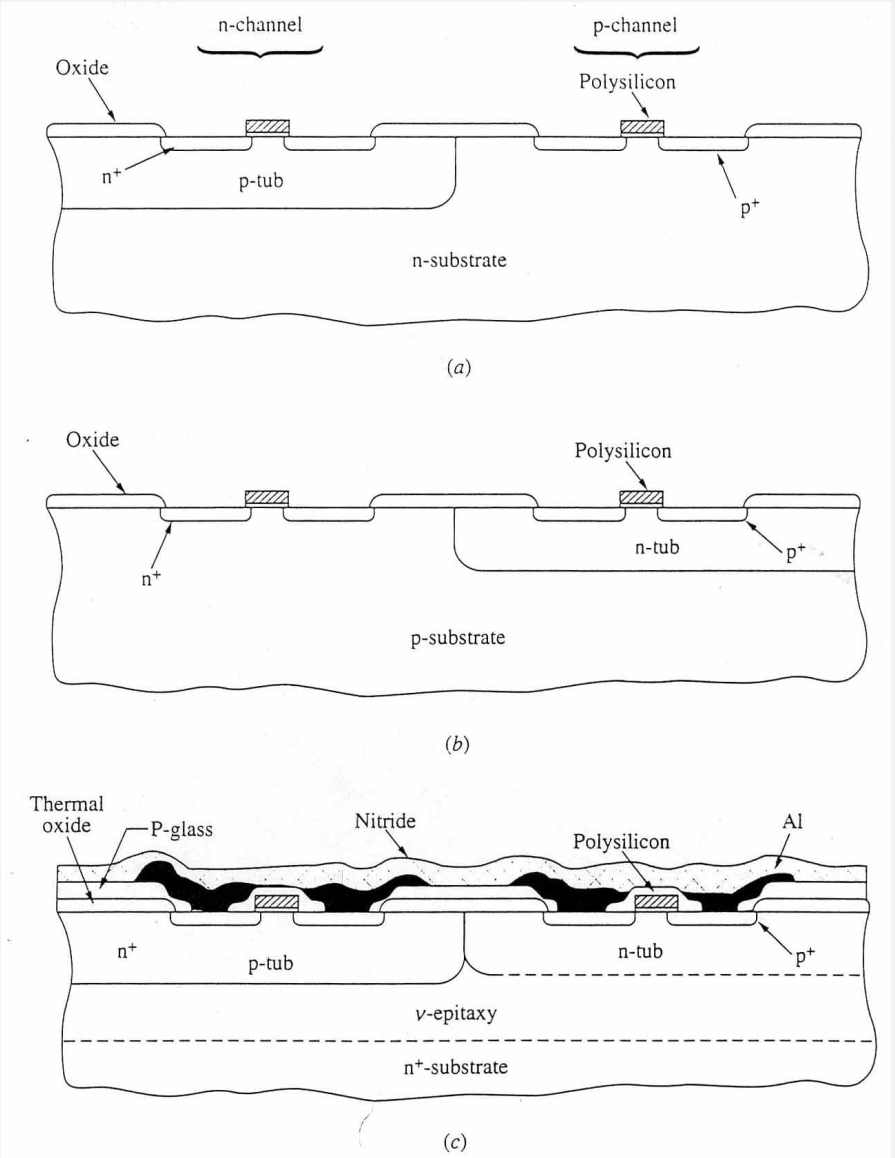


CMOS inverter

CMOS – complementary metal–oxide–semiconductor



Old - Al gate
New - poly-Si gate



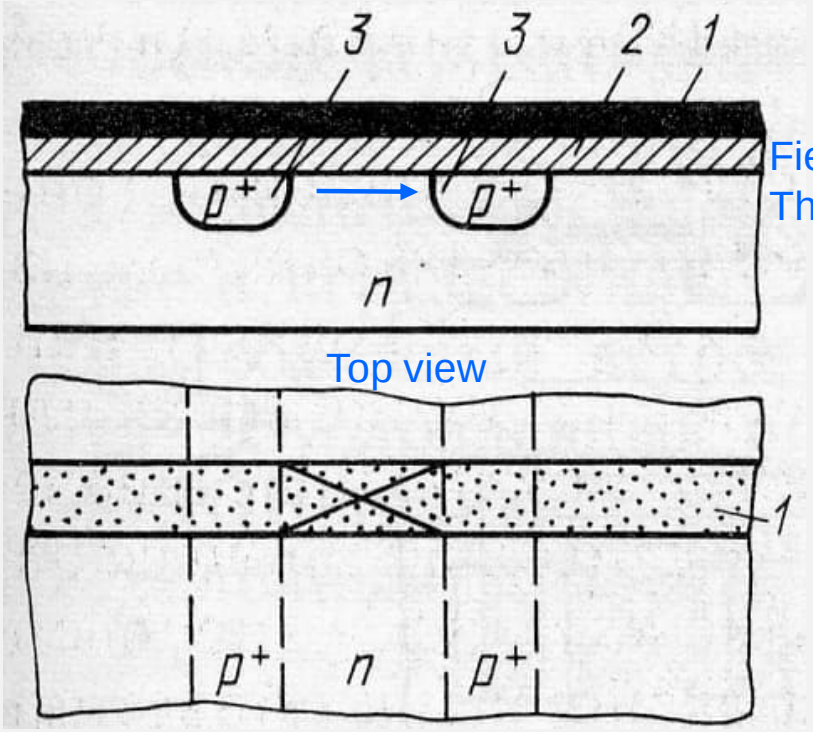
p-well

n-well

twin-well

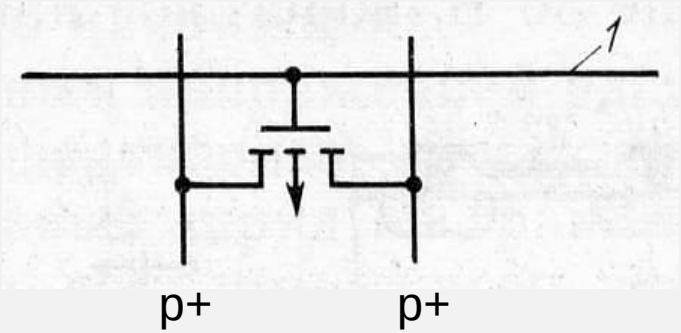
Parasitic *p*-channel FET

Field oxide – all oxides, exclude gate oxide.
To avoid parasitic FETs, field oxide must be thick!

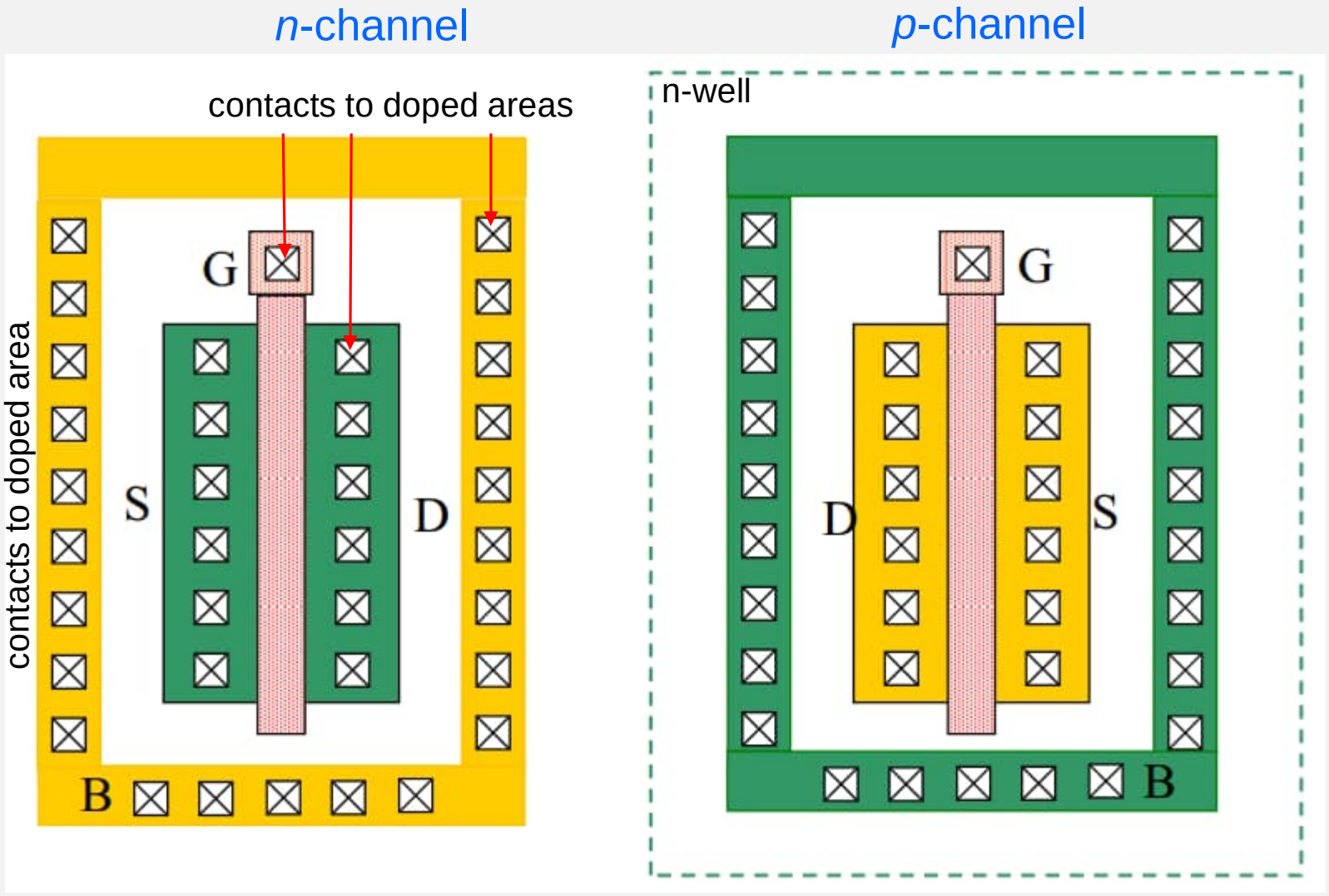


Field oxide.
The thicker, the better

1 – Al
2 – SiO_2
3 – diffused area

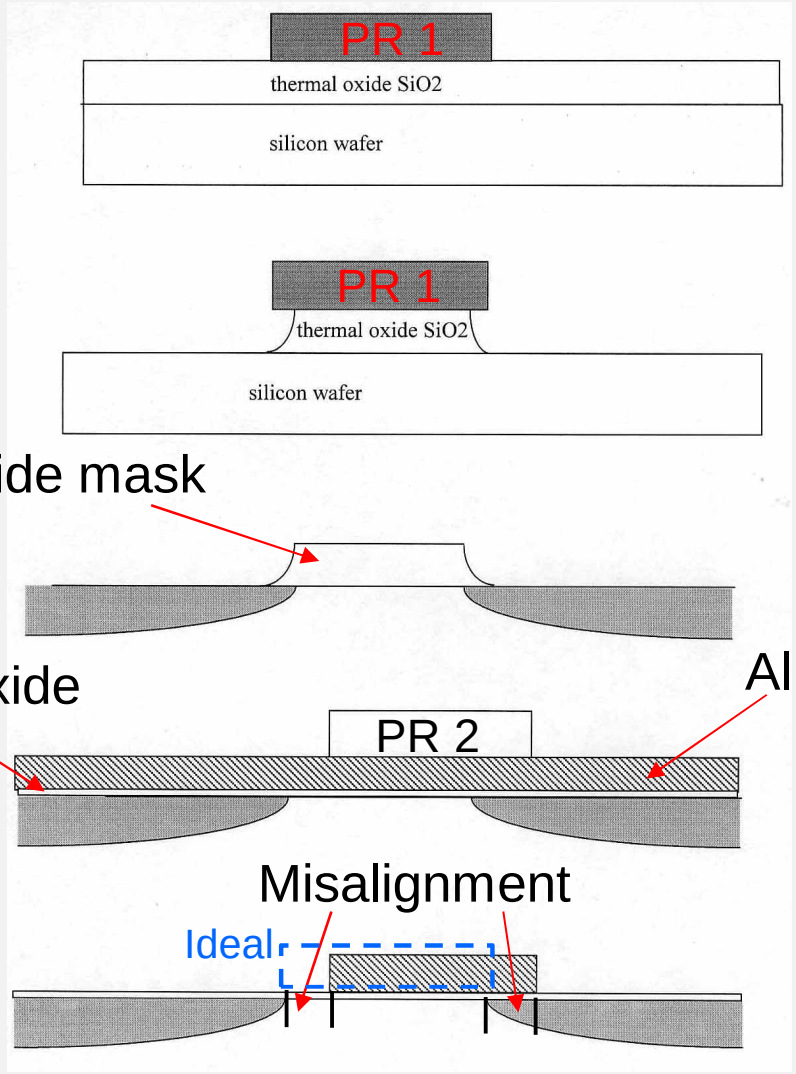


Transistor isolation by guard rings (top view)



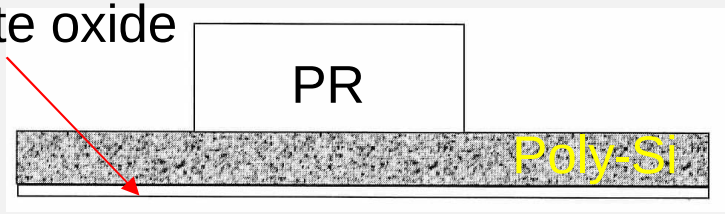
Gate self-alignment

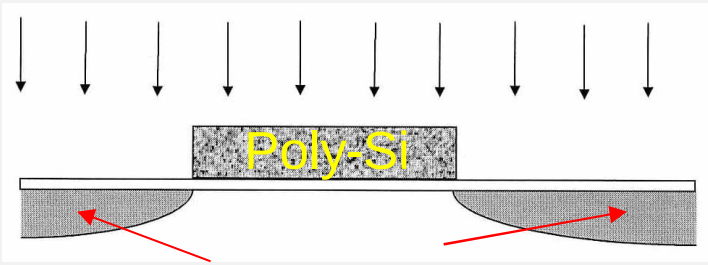
Lithographic alignment. Diffusion



Self-alignment. Implantation

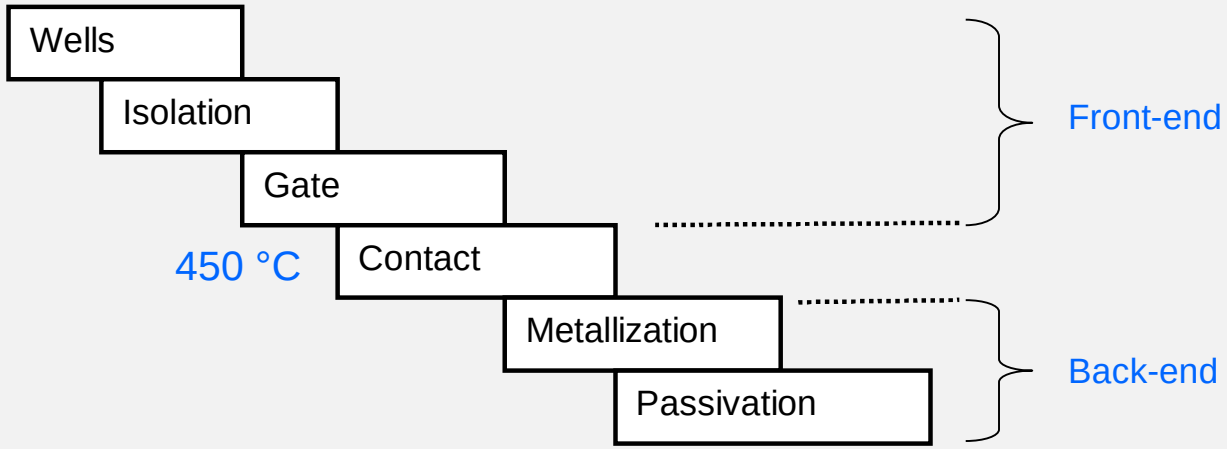
Why poly-Si?





Theoretical misalignment is zero!

Main modules of a CMOS process



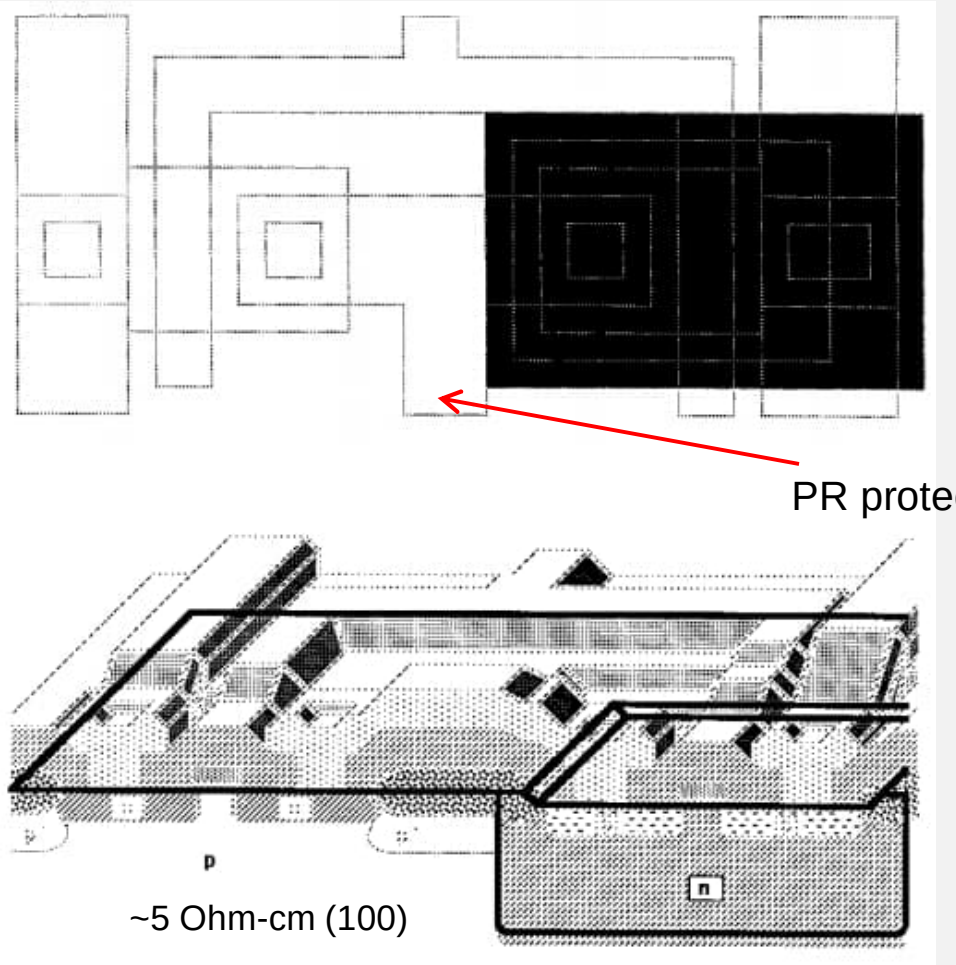
Only (100) Si wafers are used for MOS devices!

Wafer backside is metallized at the end of process to provide good thermal and electrical contact.

5 µm polysilicon gate CMOS inverter I

n-well implant (P, 50 keV, 10^{13} cm^{-2}) and drive-in (1150 °C, 8 h)

Channel-stop implant (B, 30 keV, 10^{12} cm^{-2})
Si_3N_4/SiO_2 mask



Reproduced from MIT, USA

5 µm polysilicon gate CMOS inverter II

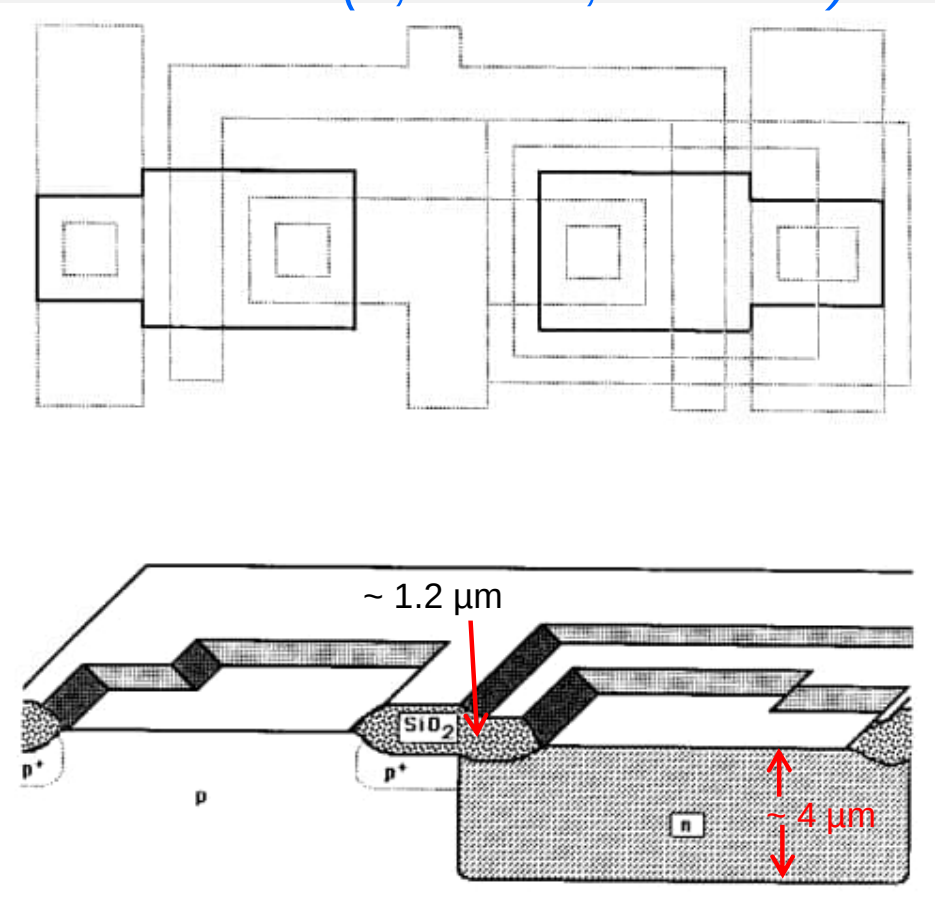
Field oxide growth (LOCOS, 1050 C, 6 h)

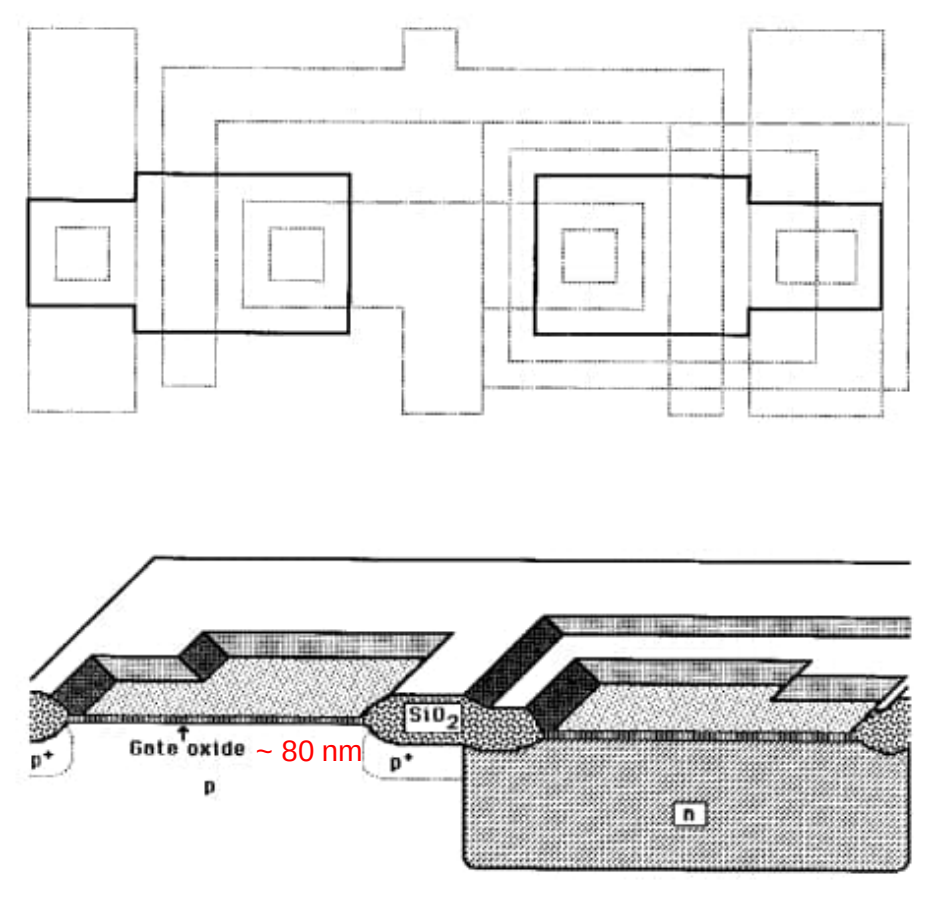
PMOS threshold implantation

(B, 50 keV, 10^{12} cm^{-2})

Gate oxide growth (blank)

1050 °C, 65 min





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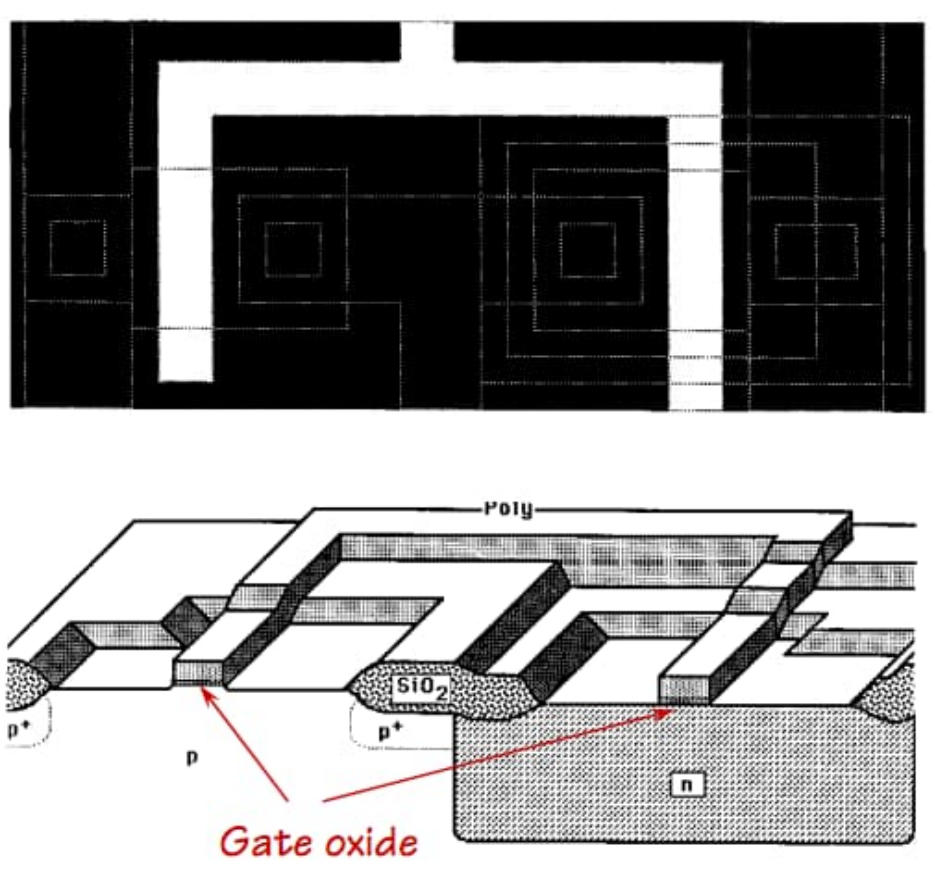
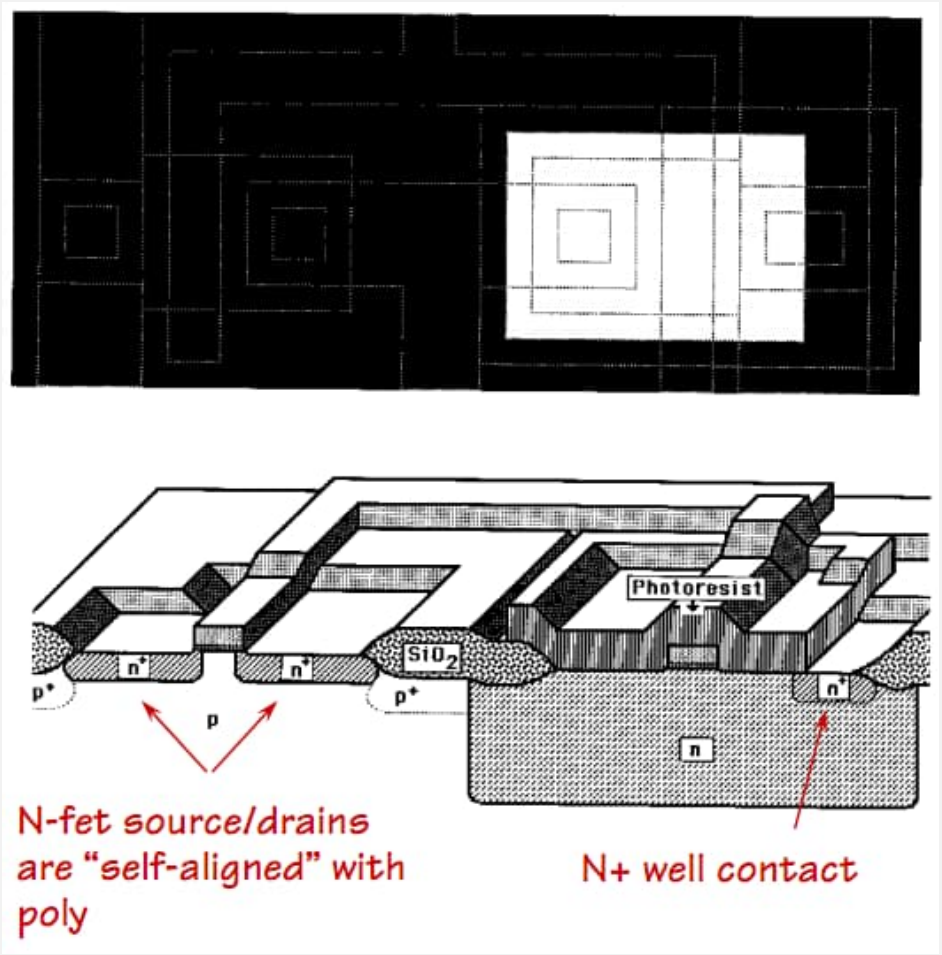
5 µm polysilicon gate CMOS inverter III

n+-poly (30 Ω/sq, 5×10^{19} cm^{-3}) deposition (500 nm) and dry etching

Doping by POCl3 after deposition



n^+ source/drain implant (50 keV,10^{15} cm^{-2})



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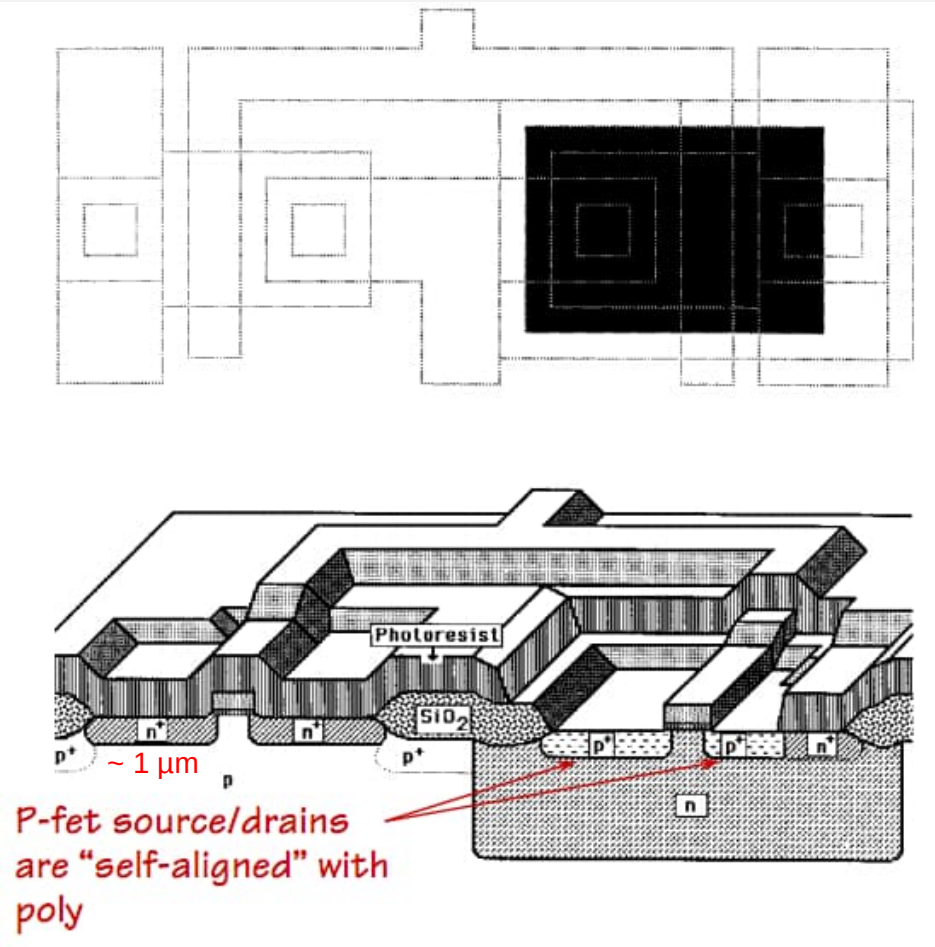
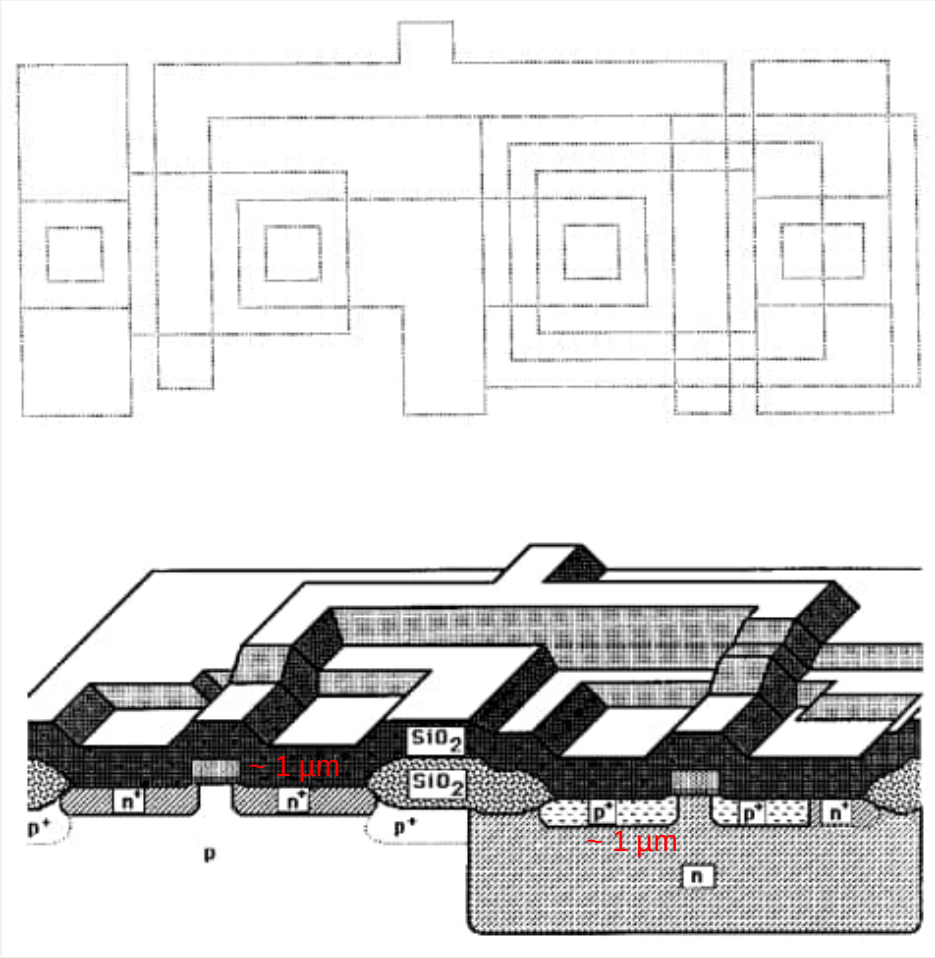
5 µm polysilicon gate CMOS inverter IV

p^+ source/drain implant (40 keV, 10^{15} cm^{-2})



Interlayer CVD oxide (PSG)

Anneal at 1050 C



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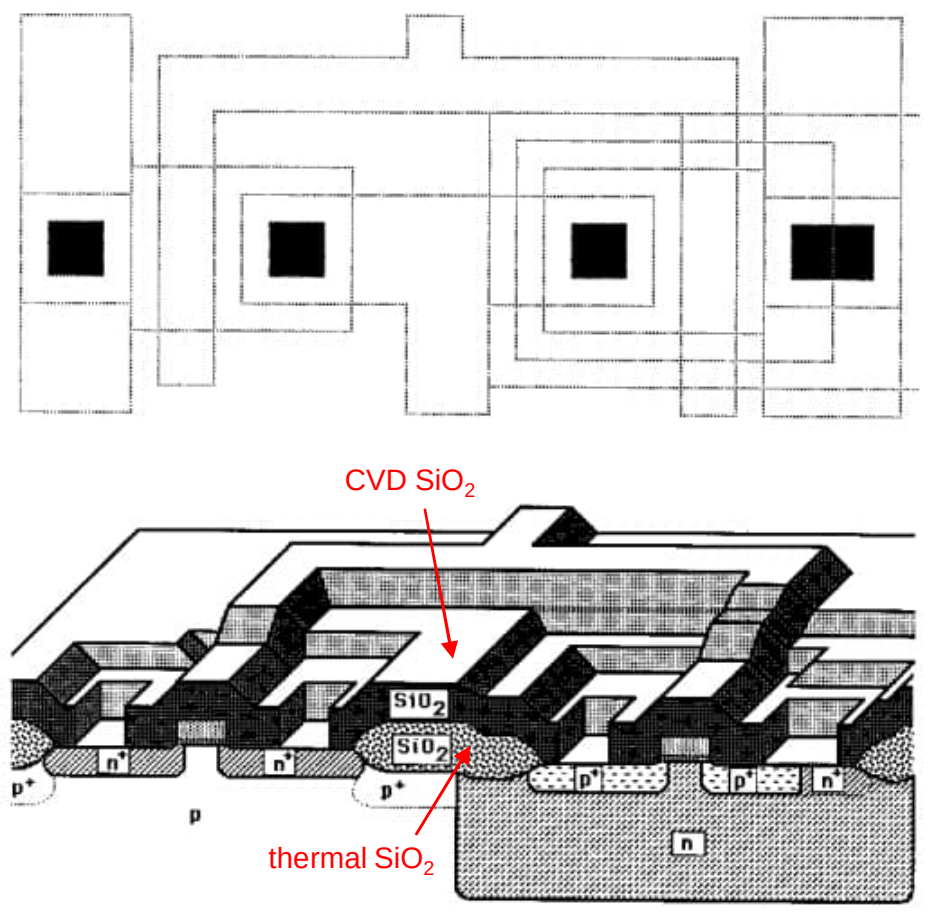
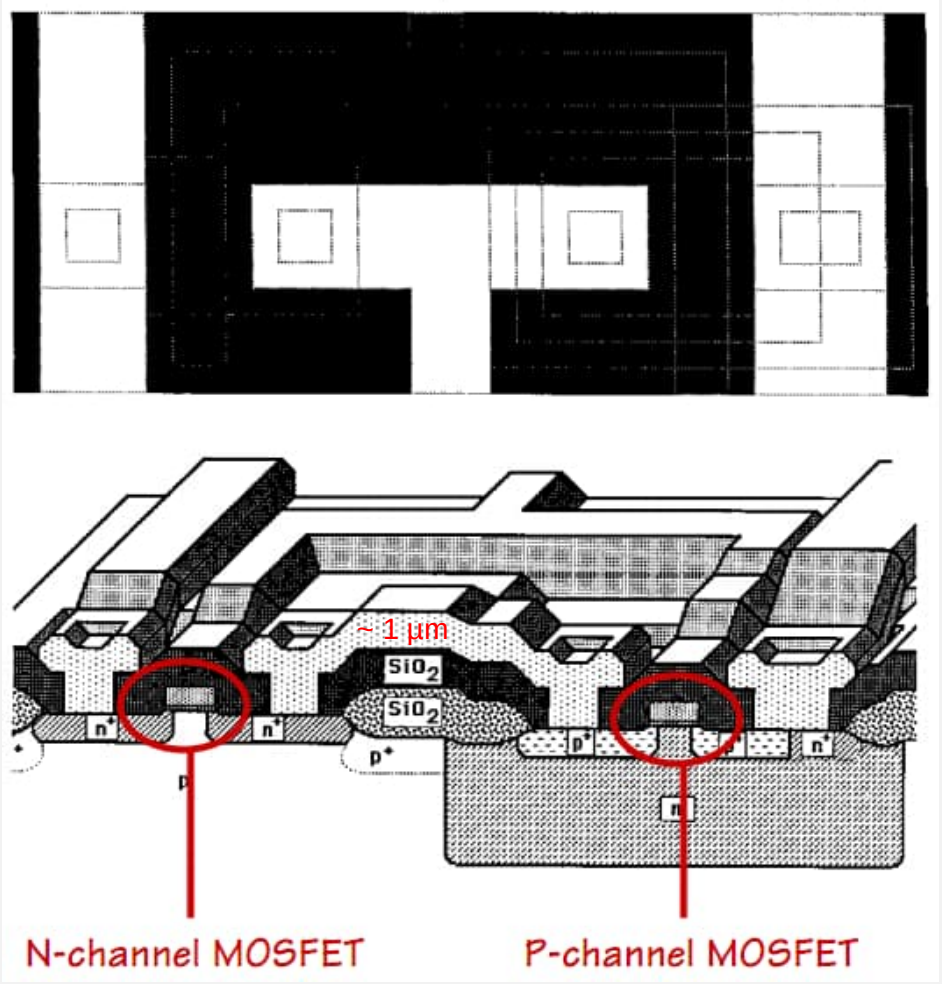
5 µm polysilicon gate CMOS inverter V

Vias opening (wet)

Al deposit, wet etching, anneal at 450 C. Passivation





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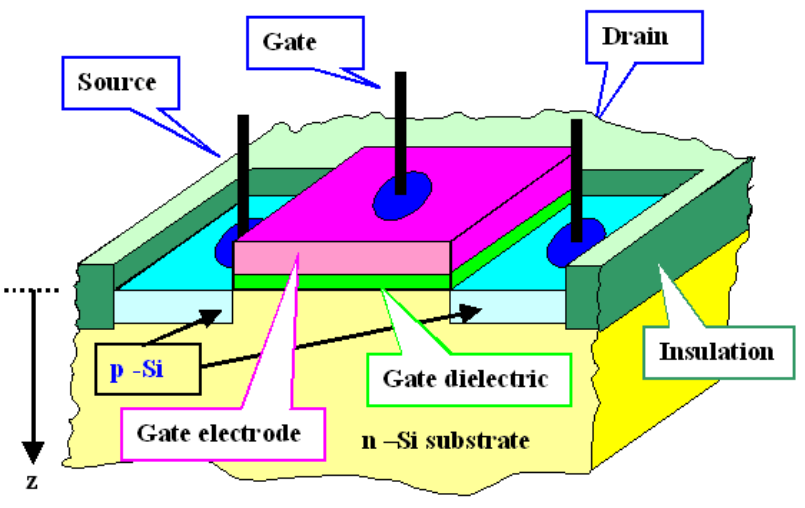
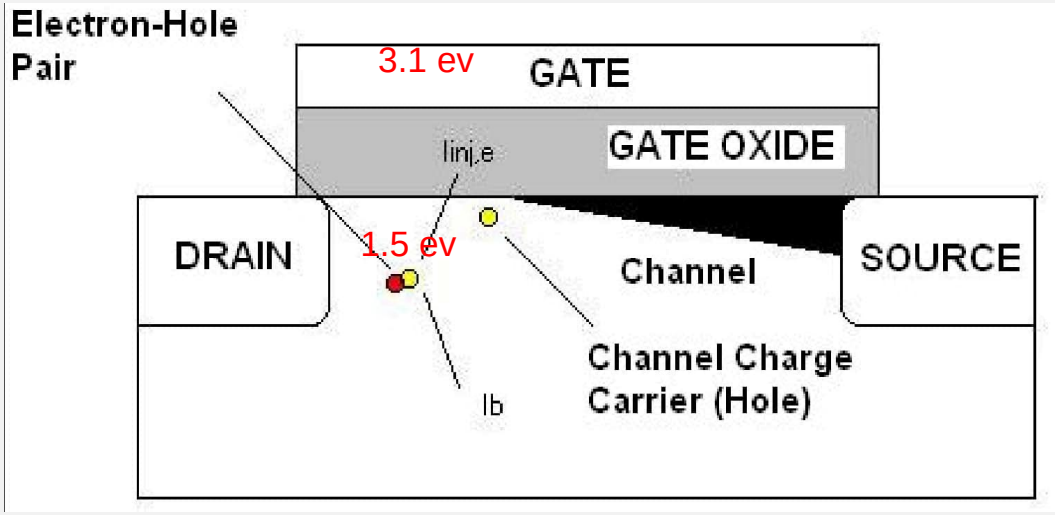
Hot-carrier formation mechanism



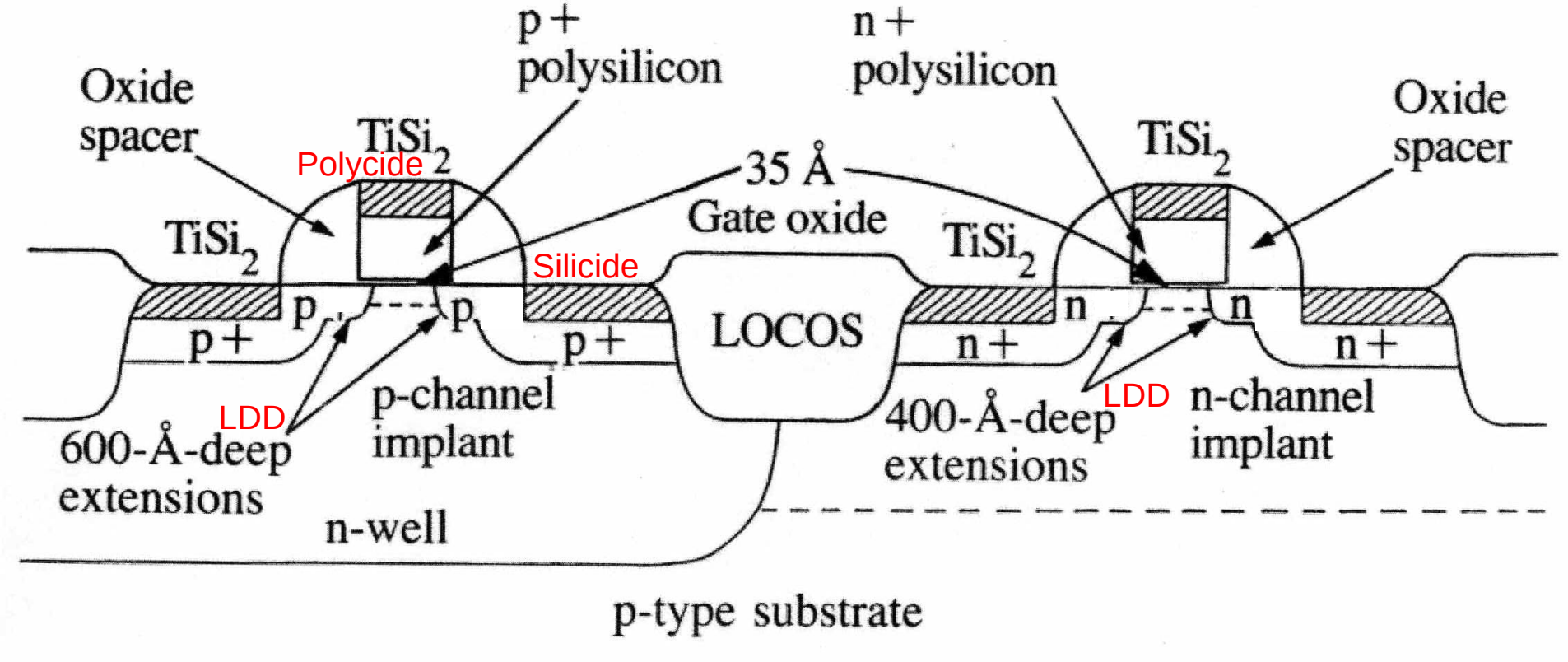
P-MOS transistor



Turk J Elec Engin, VOL.14, NO.3, 2006

0.5 µm CMOS with LDD and silicide

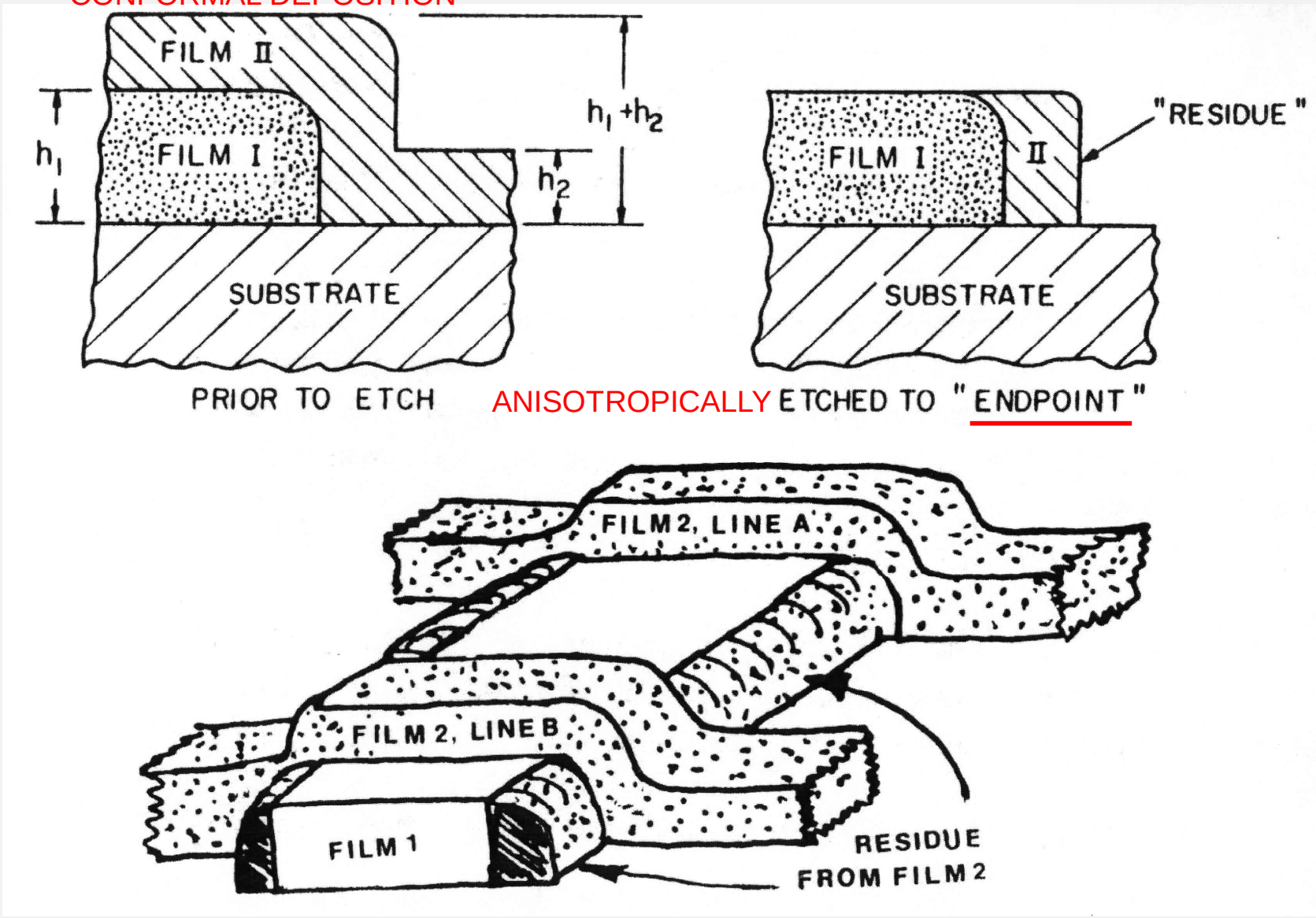
Start of RTA for Si defect removing



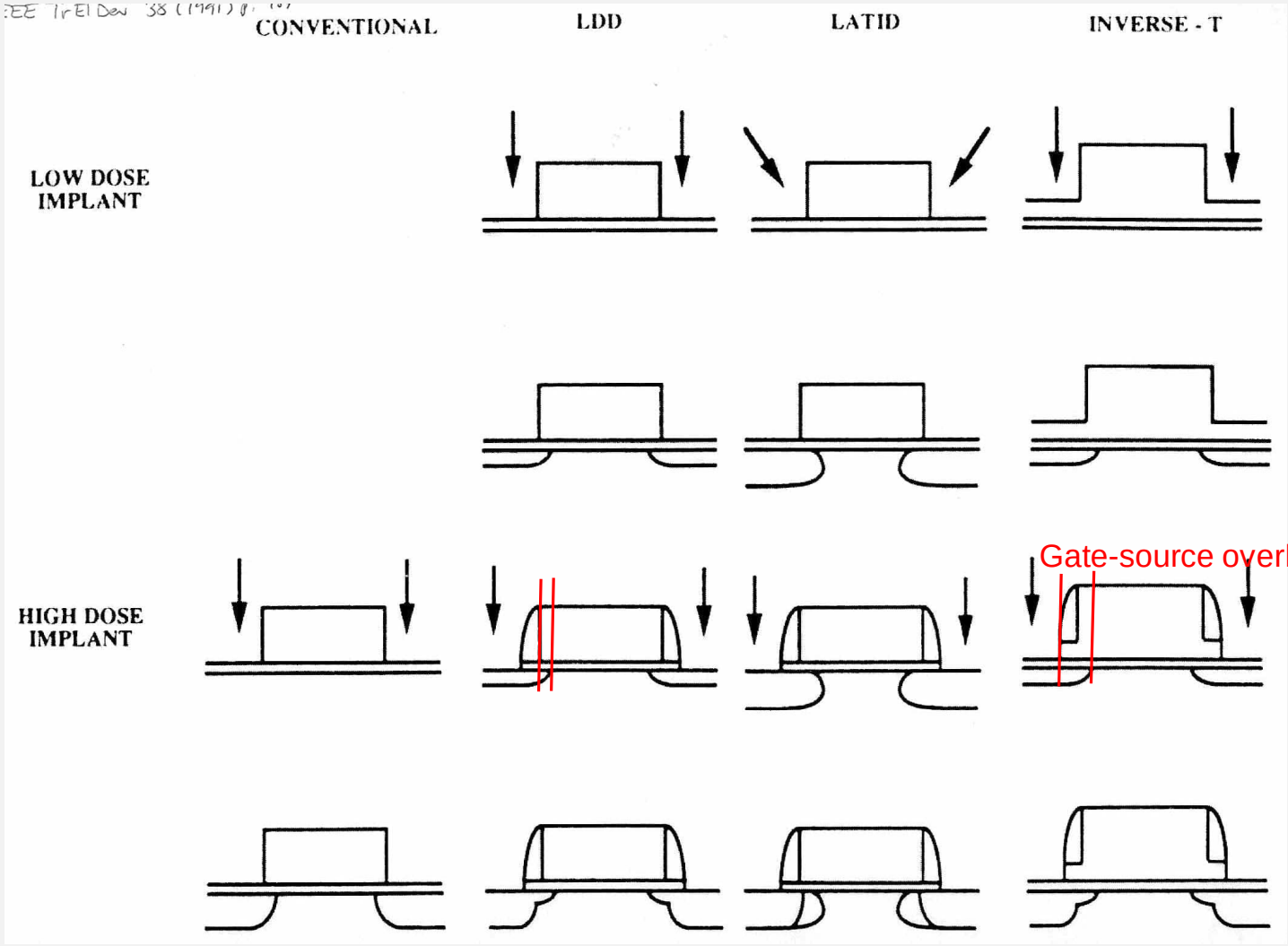
LDD size is less than photolithography resolution!

Spacers

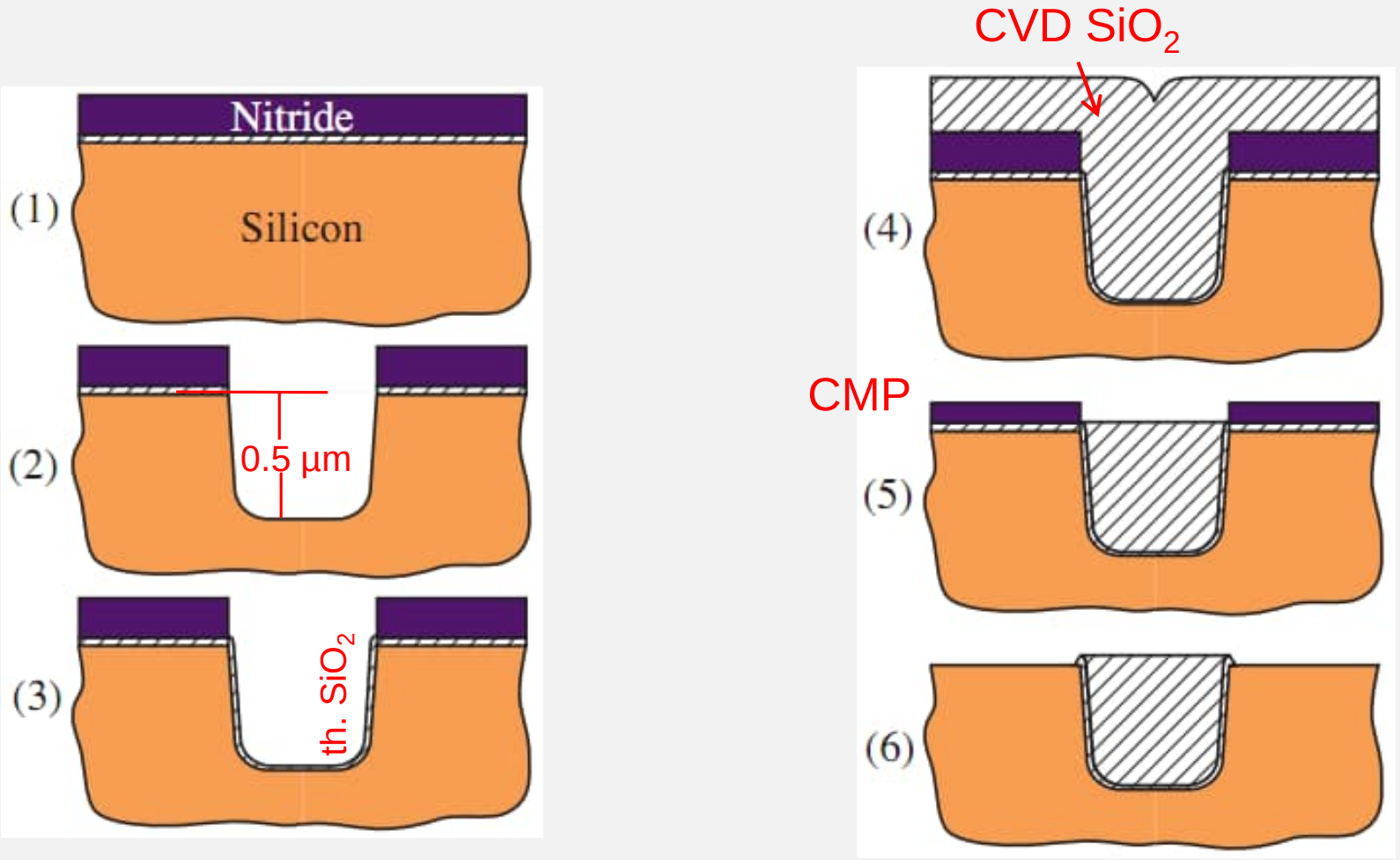
CONFORMAL DEPOSITION



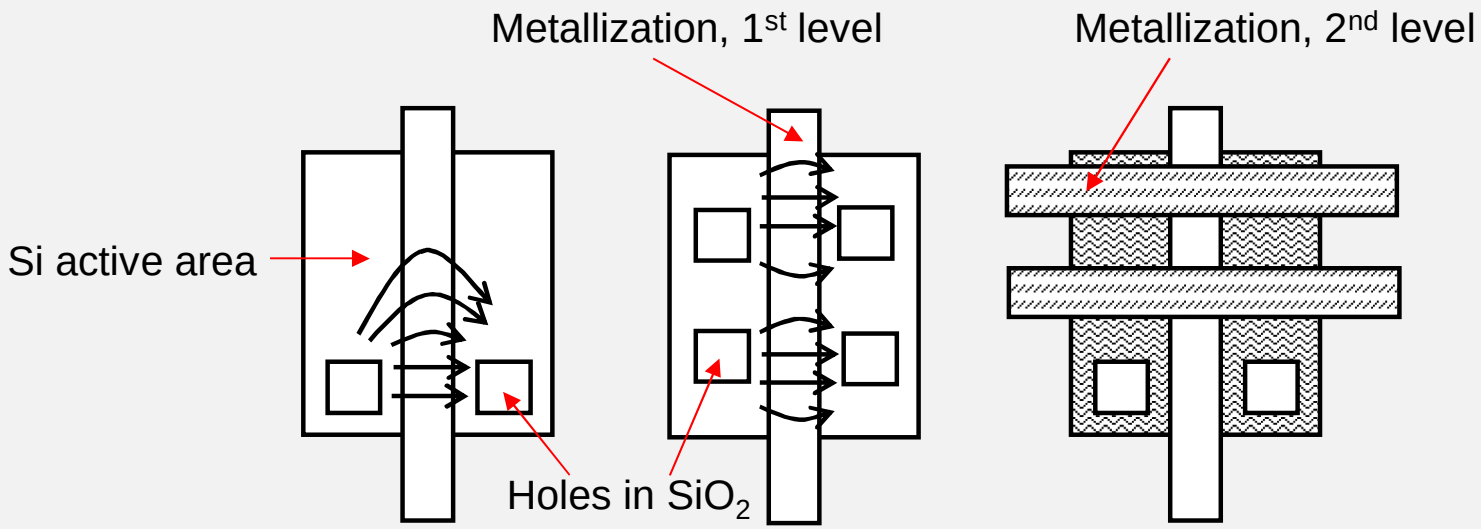
LDD variations



Shallow trench isolation STI



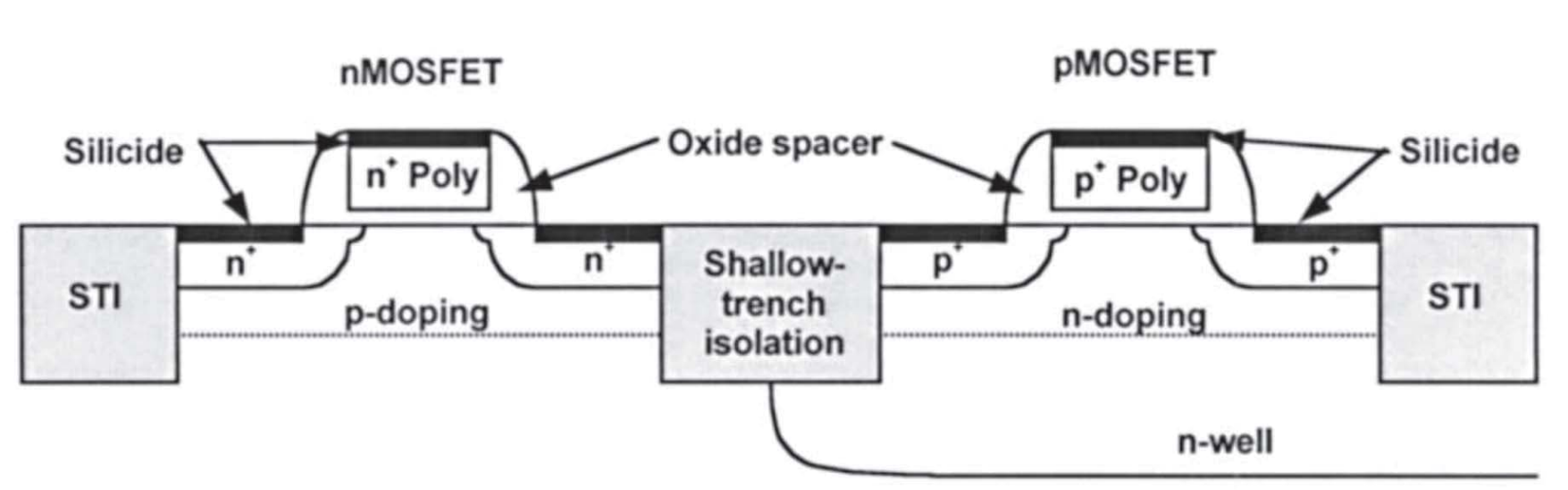
Metal and silicide contacts to Si



Al, local Al, multiple Silicide

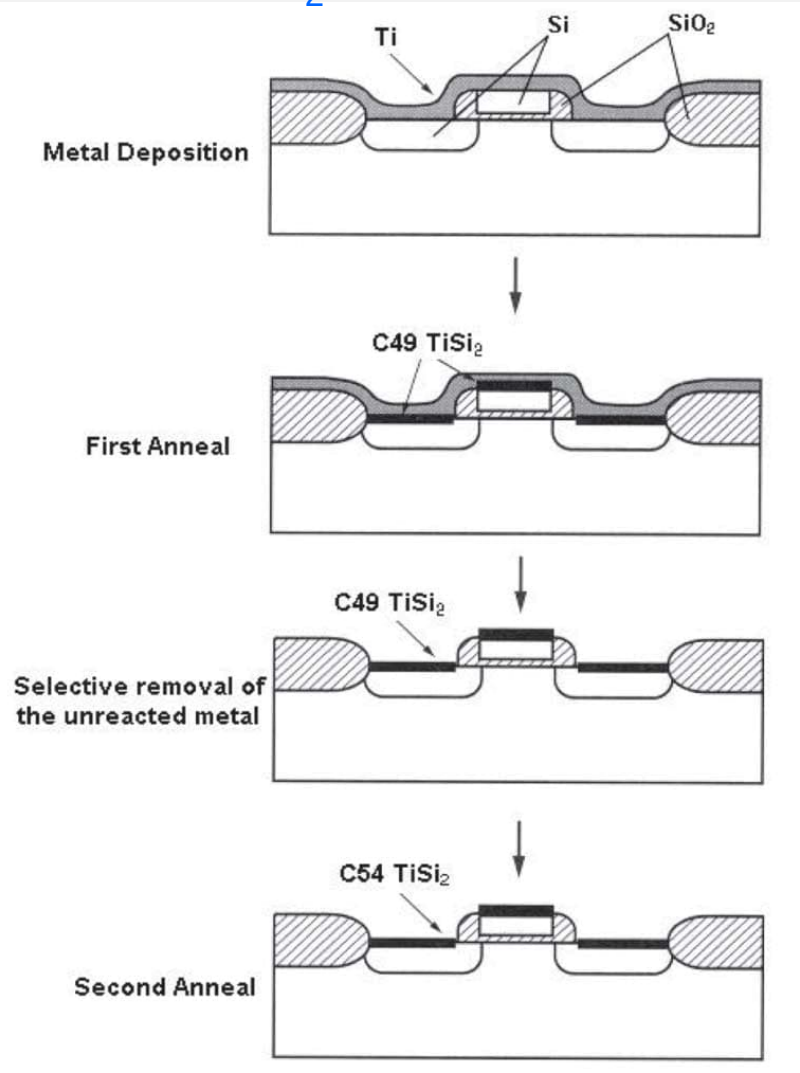
CMOS and silicide

Metal silicide – compound that combines Si and any metal

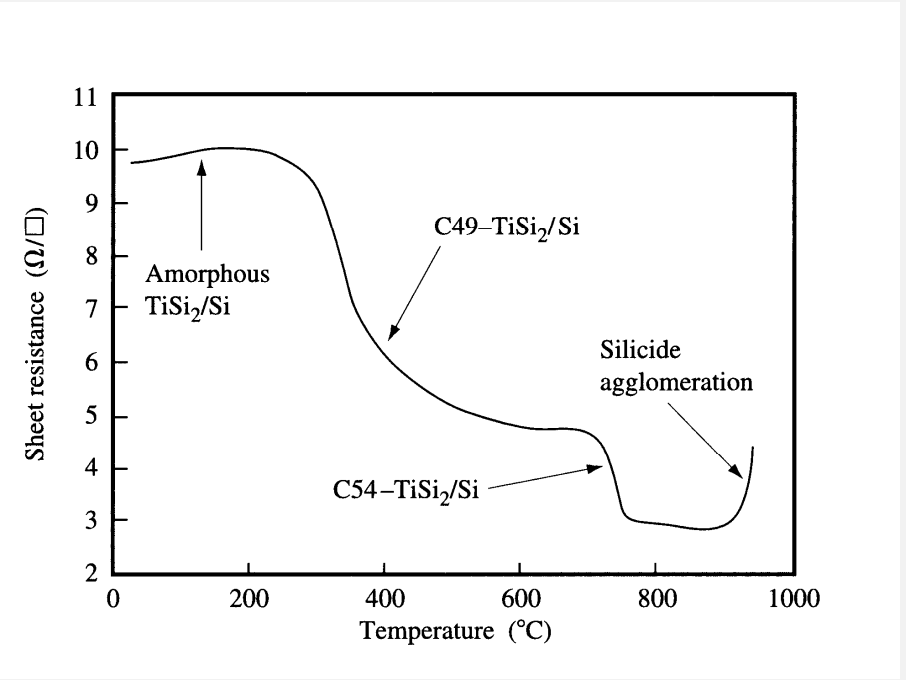


Self-aligned silicide (salicide)

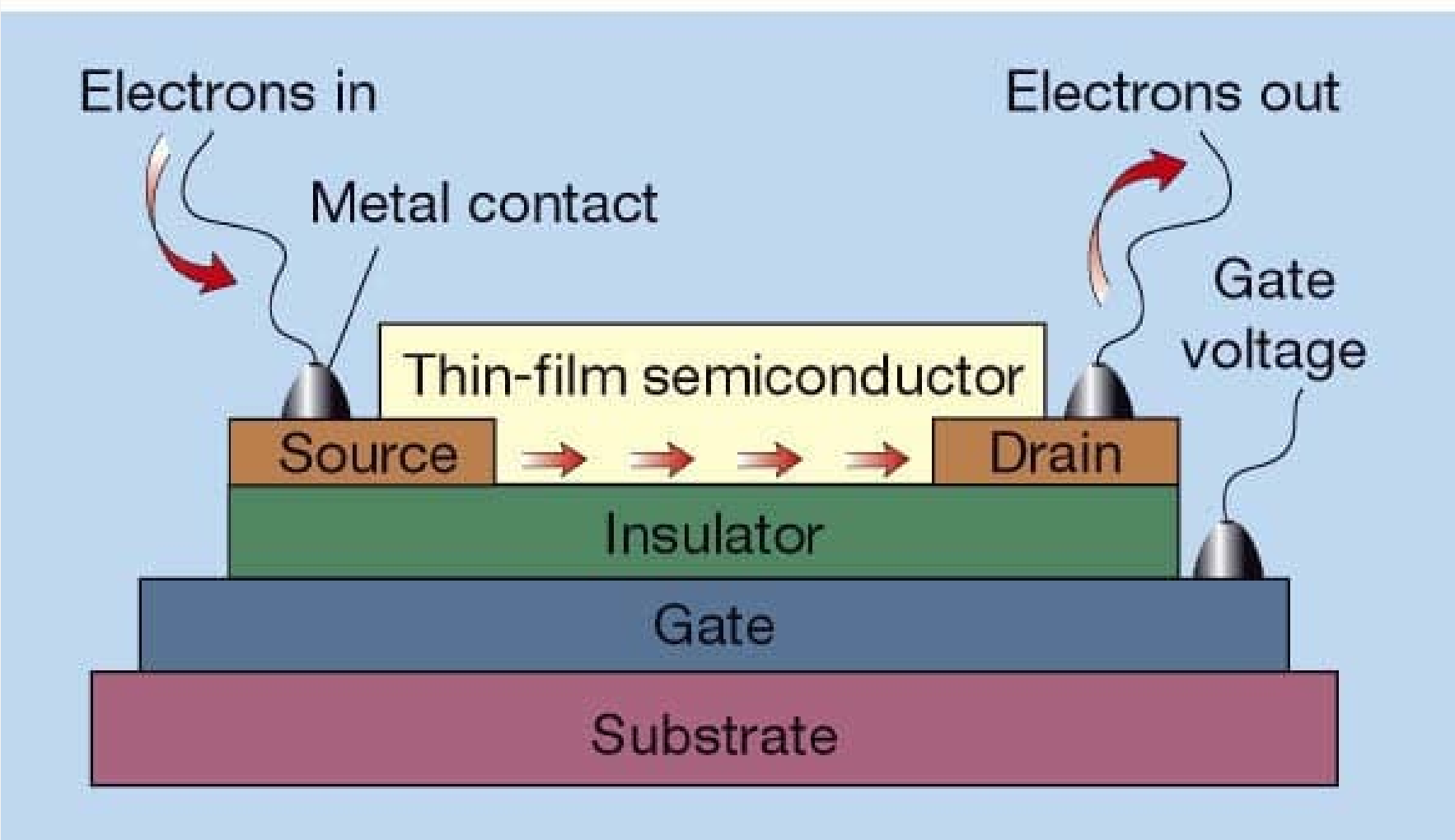
TiS_2 formation



TiS_2 phase transition



Thin-film trasistor (TFT)



Conclusions

- Al gate MOSFET is a start point of the CMOS industry
- Further development led to self-alignment and poly-Si gate solutions
- Poly-Si CMOS includes all modern process steps. It replaced Al gates at 5 µm CMOS node
- Advanced CMOS includes STI, LDD, silicide etc
- CMOS processing is a milestone of the modern semiconductor technology