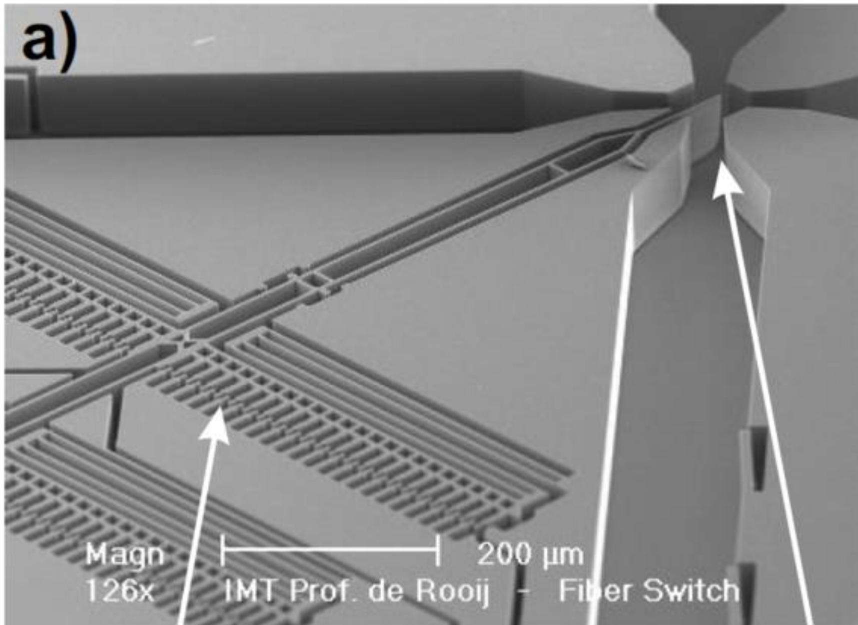
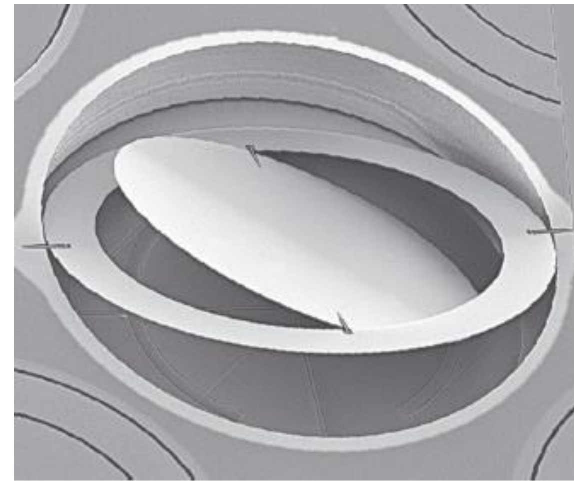
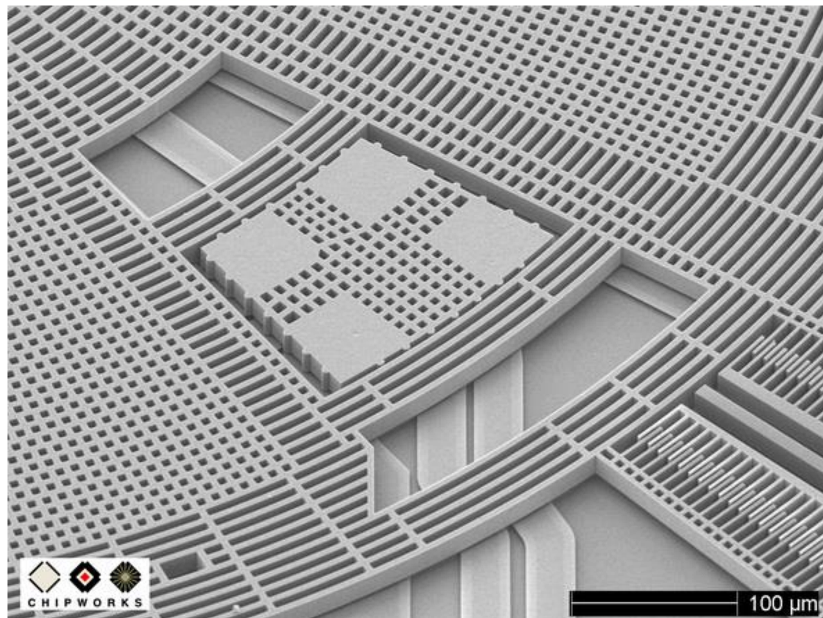
MEMS 2: Bulk, SOI & CMOS-integrated (Chapter 30)

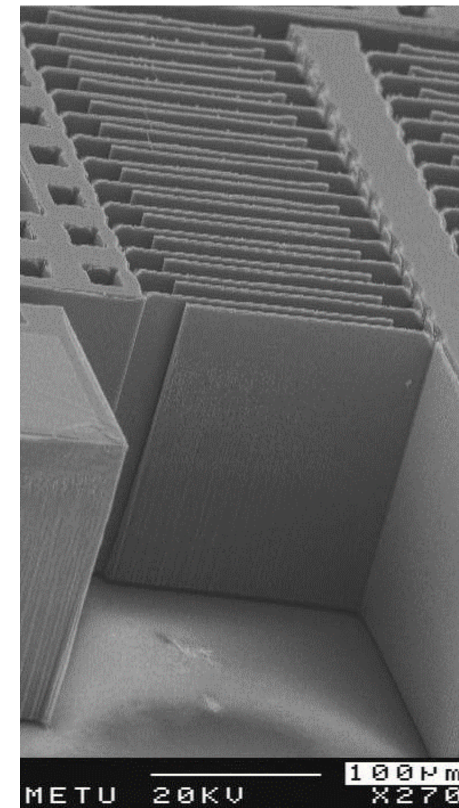
sami.franssila@aalto.fi



comb drive **mirror**







MEMS device categories

- Bulk vs. SOI vs. surface vs. CMOS-MEMS
- Double sided lithography
- Membranes and beams
- Needles in-plane and out-of-plane
- Cavity-SOI (C-SOI)
- MEMS zero-level packaging

Types of MEMS

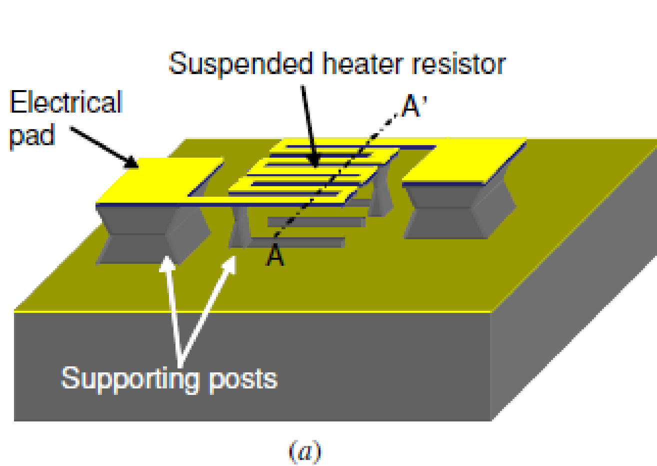
Surface MEMS: thin films etched
Bulk MEMS (=silicon wafer etching involved)

KOH or DRIE ?

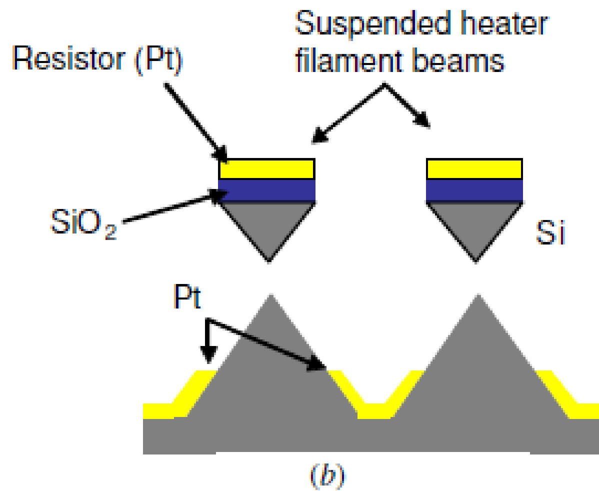
Bonding involved or not ?

In-plane or out-of-plane structures ?
Thru-wafer structures (holes)
Membrane structures (no holes)

Single litho bulk-MEMS

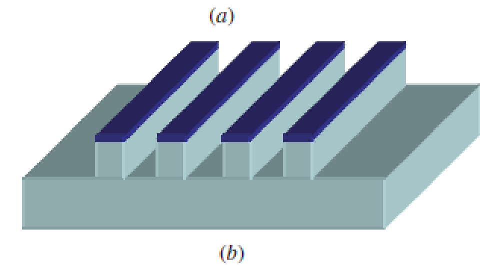


(a)



(b)

(a)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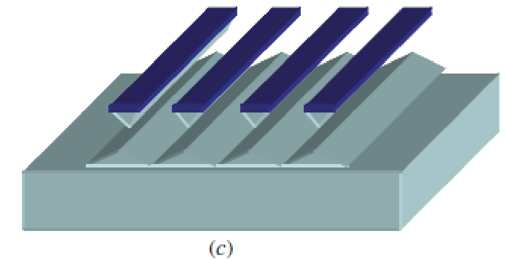
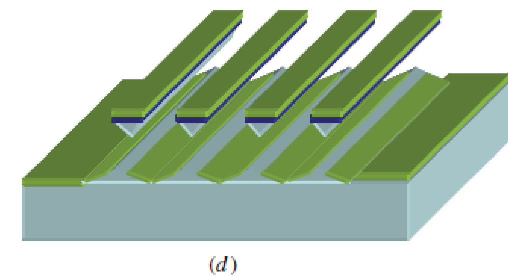
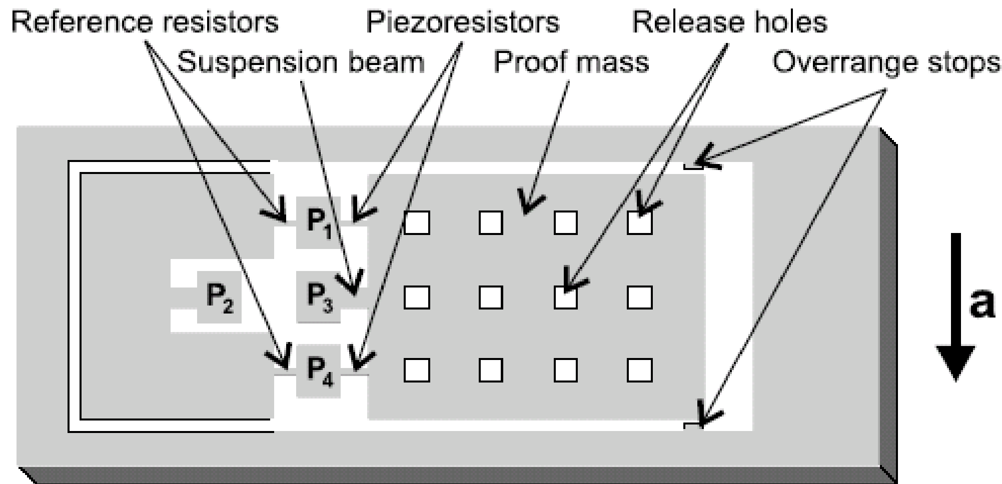

(c)


(d)

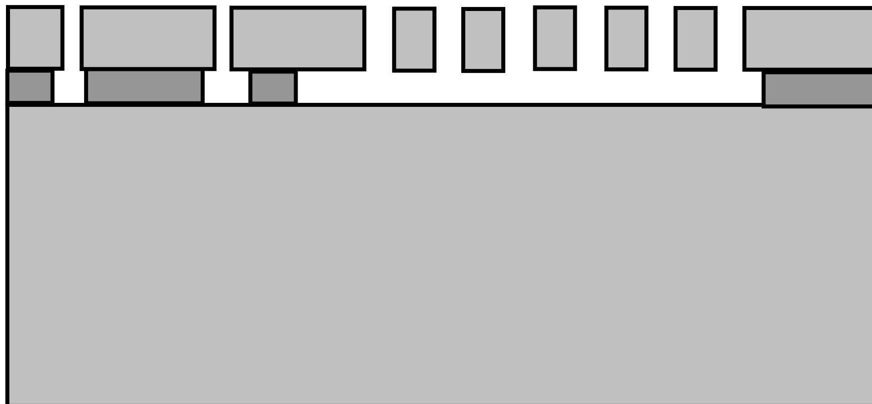
Cantilevers:
-resonant sensors
-bending sensors
-thermal isolation structures

Lee et al: http://iopscience.iop.org/0960-1317/19/11/115011)

SOI accelerometer



One-dimensional accelerometer:
P1 right-hand side piezoresistor expands,
P4 RHS resistor contracts;
left-hand sides act as reference electrodes.

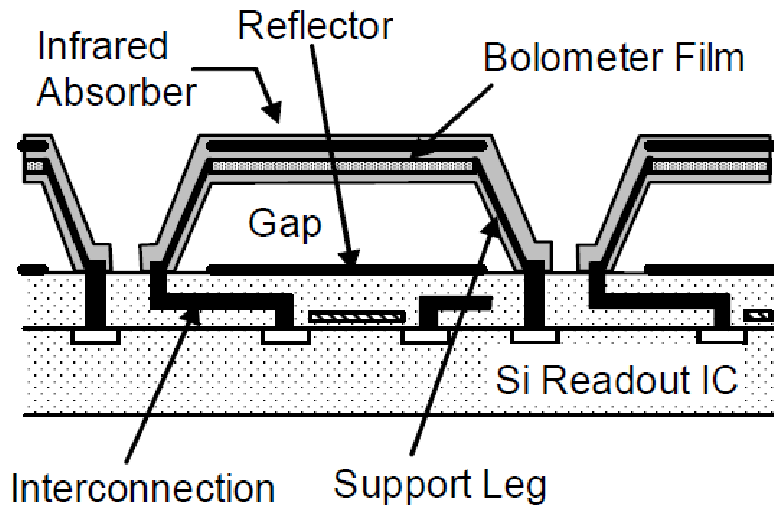


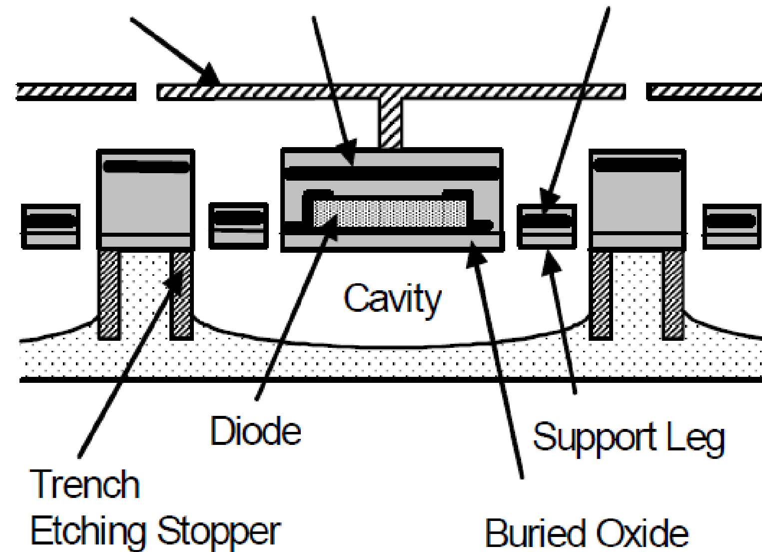
Single lithography step fabrication.

DRIE of SOI device layer.

Wet etching of buried oxide (BOX) in HF.

Surface vs. SOI-MEMS



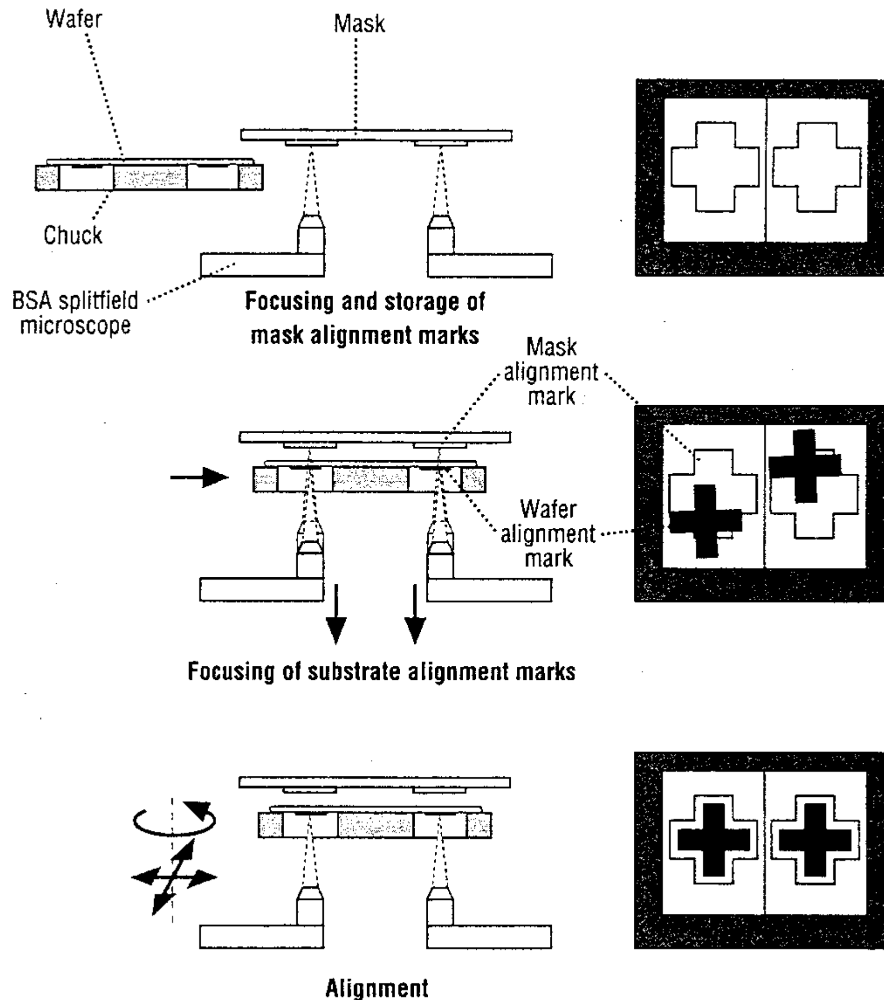


Surface MEMS: functionality is above the silicon wafer. CMOS wafer is the "passive" during MEMS fabrication, but active during device operation.

Bulk/SOI MEMS: we process the silicon itself (in this case SOI device and handle wafers are both etched)

Kimata: IEEE Transducers 2007

Double side alignment



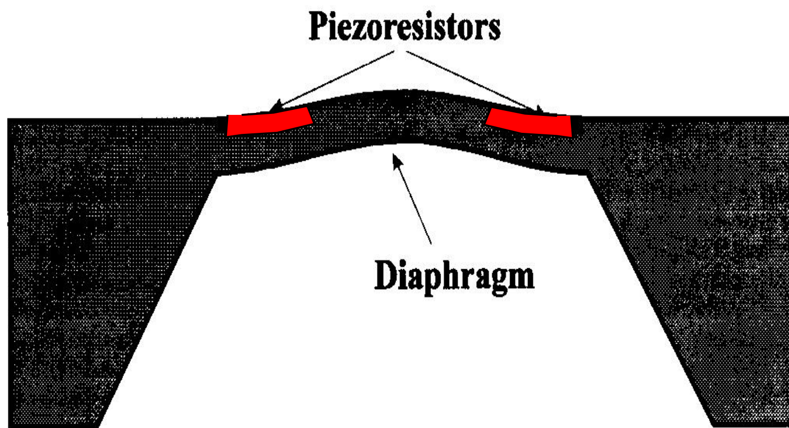
Double sided lithography requires DSP wafers

(Double Side Polished)

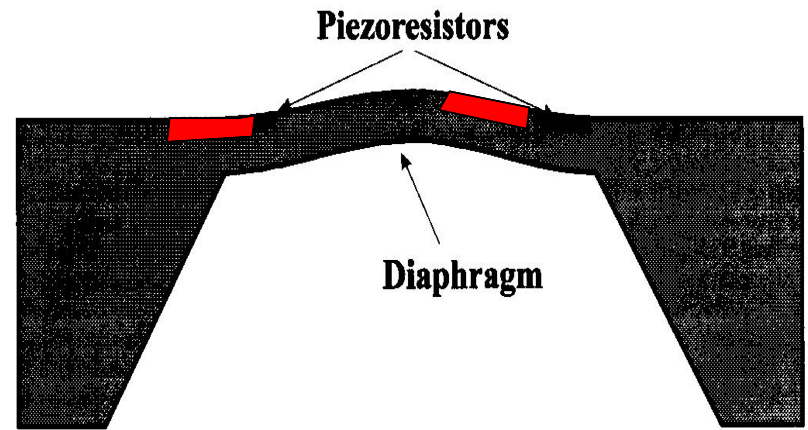
Some alignments are critical but not all !

Often the backside structures are large, and not critically aligned to top side features.

Critical backside alignment: diffused piezoresistors



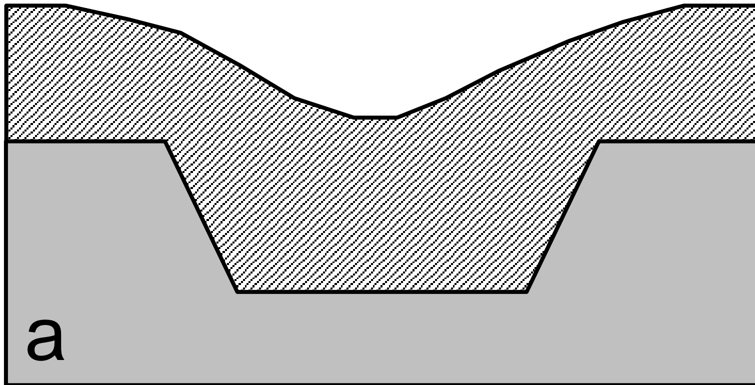
OK

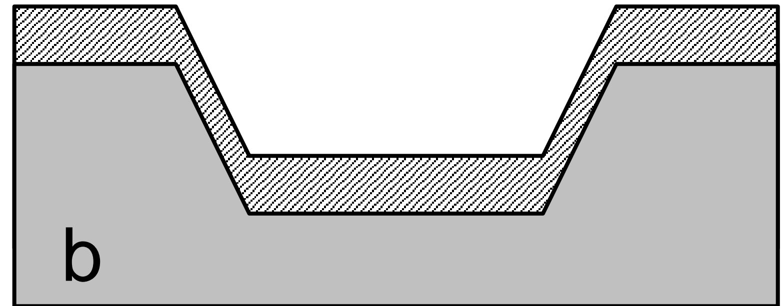


NOT OK

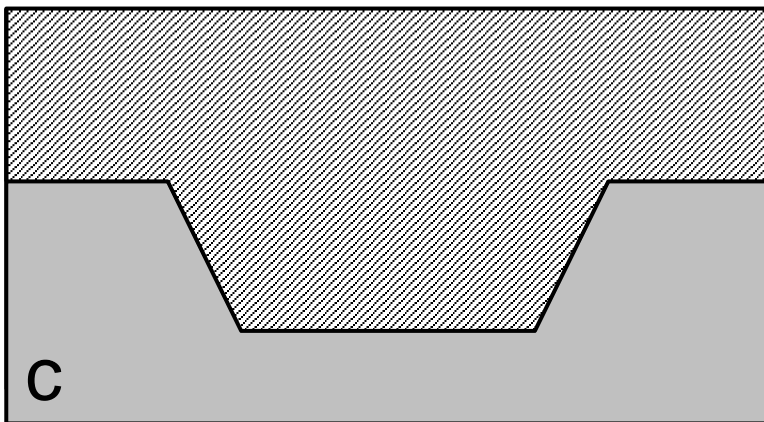
Piezoresistors have to be positioned at the maximum defelection region.

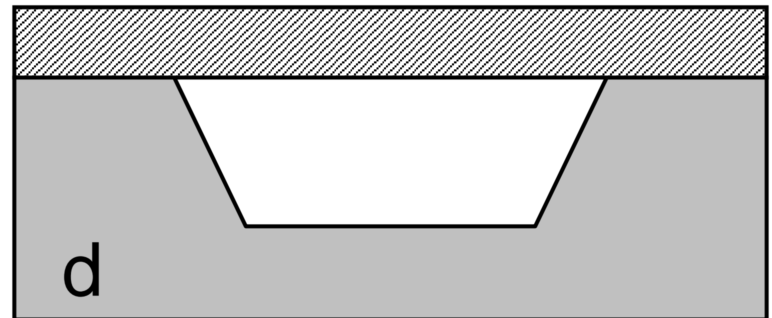
Resist over 3D topography



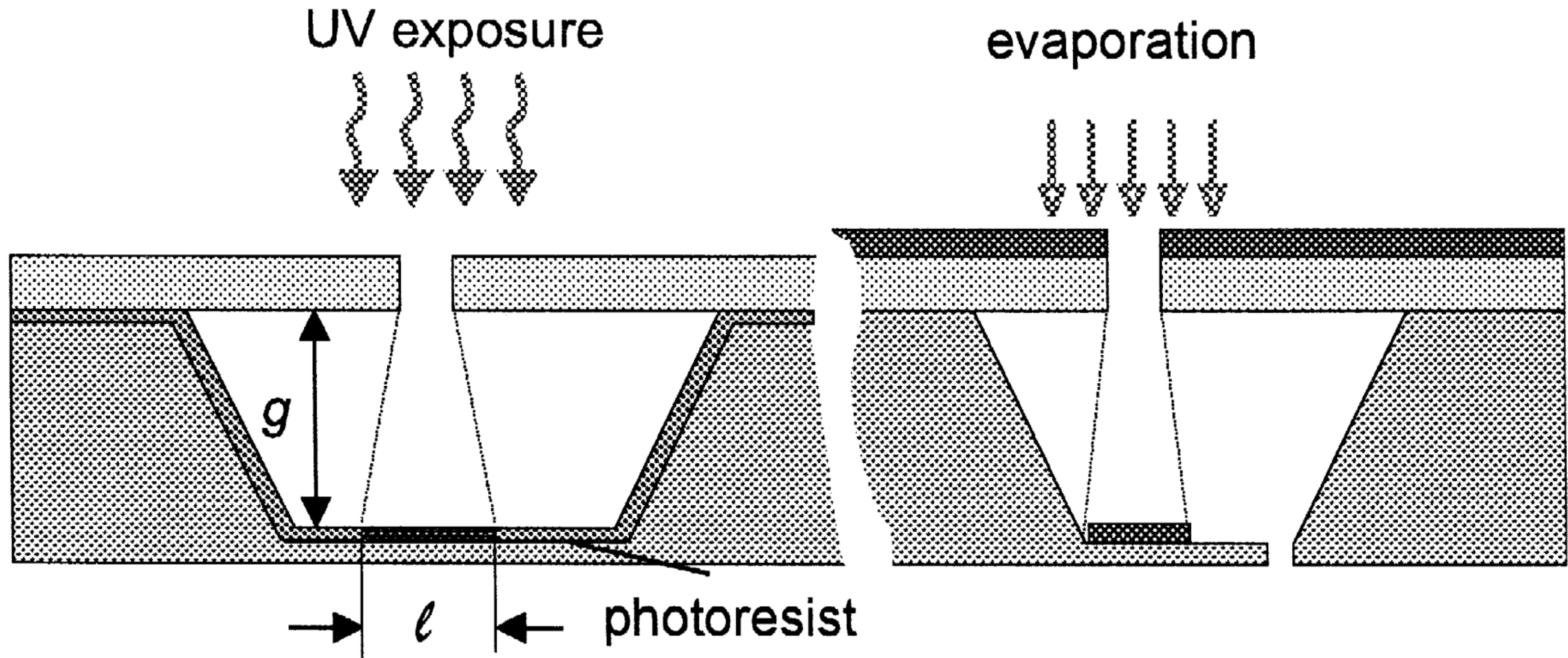


a) spin coated; b) spray coated; c) cast; d) laminated dry film.





Lithography over topography



Sensors and Actuators 76 1999. 329–334

Peeling masks: two masks before etch

Litho 1 + etch mask material 1
Litho 2, still planar surface
Etch 1 using mask 1
Remove mask 1
Etch 2 using mask 2

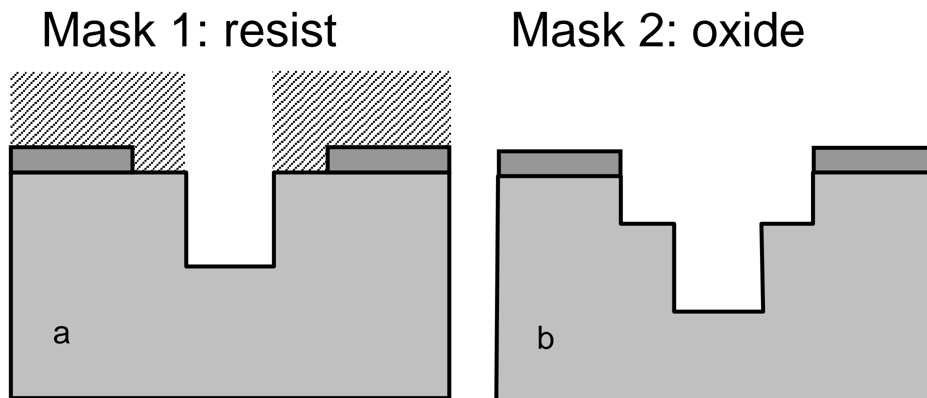
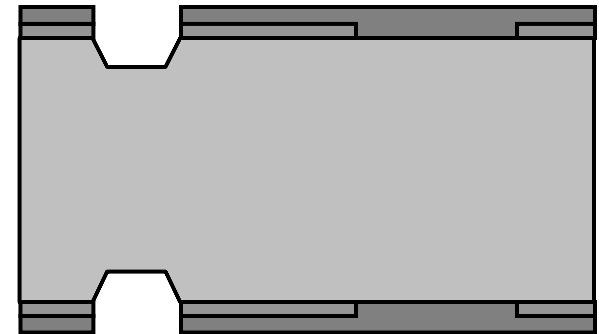


Fig. 21.17

Mask 1: oxide
Mask 2: nitride



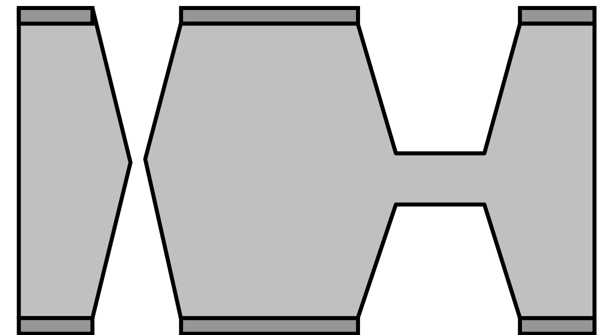


Figure 20.4

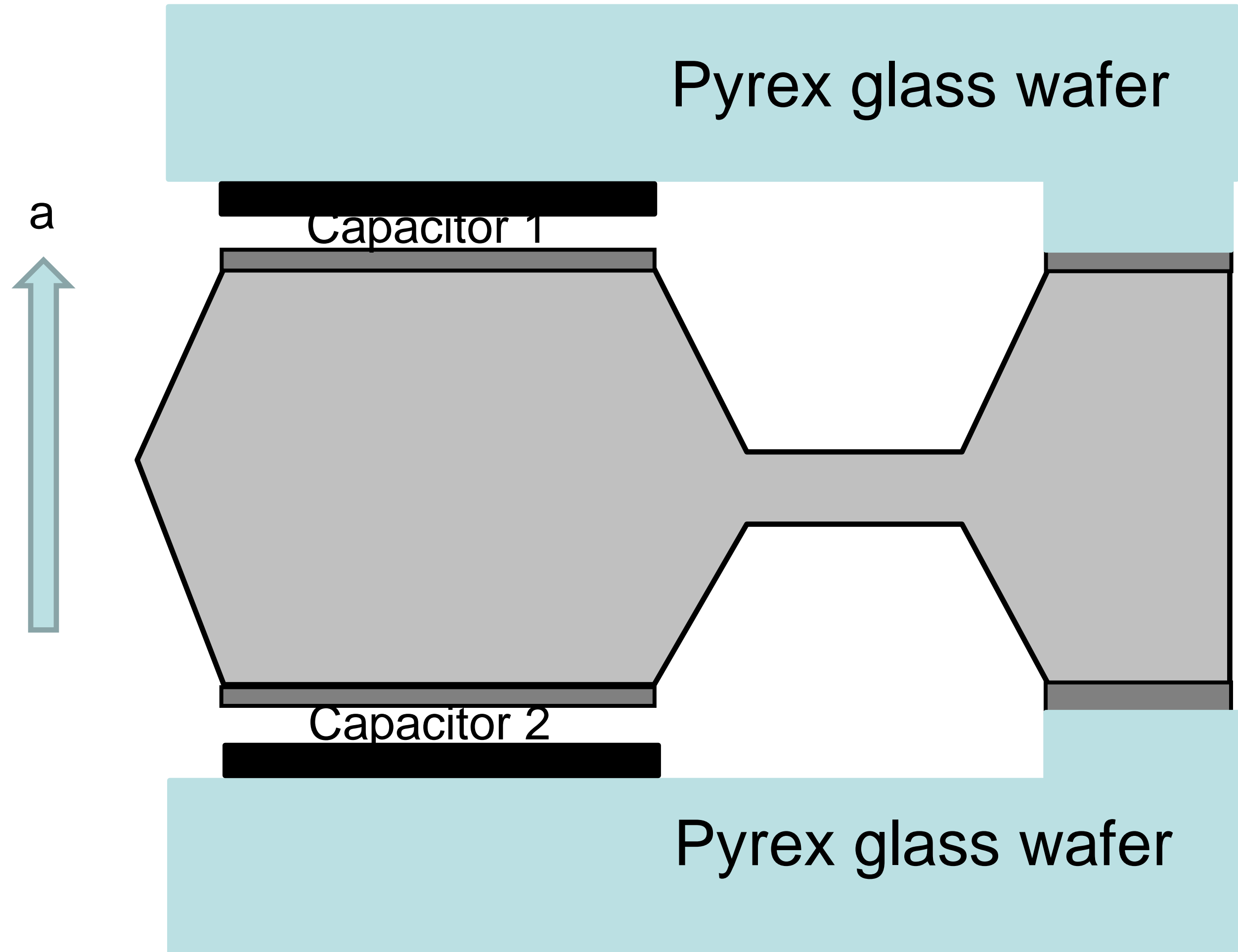
Also known as nested mask

Capacitive accelerometer

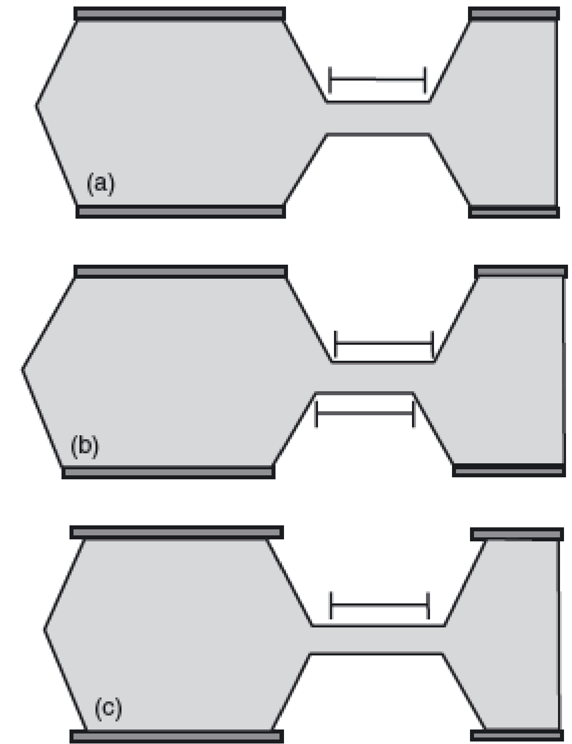
Capacitance 1 increases because gap smaller

Large differential capacitance

Capacitance 2 decreases because gap larger



Bulk MEMS, wet etching



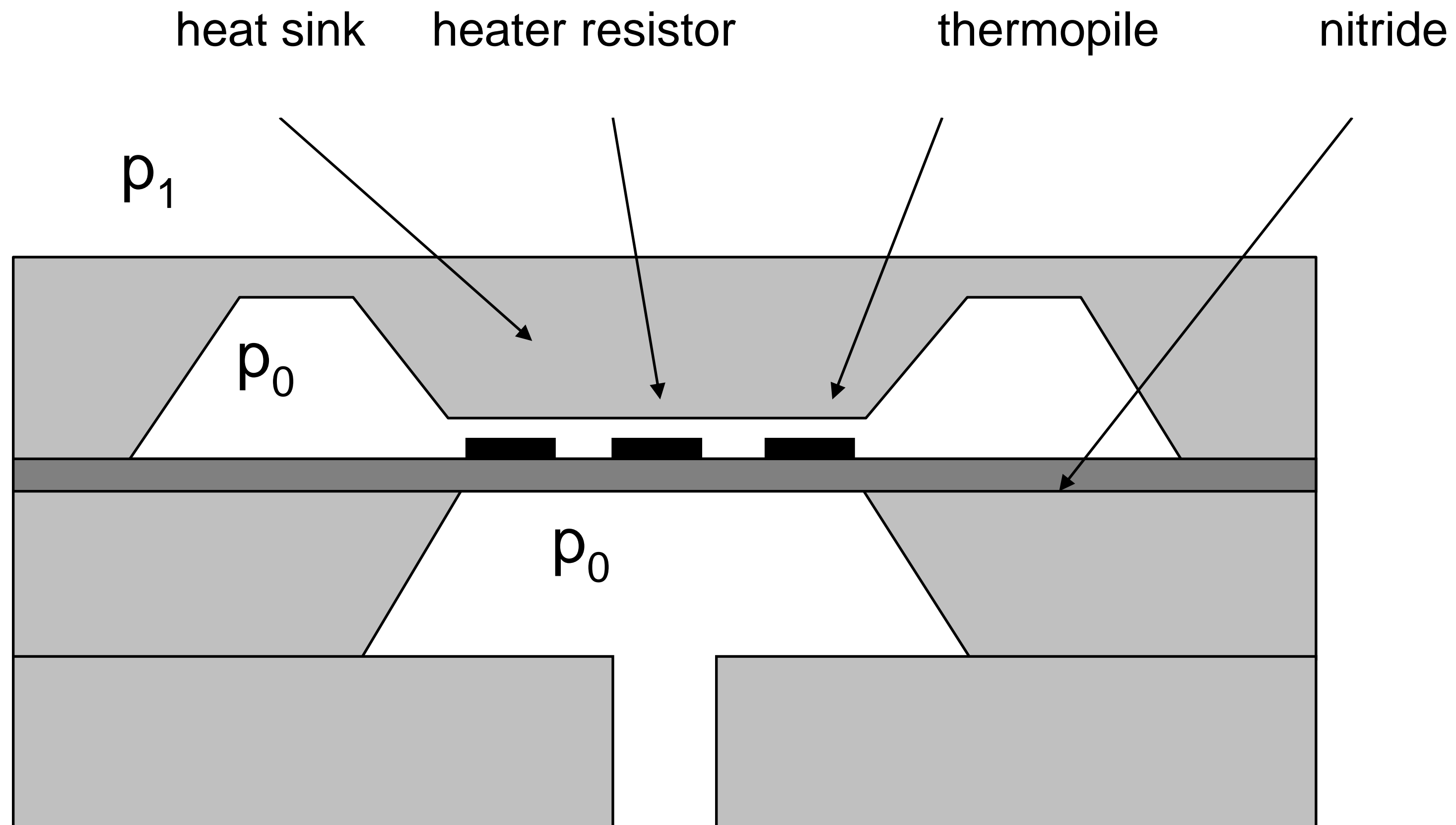
Accelerometer courtesy Murata

Pressure sensor deflection

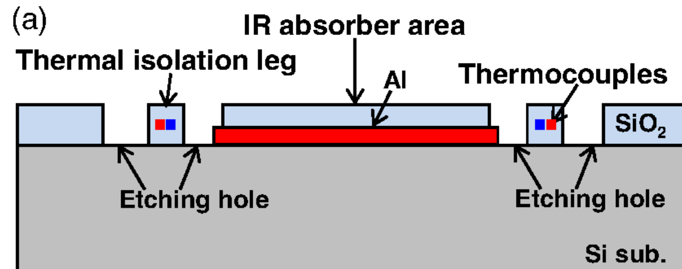
Simple membrane
➔ Not a parallel plate capacitor

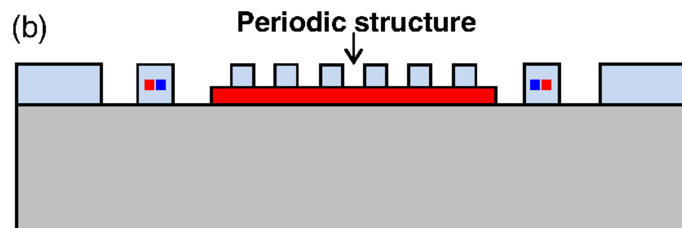
Hinged membrane:
➔ Parallel plate capacitor

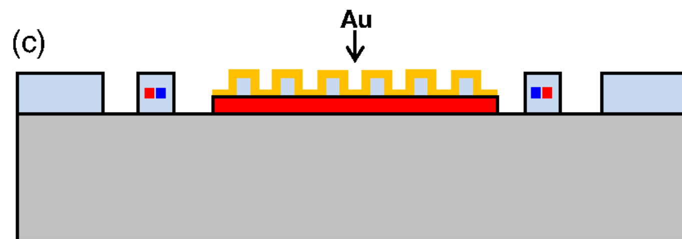
Thermal pressure sensor

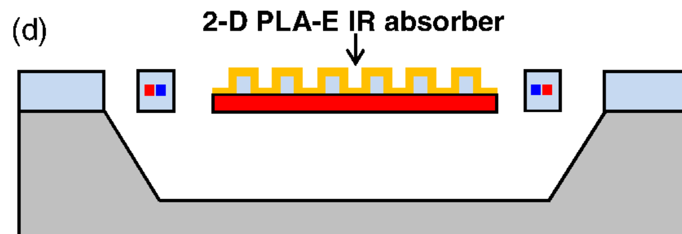


Bulk-MEMS with surface functionality







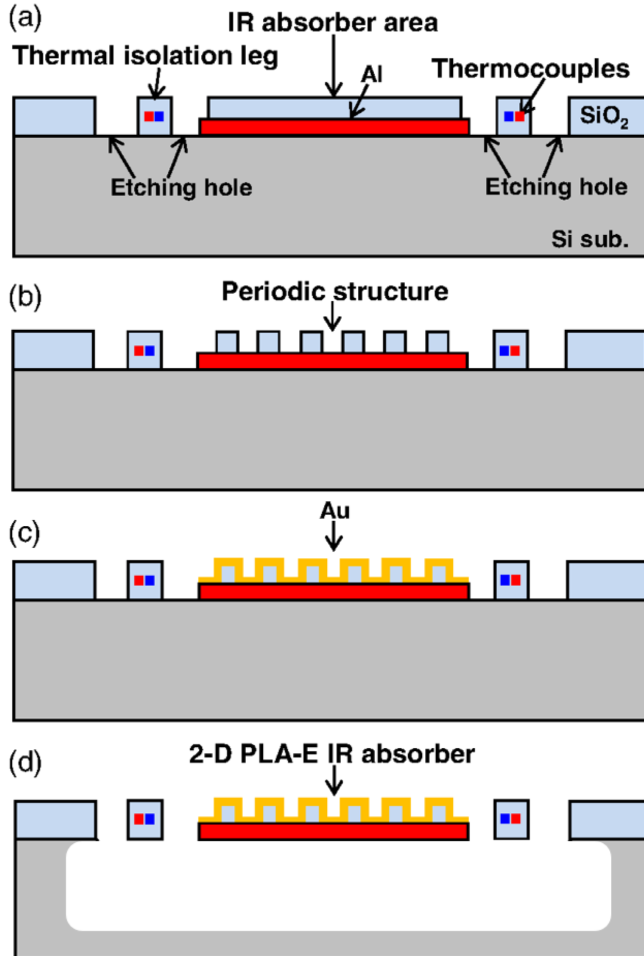


Bulk silicon etching is used to thermally isolate surface-MEMS functionality.

Etch selectivity between Si and Al: use TMAH etchant

Ogawa, Masuda, Takagawa, Kimata:
Opt. Eng. 53(10), 107110 (2014)

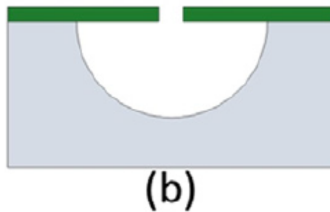
Wet vs. dry Si etch

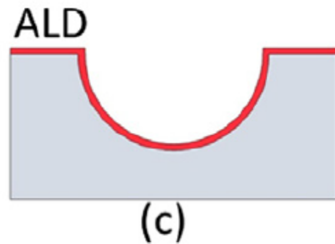


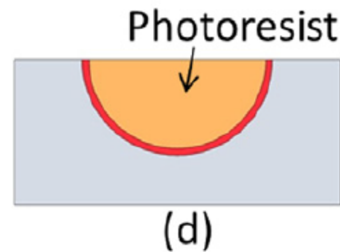
Isotropic silicon etch, SF_6 plasma, or XeF_2, selective against metals and SiO_2.

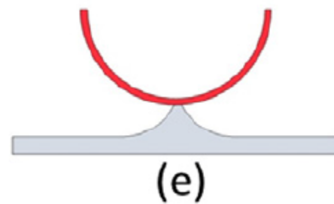
Ogawa, Masuda, Takagawa, Kimata: *Opt. Eng*. 53(10), 107110

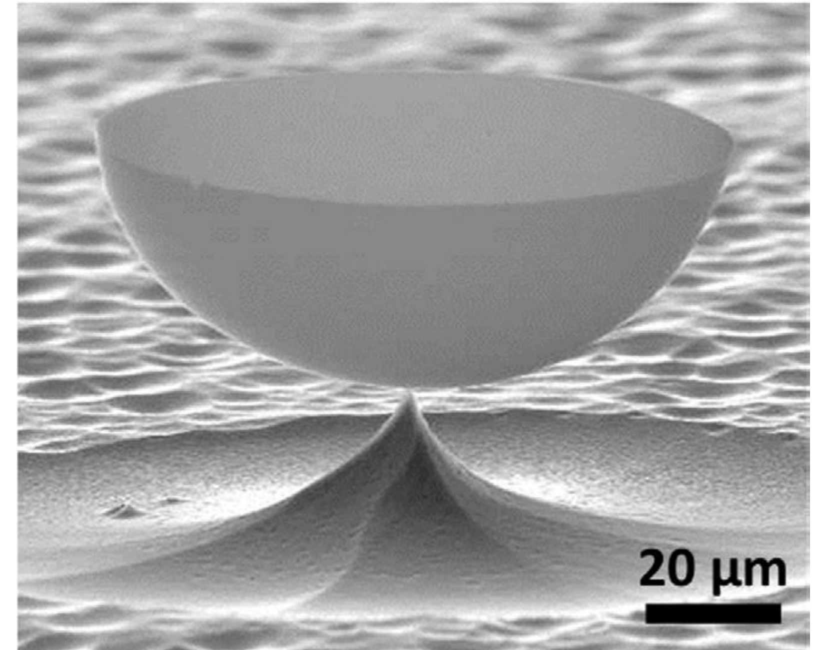
Hemispherical shapes











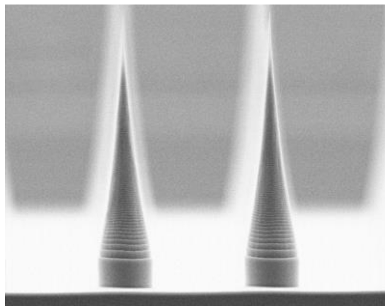
Wine-glass mode resonator

It is really difficult to get exactly hemispherical shape !

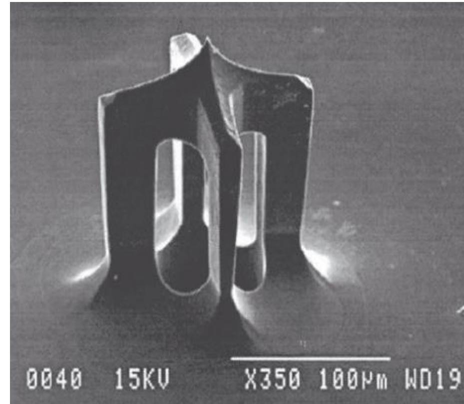
Gray et al: J. Micromech. Microeng. 24 (2014) 125028 (9pp)

Out-of-plane needles

Micralyne

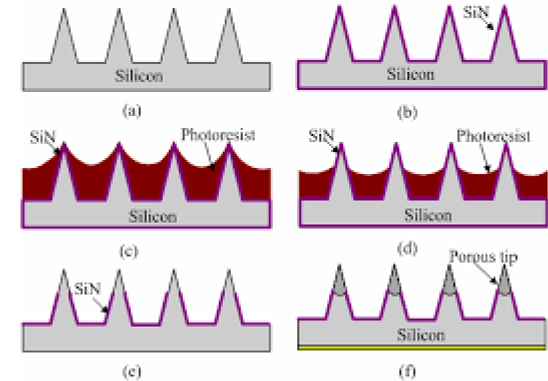


Solid silicon needles



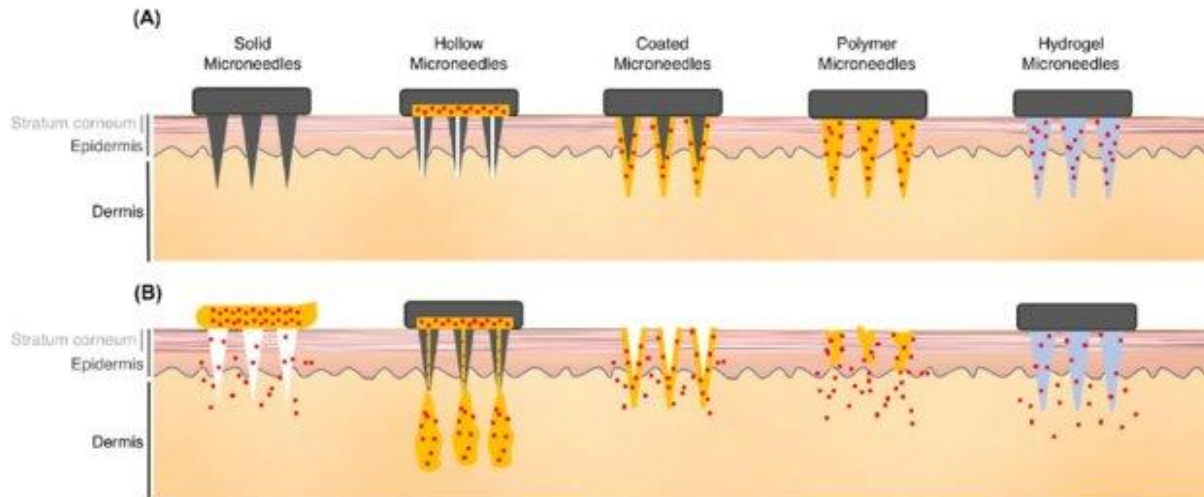
Griss & Stemme

Hollow silicon needles



Porous tip silicon needles

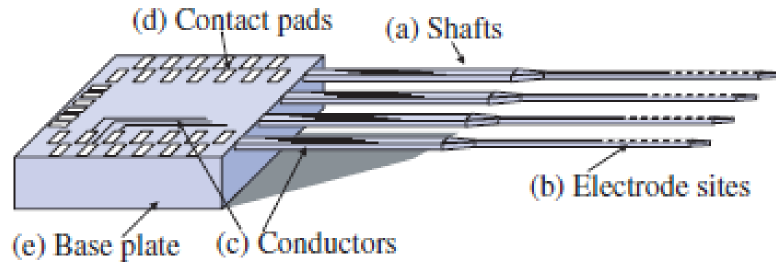
Jing Ji et al 2006
J. Phys.: Conf. Ser. 34 1127



Transdermal drug delivery systems for fighting common viral infectious diseases

- DOI:
- 10.1007/s13346-021-01004-6

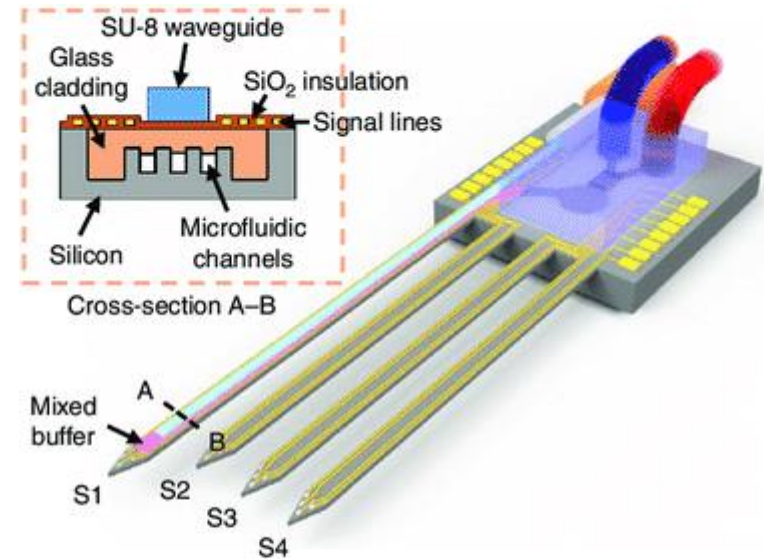
In-plane needle on SOI



Electrophysiological measurements (brain electrical signaling)

J. Micromech. Microeng. 12 (2002) 414–419

P Norlin *et al*

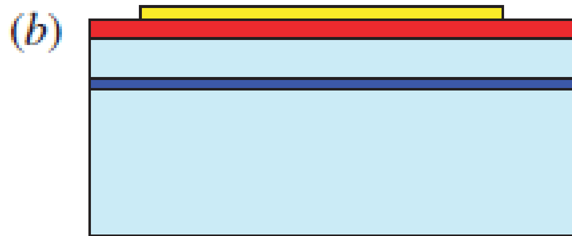


Neural probe with an optical waveguide for optical stimulation, microfluidic channels for drug delivery, and microelectrode arrays for recording neural signals

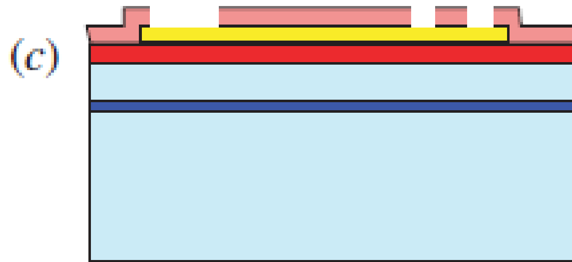
Nature Communications 10(1)
DOI: 10.1038/s41467-019-11628-5

SOI wafer

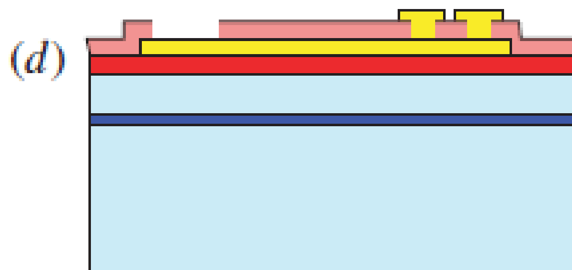
Thermal oxide and metal wiring

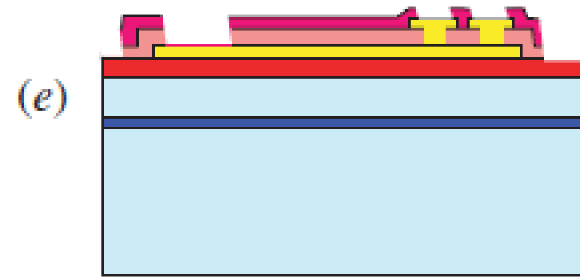


CVD oxide passivation and contact hole opening

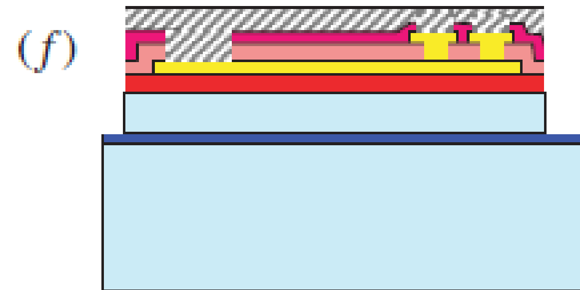


Pt for sensor metal (bio-compatible)

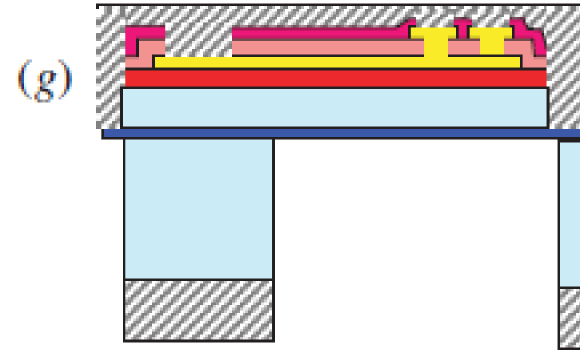




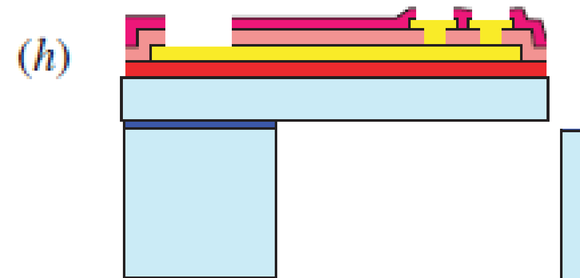
Passivation CVD oxide



Front side protection and oxide & Si etch



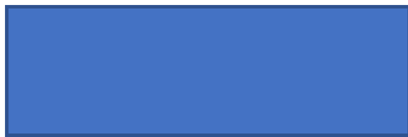
Backside litho & DRIE



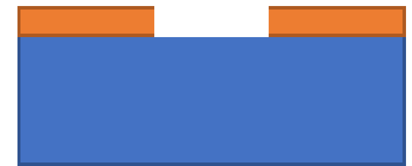
Remove protection and etch BOX

Norlin et al: J. Micromech. Microeng. **12** (2002) 414–419

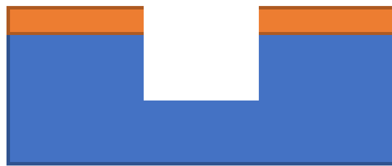
Cavity-SOI (C-SOI)



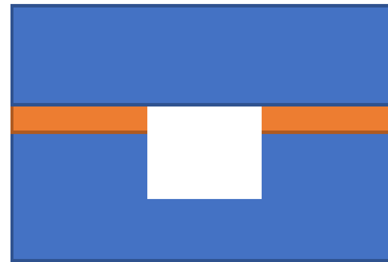
Thermal oxidation



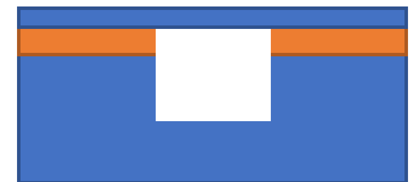
Lithography + ox etch



Si DRIE

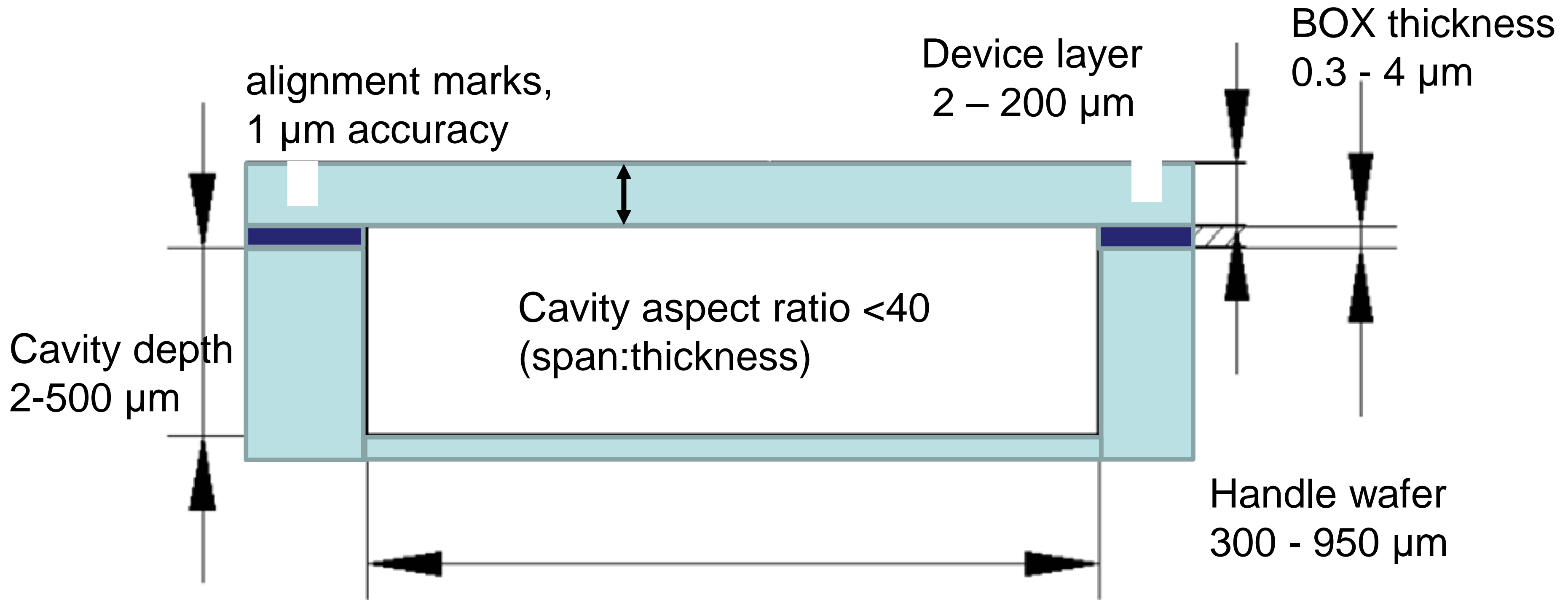


Direct bonding + anneal

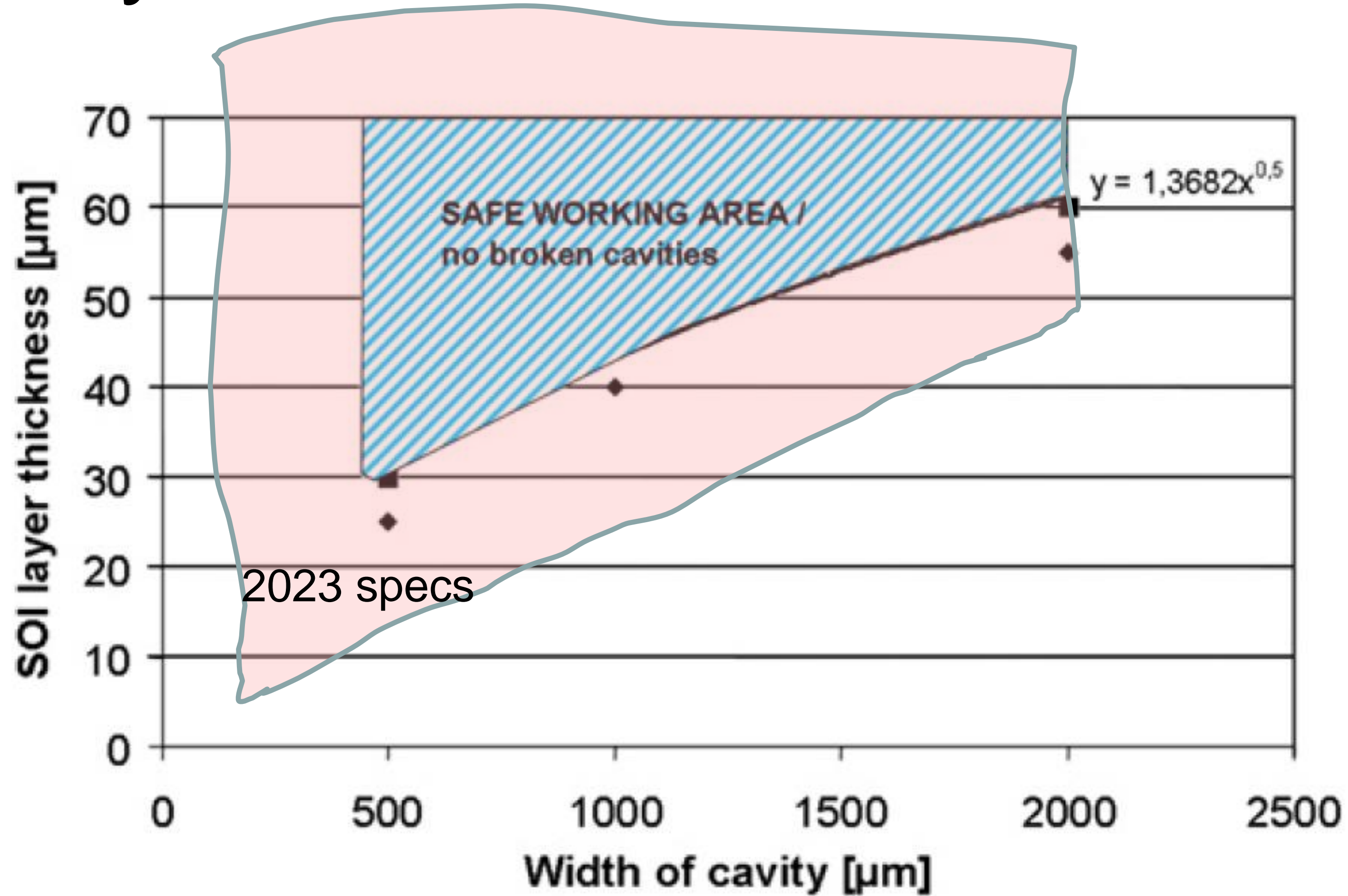


Grind or etch
+ CMP

C-SOI specifications

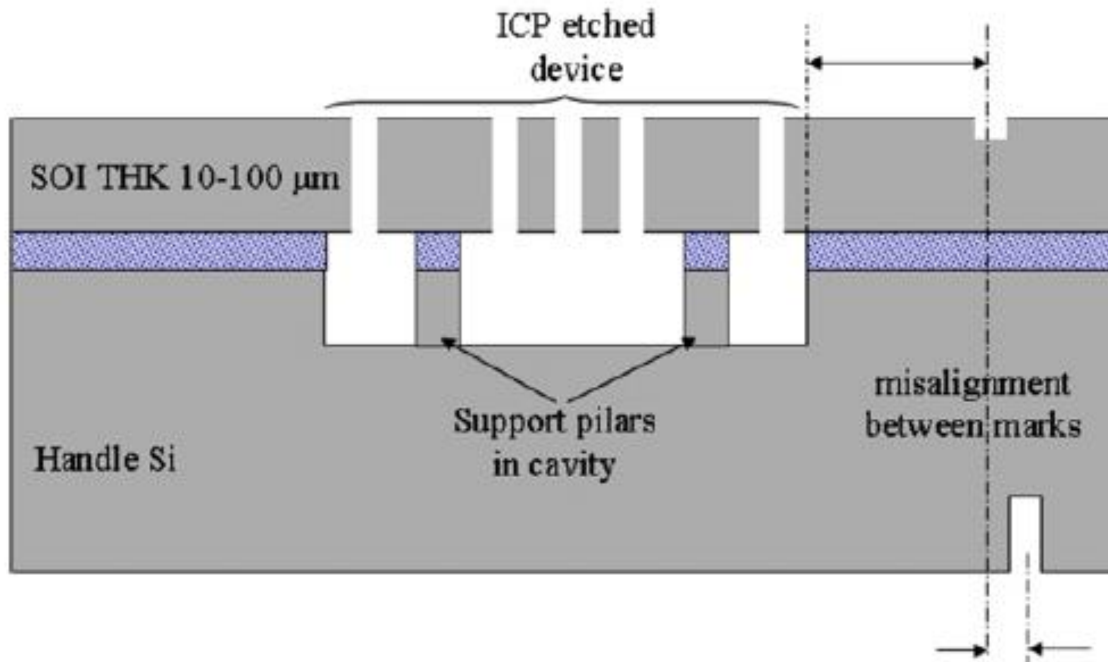


Cavity dimensions vs. SOI thickness



Luoto et al. "MEMS on cavity-SOI wafers." *Solid-State Electronics* 51.2 (2007): 328-332.

C-SOI MEMS benefits



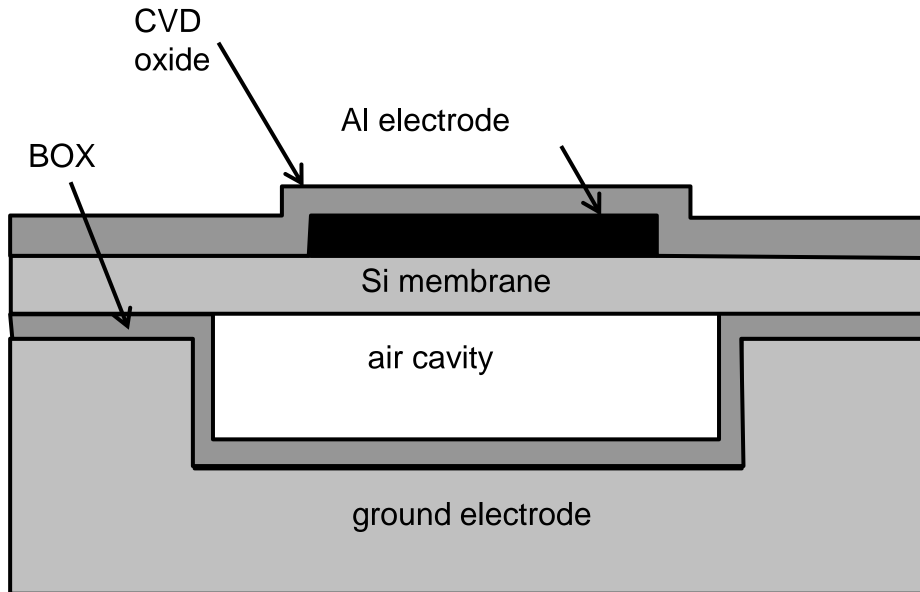
High quality single crystal silicon of device layer as mechanical material, as in SOI always.

Reduce number of process steps.

No wet etching, no surface tension and drying effects in small cavities.

Solid-State Electronics 51 (2007) 328–332

Cavity-SOI resonator

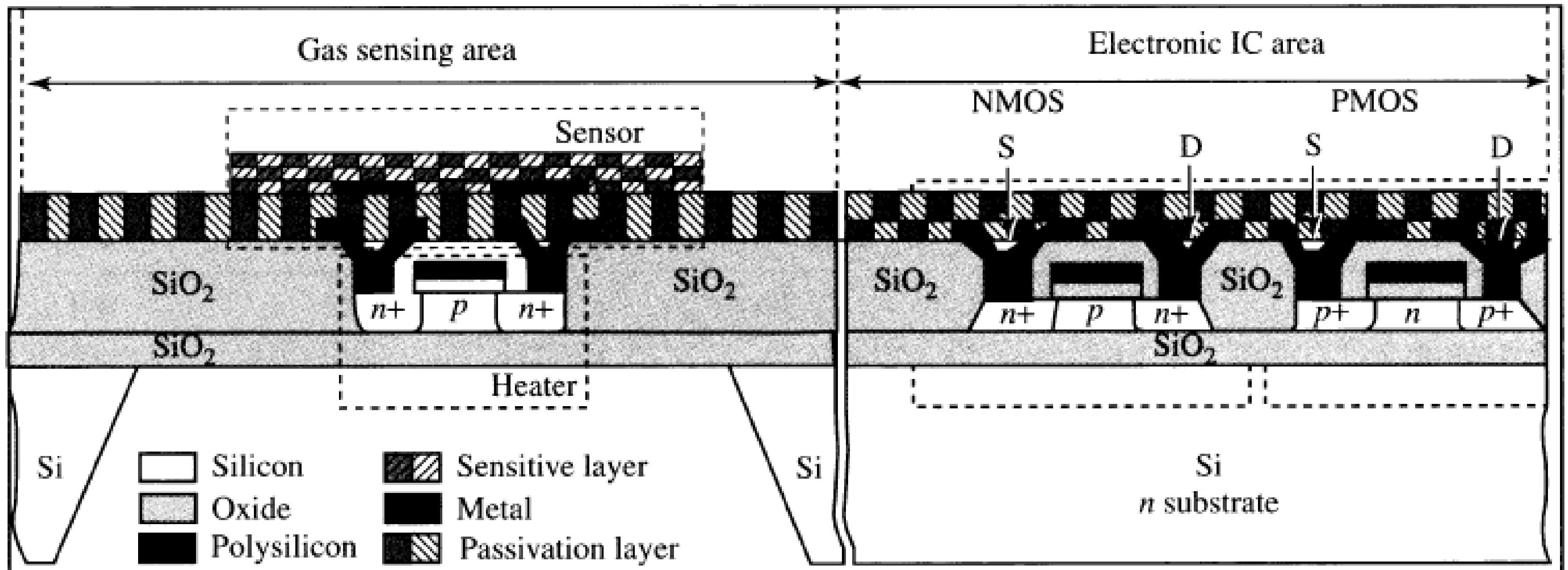


1. Al sputtering
2. Litho
3. Al etch & strip
4. CVD oxide
5. Litho & contact hole etch

CMOS-MEMS integrated

- CMOS first
  - MEMS in silicon
  - MEMS in IC thin films
  - MEMS thin films specifically
- MEMS first
  - plug-up SOI
  - polysilicon thin film MEMS
- Integrated processes

Integrated hot plate sensor



CMOS first + bulk MEMS

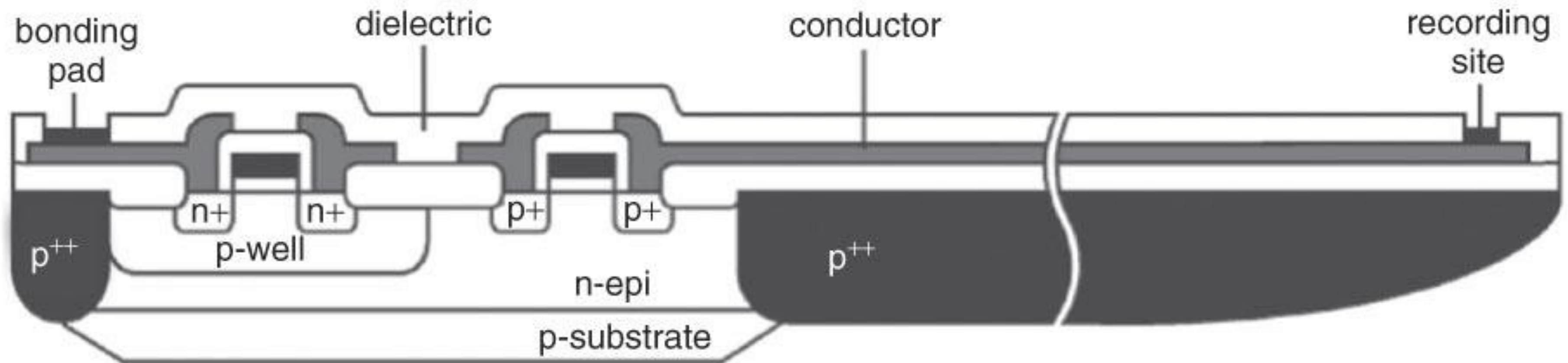


Figure 30-13

In-plane integrated CMOS microneedle for electrophysiological measurements by Ji and Wise (1992). Reproduced from Brand (2006), copyright 2006, by permission of IEEE.

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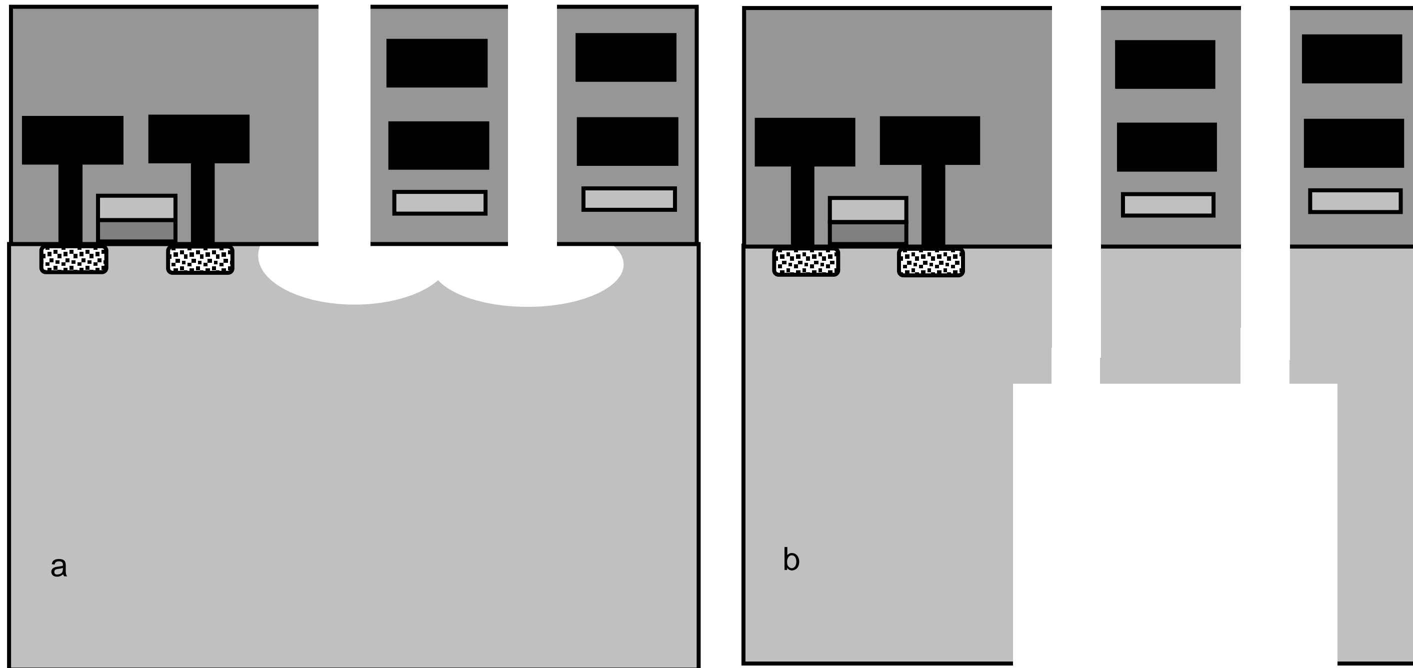
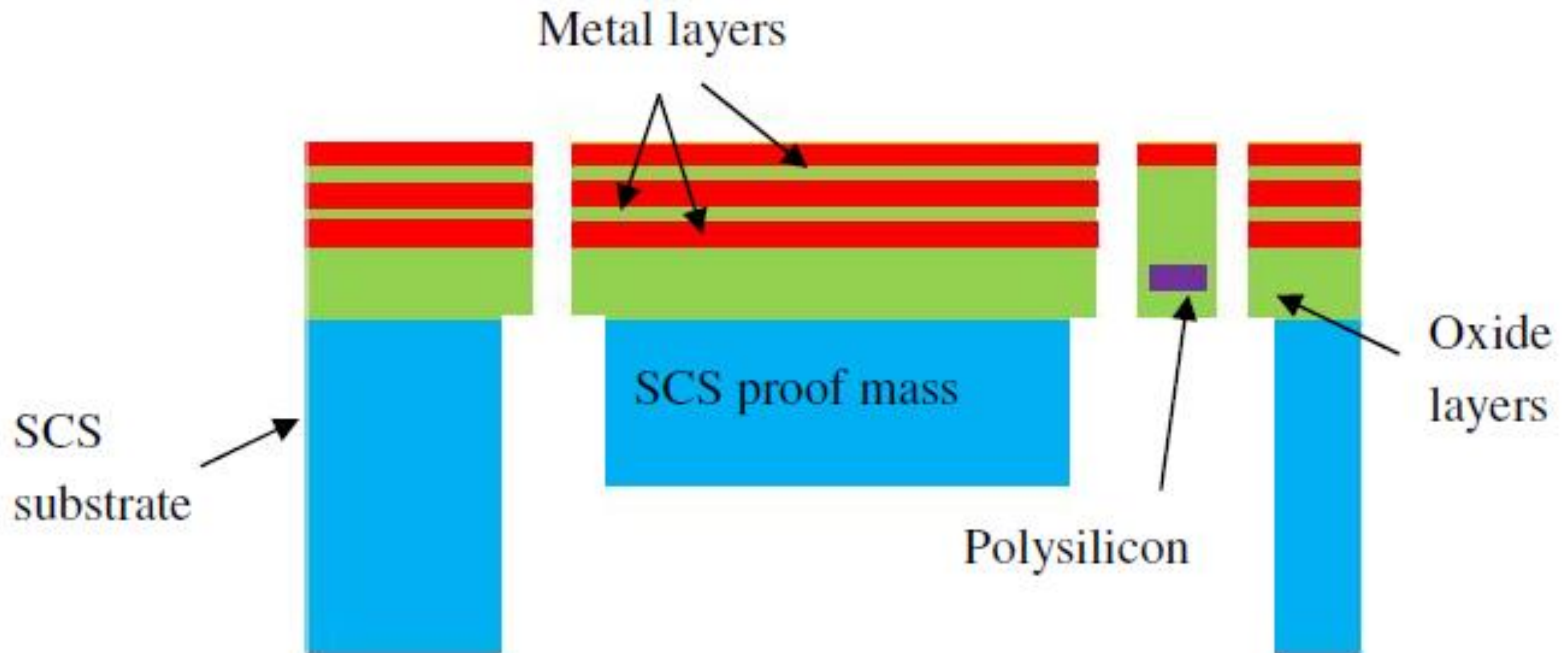
CMOS first, no additional films



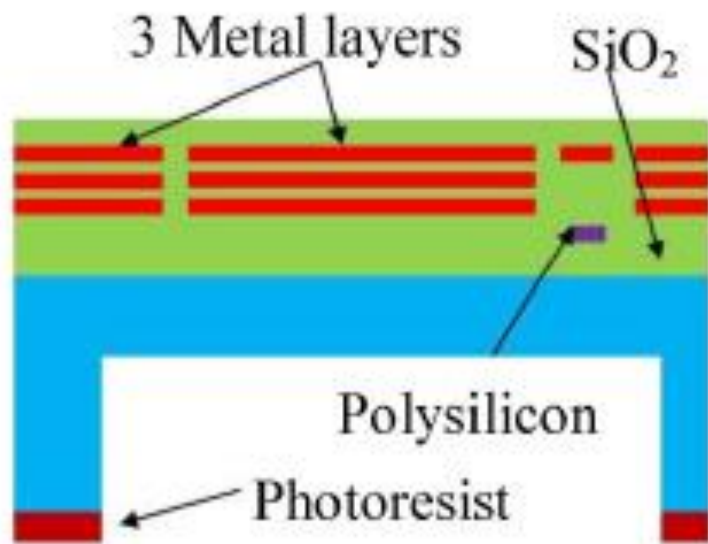
a) thin film MEMS by front side dry plasma release;

b) single crystal silicon MEMS byDRIE

CMOS-MEMS Piezoresistive Accelerometer

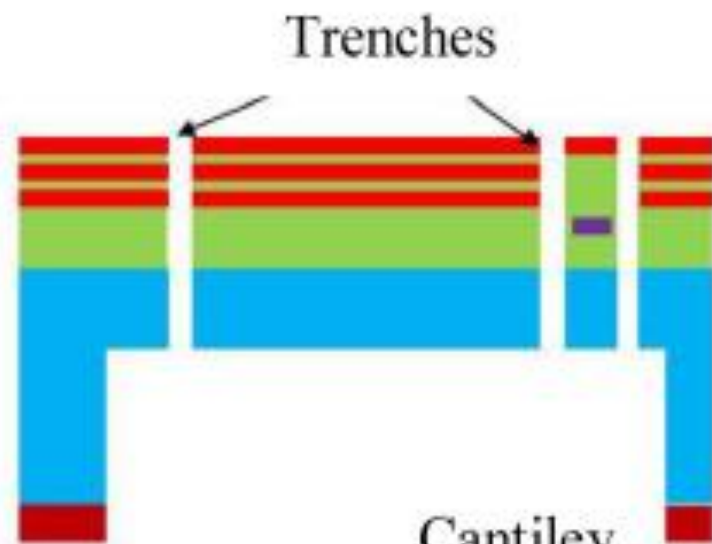


Khir *Sensors* **2011**, *11*, 7892-7907;

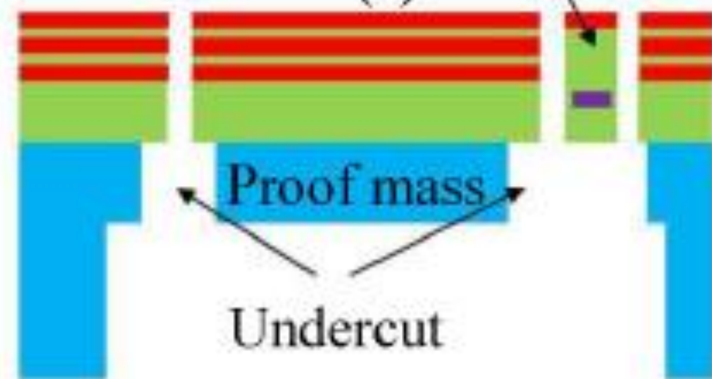


(a)

(b)



(c)



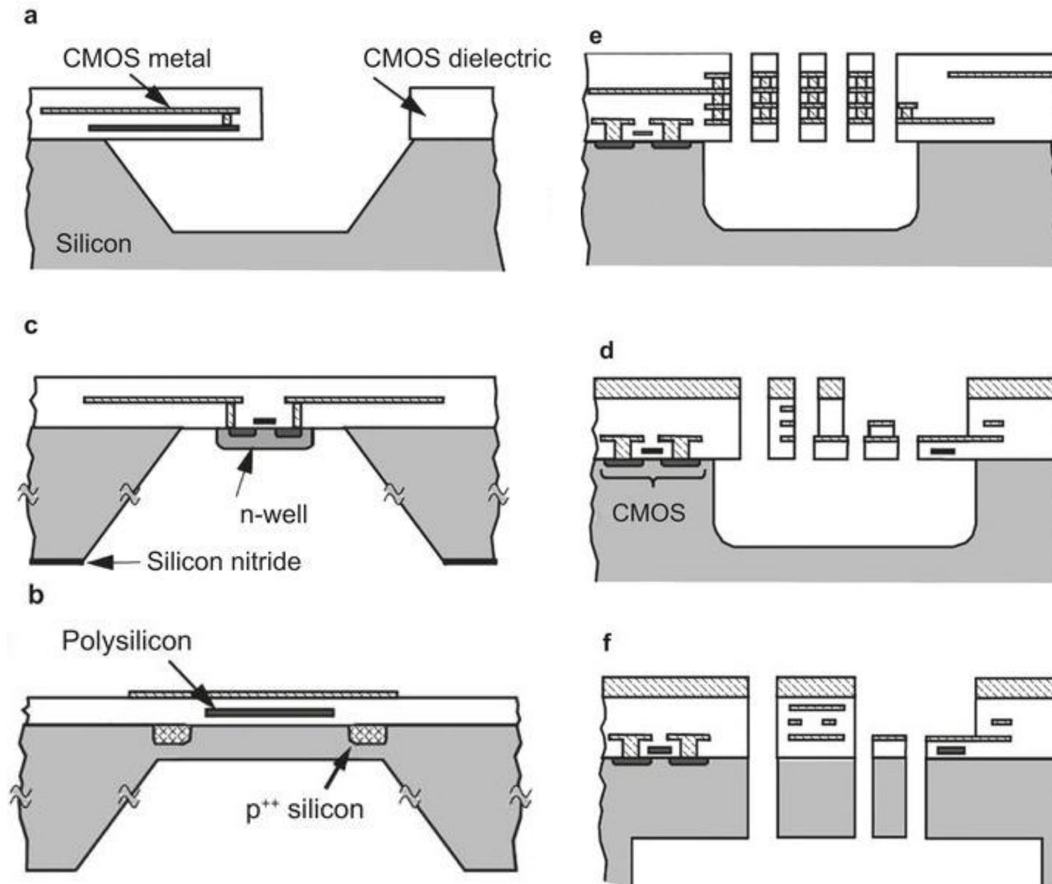
(d)

CMOS-MEMS in six ways

Bulk-MEMS

Design of MEMS elements separate from CMOS.

Separate process steps for MEMS.



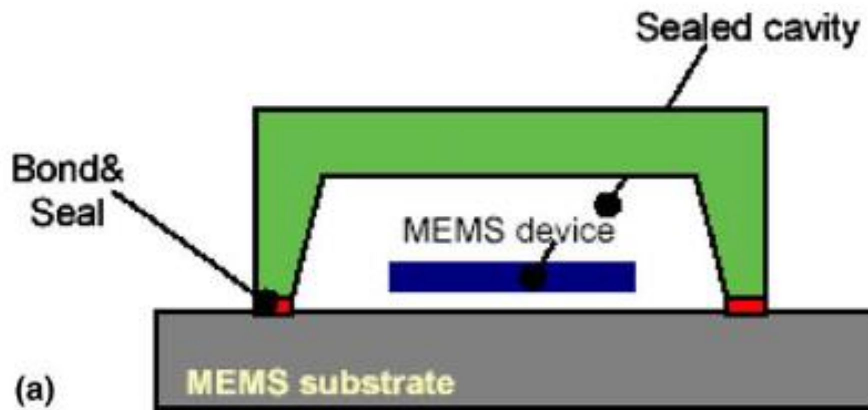
Bulk or SOI-MEMS

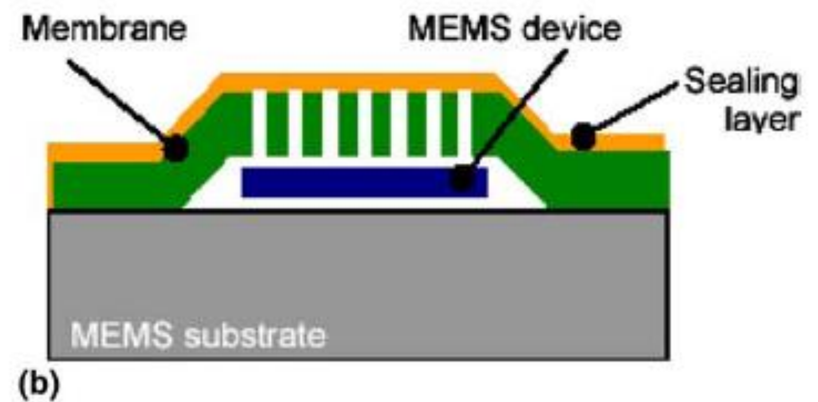
Design of MEMS elements is part of CMOS design.

MEMS and CMOS use same thin films.

https://media.nature.com/m685/nature-assets/micronano/2015/micronano20155/images_hires/micronano20155-f10.jpg

MEMS packaging





Capping wafer

Thin film sealing

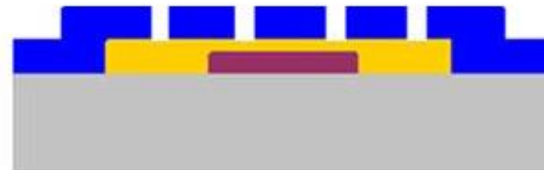
A. Witvrouw et al. / Microelectronic Engineering 76 (2004) 245–257

Zero-level package by thin films

(a) MEMS structure fabrication.

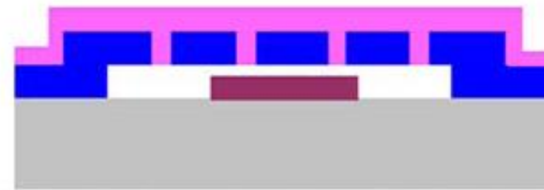
(b) Sacrificial layer deposition above MEMS.

(c) First thin film packaging layer deposition.

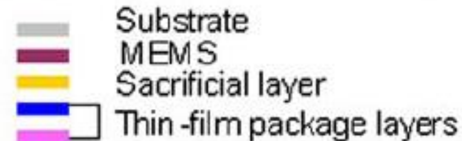


(d) Etching holes on the first thin film packaging layer.

(e) Releasing the sacrificial layer.



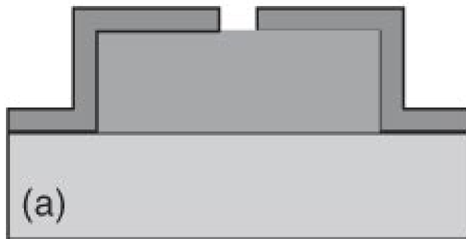
(f) Sealing the package by another thin film layer.

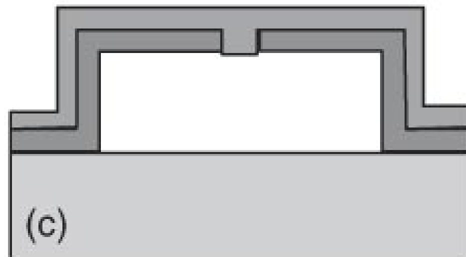


Qian Li · Hans Goosen · Fred van Keulen · Joost van Beek · Guoqi Zhang

Packaging by deposition

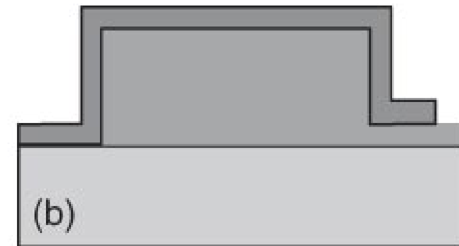
Release hole defined by lithography

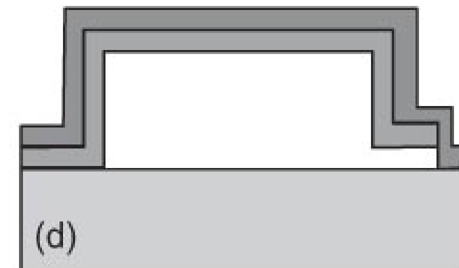




Conformal deposition of sealing material required.

Release hole defined by thin film deposition





Conformality of sealing material deposition not required.

Introduction to Microfabrication Sami Franssila
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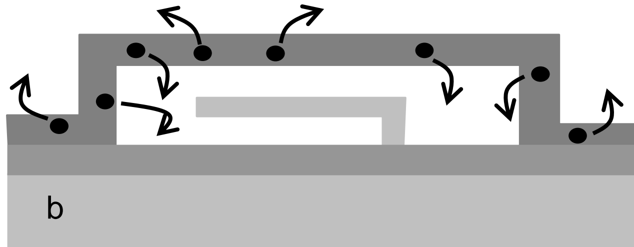
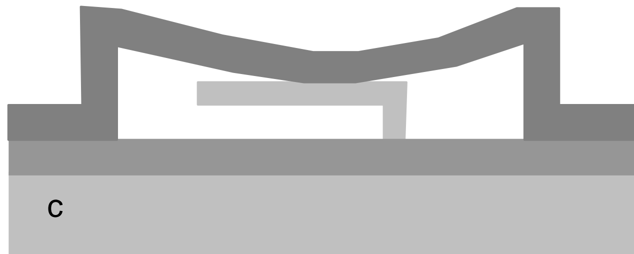
Problems with thin film roofs

a) cracks

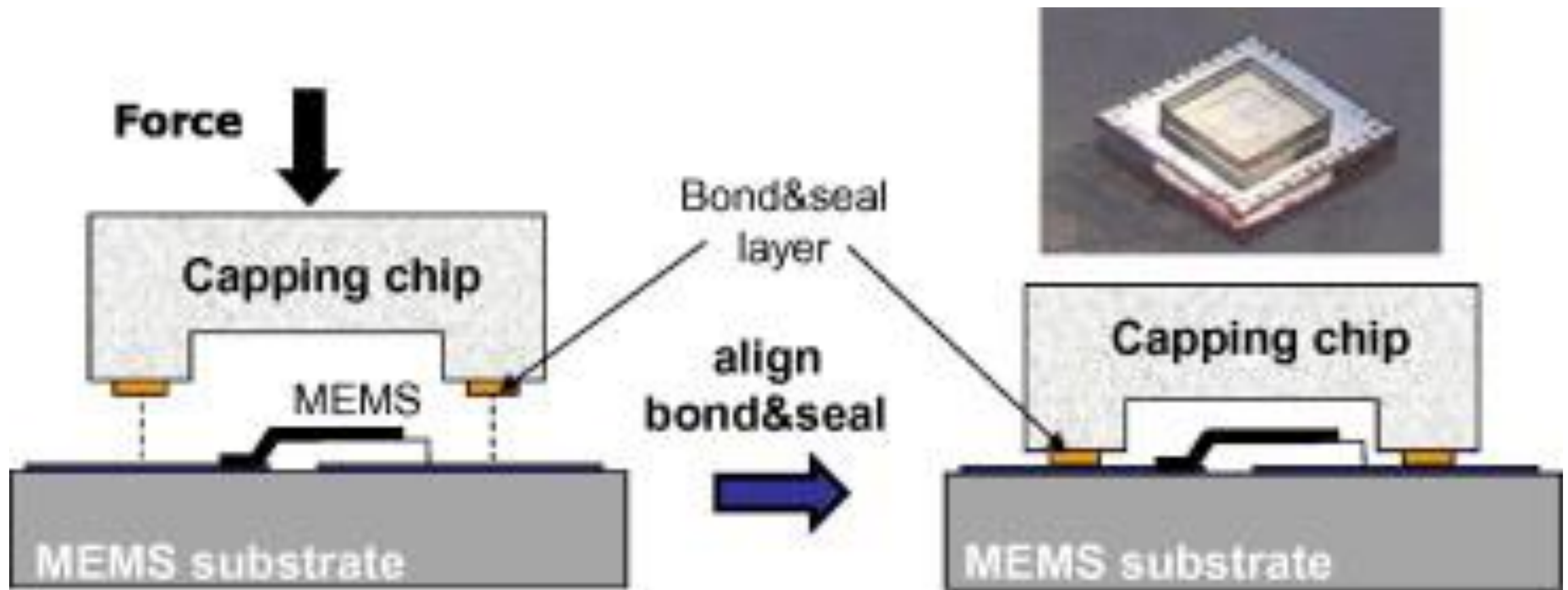


b) outgassing



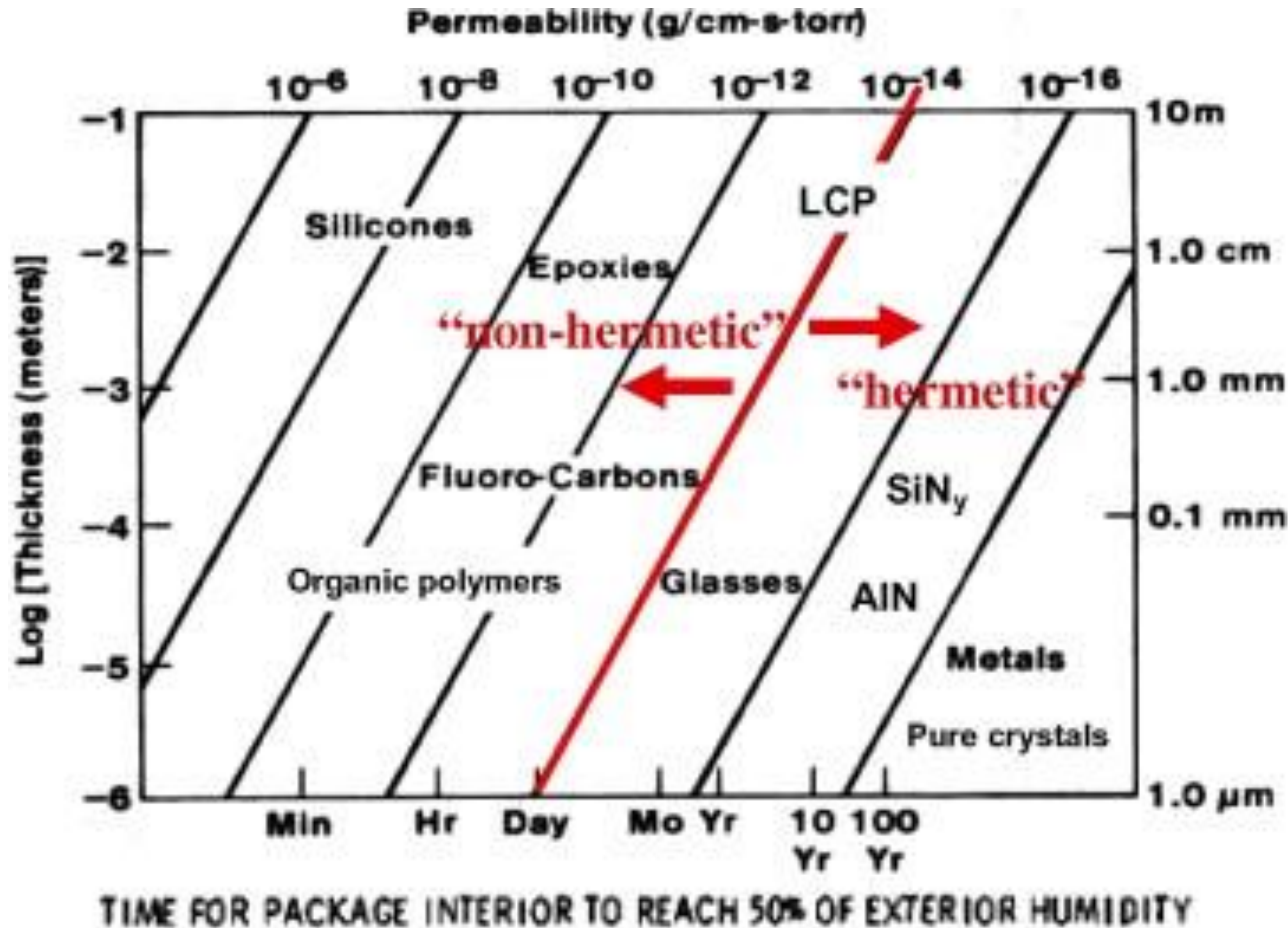
c) collapse

Zero-level package by bonding



Tilmans, Witvrouw: Microel. Rel. 2012, https://doi.org/10.1016/j.microrel.2012.06.029

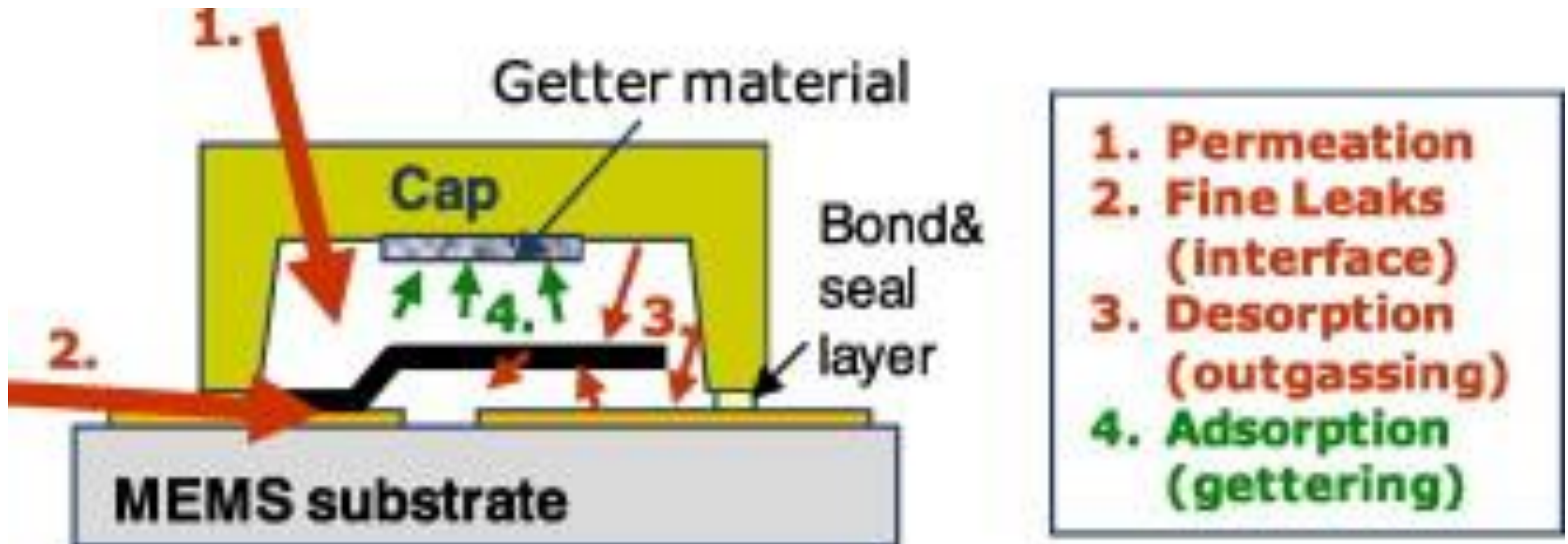
Hermeticity



Tilmans, Witvrouw: Microel. Rel. 2012, https://doi.org/10.1016/j.microrel.2012.06.029

Gettering

Removal of residual gas from a partial vacuum by use of a getter. Getters are reactive metals, e.g. titanium, which readily reacts with oxygen, forming solid TiO_2, and lowering pressure.



Tilmans, Witvrouw: Microel. Rel. 2012, https://doi.org/10.1016/j.microrel.2012.06.029