Surface MEMS
(based on chapter 29)
with audioclips

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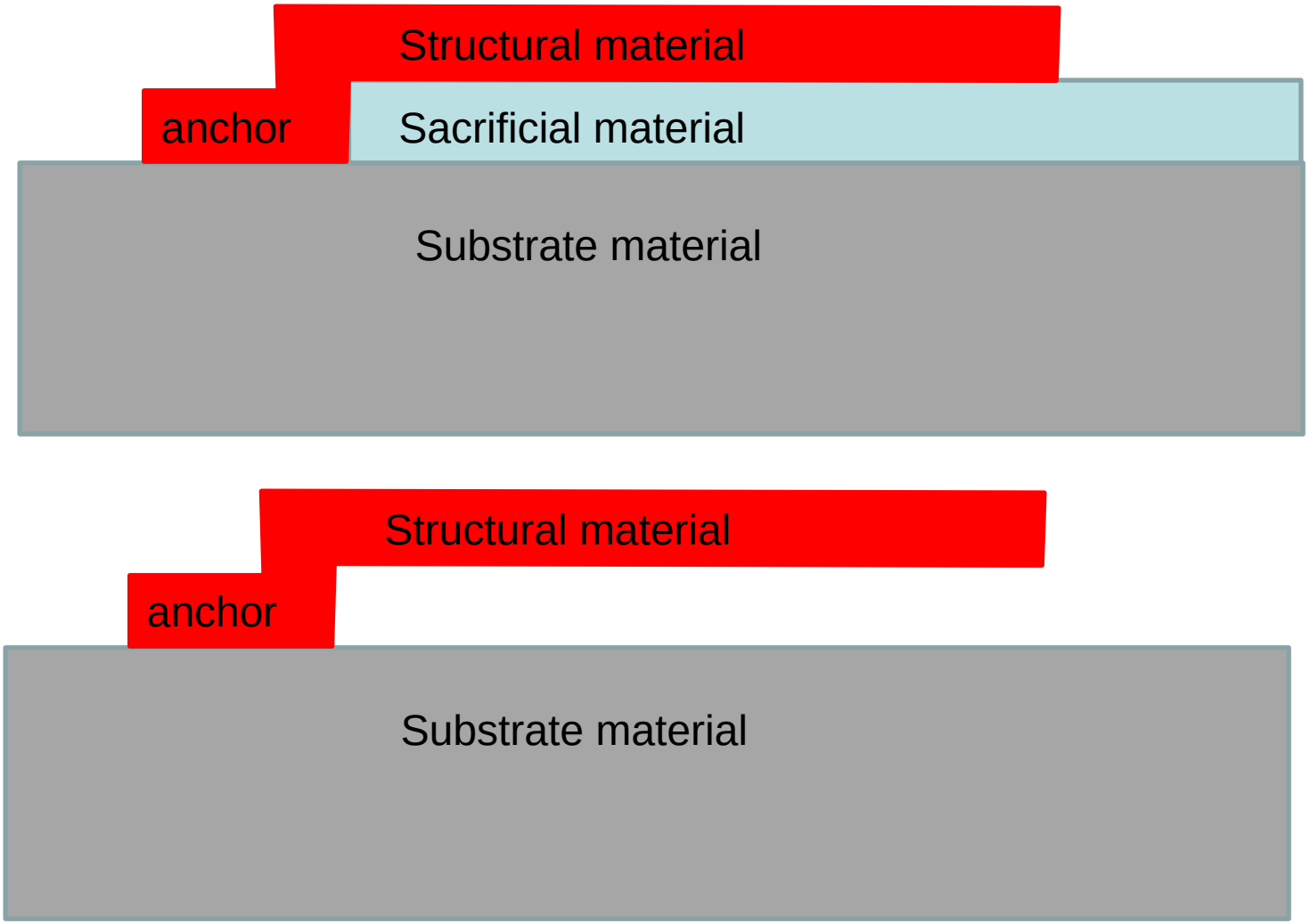
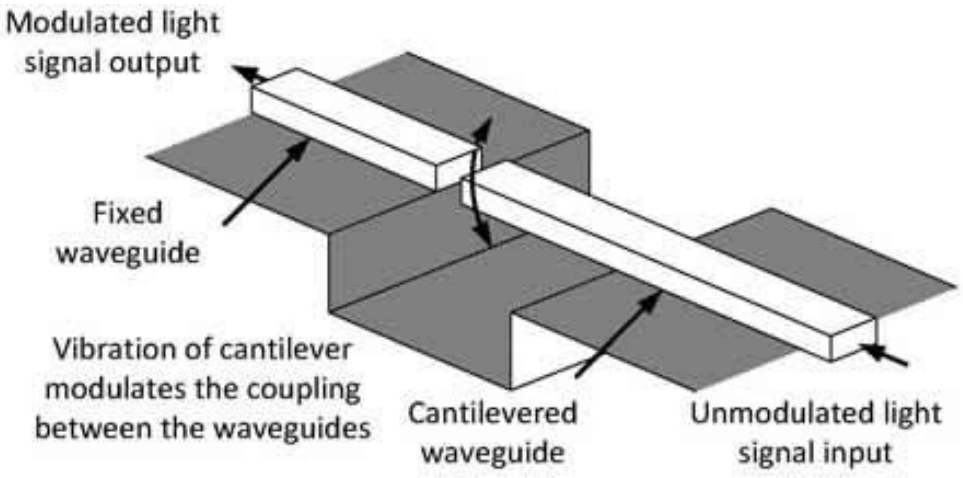
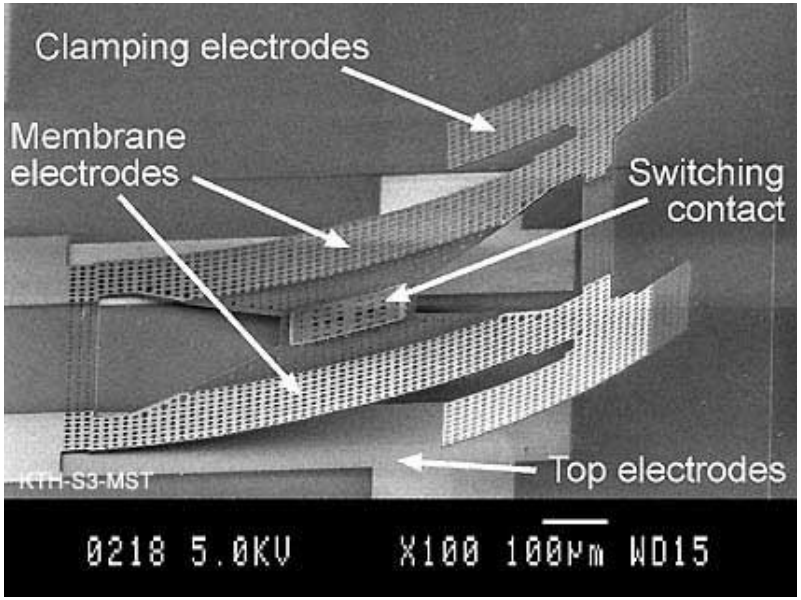
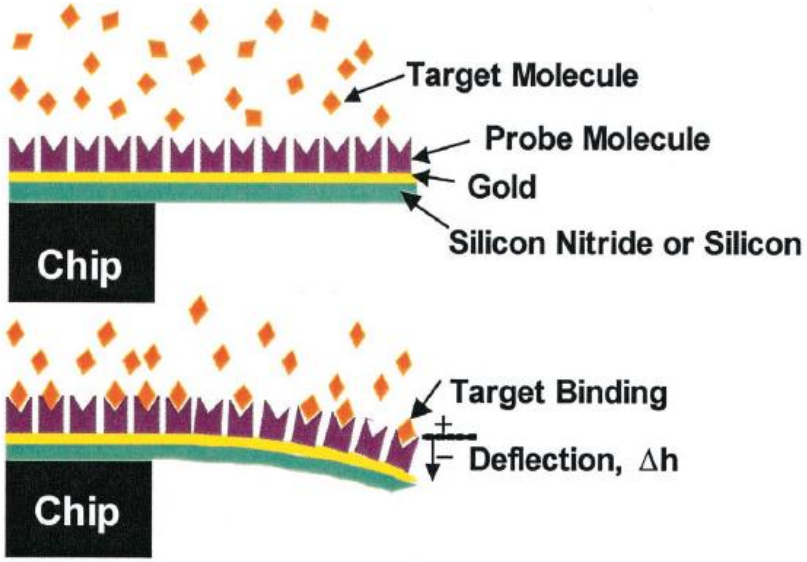
Generic structure

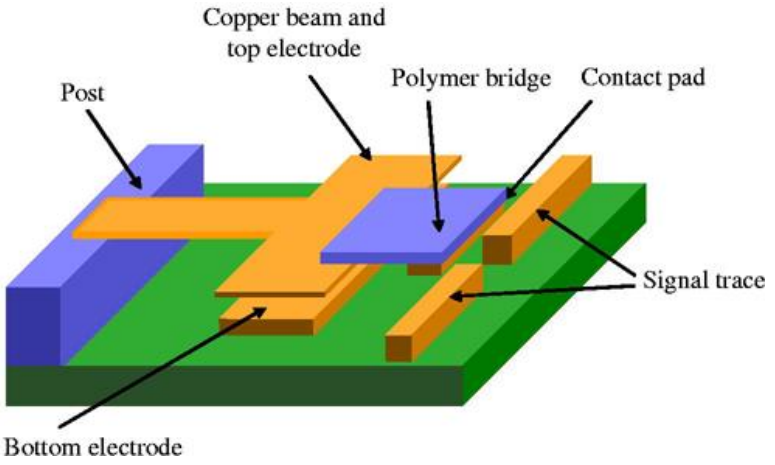


Applications





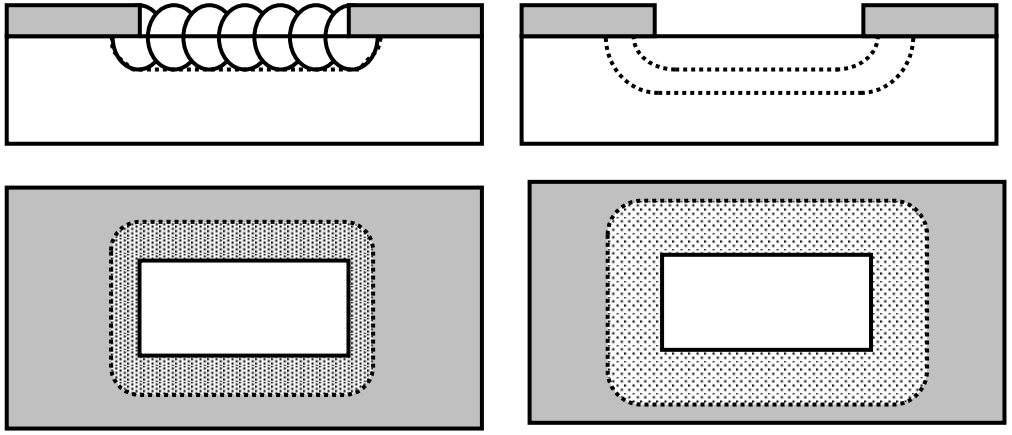


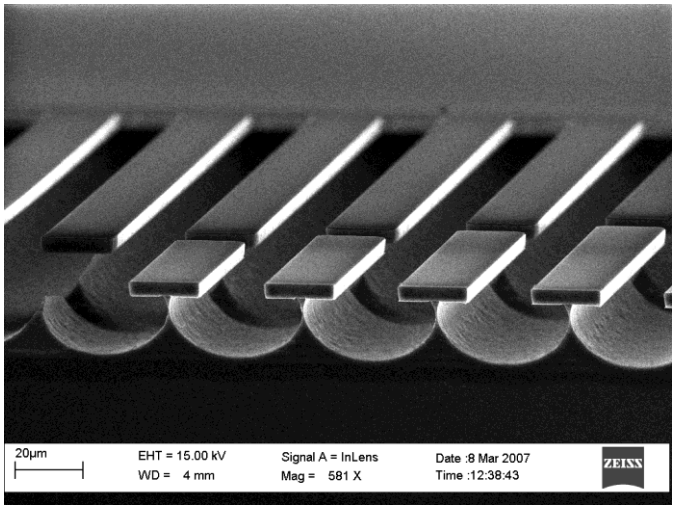


Isotropic etching

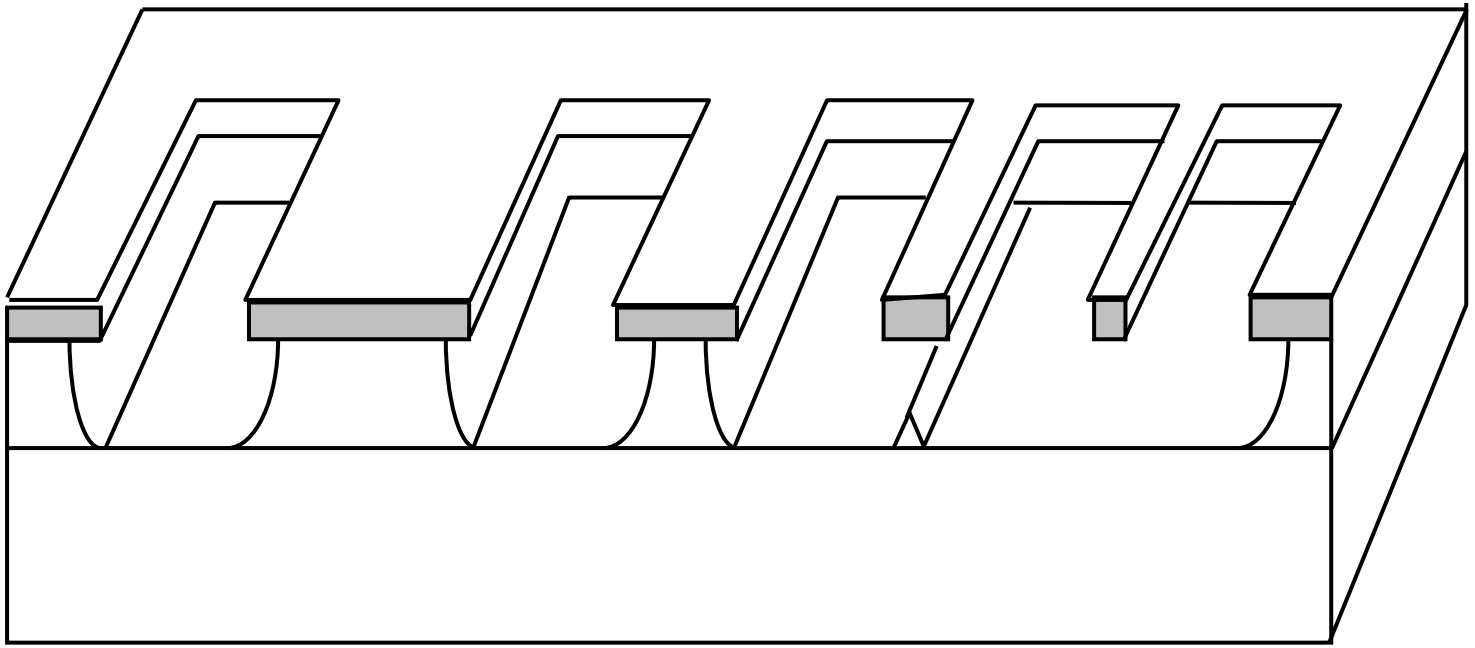
- Proceeds as a spherical wave
- Undercuts structures (proceeds under mask)
- Most wet etching processes are isotropic

e.g. HF etching of oxide, H_3PO_4 etching of Al



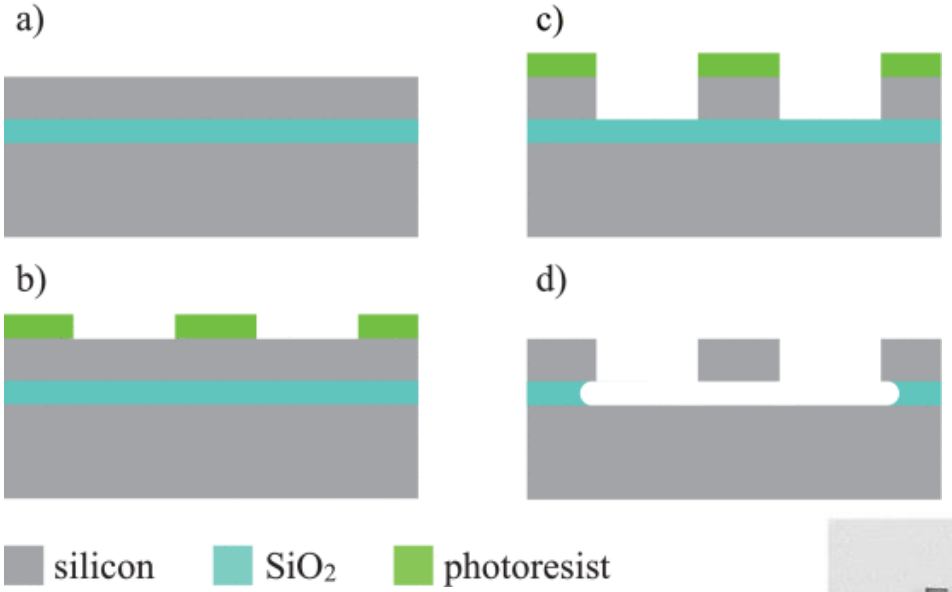


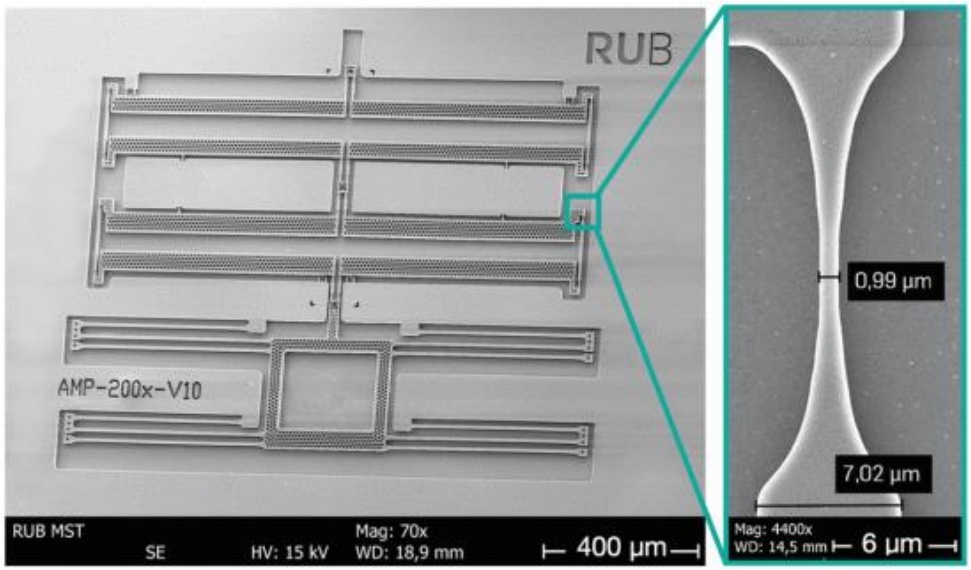
Isotropy: good and bad



If you want closely spaced lines (as in comb-drive capacitor), undercutting is bad, but if...

Single-mask mechanical amplifier



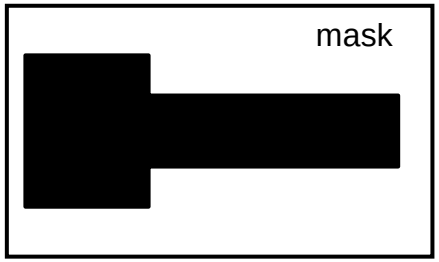


P. Schmitt and M. Hoffmann, "Engineering a Compliant Mechanical Amplifier for MEMS Sensor Applications," in *Journal of Microelectromechanical Systems*, vol. 29, no. 2, pp. 214-227, April 2020.

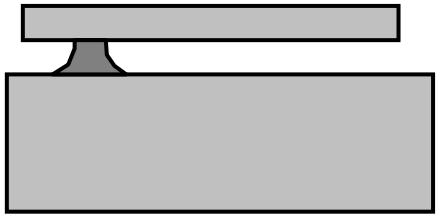
Single mask vs. two mask cantilever

Single mask process

Etch structural layer with resist mask, strip resist

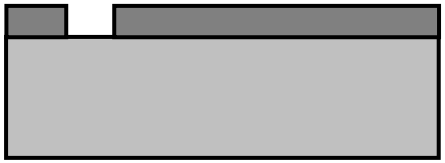


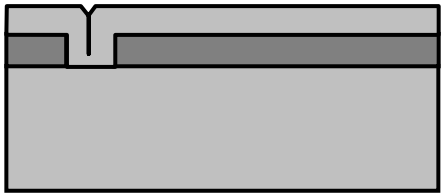
Etch sacrificial layer



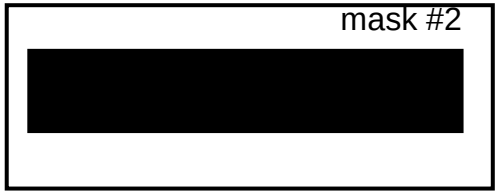
Two mask process

Litho 1
Etch anchor hole in sacrificial layer, strip resist

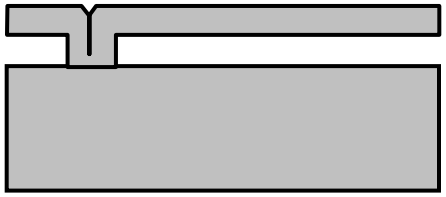




Deposit structural layer



Litho 2
Etch structural layer, strip resist



Etch sacrificial layer

Material pairs & etchants

Structural film	Sacrificial film	Sacrificial etch(es)
polysilicon	oxide	HF, HF vapor
silicon nitride	oxide	HF
silicon nitride	Al	$NaOH$, H_3PO_4
nickel	Cu	HCl
nickel	resist	oxygen plasma
aluminum	resist	oxygen plasma
gold	Cu	HCl
gold	resist	oxygen plasma
copper	resist	oxygen plasma
Parylene	resist	acetone, other solvents
SU-8	Cu	HCl
CVD oxide	CVD polysilicon	SF_6 plasma, XeF_2 vapor

Must handle 300°C

Deposition >300°C

HF etching of SiO_2 and other materials

Thermal oxide

These are CVD oxides

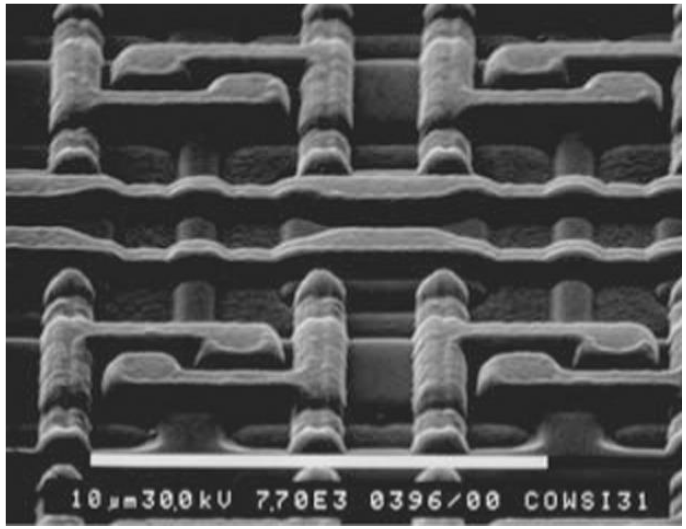
Etchant	Material					
	SiO_2	TEOS	PSG	Si_3N_4	Al	Mo
HF (49%)	1763	3969	4778	15	38	0.15
BHF	133	107	1024	1	3	0.5
1:10 HF	48	157	922	1.5	320	0.15

Etch rates in nm/min

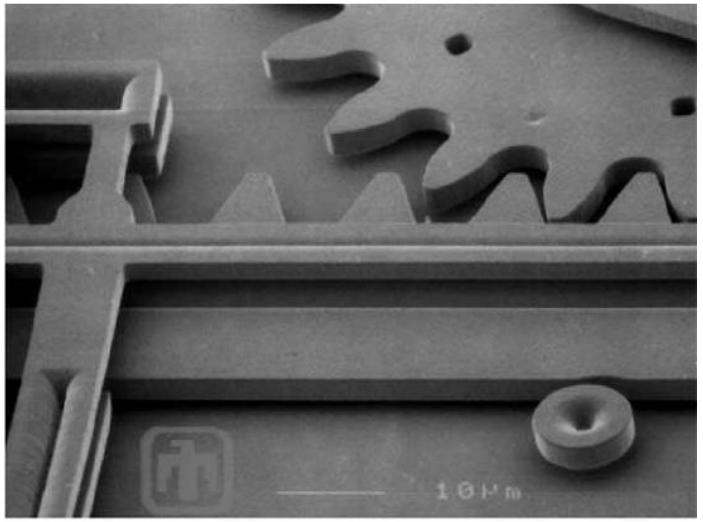
Thermal oxide properties are always the same, but (PE)CVD oxide properties are strongly deposition process dependent

Polysilicon

- SiH_4 (g) ==> Si (s) + 2 H_2 (g)
- Deposited by CVD at 625^{o}C ➔ true poly
- Can be deposited at 575^{o}C ➔ amorphous
- Typical thickness 100 nm-2 μm



CMOS gate electrodes



MEMS rotors

Poly vs. <Si>

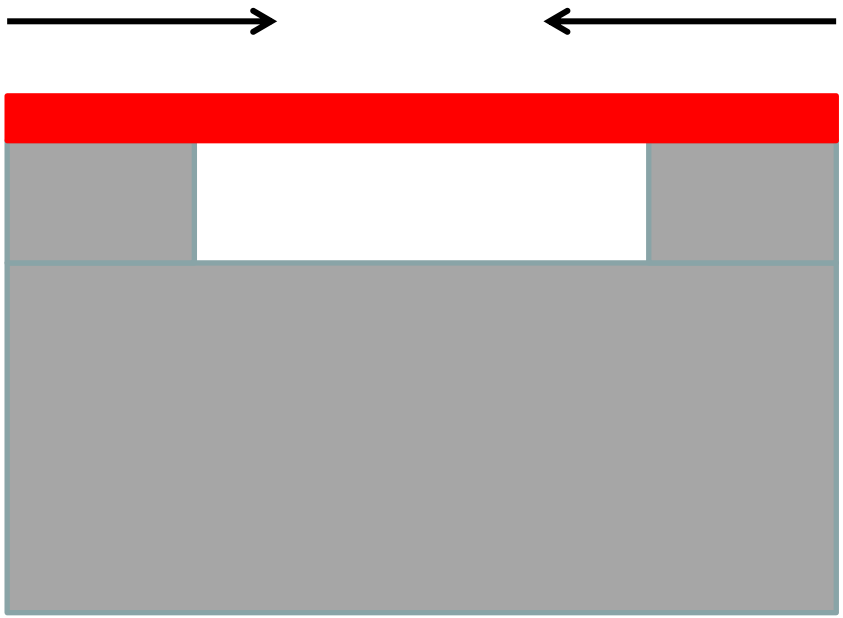
Density: same for both 2.3 g/cm^3

Young's modulus: same for both 170 GPa

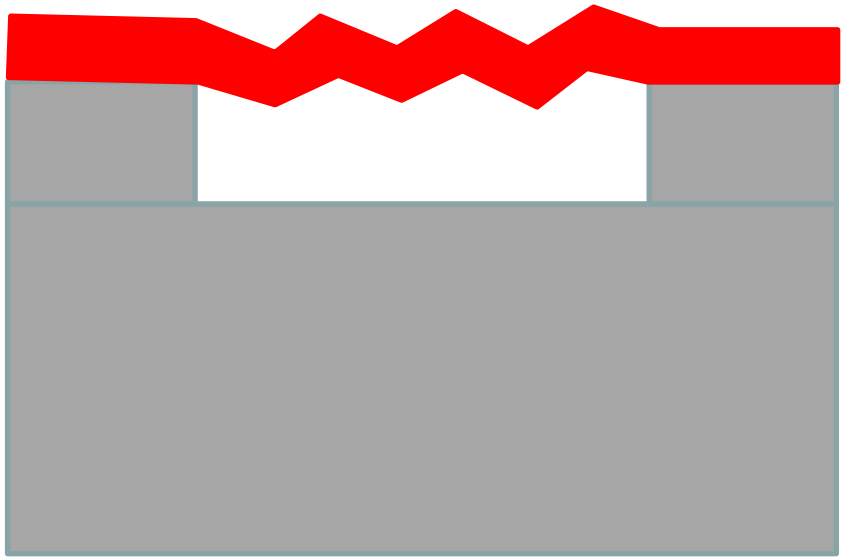
CTE: same for both 2.5 ppm/K

Thermal conductivity:	<Si>	156 W/K*m
	poly	32 W/K*m
Carrier mobility:	<Si>	100 cm^2/Vs
	poly	10 cm^2/Vs

Compressive stresses in film



buckling



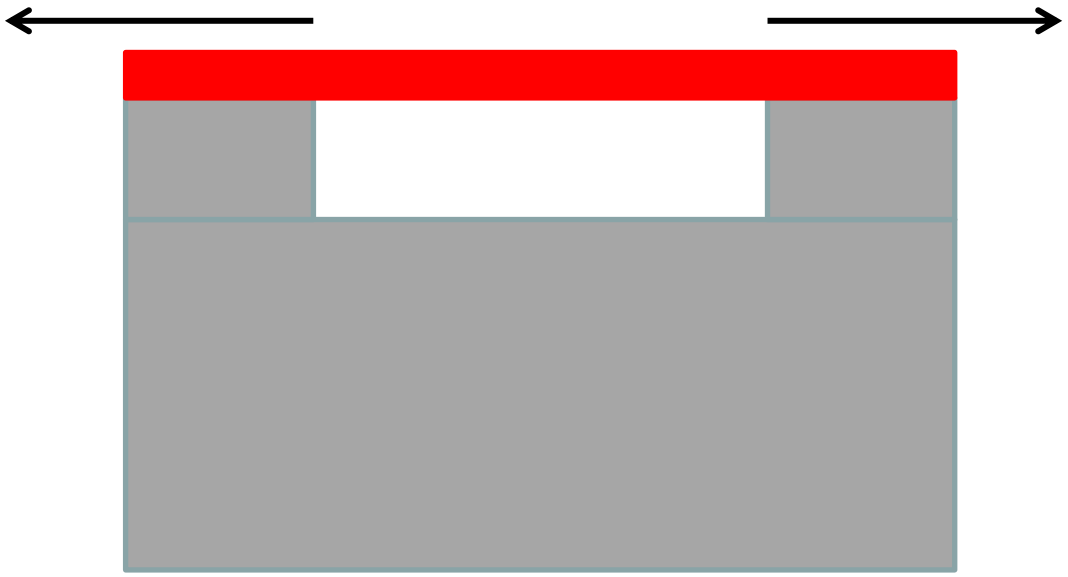
Buckling depends on:

- Material (E, υ)
- Bridge span (L)
- Bridge thickness (t)

$$\sigma_{cr} = \frac{\pi^2 E t^2}{3L^2(1-\nu)}$$

Critical buckling stress

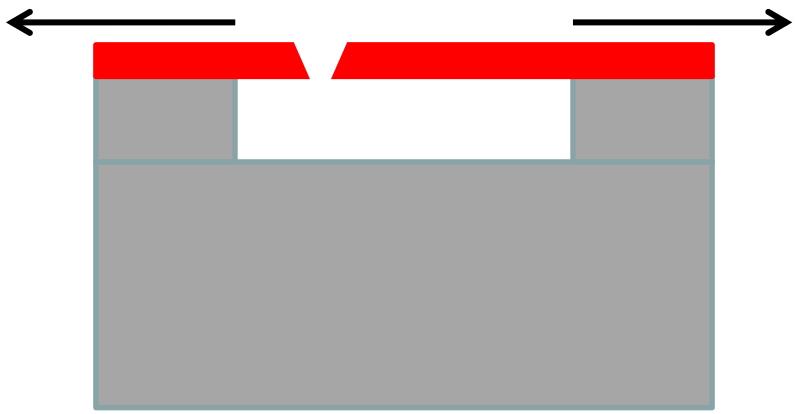
Desired state of affairs in most cases: structural layer is flat after release



This is achieved by (small) tensile stress

Tensile stress issues

Film stays flat.

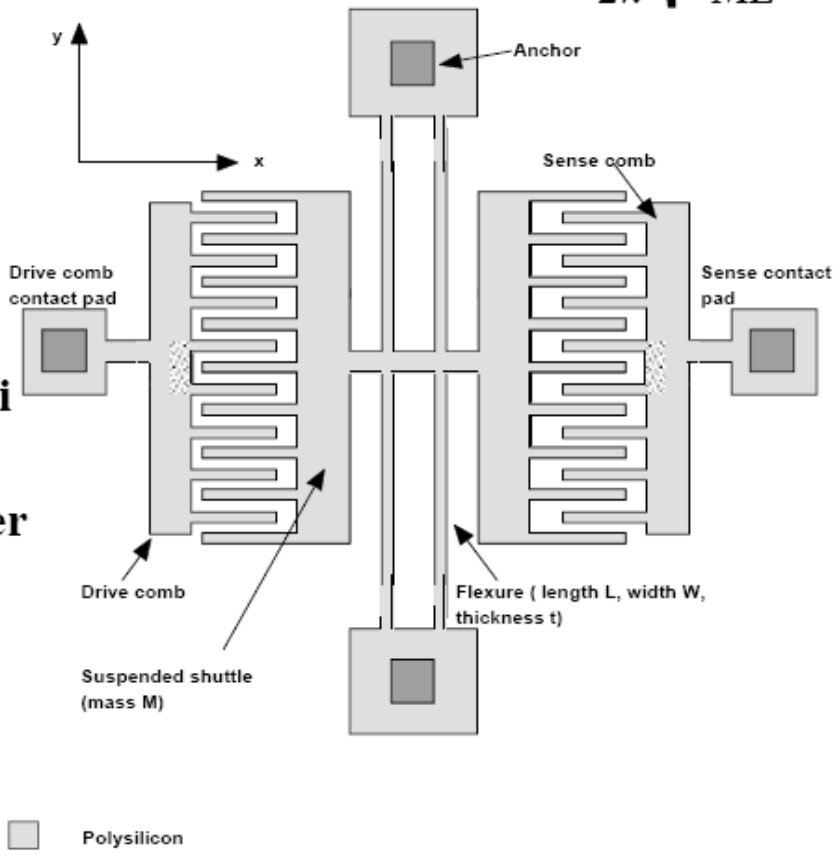


Defects (e.g. cracks) initiate breakage (aided by high tensile stresses).

Control of film stress

- With L=150 µm and W=t=2 µm, f_o=10 to 100 kHz
- Annealing at high temperature (900-1150°C)
- Fine-grained tensile vs large grained compressive
- Doping elements
- Sandwich doping and annealing
- Vary material composition e.g Si rich Si_3N_4
- In PECVD: change the RF power and frequency
- In sputtering: gas pressure and substrate bias

$$f_o \approx \frac{1}{2\pi}\sqrt{\frac{4EtW^3}{ML^3}+\frac{24\sigma_r tW}{5ML}}$$



Marc Madou

Perforation to release large area structures

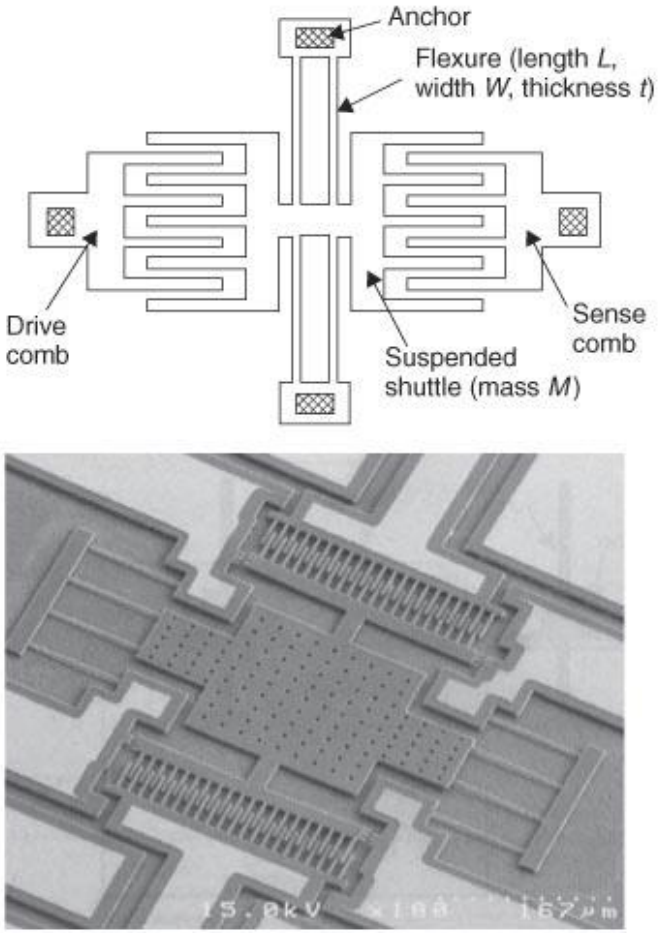
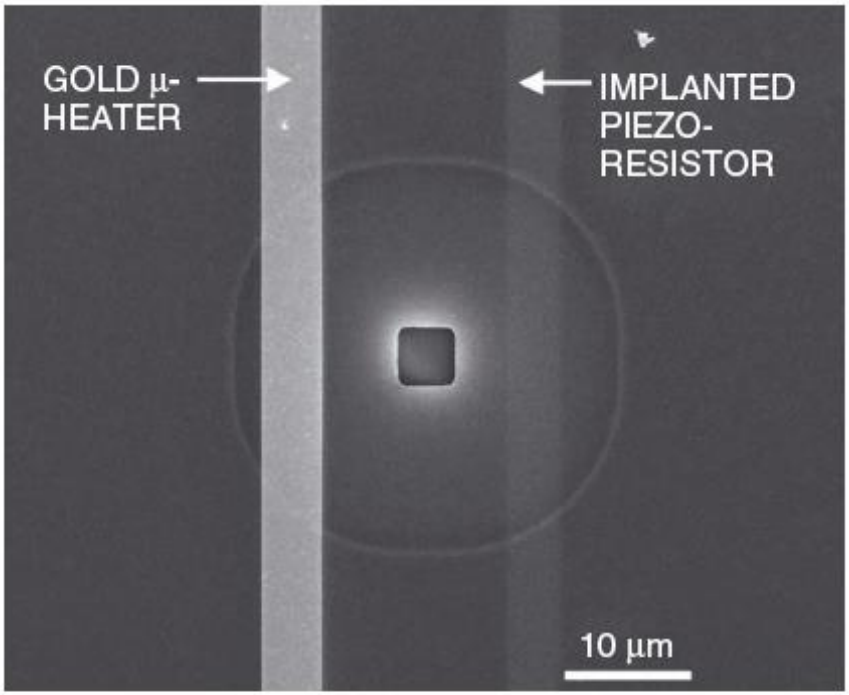
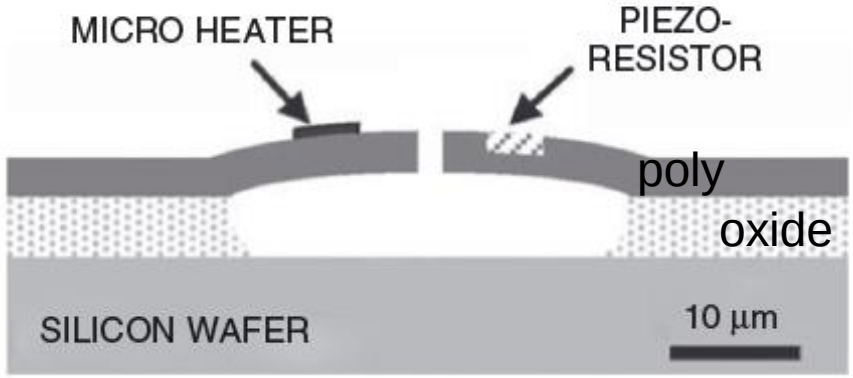


Figure 29-11

Comb drive with suspended shuttle mass. Plate release has been aided by using perforations in the plate. Reproduced from Bustillo *et al*. (1998) by permission of IEEE.

Thermally excited resonator

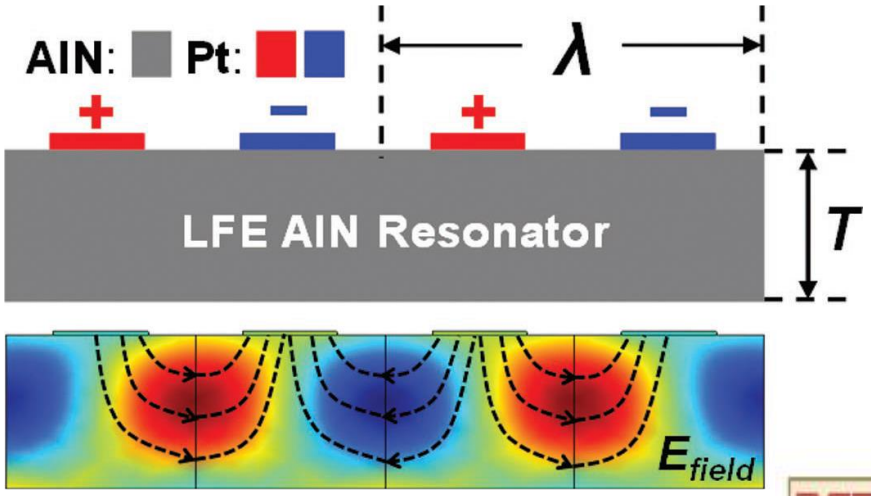


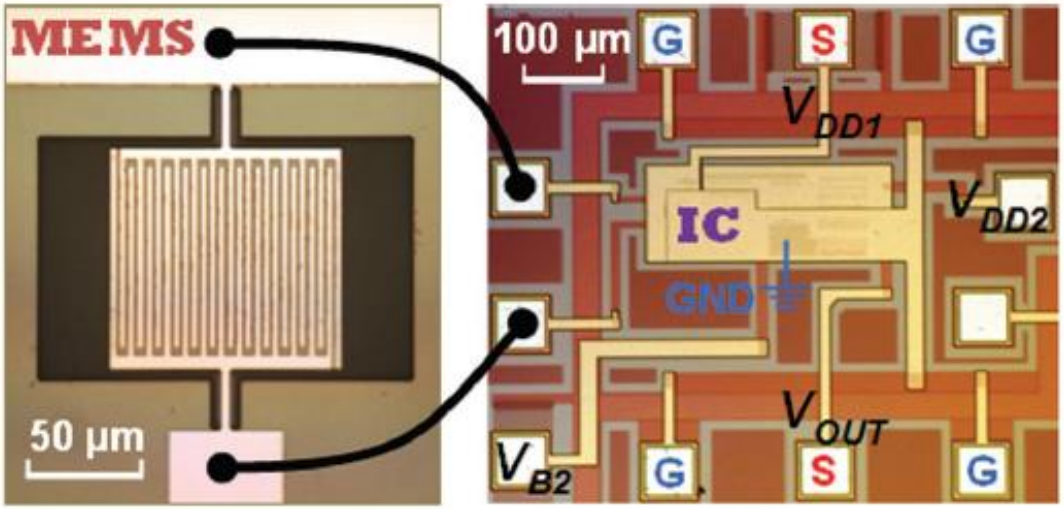


Reichenbach, R.B. et al:, IEEE EDL 27 (2006) p. 805

1. CVD oxide deposition
2. Poly deposition
3. Lithography piezoresistor
4. Implant piezo & strip
5. Clean
6. Anneal implant damage
7. Au evaporation
8. Litho for heater
9. Au heater etch & strip
10. Litho for poly hole
11. Poly etch & strip
12. Oxide wet etch in HF
13. Rinse & dry

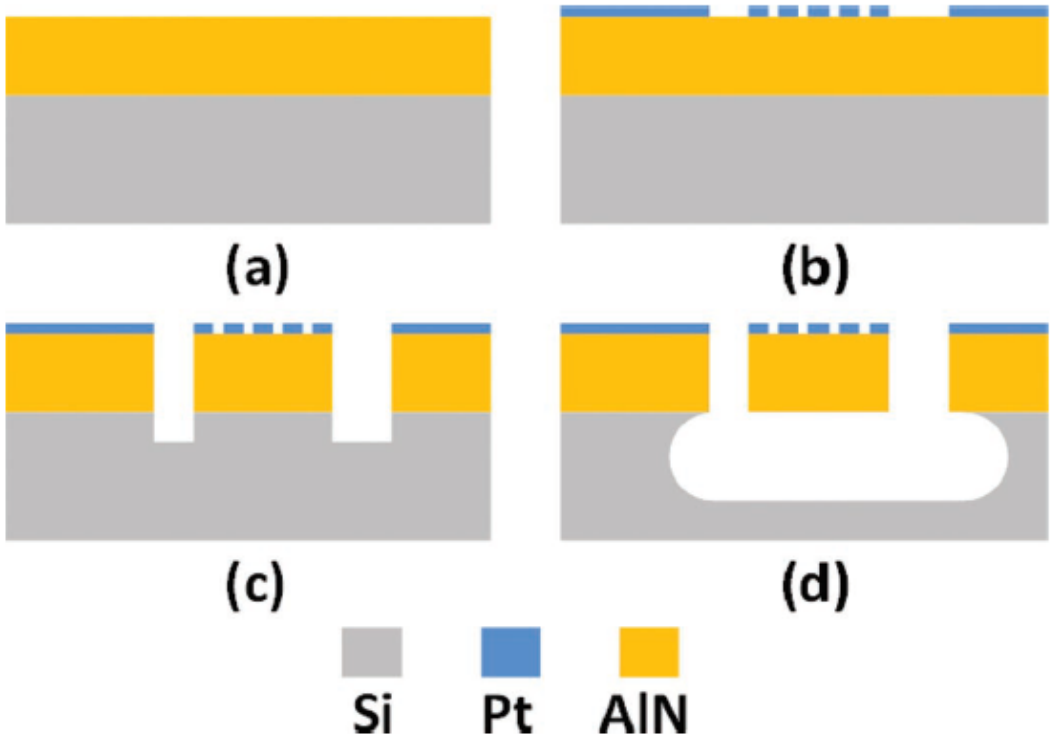
Lateral-field-excited (LFE) piezoelectric AlN contourmode





Zuo *et al.*: CMOS oscillator based on contour-mode MEMS resonators, IEEE 2010

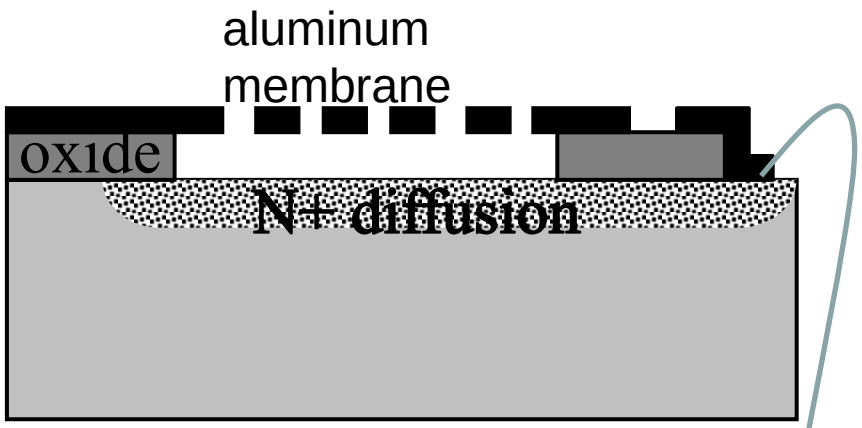
LFE AlN fabrication



(a) AlN sputter deposition on top of Si wafers
(b) lithography, Pt electrode deposition evaporation, lift-off
(c) AlN lithography and plasma etching using Cl_2 and BCl_3, continue to etch into Si
(d) structure release by Si dry etching in XeF_2.

Zuo *et al.*: CMOS oscillator based on contour-mode MEMS resonators, IEEE 2010

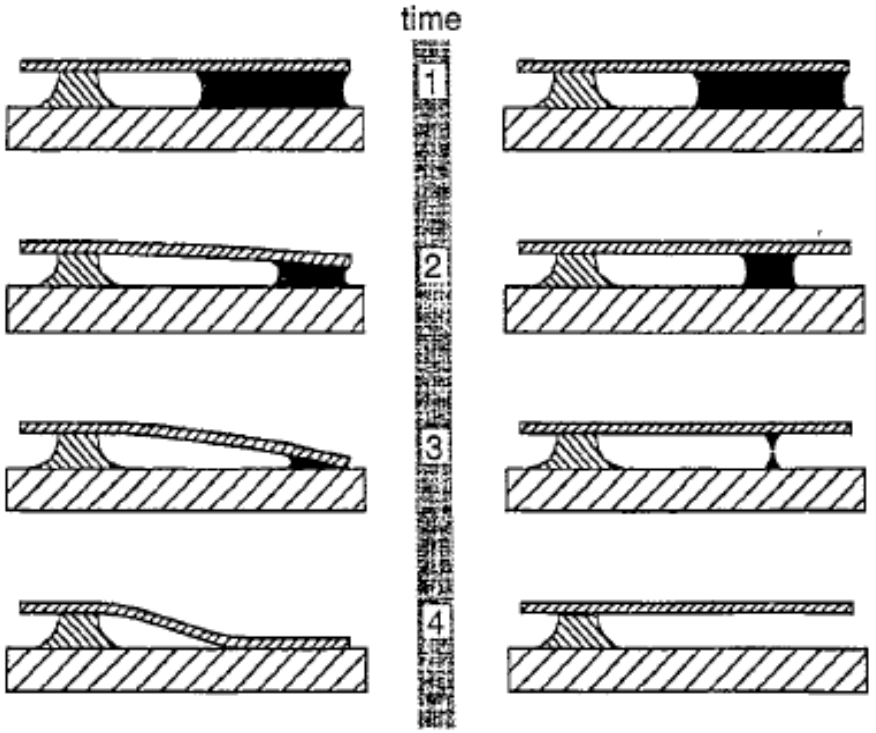
Microphone



0. SSP wafer, low n-doping
1. Thermal oxide
2. 1st litho for diffusion
3. Etch oxide & strip resist
4. Clean
5. N+ diffusion, heavy doping
6. Etch all oxide away
7. CVD oxide deposition
8. 2nd litho: open contact to n+
9. Etch oxide & strip resist
10. Aluminum sputtering
11. 3rd litho: holes in Al membra
12. Etch aluminum & strip resist
13. Etch oxide, rinse & dry

Stiction (←sticking + friction)

Capillary force of liquid exceeds mechanical strength of the released beam, and the released beam attaches to substrate



Stiction, permanent

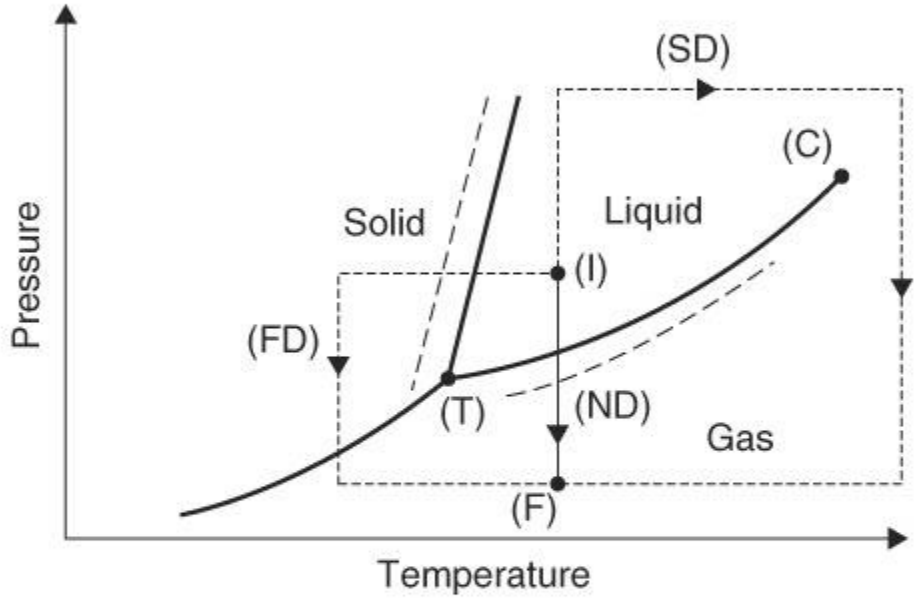
correct release

Stiction prevention

- Replace water by something that has lower surface tension, like isopropyl alcohol
- Use stronger structure shapes (H, T, I, U beams)
- Change structural material
- Redesign so that shorter beams needed
- Redesign larger gap (not always possible)
- Make surfaces rough (opposite of good bonding!)
- Use dry release ➔ no drying needed
- Use more elaborate drying (more on next slide)

Alternative drying

FD: Via solid phase, directly to gas, eliminating liquid phase

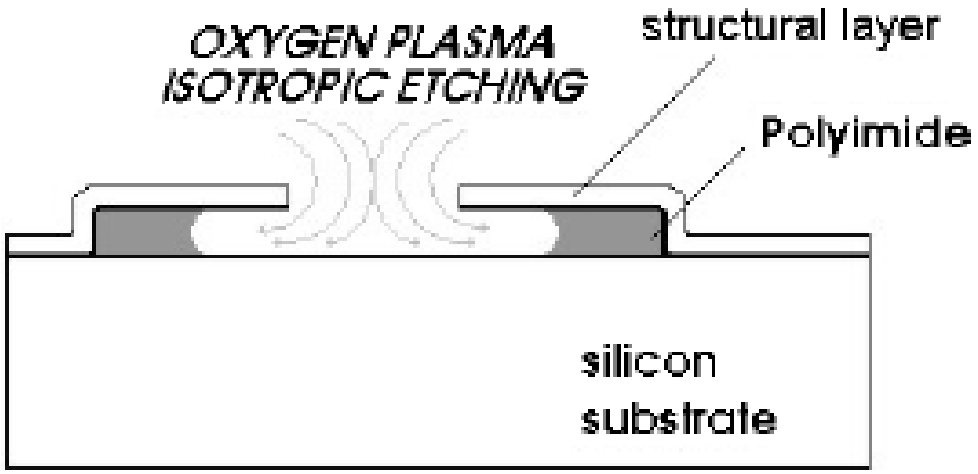


SD: Via vapor phase ➔ no surface tension effects

Figure 29-13

Thermodynamics of drying: I, initial stage; F, final stage; N, normal drying; FD, freeze drying; SD, supercritical drying. Reproduced from Bellet and Canham (1998) by permission of Wiley-VCH.

Stiction prevention: plasma release



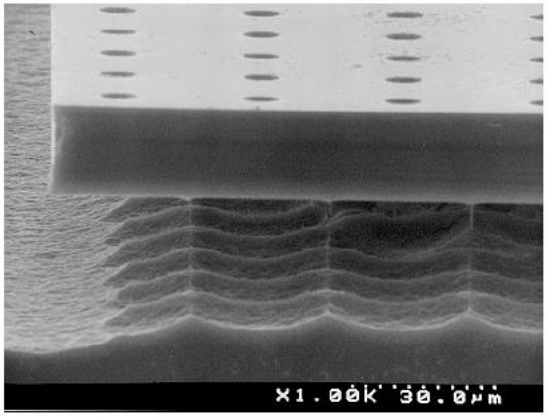


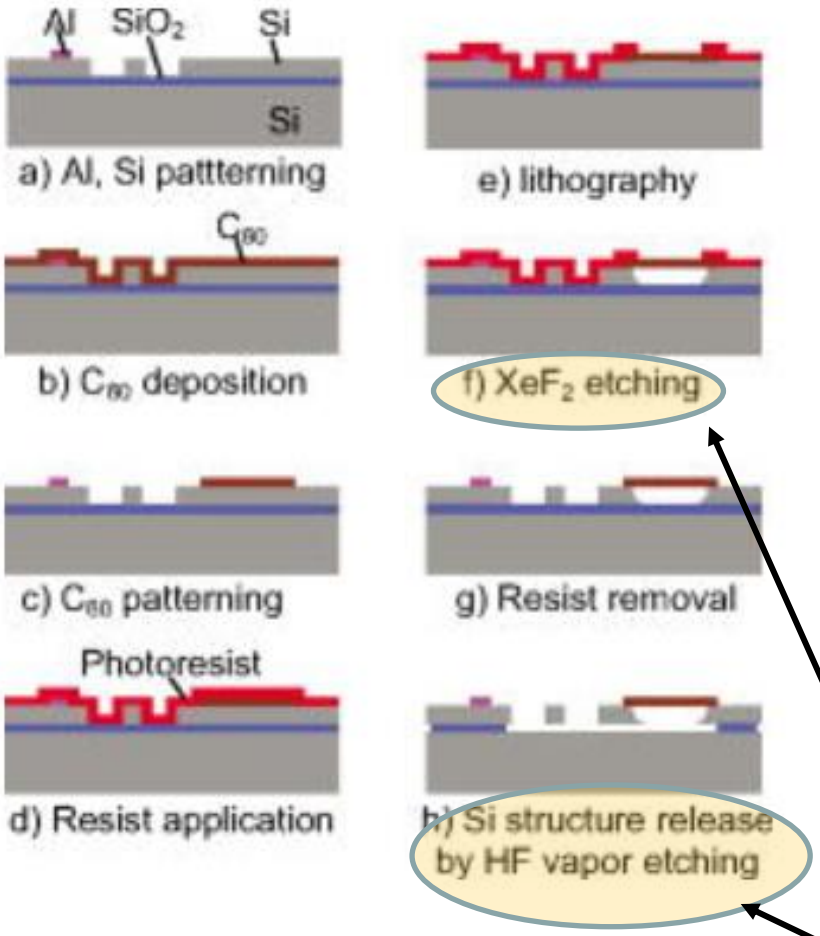
Figure 4. Close-up of the air gap profile near the external edge of the resonator. The holes in the membrane are used to underetch large areas.

No liquid, no surface tension, no capillary forces.

Other plasma releases:

- SF_6 isotropic plasma etching of silicon
- NF_3, ClF_3, also sources of fluorine to etch silicon

Dry release, but no plasma



XeF_2:
etches silicon, silicon nitride and molybdenum.
Selectivity to oxide >1000:1

HF vapor:
etches SiO_2.
Of course, CVD oxides still etch faster than thermal oxide.

Aluminum OK. Nitride selectivity 40-600:1, depends on details.

Two different sacrificial layers !

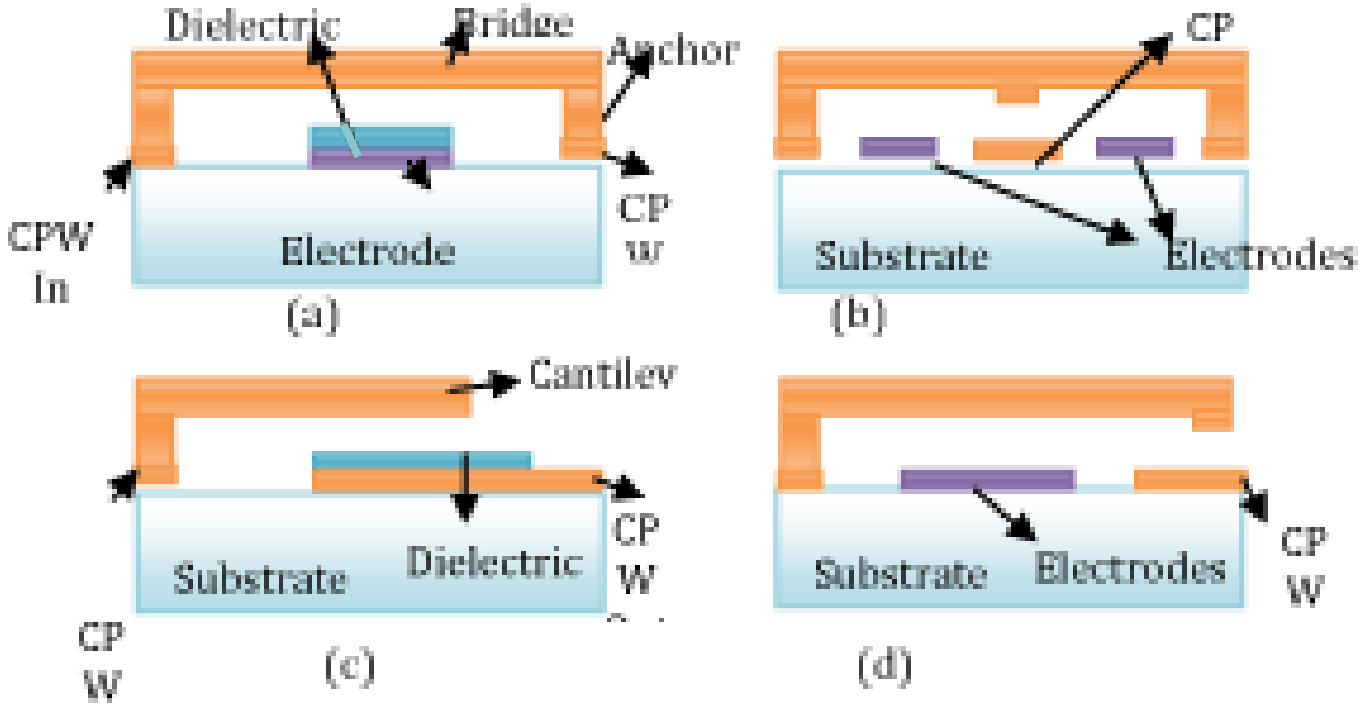
Free-standing C_{60} nanowire fabricated using XeF_2 sacrificial dry etching

Toshiyuki Tsuchiya; Yasutake Ura; Yomoya Jomori; Koji Sugano; Osamu Tabata

Author Affiliations +

J. of Micro/Nanolithography, MEMS, and MOEMS, 8(1), 013020 (2009). https://doi.org/10.1117/1.3094745

MEMS switches



(a) Capacitive Shunt,
(c) Capacitive Series,

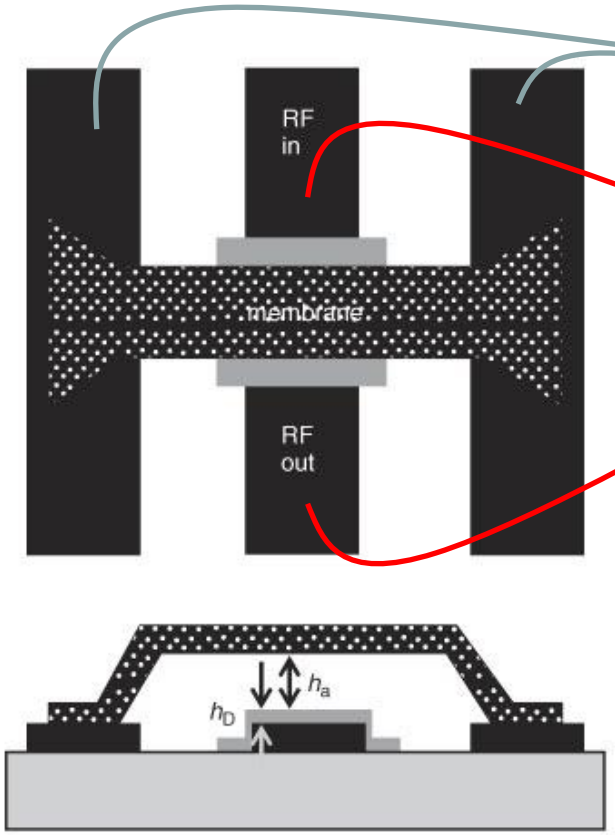
Dielectric between metals

(b) Resistive Shunt,
(d) Resistive Series.

Metal-metal contact

K. Srinivasa Rao, Lakshmi Narayana Thalluri; Journal of Biosensors, Biomarkers and Diagnostics

Capacitive shunt switch



Electrodes for actuation voltage

RF signal electrodes

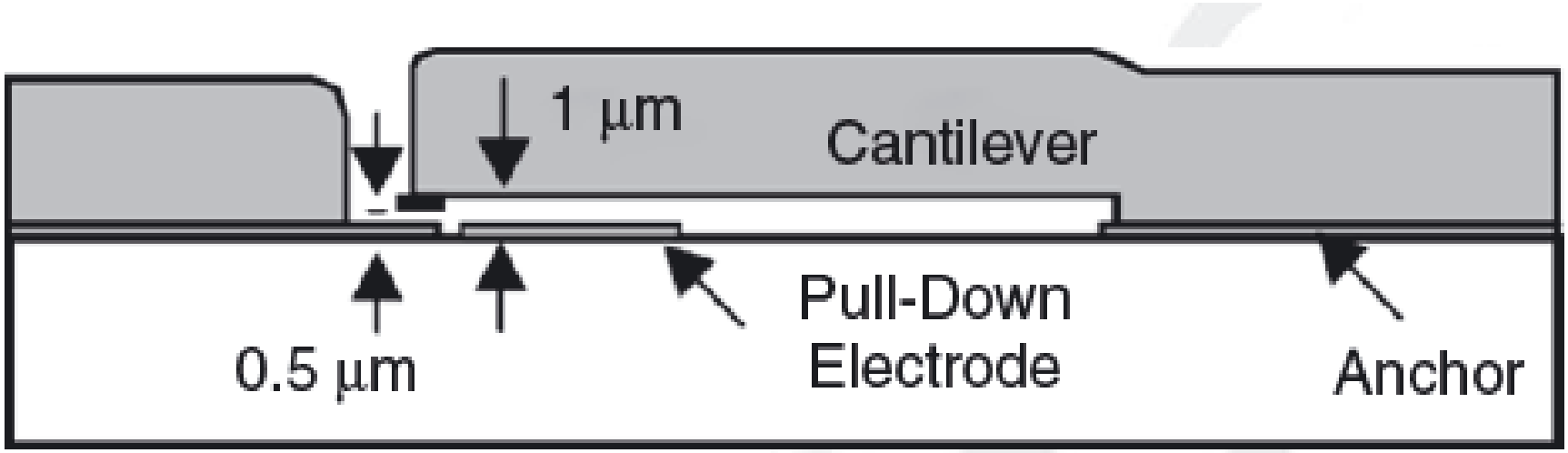
Off-state when up.

On-state when pulled down.

Figure 29-4

RF switch with nickel membrane, top and cross–sectional views: air gap h_a created by photoresist sacrificial etching.

Electroplated gold switch



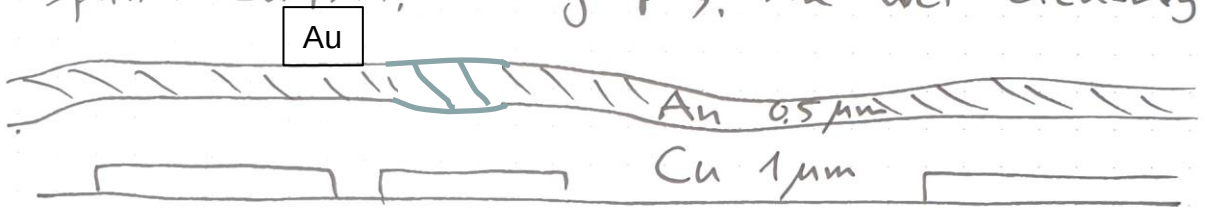
Pull down electrode: Cr/Au, 50/250 nm. 1st deposition, sputter
Sacrificial material: 1 µm Cu
Top contact metal: Au, 0.5 µm
Cantilever: Au, 8 µm

} 2nd deposition, sputter

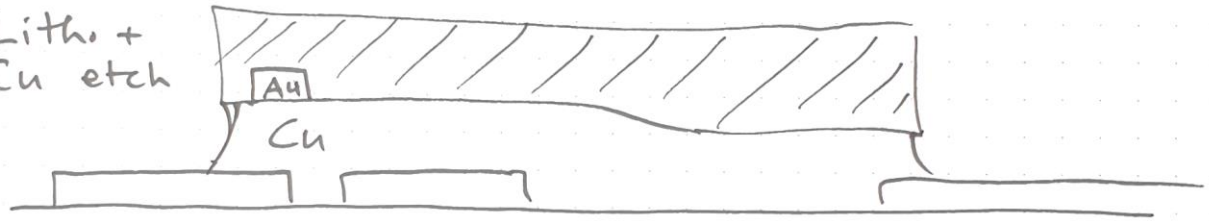
3rd deposition, electroplating

Cr/Au : metal deposition, lithography, etching

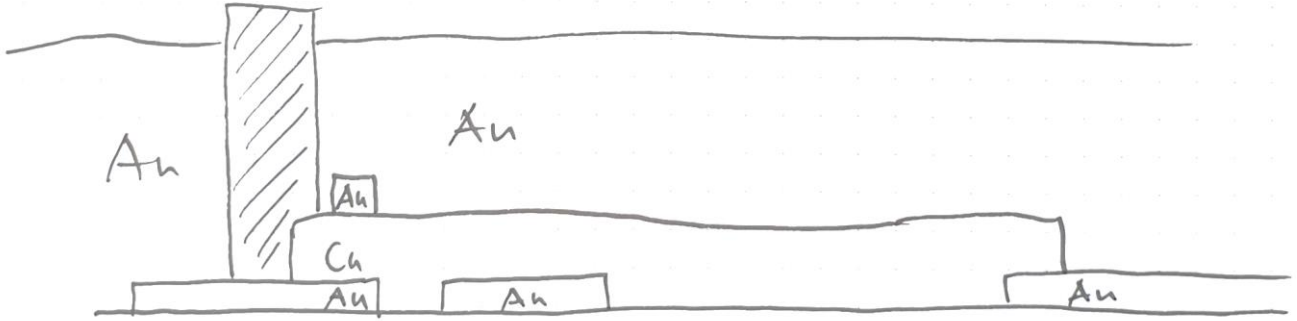
Sputter Cu/Au, lithography, Au wet etching



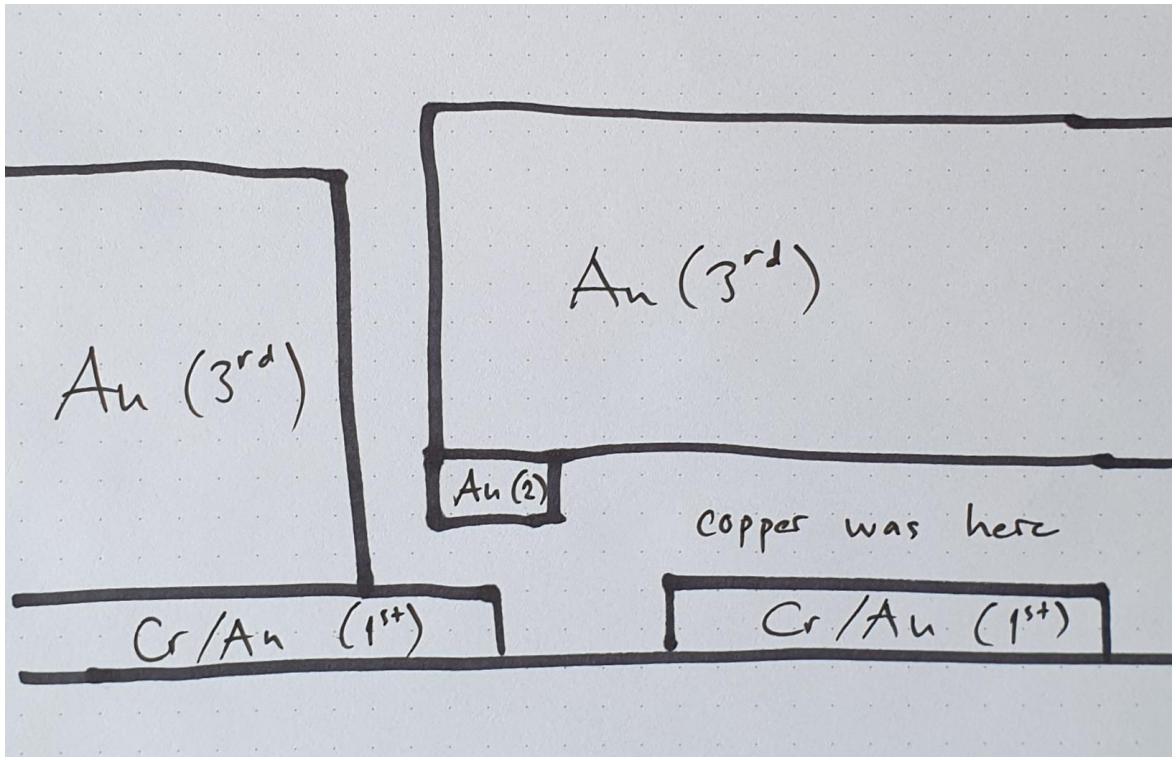
Litho + Cu etch



Lithography + gold electroplating



Electroplated gold switch

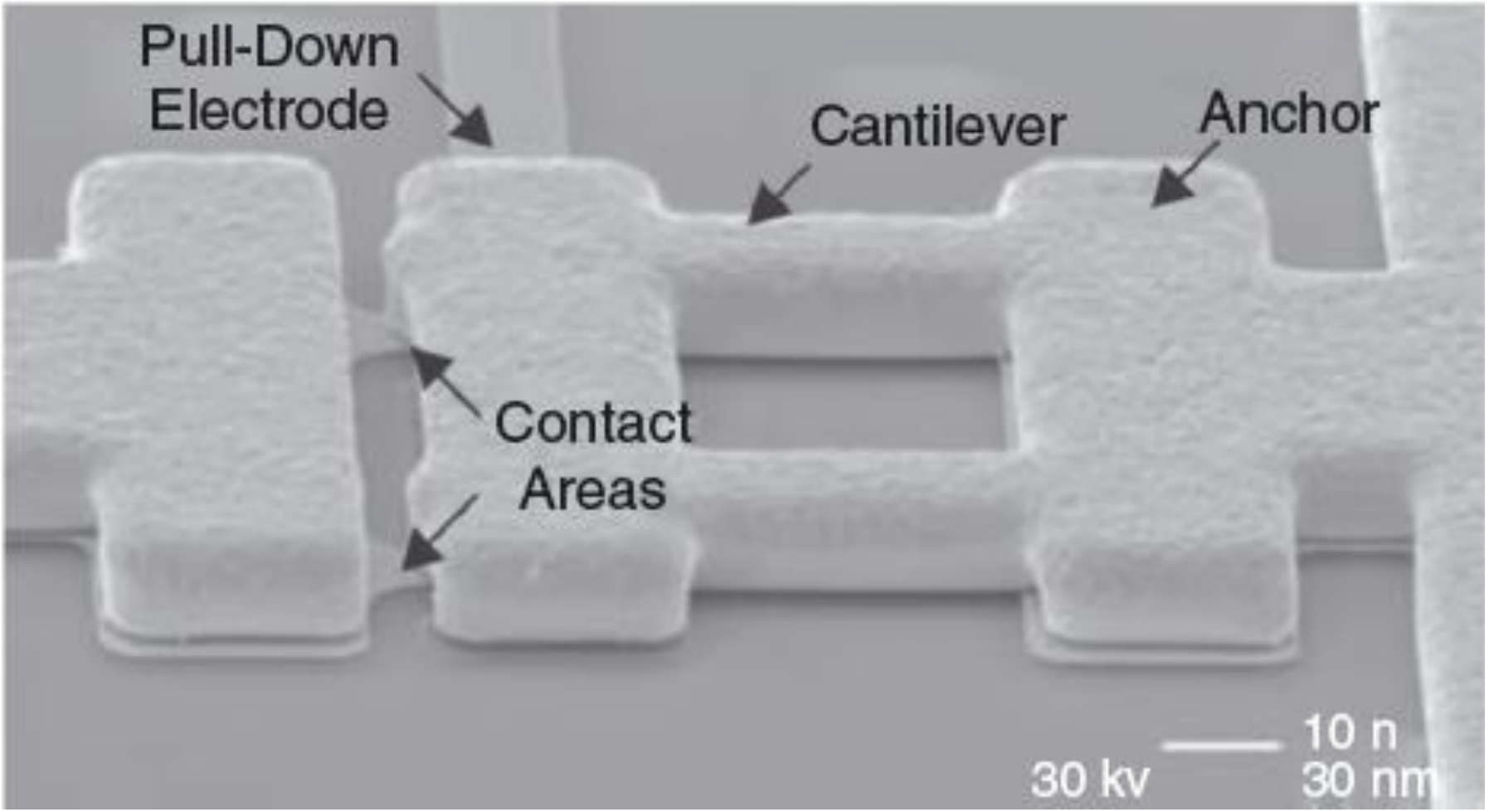


Pull down electrode: Cr/Au, 50/250 nm. 1st deposition, sputter
Sacrificial material: 1 µm Cu
Top contact metal: Au, 0.5 µm
Cantilever: Au, 8 µm

} 2nd deposition, sputter

3rd deposition, electroplating

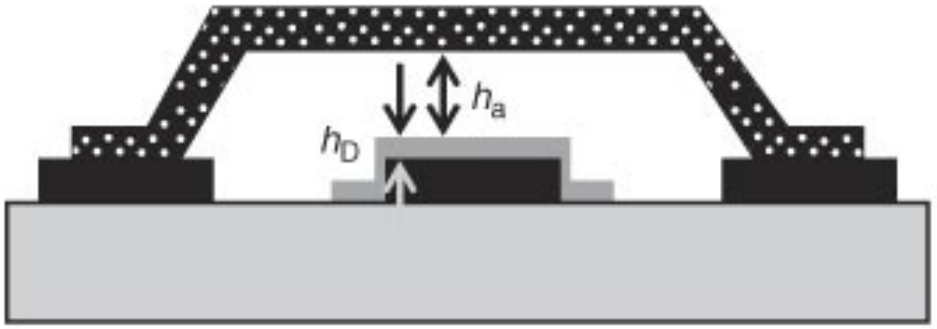
Electroplated gold switch



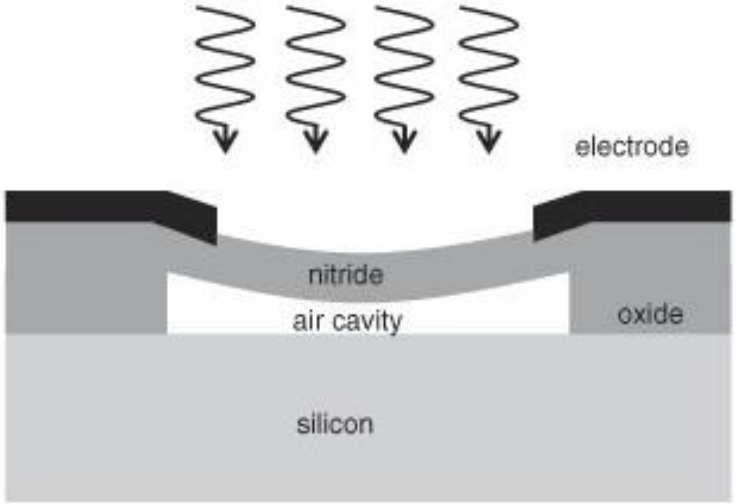
Rebeiz, G.M. & J.B. Muldavin: IEEE Microwave Magazine, Dec. 2001, p. 59

Critical release gap

Sometimes gap height is critical for device operation. These gaps are often ~ 1 μm in size.



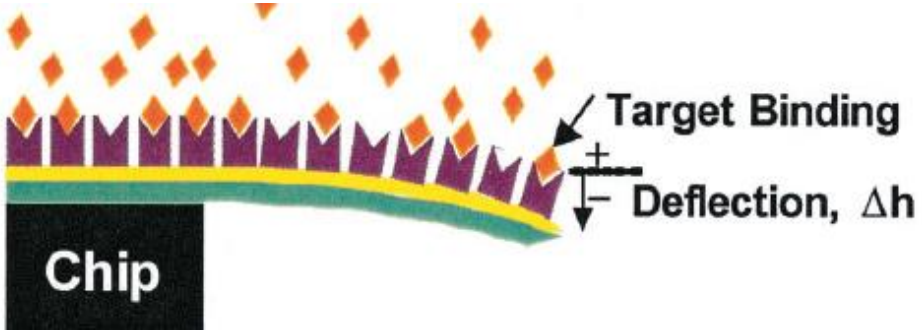
Actuation voltage depends on gap height. If gap bad reproducibility ➔ voltage differences in actuation.

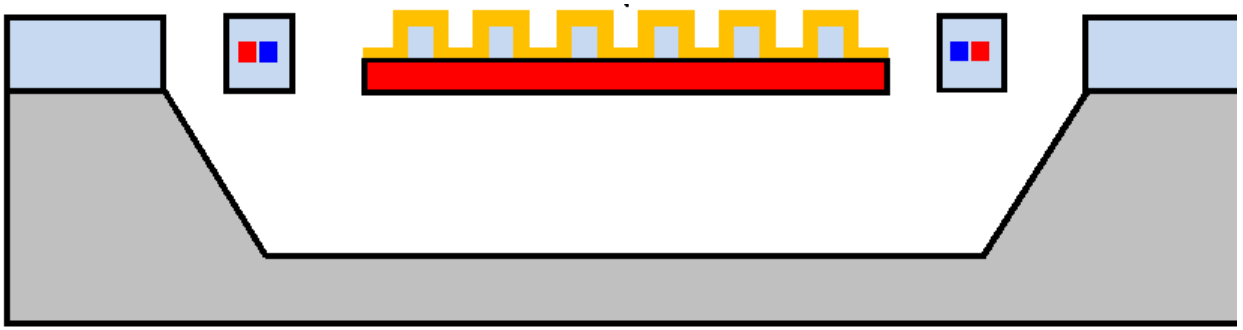


Optical path length depends on gap. If gap control bad ➔ no display of colors.

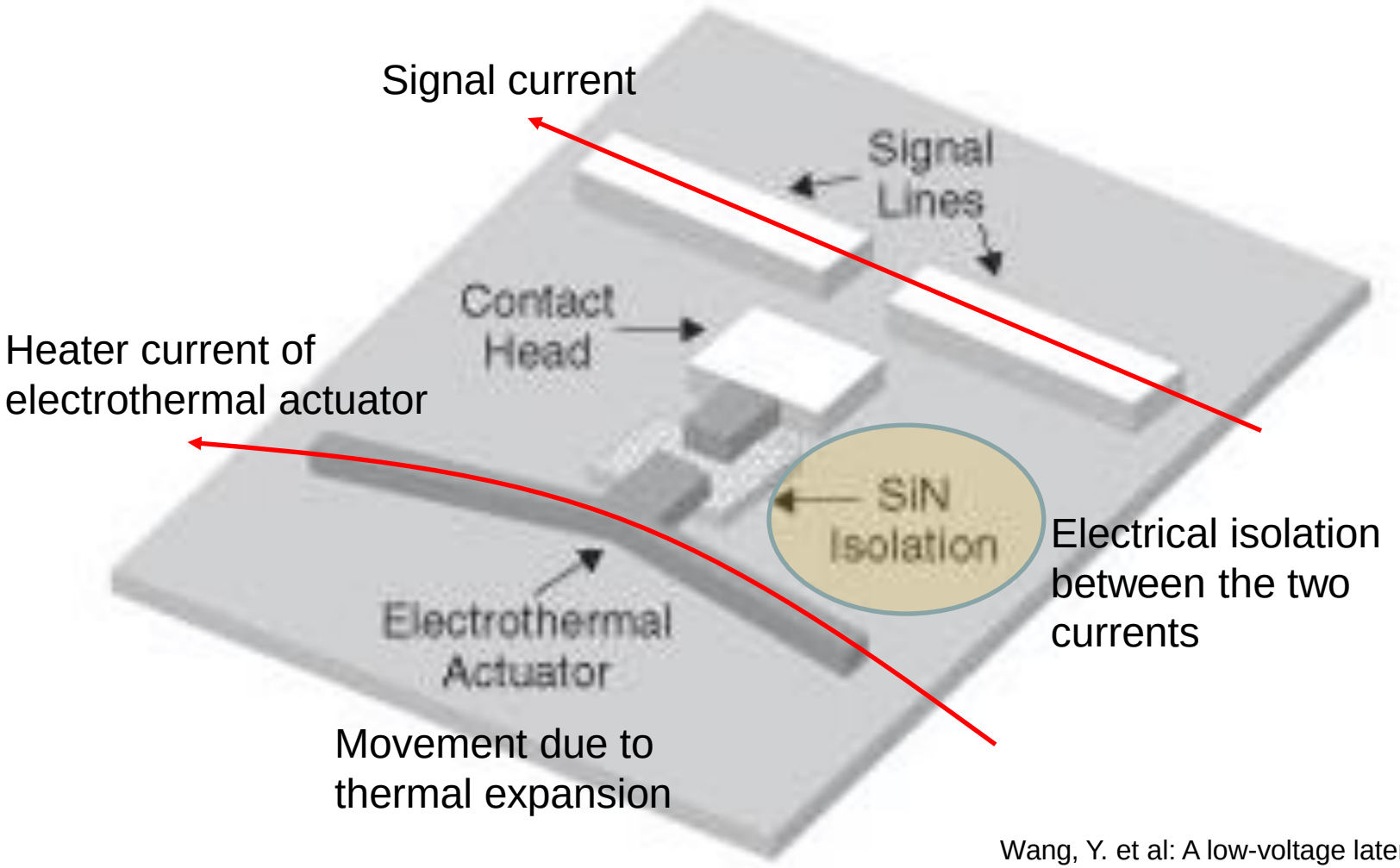
Non-critical release gap

Gap provides space so that elements can move;
or gap provides thermal isolation. Large: >> 1 µm



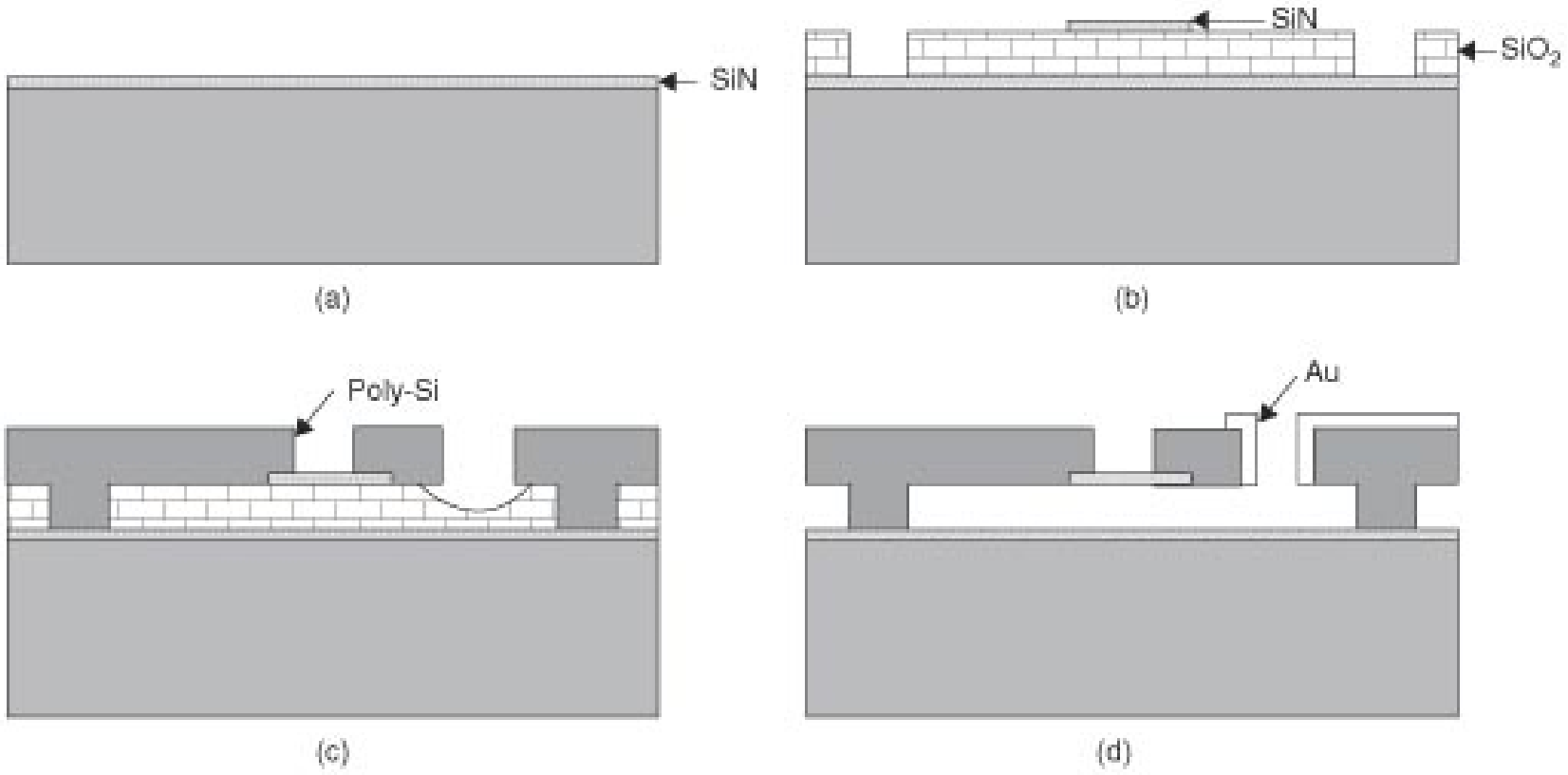


Sideways movement thermal relay



Wang, Y. et al: A low-voltage lateral MEMS switch with high RF performance, J.MEMS 13 (2001) pp. 902-911

Sideways movement thermal relay



Wang, Y. et al: A low-voltage lateral MEMS switch with high RF performance, J.MEMS 13 (2001) pp. 902-911

Hinged structures (1)

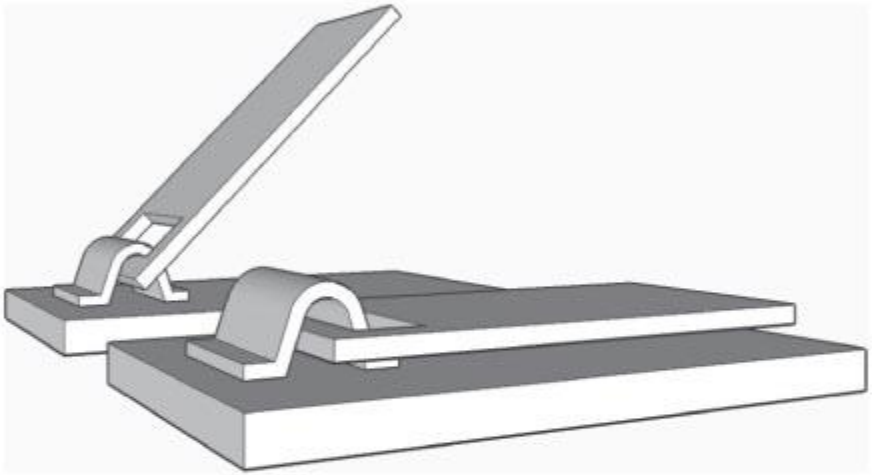


Figure 29-22

Two-poly staple hinge. Adapted from Pister *et al*. (1992) by Jorma Koskinen.

Hinged structures (2)

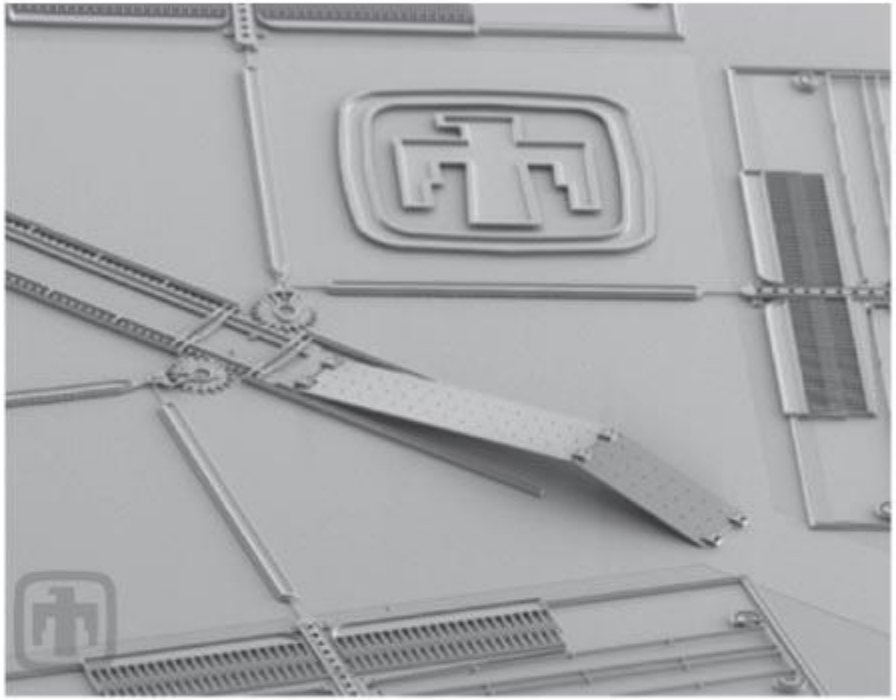


Figure 29-23

Comb-drive actuator–gear system lifts up a hinged mirror.
Courtesy Sandia National Laboratories.

Hinged structures (3)

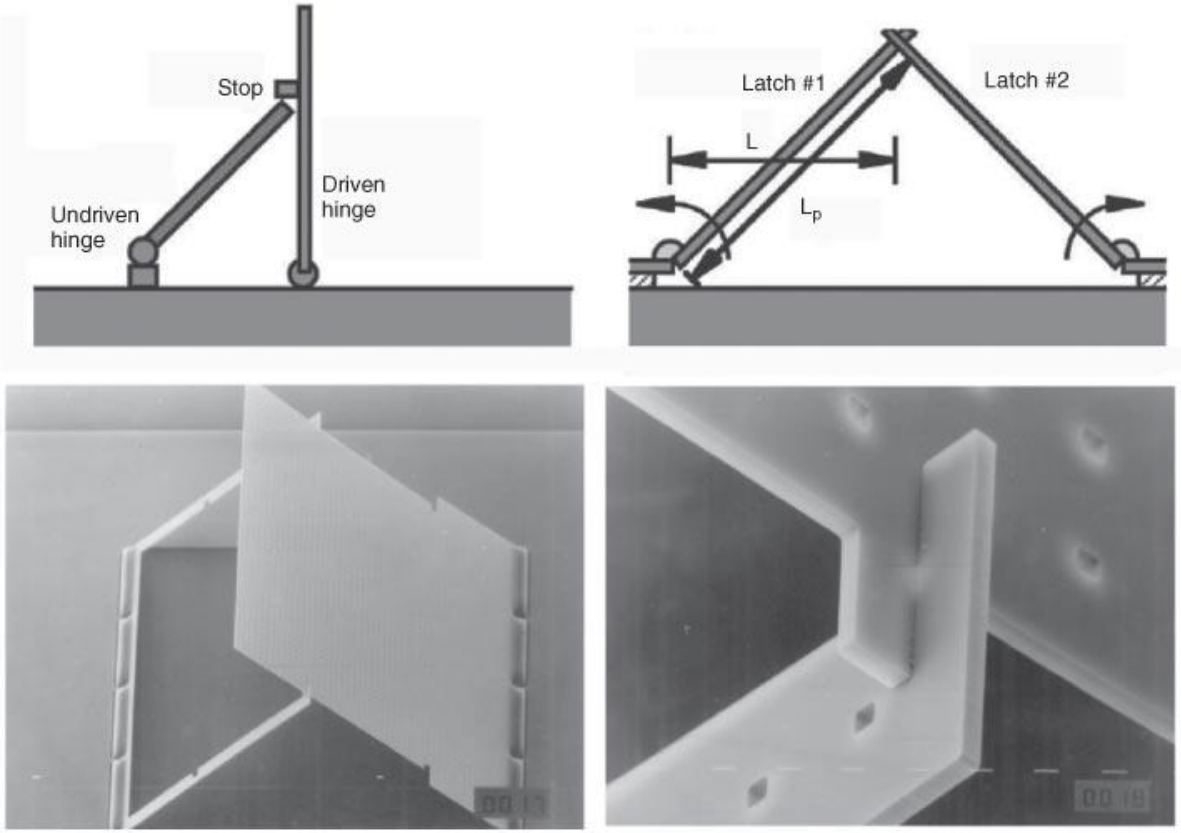
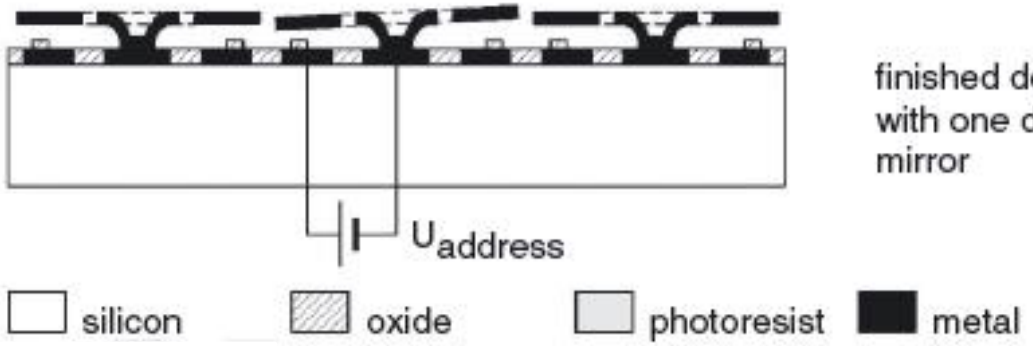
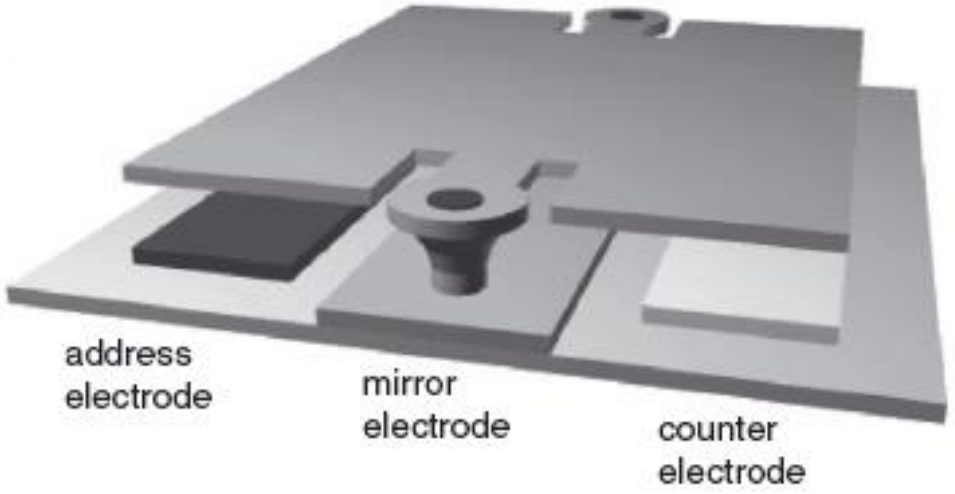


Figure 29-24

Pop-up mirrors with latches. Reproduced from Syms *et al.* (2001), copyright 2001, by permission of IEEE.

µ-mirror array on CMOS





Ljungblad, U. et al: New laser pattern generator for DUV using a spatial light modulator, Microel.Eng. 57–58 (2001) pp. 23–29

Bulk

<Si> structure heights
380 µm/500 µm
(= thru-wafer)

Etched either by KOH or by DRIE.

Hard mask (e.g. SiO_2) needed for thru-wafer etching.

SOI

Device functionality in SOI device layer

5-50 µm typical device layer thicknesses

Utilizes DRIE to make closely spaced structures like comb-drives.

Aspect ratios e.g. 10:1 or 20:1

Surface

Device functionality is in thin films (oxide, nitride, poly, aluminium…).

Substrate usually silicon, but can be glass, sapphire,…

Structure heights 1-2 µm (= typical sputter & CVD film thicknesses).

Isotropic sacrificial etching must be used.