# Economics of microfabrication

(mostly chapter 37, some 31 stuff)

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# Microindustries are big

| | |
|---|---|
| Integrated circuits | $550 B |
| Other semiconductors | $115 B |
| (of which MEMS/sensors | $21 B) |
| Flat panels displays | $130 B |
| Solar cells | $170 B |
| Hard disks | $35 B |
| | |
| Equipment | $100 B |
| Materials | $50 B* |

Best source: semi.org

* Includes packaging materials, leadframes etc.

2021 data

# Fab size scaling

| Year | Wafer size | LW | WPM* |
|---|---|---|---|
| 1970 | 3” | 10 µm | 1000 |
| 1980 | 100 mm | 2 µm | 5000 |
| 1990 | 150 mm | 0.8 µm | 10 000 |
| 2000 | 200 mm | 0.18 µm | 20 000 |
| 2010 | 300 mm | 32 nm | 50 000 |
| 2020 | 300 mm | 11 nm | 100 000 |

* Fab size measure: Wafer starts per month

# Fab cost scaling

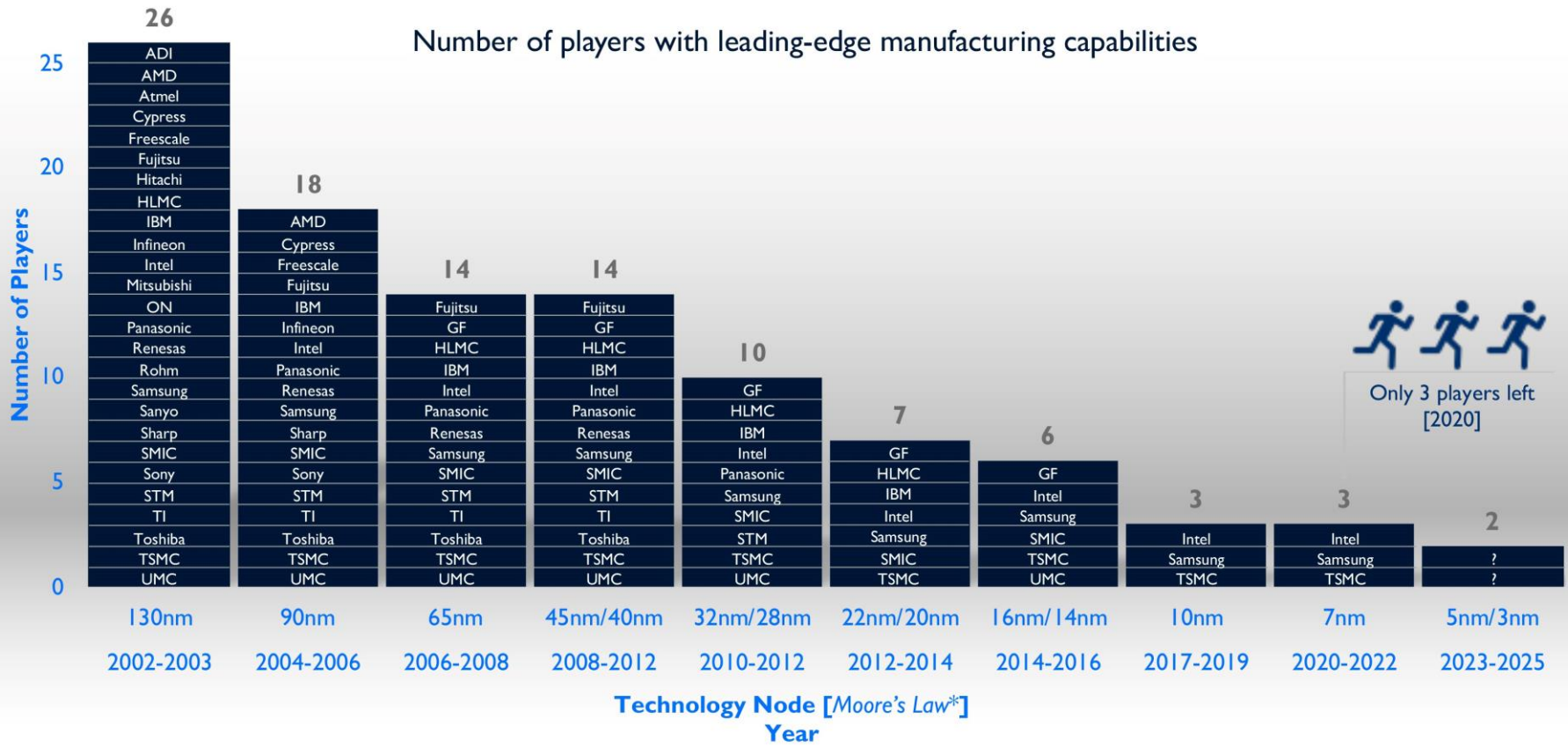
| | |
|---|---|
| 1957 | 0.2 M$ |
| 1967 | 2.5 M$ |
| 1977 | 10 M$ |
| 1987 | 100 M$ |
| 1997 | 1000 M$ |
| 2007 | 3000 M$ |
| 2017 | 6000 M$ |

Economist 2018:
TSMC new fab will cost $20B.

Economist 2023:
Samsung will invest $230B in 10 years.

# Semiconductor industry evolution

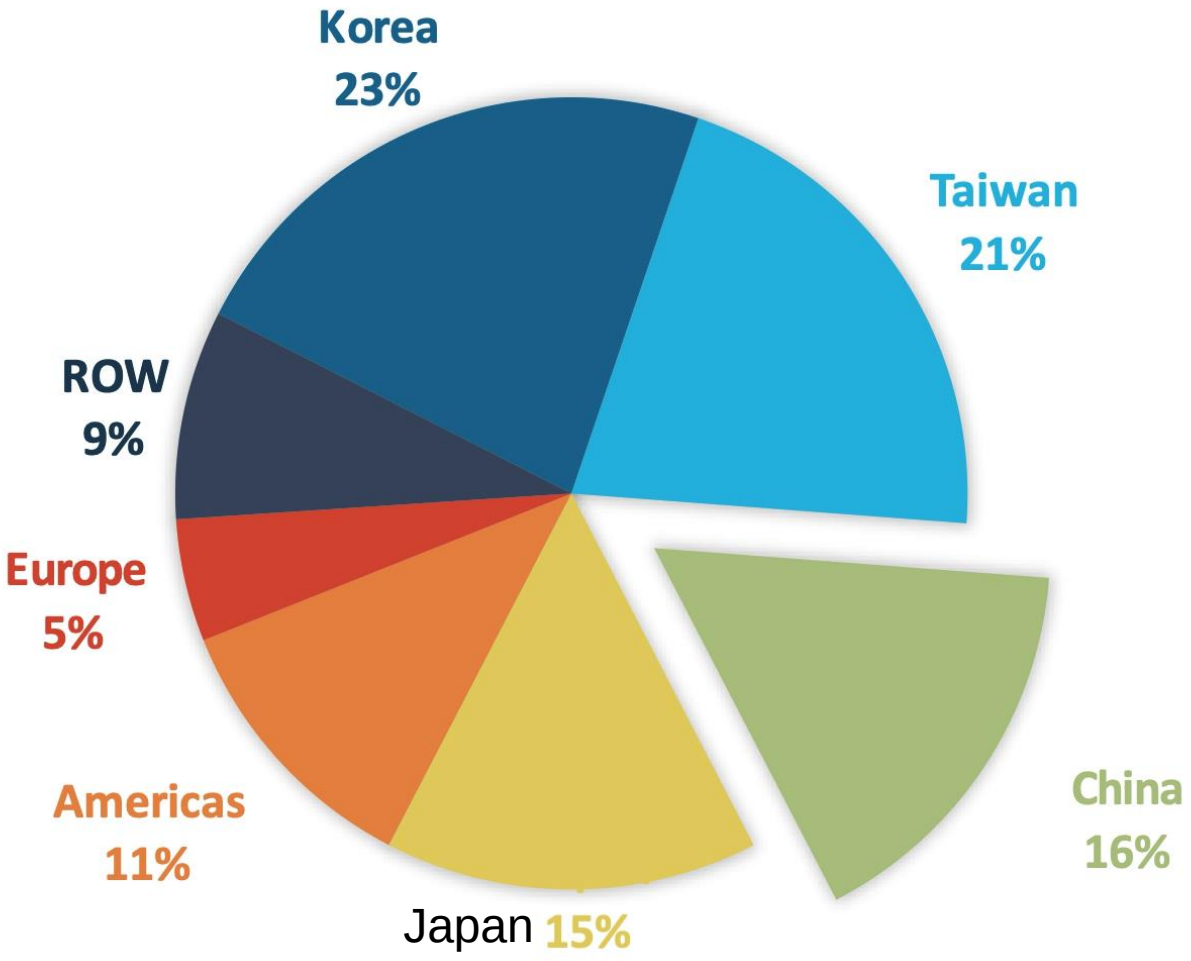
*(Source: High-End Performance Packaging: 3D/2.5D Integration report, Yole Développement, 2020)*




* Moore's law states that the number of transistors in an integrated circuit chips doubles every 2 years
Data referenced from Intel and WikiChip

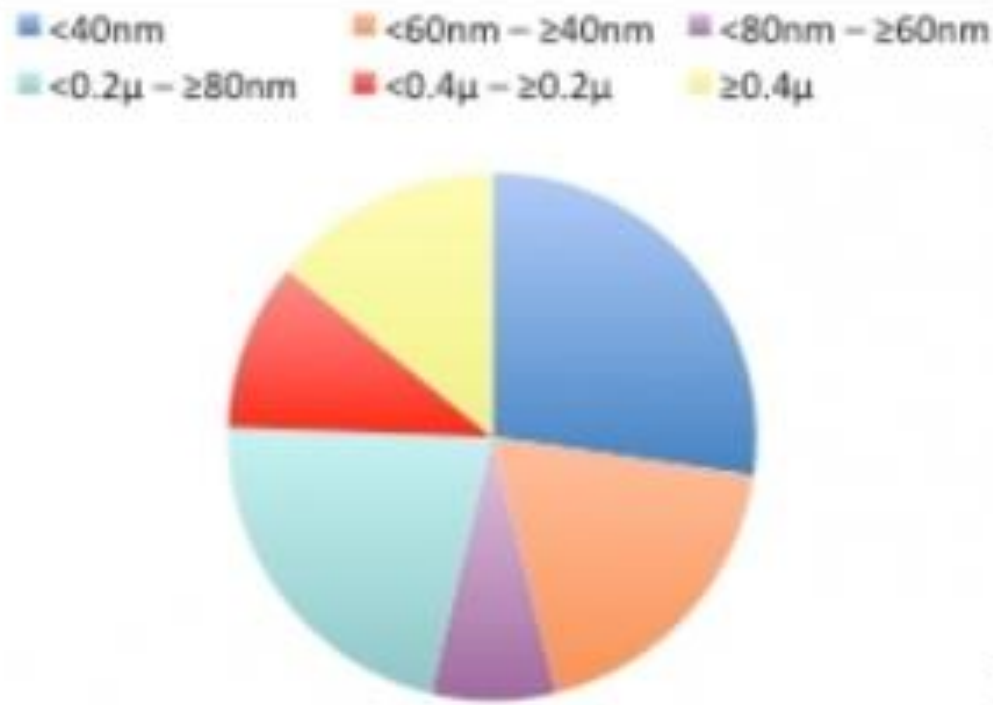
# Global IC Wafer Capacity at Dec-2021 – by Fab Location

(21.6M 200mm-equiv. Wafers per Month)



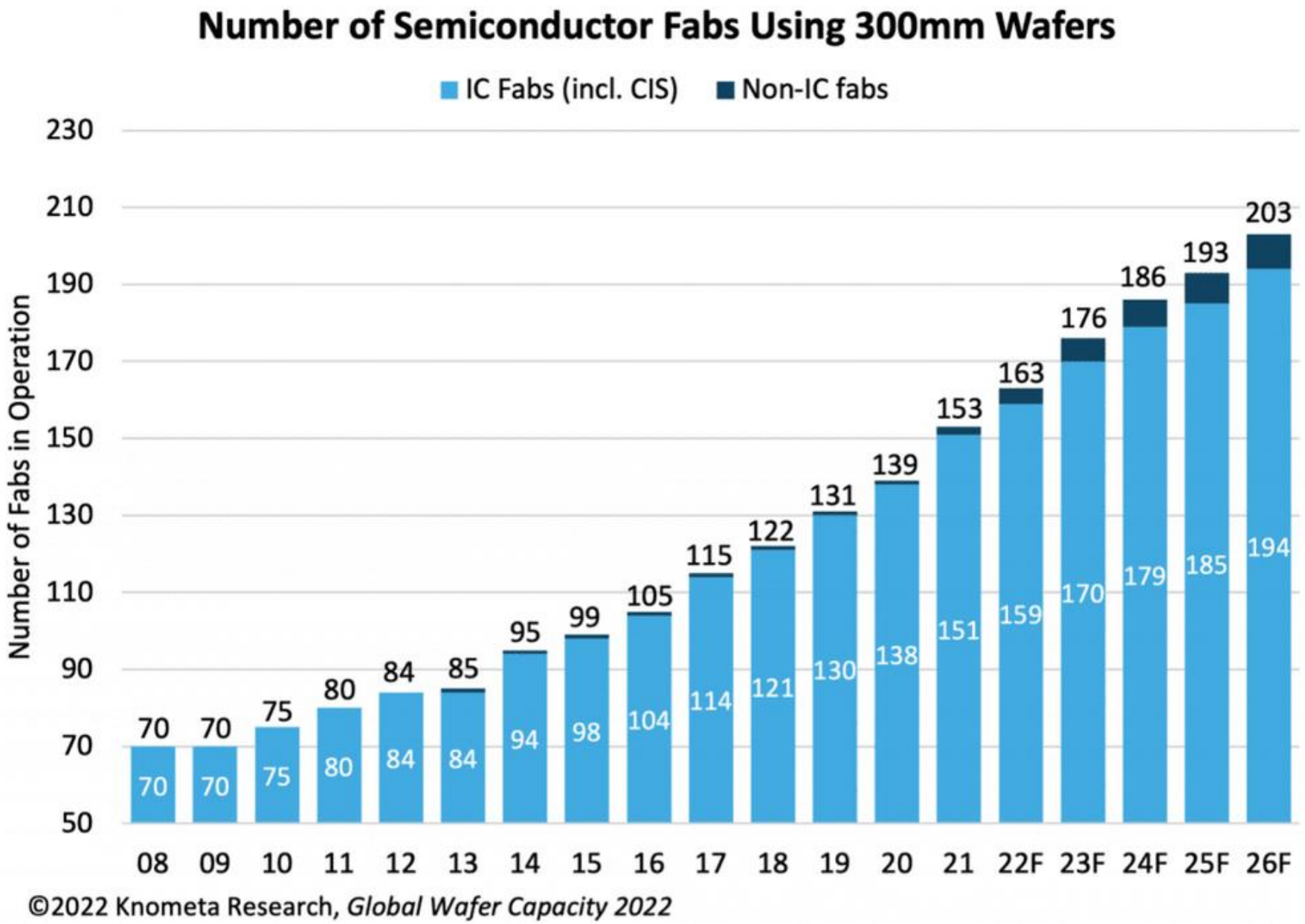
# Worldwide Capacity by Minimum Geometry as of Dec-2012

## (Installed Monthly Capacity in 200mm-Equiv. Wafers x1000)



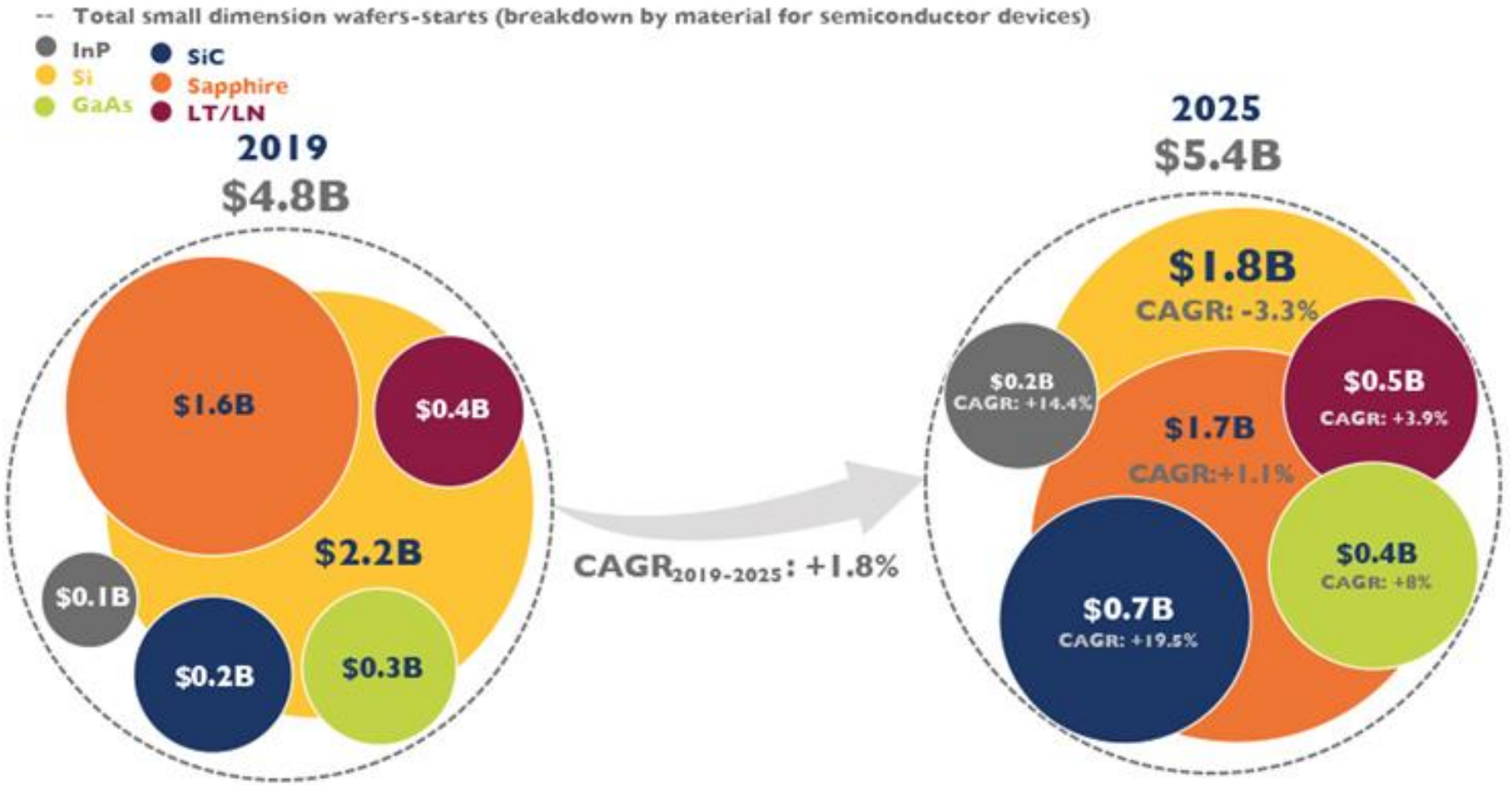

| Minimum Geometry | Installed Capacity (K w/m) | % of Worldwide Total |
|---|---|---|
| <40nm | 3,963.1 | 27.3% |
| <60nm – ≥40nm | 2,721.0 | 18.8% |
| <80nm – ≥60nm | 1,106.6 | 7.6% |
| <0.2µ – ≥80nm | 3,165.5 | 21.8% |
| <0.4µ – ≥0.2µ | 1,495.8 | 10.3% |
| ≥0.4µ | 2,044.9 | 14.1% |
| TOTAL | 14,497.0 | 100% |

Source: IC Insights


Number of Semiconductor Fabs Using 300mm Wafers
IC Fabs (incl. CIS)
Non-IC fabs
Number of Fabs in Operation
230
210
190
170
150
130
110
90
70
50
08 09 10 11 12 13 14 15 16 17 18 19 20 21 22F 23F 24F 25F 26F
70 70 75 80 84 85 95 99 105 115 122 131 139 153 163 176 186 193 203
70 70 75 80 84 84 94 98 104 114 121 130 138 151 159 170 179 185 194
©2022 Knometa Research, *Global Wafer Capacity 2022*

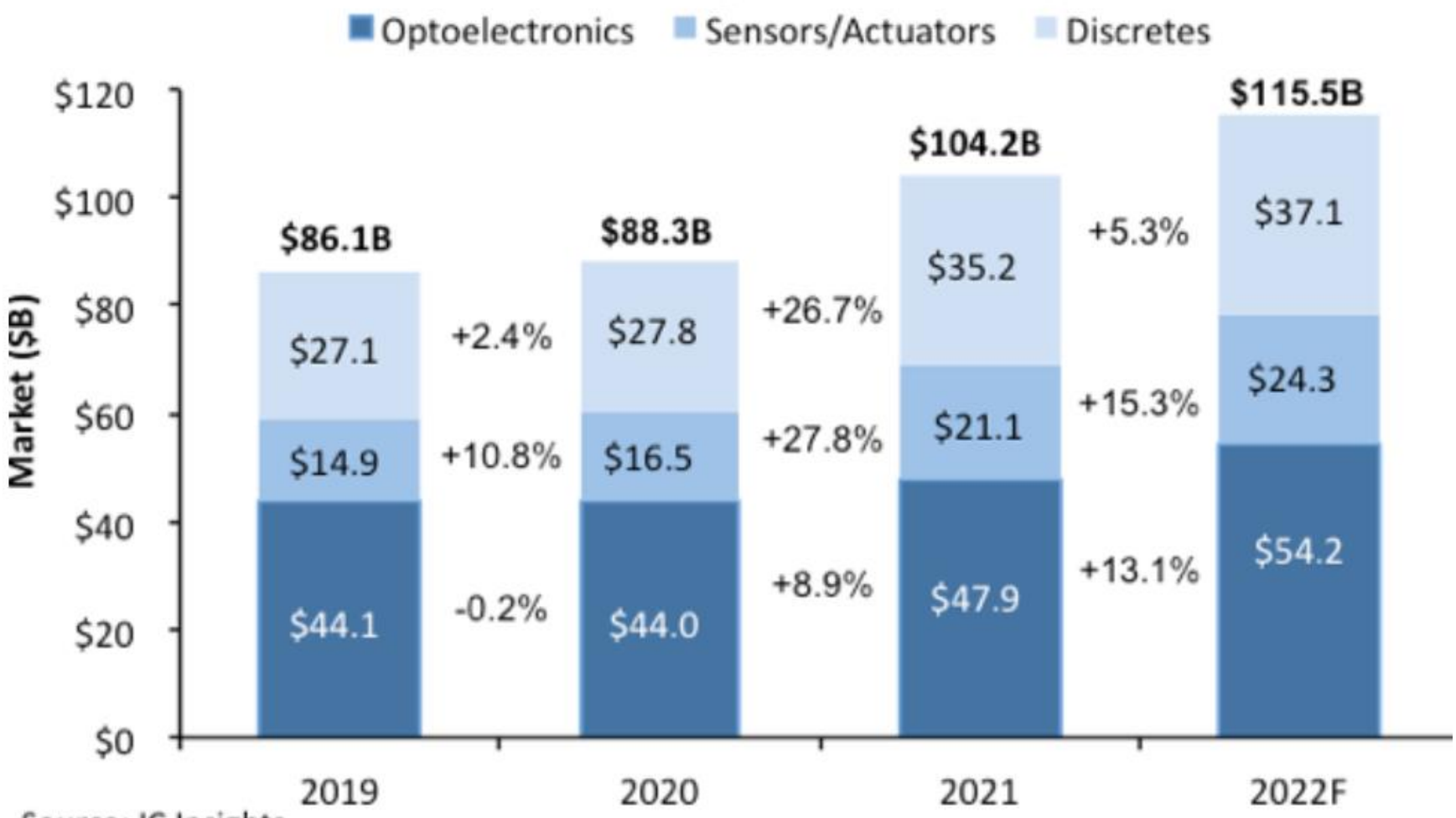
# 2019-2025 total annual small dimension (≤ 6'') market in revenues

*(Source: 6'' and Below: Small-Dimension Wafer Market Trends 2020, Yole Développement, September 2020)*




Yole development

# O-S-D Sales by Market Segments




Source: IC Insights

# Silicon consumption*

| | 2014 | 2015 | 2016 | 2017 | 2018 | 2019 | 2020 |
|---|---|---|---|---|---|---|---|
| Millions of square inch | 10,098 | 10,434 | 10,738 | 11,810 | 12,732 | 11,810 | 12,407 7 $km^2$ |
| Billions of dollars | 7.6 | 7.2 | 7.2 | 8.7 | 11.4 | 11.2 | 11.2 |

* Solar cell silicon is not included in this data.

Source: SEMI (www.semi.org), January 2021

# Silicon production

| | 2012 | 2013 | 2014 | 2015 | 2016 | 2017 | 2018 | 2019 | 2020 | 2021 | 2022 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Area Shipments (MSI) | 9,031 | 9,067 | 10,098 | 10,434 | 10,738 | 11,810 | 12,732 | 11,810 | 12,407 | 14,165 | 14,713 |
| Revenues ($Billion) | 8.7 | 7.5 | 7.6 | 7.2 | 7.2 | 8.7 | 11.4 | 11.2 | 11.2 | 12.6 | 13.8 |

Source: SEMI (www.semi.org), February 2023

MSI = million square inch

14713 MSI = 9.5 $km^2$

Silicon price = 13.8B/9.5 $km^2$
= 15 $c/cm^2$

# Silicon wafer costs and prices

- ~11 billion dollars used for silicon wafers
- ~ 7 $km^2$ of silicon wafers used

➔300 mm wafer (700 $cm^2$ ) ≈ 100 dollars
➔140 million wafers annually

A big fab has 100 000 wafer starts per month (WPM)
➔No more than ~140 big wafer fabs in the world
➔(compare slide 6: 176)

# Cost of processed silicon

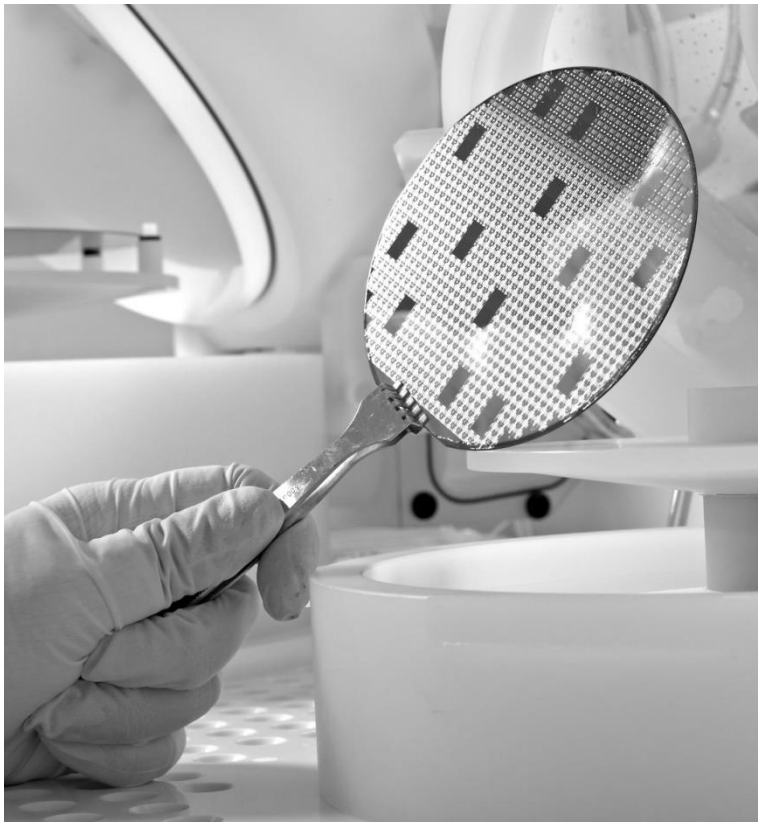
IC industry annual turnover (2022) 574 billion,

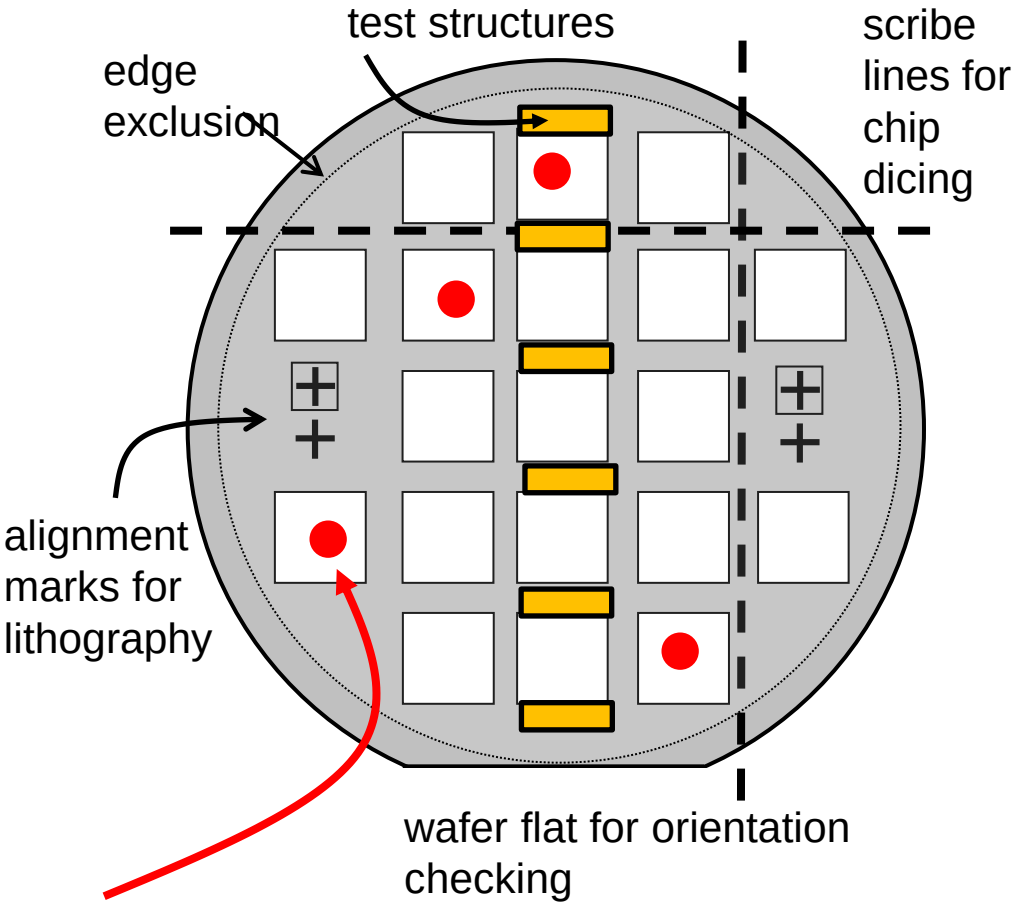
Price of processed silicon is:
$574*10^9\$/9.5*10^{10}cm^2 \approx 6\ \$/cm^2$

Because profits are very small, the cost of processing silicon is close to 6 $\$/cm^2$

Silicon wafer cost  is only ~2% of IC cost

# Real estate: area usage on wafer



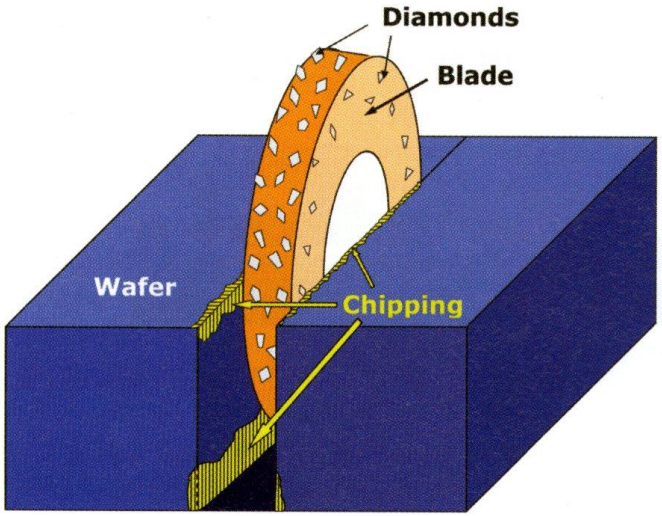



Inked chip = after electrical testing
non-functional chips are inked

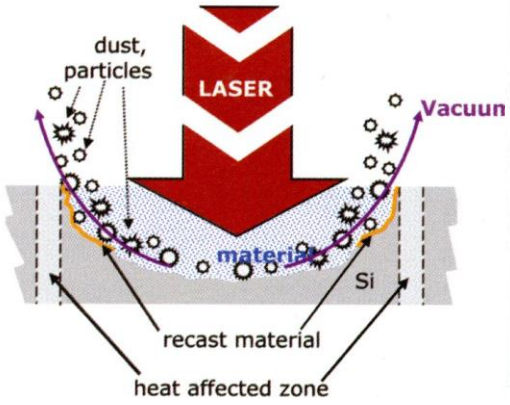
Note: chip = die

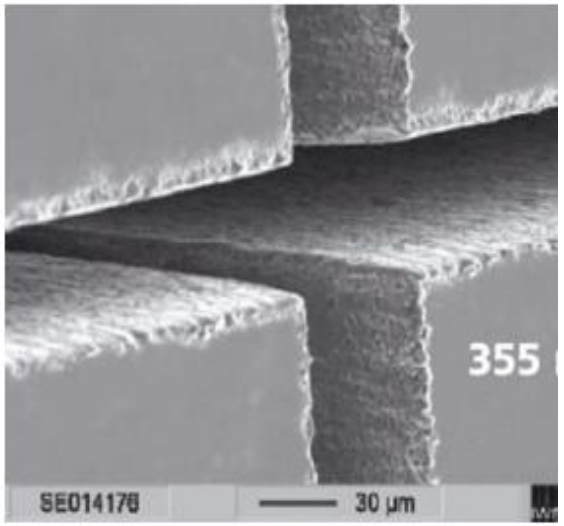
# Dicing wafer into chips

## Diamond blade saw



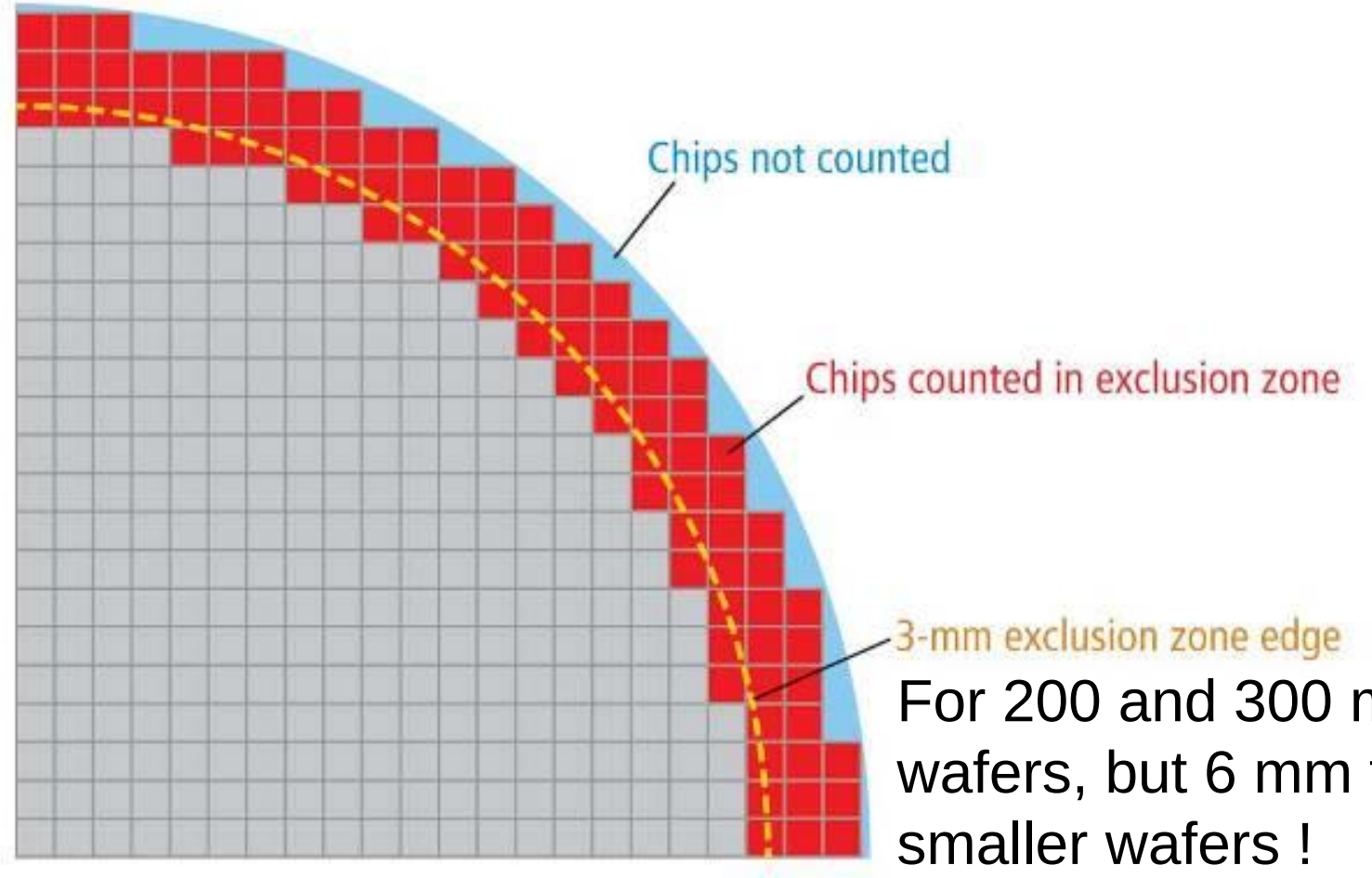

## Laser dicing




Blade width or laser spot is e.g. 50 µm, but damaged area is larger ➔ need e.g. 100 µm between chips.

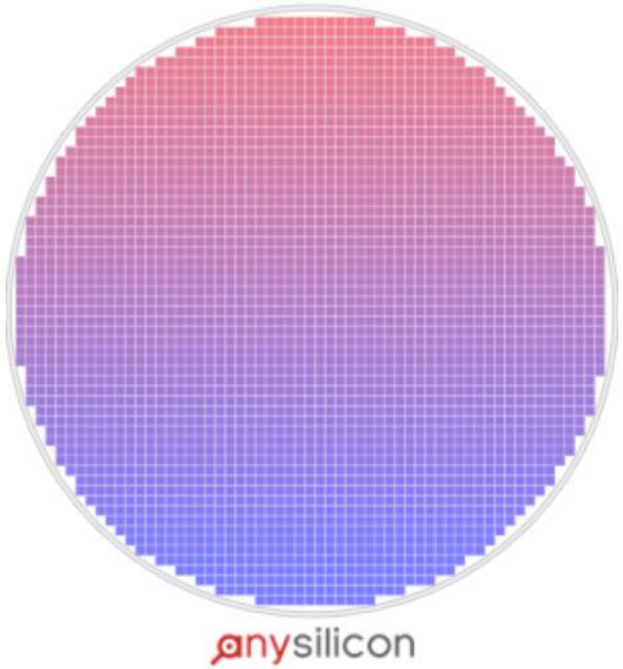
# Useful chips & edge exclusion



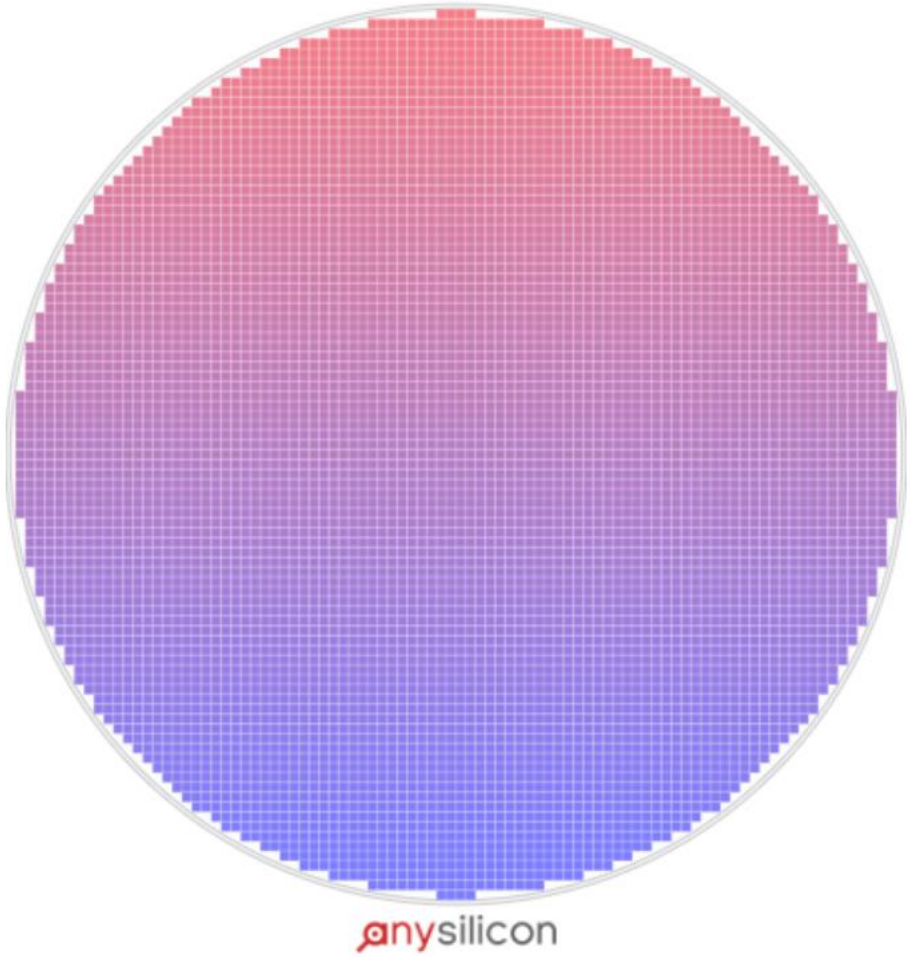

For 200 and 300 mm wafers, but 6 mm for smaller wafers !

# 200 mm vs. 300 mm
# 10 $mm^2$ chip

DPW (8"): 2745



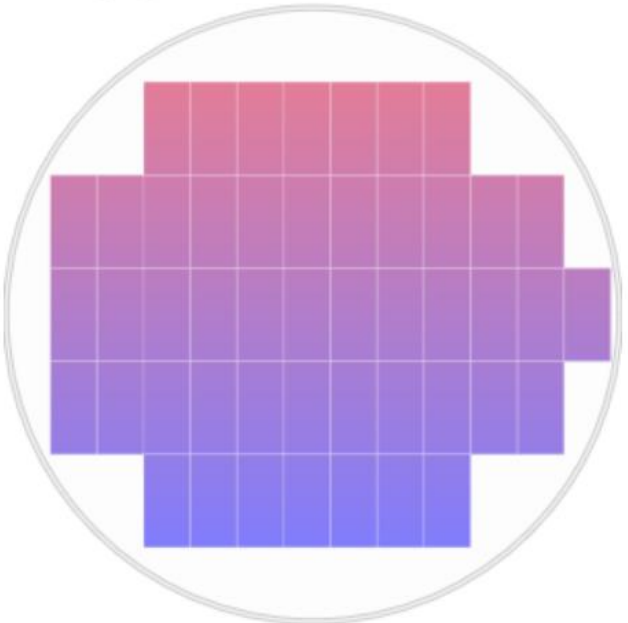

DPW (12"): 6334



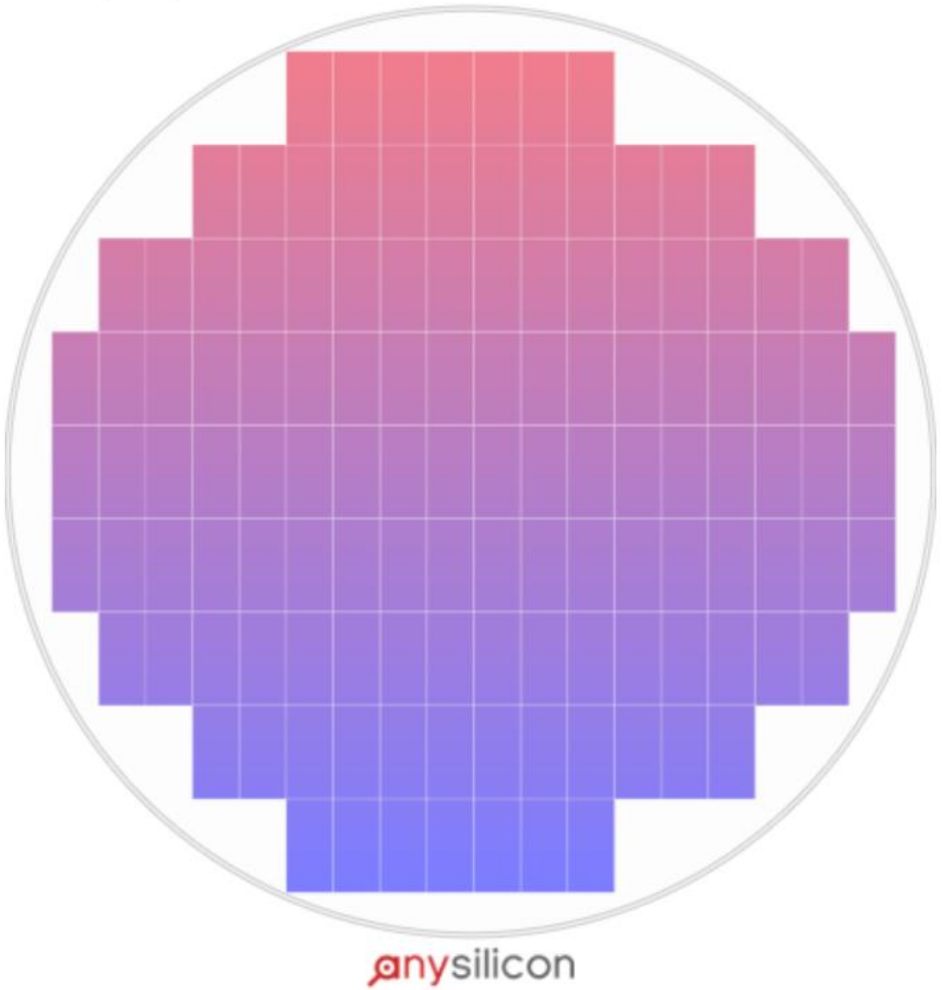
# 200 mm vs. 300 mm

## 30*15 mm chip

DPW (8"): 48




DPW (12"): 124



# Chip size vs. wafer size

Chip calculator:
https://anysilicon.com/die-per-wafer-formula-free-calculators/

200 mm wafer, chip size 10 $mm^2$ ➔ 2700 die
300 mm wafer, chip size 10 $mm^2$ ➔ 6300 die

Cost of processed silicon is 6 $/$cm^2$,
200 mm wafer ➔ 1900 $ ➔ 0.70 $/die
300 mm wafer ➔ 4200 $ ➔ 0.67 $/die ➔ 4% reduction

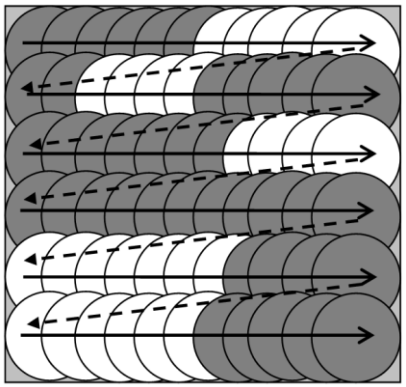
200 mm, 4 $cm^2$ ➔ 48 die ➔ 40 $/die
300 mm, 4 $cm^2$ ➔ 124 die ➔ 34 $/die ➔ 15% reduction

# Electron beam lithography (EBL)

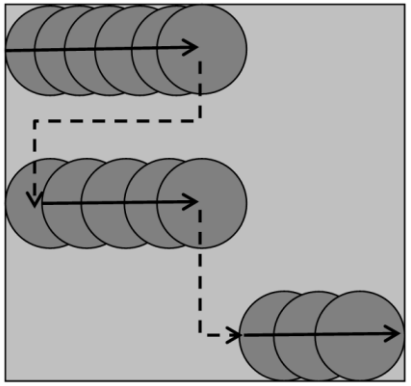
Use electrons instead of UV photons to expose the resist.

Needs no photomask, just scan the wafer, and shoot an electron dose at those pixels that need exposure. Fantastic time and cost savings possible, because no mask cost and no wait time for mask delivery.

The problem is that even a 100 mm wafer may contain$10^{10}$ pixels, and writing the whole wafer can take hours, or even days.



Raster scan EBL: scan the whole field and make expose/skip decision at every pixel.



Vector scan EBL: smart skipping of pixels that do not need exposure.

# E-beam lithography vs. optical

Assuming 90 nm CMOS process (30 litho steps):

- identical capital investment (10 M$)
- Identical running costs (1 M$/year)

Thruput: (on 300 mm wafers)

- 100 wafers/hour for optical  (WPH)
- 1 wafer per hour for EBL

90 nm mask set (30 masks) cost is $500 000.
EBL needs no masks.

# EBL vs. optical (2)

Optical litho cost over 5 years:

$15M/4.3M exposures = $3.5 for each litho step

EBL cost over 5 years:

$15M/43800 exposures= $350 for each litho step

Advanced CMOS has 30 mask levels

➔ cost of optical litho is 100 $/wafer

➔ cost of EBL litho is 10000 $/wafer

# EBL vs. optical (3)

1 wafer by optical lithography is 500 100$

10 wafers $500 000 + $1000 = 501 000 $

100 wafers $500 000 + $10000 = 510 000 $

1000 wafers $500 000 + $100000 = 600 000 $

For EBL:
1 wafer = $10 000 $
10 wafers = $100 000 $
100 wafers = $1 000 000 $
1000 wafer = $ 10 000 000 $

The breakeven is roughly 50 wafers.
This means ~5 000 – 100 000 chips ➔ maybe industrial equipment, military app, medical app; not consumer !

# Cost of ownership (CoO)

$$CoO = \frac{\text{capital cost} + \text{operating cost} + \text{yield cost}}{\text{throughput} \times \text{utilization}}$$

Thruput: how many wafers per hour

Utilization: percentage of time tools is producing chips for sale (other times idle, in repair, or running test wafers)

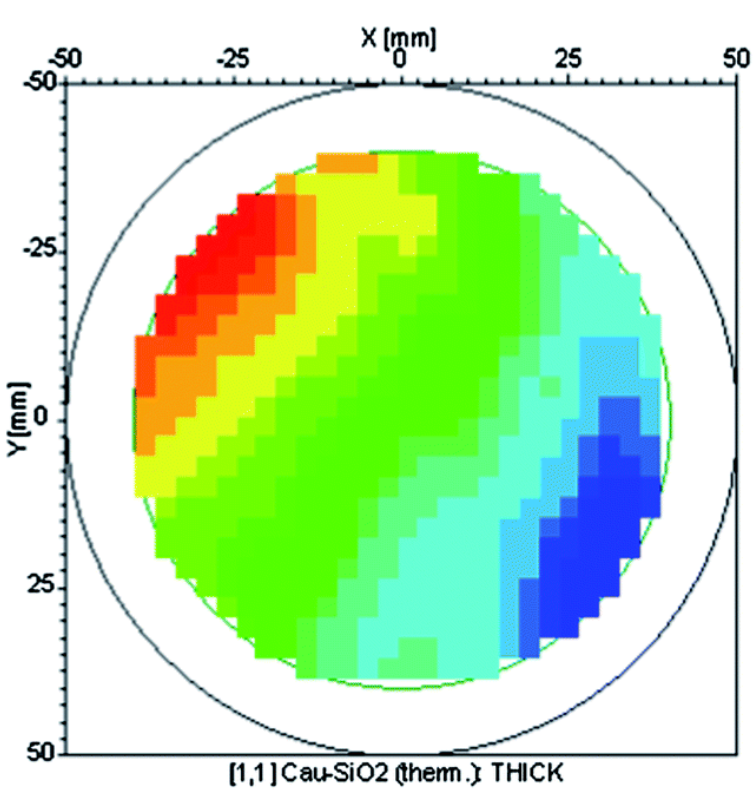
Yield cost: value lost due to non-functional chips.
If memory wafer has 200 chips worth $20, and yield is 95%, 5% of chips scrap = 10 chips ➔ yield cost is $200/wafer.

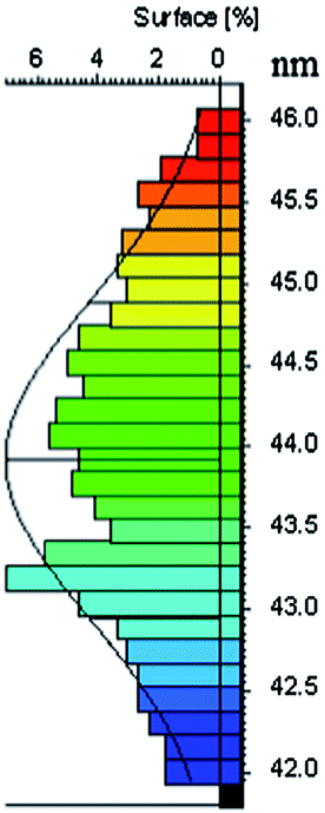
# Cost-of-ownership for RIE

| | A | B |
|---|---|---|
| Purchase price | 1 000 000 € | 1 500 000 € |
| Operating costs | 250 000 €/yr | 120 000 €/yr |
| 5 years costs | 1 750 000 € | 2 100 000 € |
| Utilization | 85% | 90% |
| Throughput | 45 WPH | 55 WPH |
| Wafers/5 yrs | 1.68M | 2.17M |
| Yield | 99% | 99.8% |
| Good wafers | 1.66M | 2.16M |
| Cost/good wafer | 1.05 € | 0.97 € |

# Mapping and uniformity

To check something across the wafer, we must have a quick monitoring measurement that can be repeated many times.



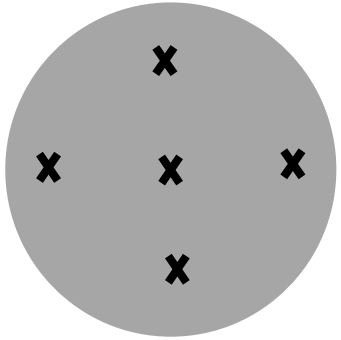




Ellipsometer measurement of oxide thickness, takes a second per data point.

http://pubs.rsc.org/en/content/articlehtml/2014/tc/c4tc00046c

# (Non)Uniformity

$$U = \frac{\max - \min}{2 \cdot average}$$



$$U = \frac{\max - \min}{\max + \min}$$

Thermal oxidation
Spin coating
ALD

} Excellent uniformity, 1%

RIE
CVD
Sputtering

} Uniformity 3-5%

CMP — 10% uniformity

# Cost of measurement

If the wafer cannot be returned to process ➔ tens of euros

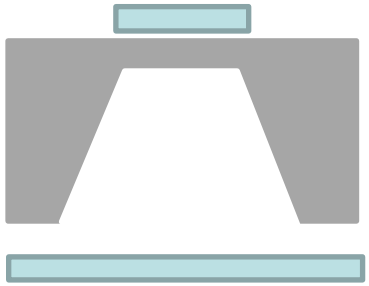
Measurement equipment capital cost 100 000 €
operator cost 100 000€ for 5 years

1 sec/measurement,
49 points/wafer ➔ 1500 wafers/day,
2.5 million/5 years
➔ cost of mapping the wafer is 8 cents.

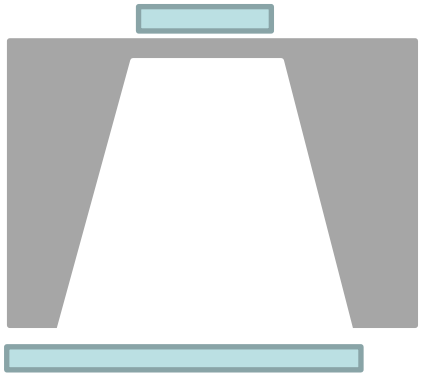
If 20 000 chips/wafer ➔ 4 µcents/chip

# Wafer thickness scaling in MEMS

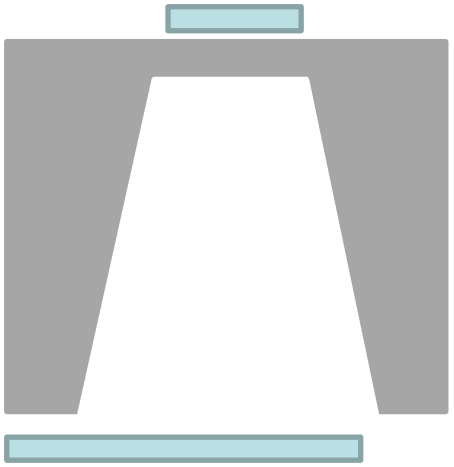
3” mm/380 µm



100 mm/525 µm

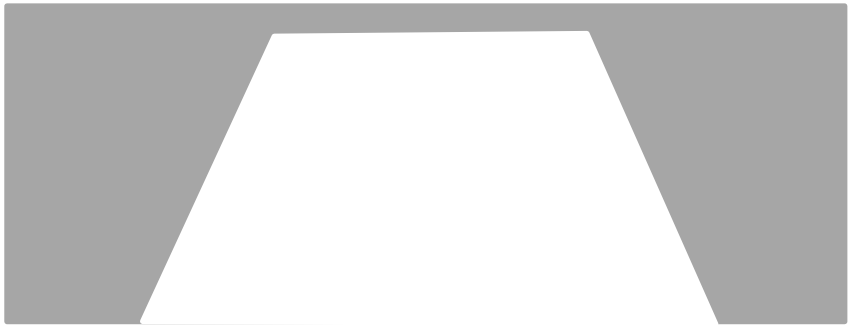


150 mm/675 µm



Slanted sidewall from KOH wet etching wastes area.

# Pressure sensor scaling



$$\sigma = \frac{1.02\,pa^2}{h^2}$$

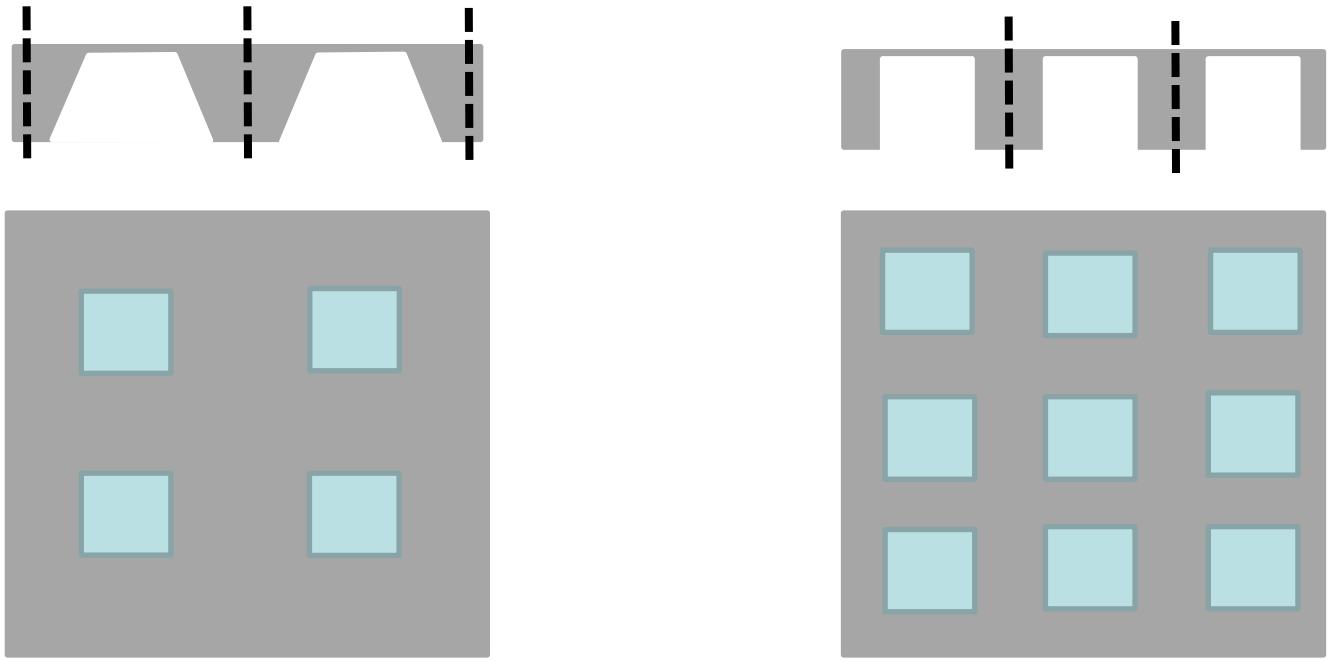
σ = stress
p = pressure
a is membrane edge length
h is membrane thickness

Membrane edge length is scaled 50%
➔ Membrane thickness needs to be scaled 50% to keep stress the same, for same pressure.

# Cost scaling in MEMS

Chip edge scaling 50% ➔ chip area scaling by 75%

100 wet etched chips ➔ >200 DRIE chips can be fitted



# KOH etching

200 000 € wet bench
25 wafers in batch
400 min/etch (≈8 h ➔ 3/day)
KOH cost 10 €/batch
Operator cost 10€/batch

5 year cost:
200 000+ (5*365*3*20)
≈ 300 000 €
5 year wafers: 5*365*3*25 ≈ 130 000 wafers
➔ **2.3 €/wafer**

# DRIE etching

500 000 € etcher
Single wafer, 20 µm/h
➔ 20 min/wafer = 3 WPH
Gas & operator cost 30€/day

5 year cost:
500 000 + (5*365*30)
≈ 550 000€
5 year wafers:
5*365*24*3 ≈ 130 000
➔ **4 €/wafer**
➔ BUT >TWICE AS MANY CHIPS/WAFER !!

# MEMS accelerometer cost (1)

**Assumptions (for a small fab):**

| | |
|---|---|
| Cost of a fab | 20 M€ (cleanroom and equipment) |
| Operating cost | 10 M€/year (personnel, chemicals, …) |
| Wafer starts | 1500 WPM (=18 000 wafers per year) |
| Wafer cost | 20€ (150 mm silicon wafers) |
| Cap wafer | 10 € (150 mm glass wafers) |
| Die size | 1 $mm^2$ |
| Die/wafer | 1500 |
| Yield | 90% |

Note: salaries of design, sales, office… not included in this calculation !

# MEMS costs (2)

**5 year period:**
90000 silicon wafers processed
135 M total chips
120 M functional chips

**Costs (fixed cost + operating cost + wafer cost):**
20 M + (5*10 M) + (90000 * (20+10)) = 73 M€

**Cost per chip:**
73 M€/120 M functional chip ≈ 0.6 €

**Cost of a system:**
MEMS silicon chip is often 10-30% of total cost ➔ 2-6 €

**Note:**
These must be automotive/aerospace/medical chips, because mobile phone MEMS cost less than 1€.

# Quality measurements

- raw yield: working YES/NO
- parametric yield, within specs for
  - -threshold voltage
  - -power consumption…
- some parameters require package:
  - -phase angle drift
  - -temperature stability…
- testing cost can be > chip process cost !

# Packaged chip testing (2)

- accelerated tests (high voltage/high temperature)
- 85/85 (temperature/humidity)
- thermal cycling
- shock tests
- vibration tests (frequency !)
- pull tests (wires)
- pressure
- hermeticity
- chemicals (salts, ...)

# Summary

**Public data exists for many key variables:**

- Sales/turnover by companies
- Chip average selling prices (ASP) (needed for trade policy)
- Number of wafers sold annually
- Number of photomasks and photomask industry size (4 B USD)

**Proprietary data includes:**

- Yield
- Costs

**Many factors can be estimated**

- Cost of a fab (based on cleanroom area and technology)
- Cost of processed silicon as we did

**Many more can be calculated from the above !**