Yield. Reliability

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Chapter 36

Previous material

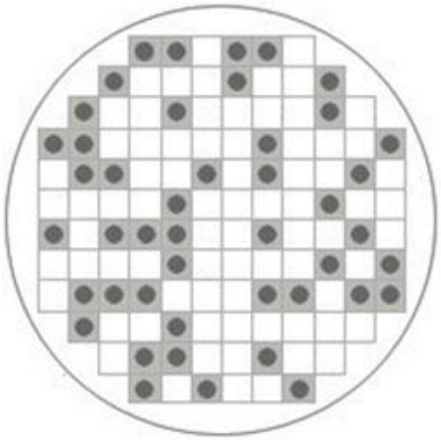
- CMOS
- MEMS

Content

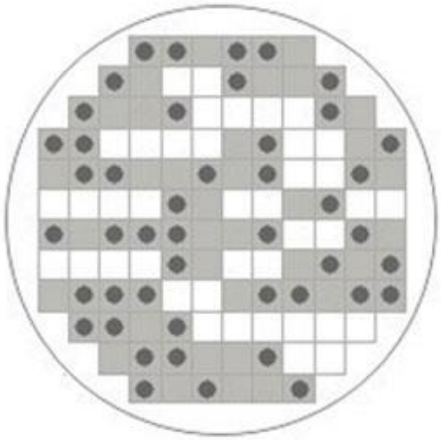
- Yield
- Failure mechanisms
- Reliability

Chip yield

$$\frac{\text{Total number of functional chips produced}}{\text{Number of designed chips}} \times 100 = \text{Yield}$$



(a) About 60% yield



(b) About 30% yield

SAMSUNG TOMORROW

Yield calculation

It is a quotient of good outcomes to total (wafers, chips)

$$Y = \frac{N_{good}}{N_{total}}$$

If a process consists of several steps

$$Y = \prod_i y_i$$

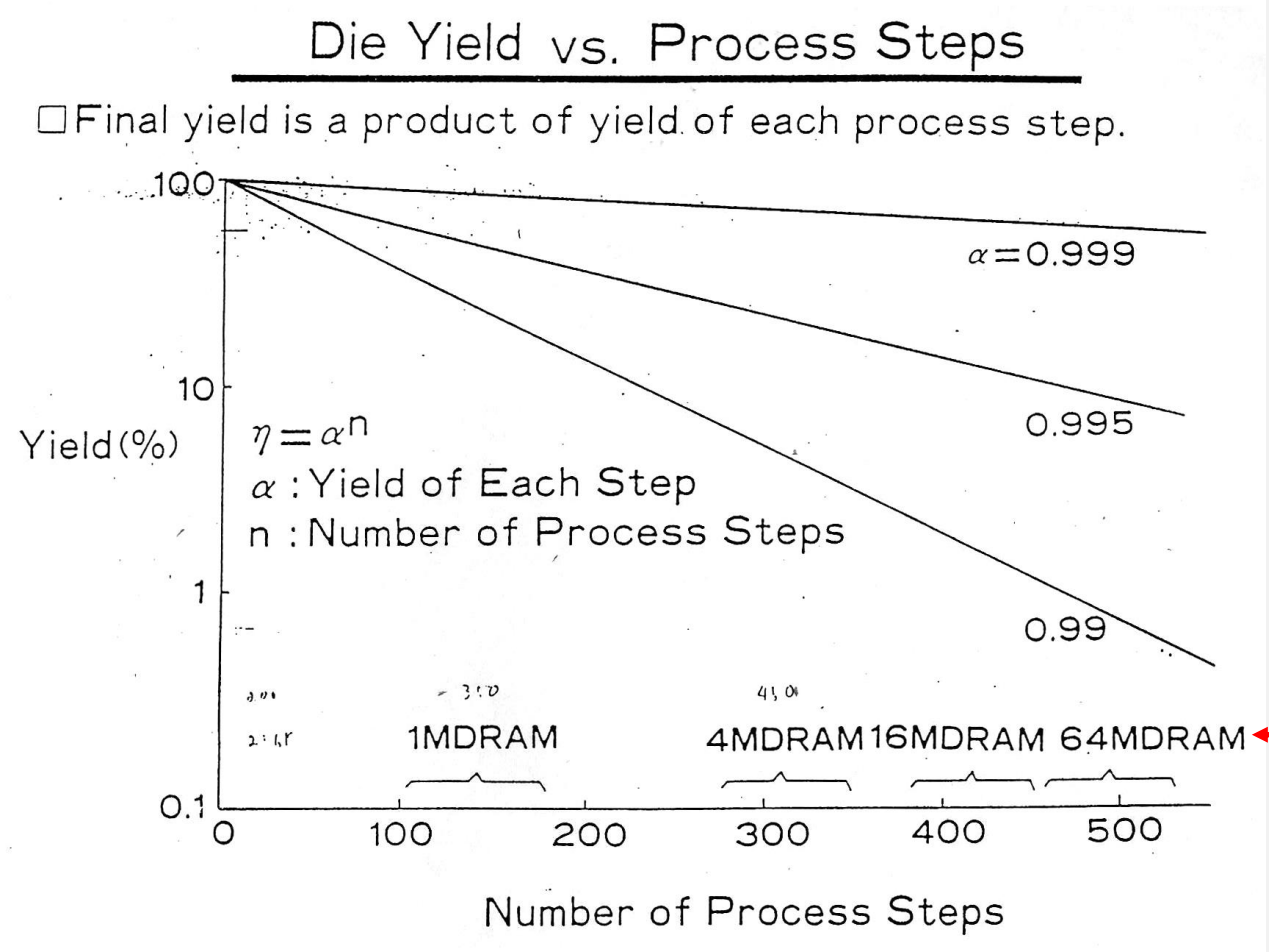
where *i* notes yield of individual step.

In case of systematic and random components

$$Y = Y_{sys} * Y_{rand},$$

global disturbance (wrong etching depth) Y_{sys} and spot defects (particles) Y_{rand}

Effect of process step number



$$Y = \prod_i y_i$$

y_i - yield of *i*-th step

Year - 1996
Node - 0.32 µm

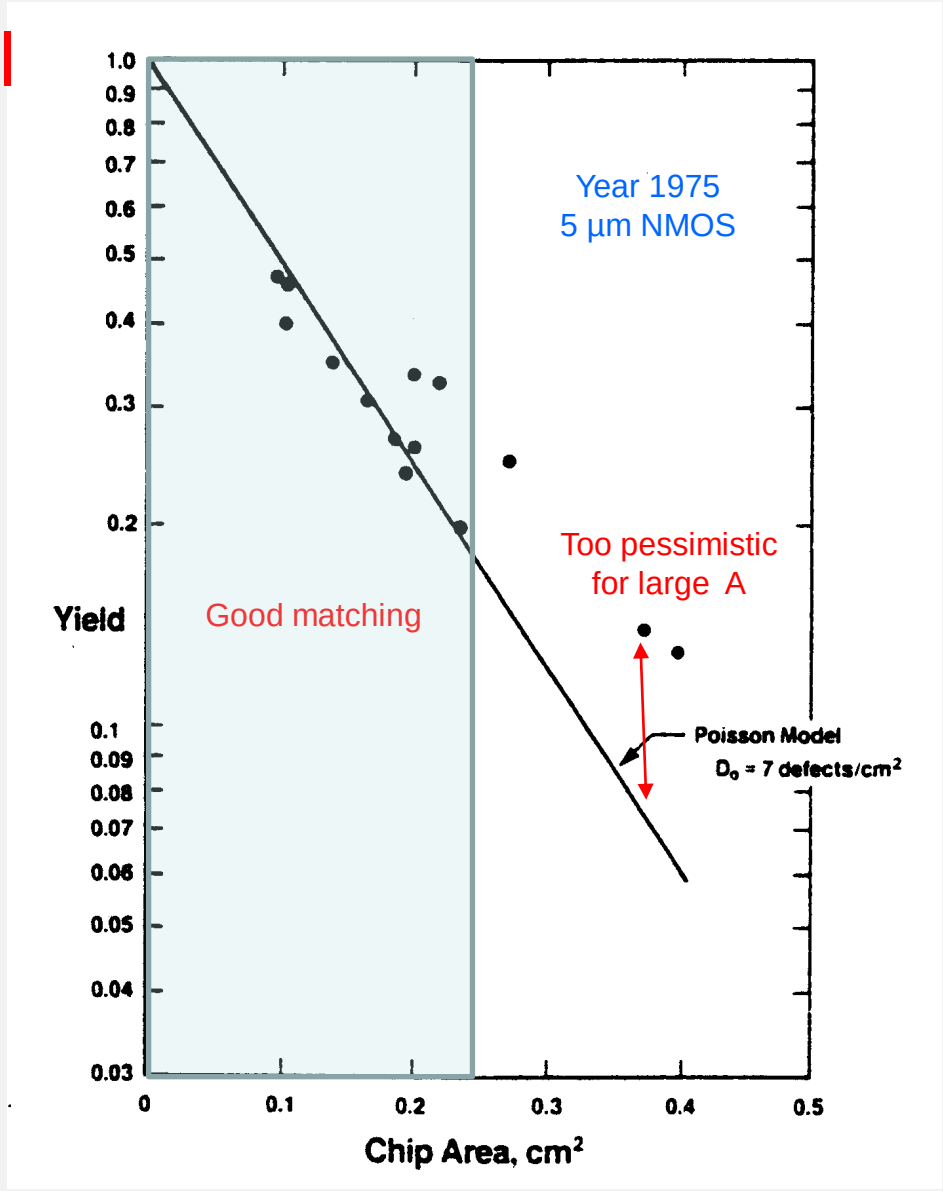
Poisson yield model

One parameter (D*A) distribution.
D*A –average number of faults per chip

The random-yield Y_{rand}

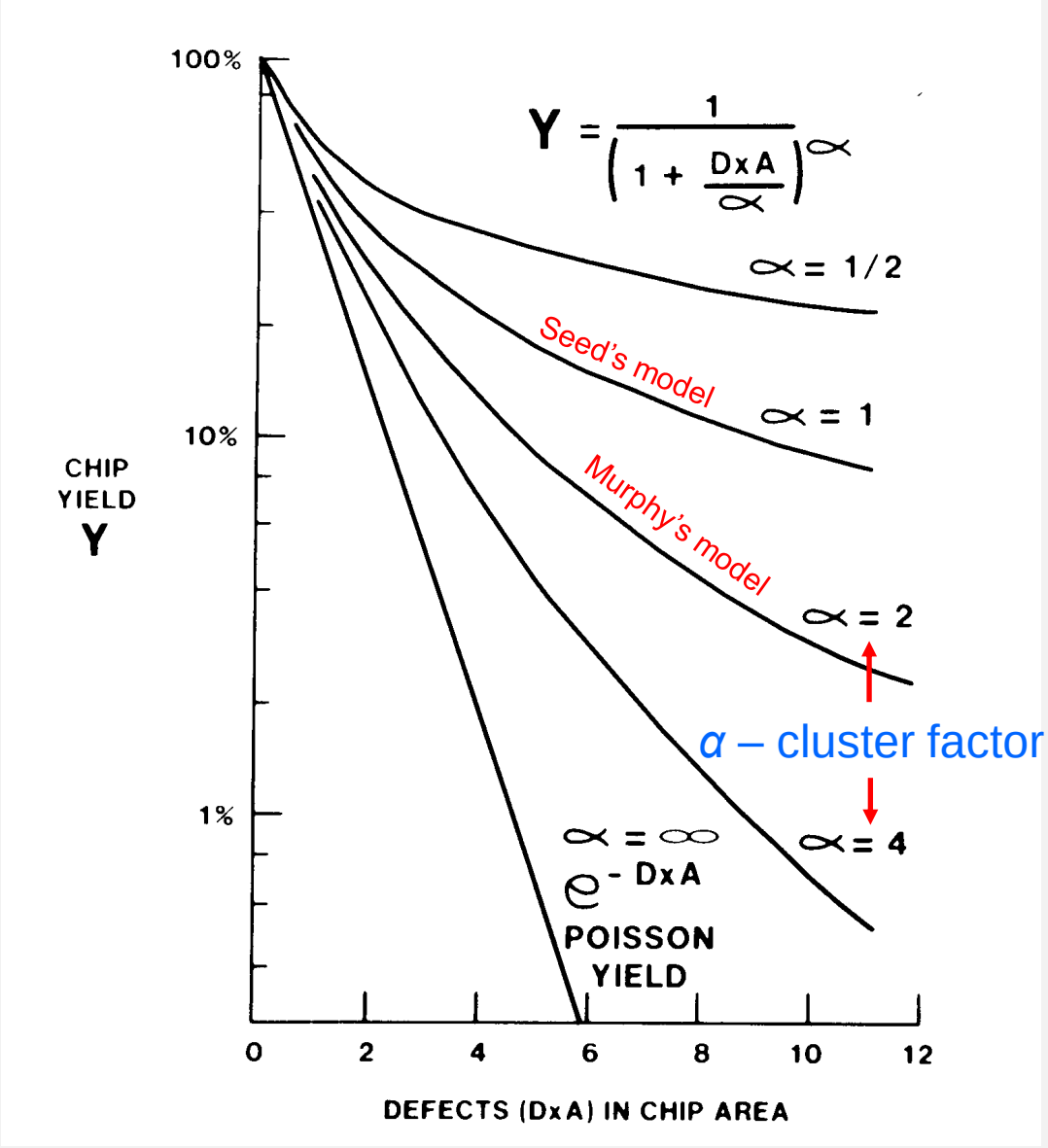
$$Y = e^{-DA}$$

D – defect density,
A – chip area

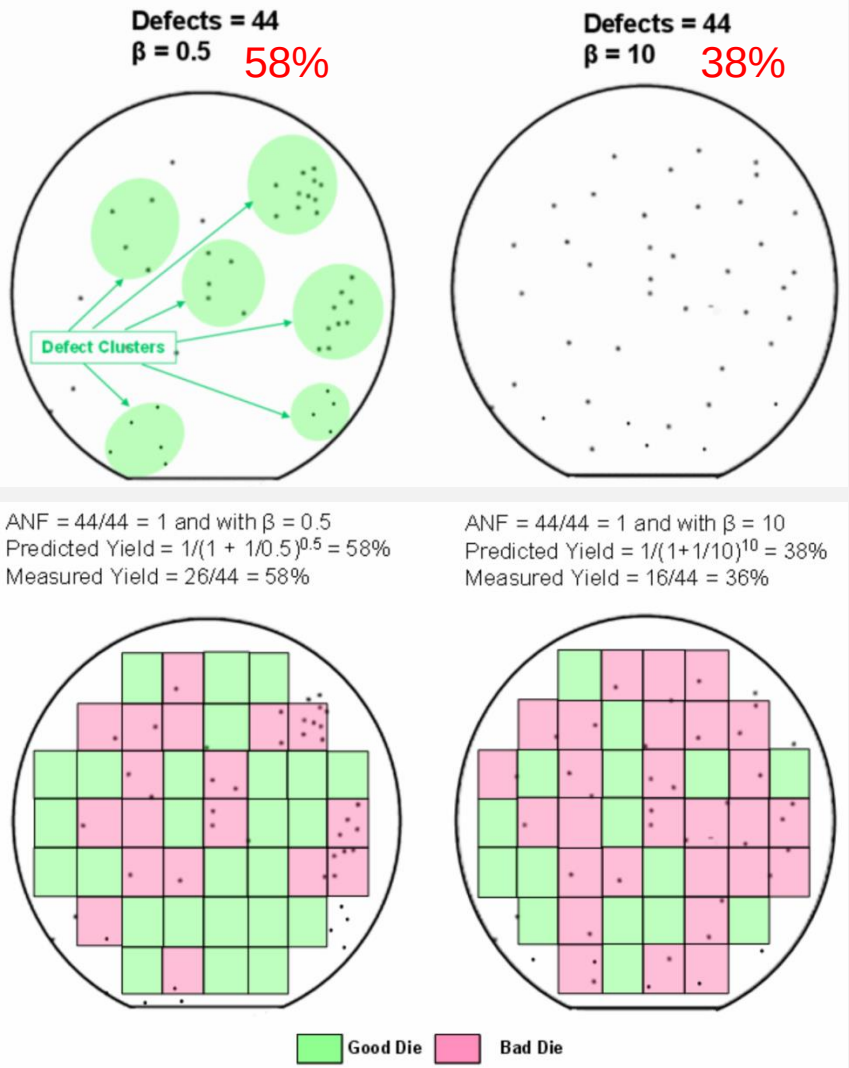


General yield model (negative binomial)

All models present random part of yield Y_{rand}!



Yield and clustering coefficien β

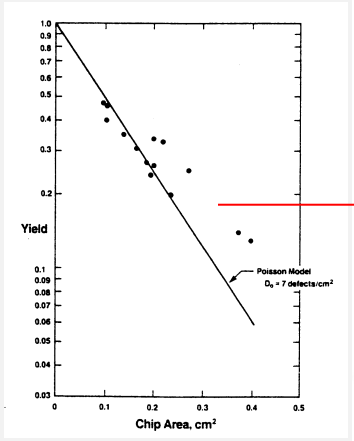


β = α – cluster factor
in general yield model

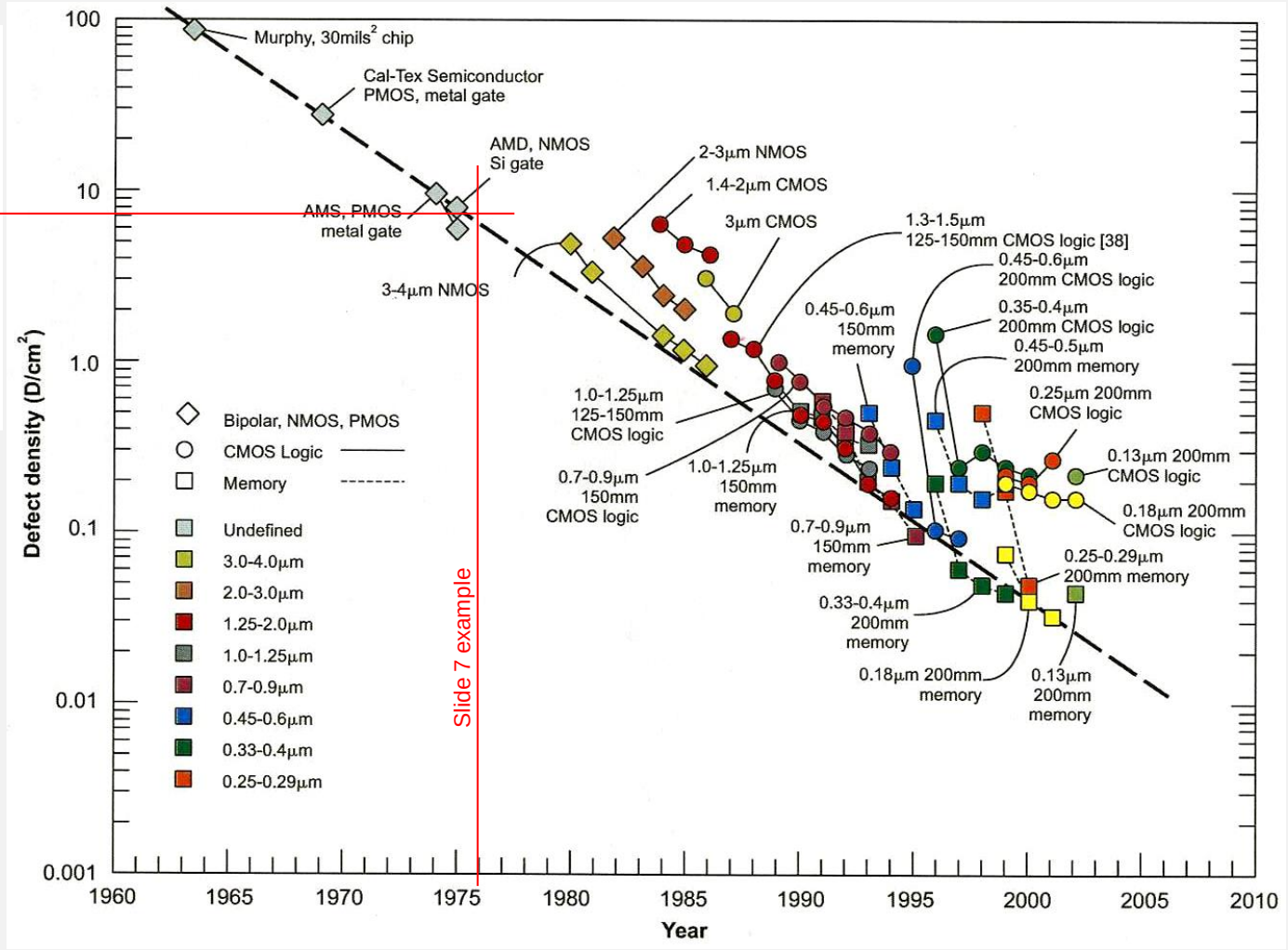
ANF = D*A –average number of faults per chip

$$Y_P = e^{-1} = 36.8\%$$

Defect densities

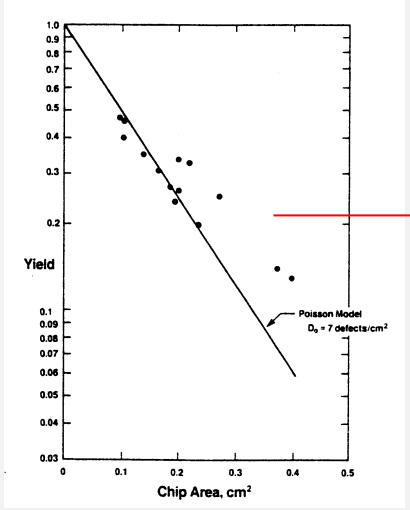


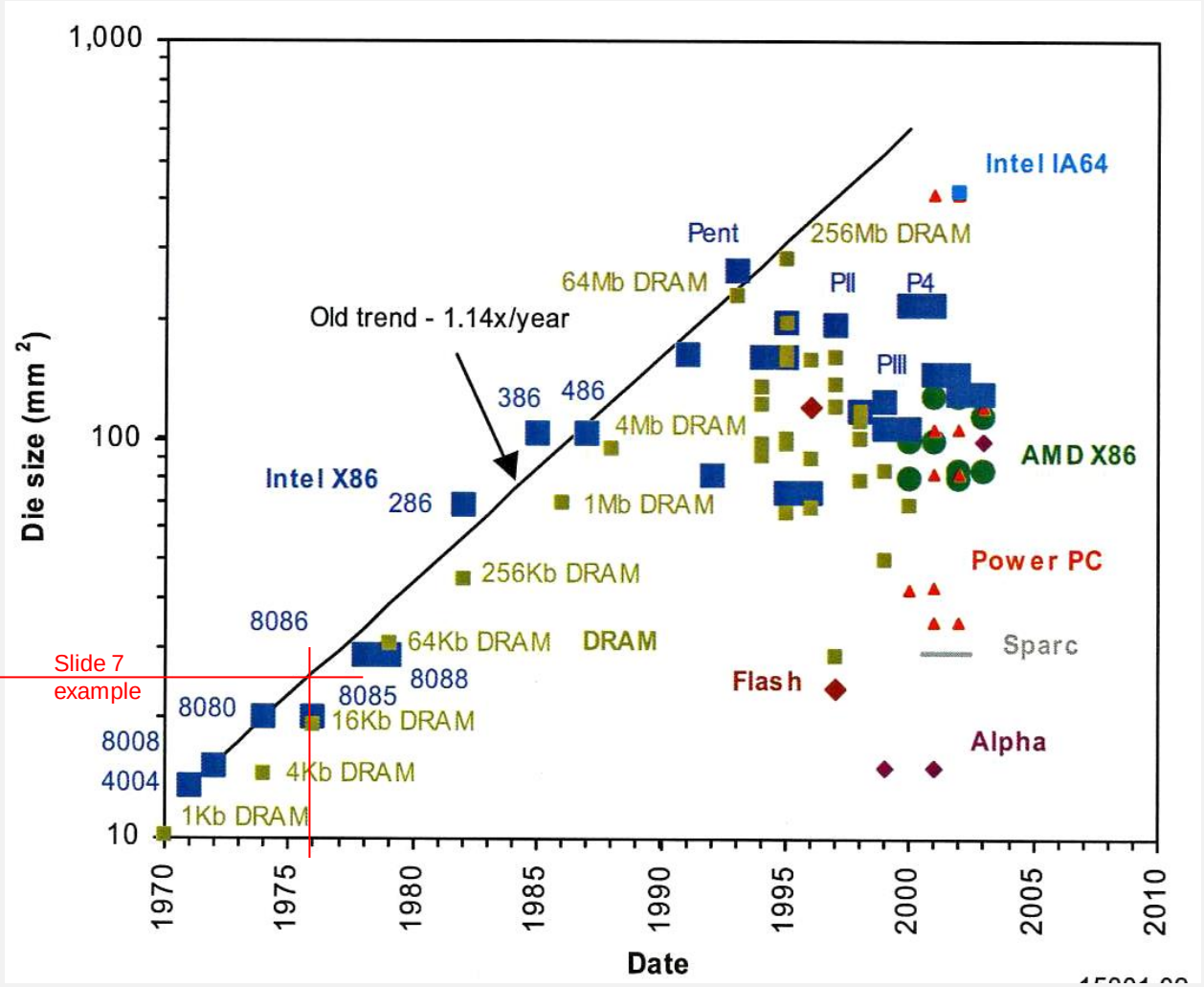
New equipment and technology have driven down defect densities and ultimately improved yields.



Die size

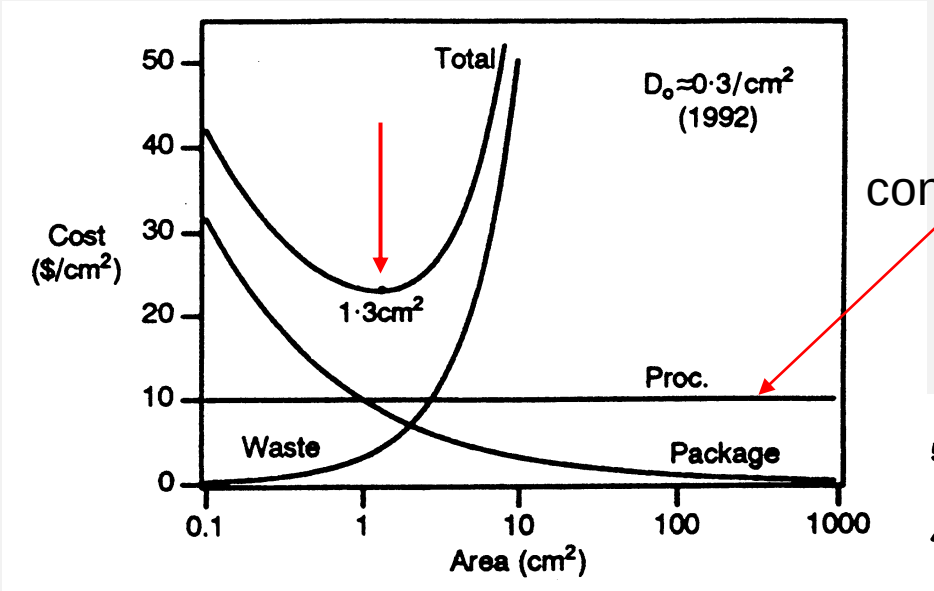
Rate of growth in die size is 1.14x per year.





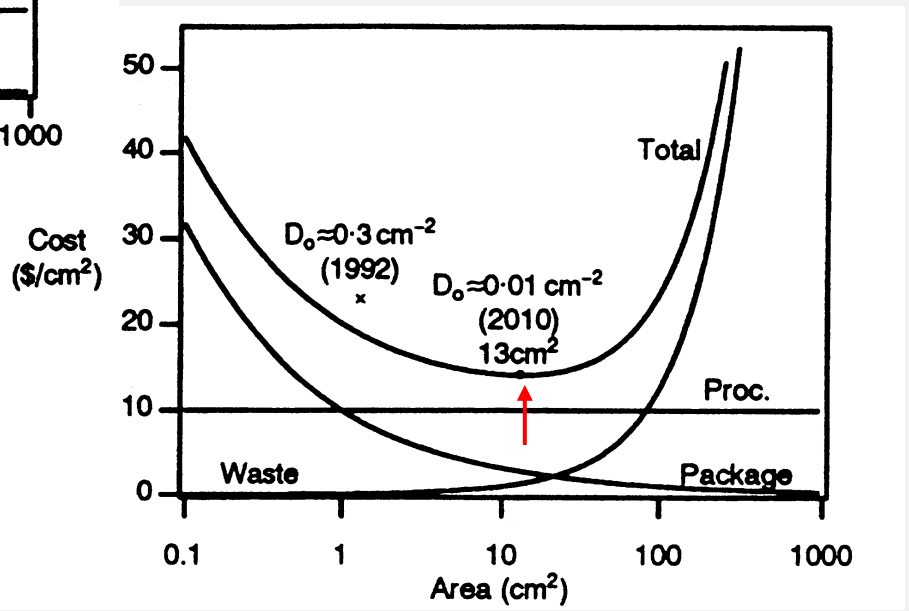
Optimum chip size

Year 1992

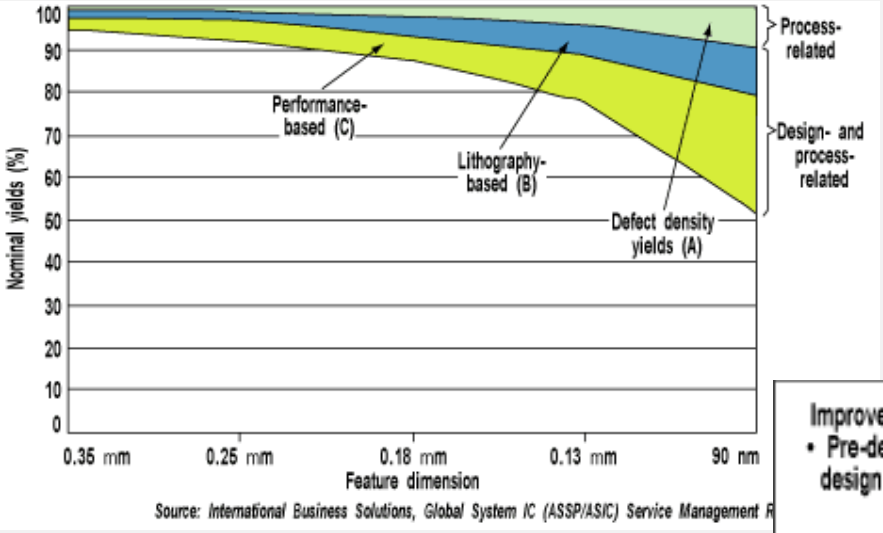


constant over 30 years!!!

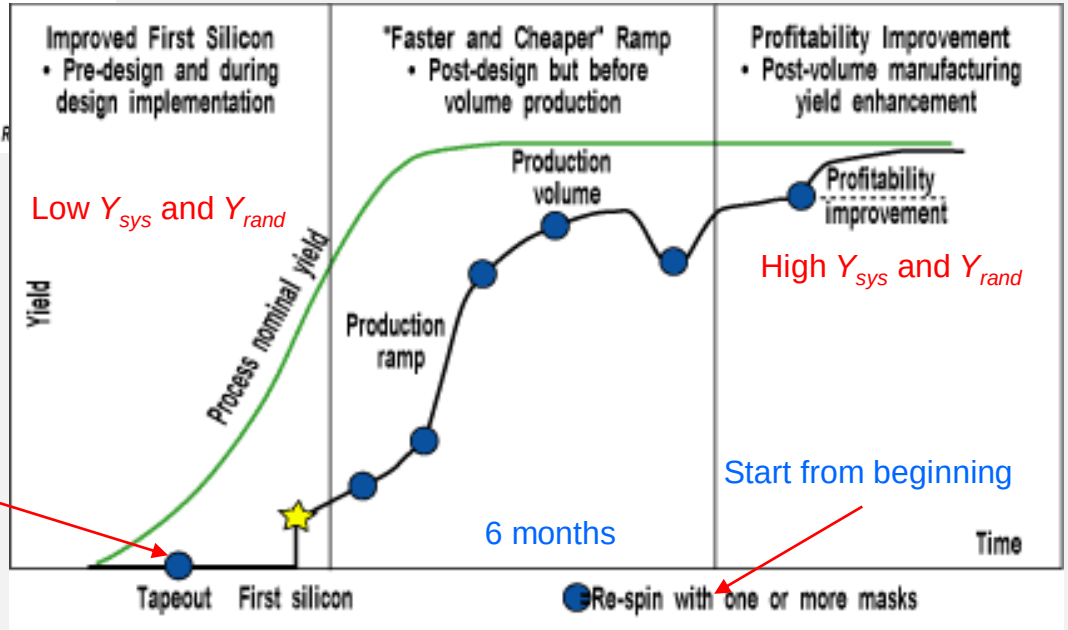
Year 2010



Yield loss contributors and yield ramp

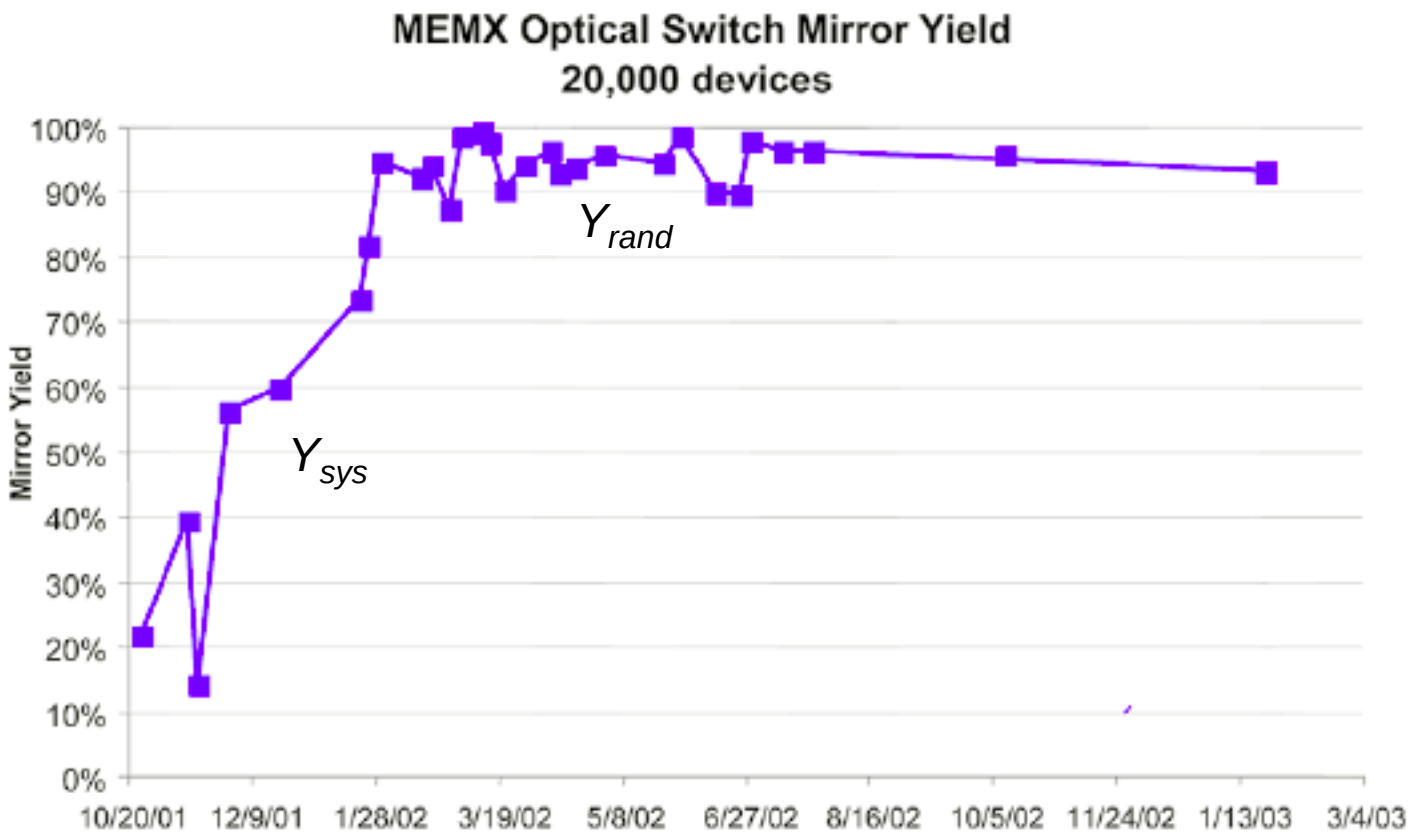


Traditional IC



Yield ramping - MEMS

A.D. Romig, Jr et al. / Acta Materialia 51 (2003) 5837–5866

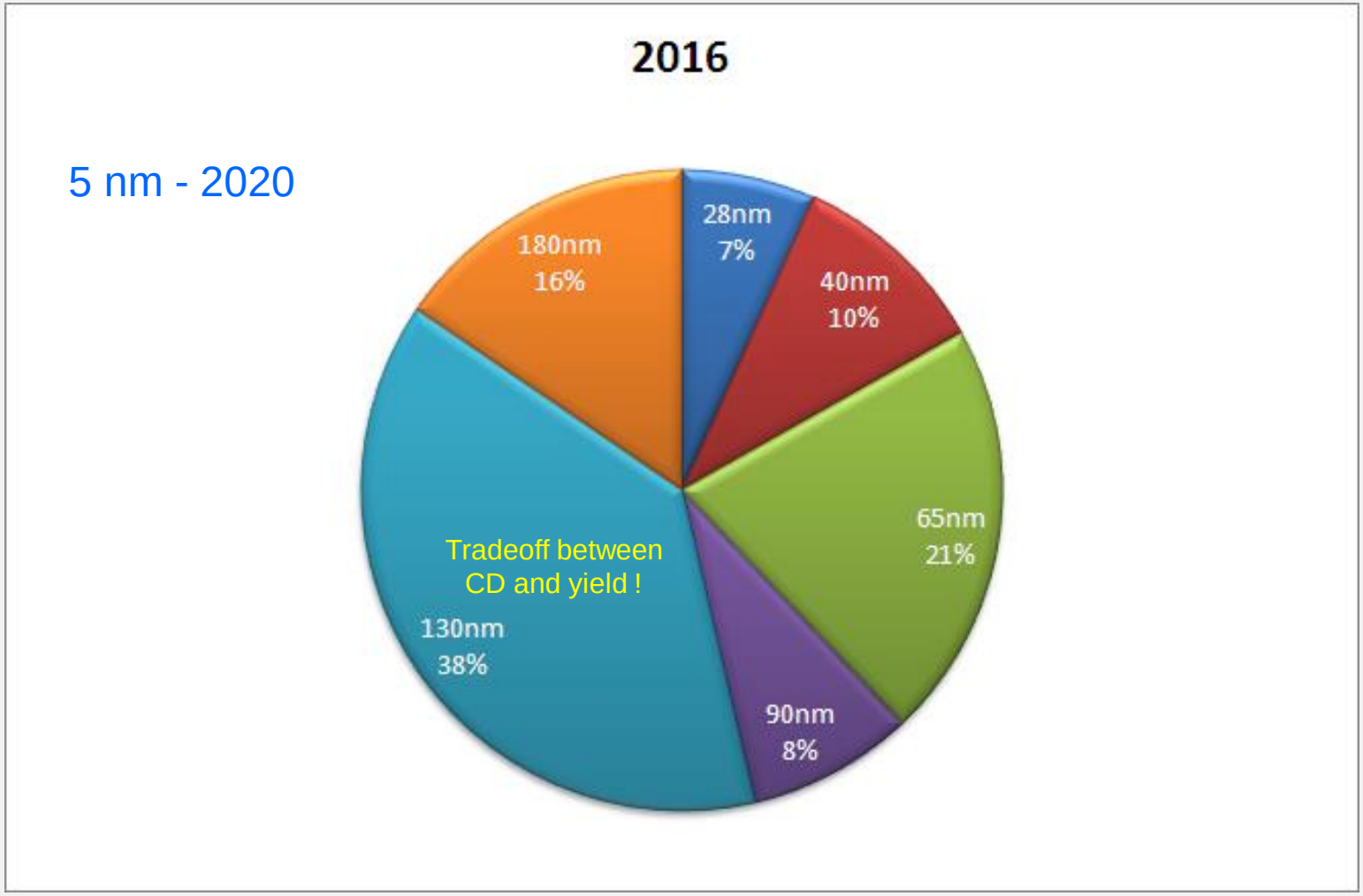


Yield stability

Yield must be stable, because it is a yardstick for process development.

If yield is not stable,
random yield improvement can be interpreted being due to engineering action Y_{sys}, even though it might be just random Y_{rand}.

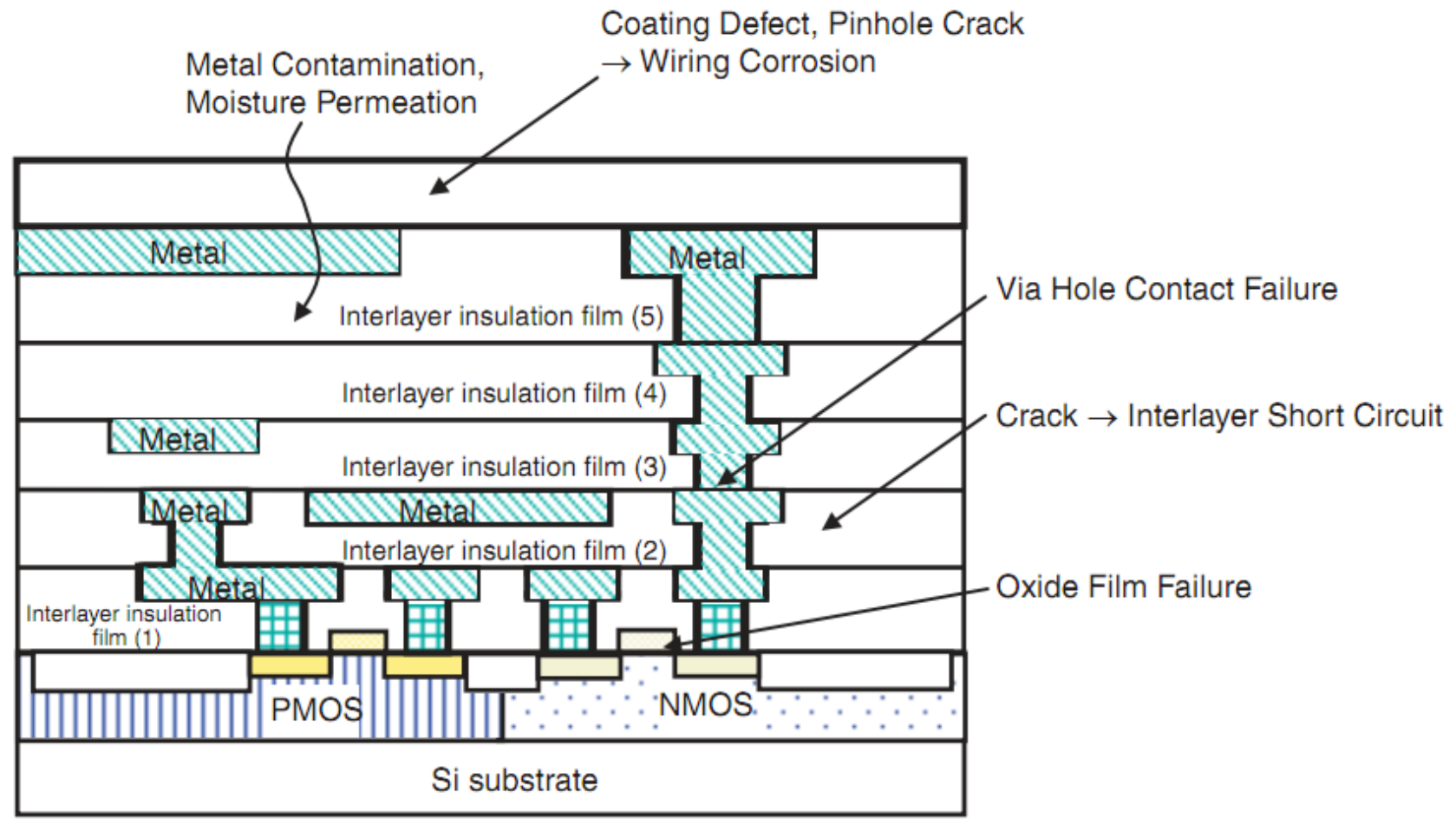
Technology nodes and market



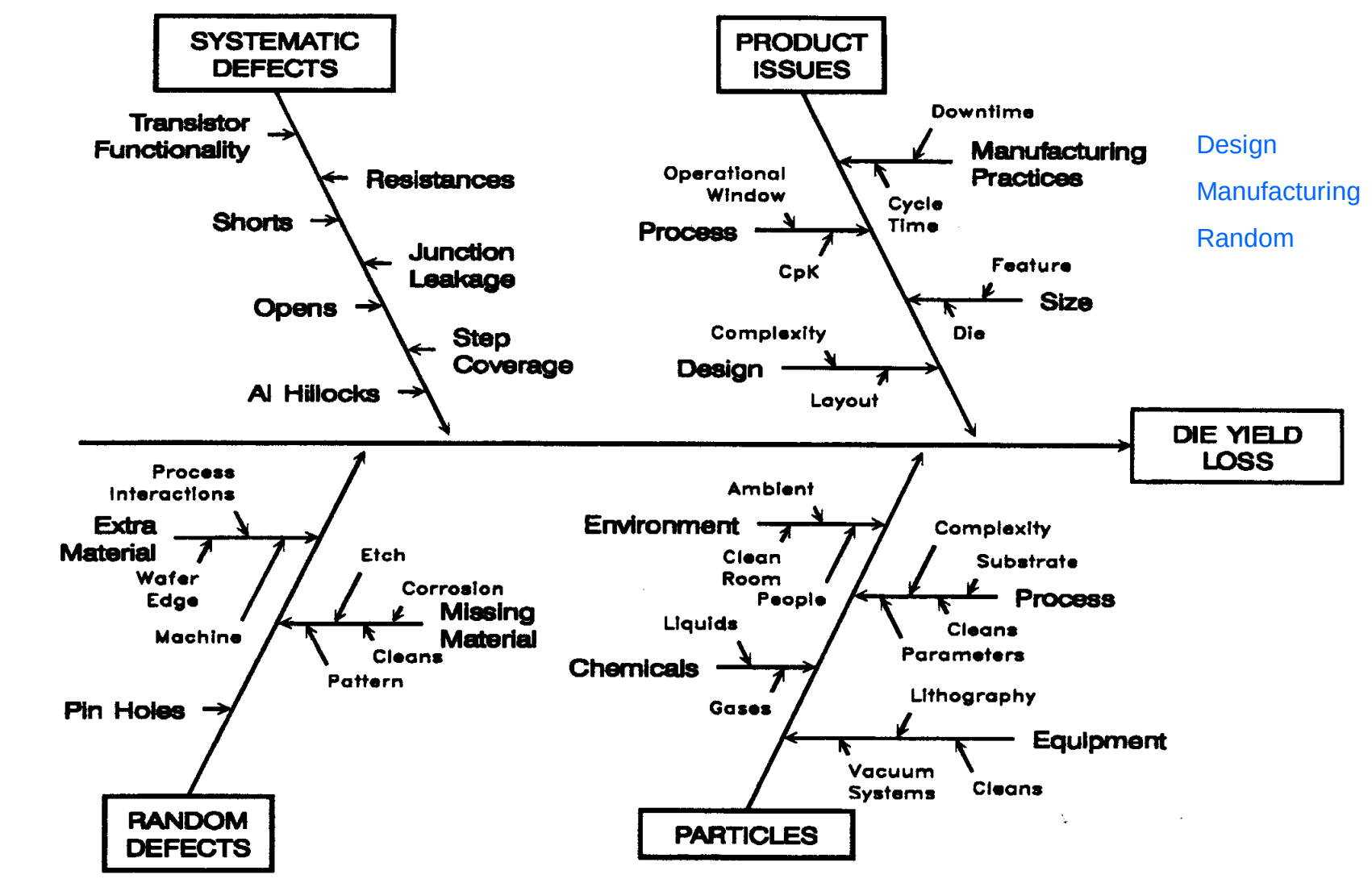
Why do we talk about yield?

- High yield leads to high profit
- Yield value tell us about the process quality
- Yield variations reflect process changing:
  - materials
  - environment
  - tools
  - operator skill
  - device desing
  - ...

IC defects I

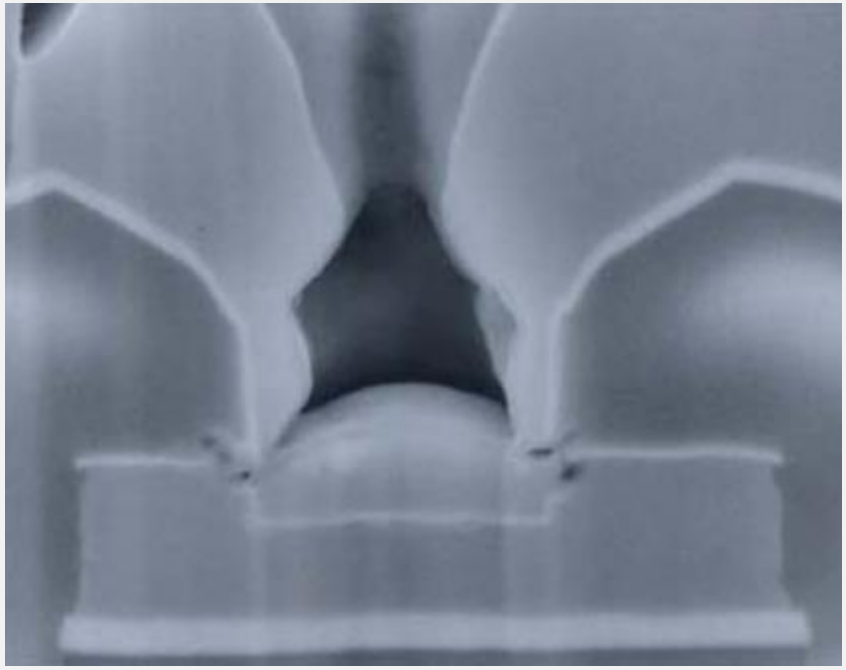

Coating Defect, Pinhole Crack
→ Wiring Corrosion
Metal Contamination,
Moisture Permeation
Metal
Metal
Interlayer insulation film (5)
Via Hole Contact Failure
Interlayer insulation film (4)
Crack → Interlayer Short Circuit
Metal
Interlayer insulation film (3)
Metal
Metal
Interlayer insulation film (2)
Metal
Oxide Film Failure
Interlayer insulation
film (1)
PMOS
NMOS
Si substrate

Defect fishbone diagram

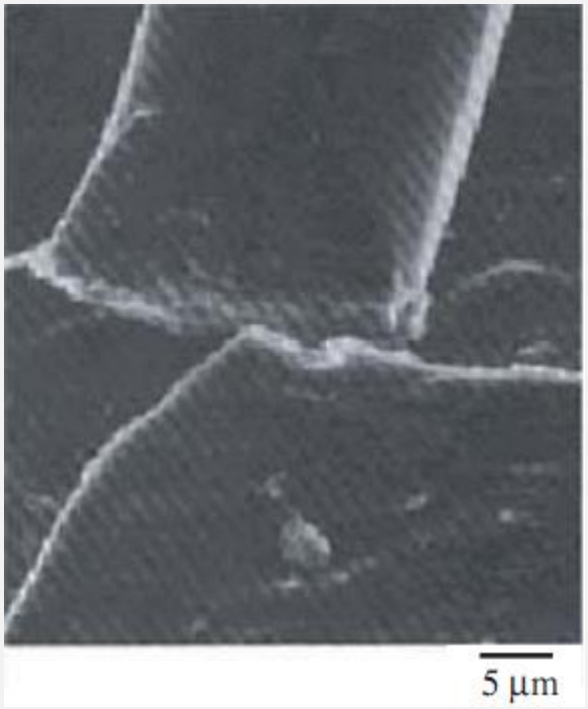


Metallization damage

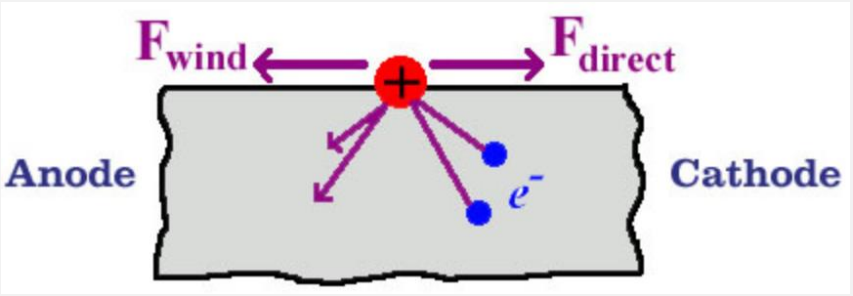
Al Wiring Coverage Disconnection

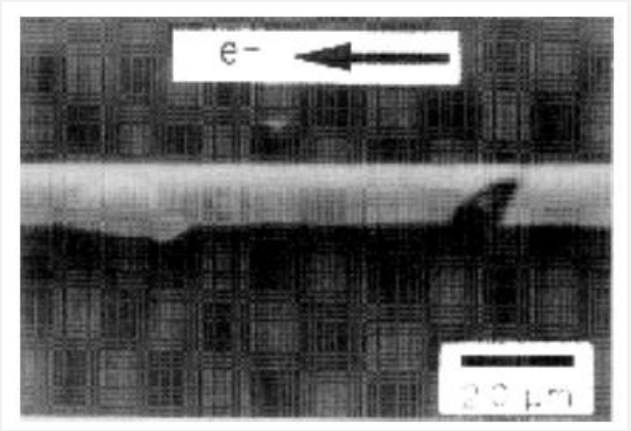


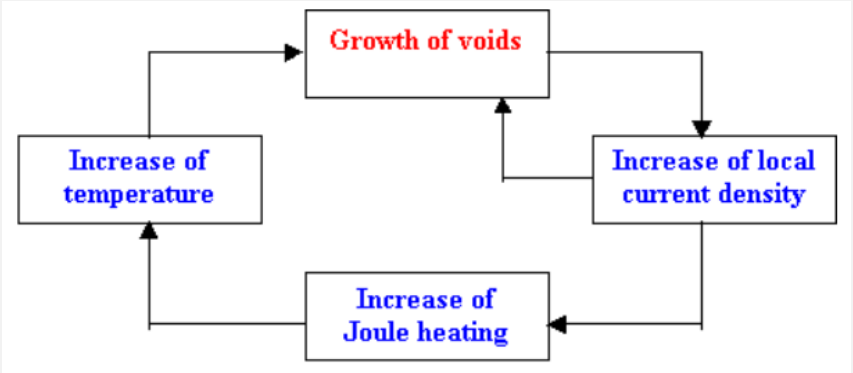
Damage on Wire Due to Ultrasonic Fatigue

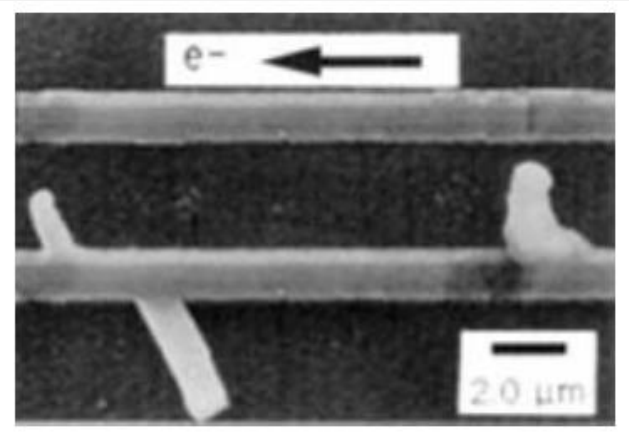


Electromigration concept





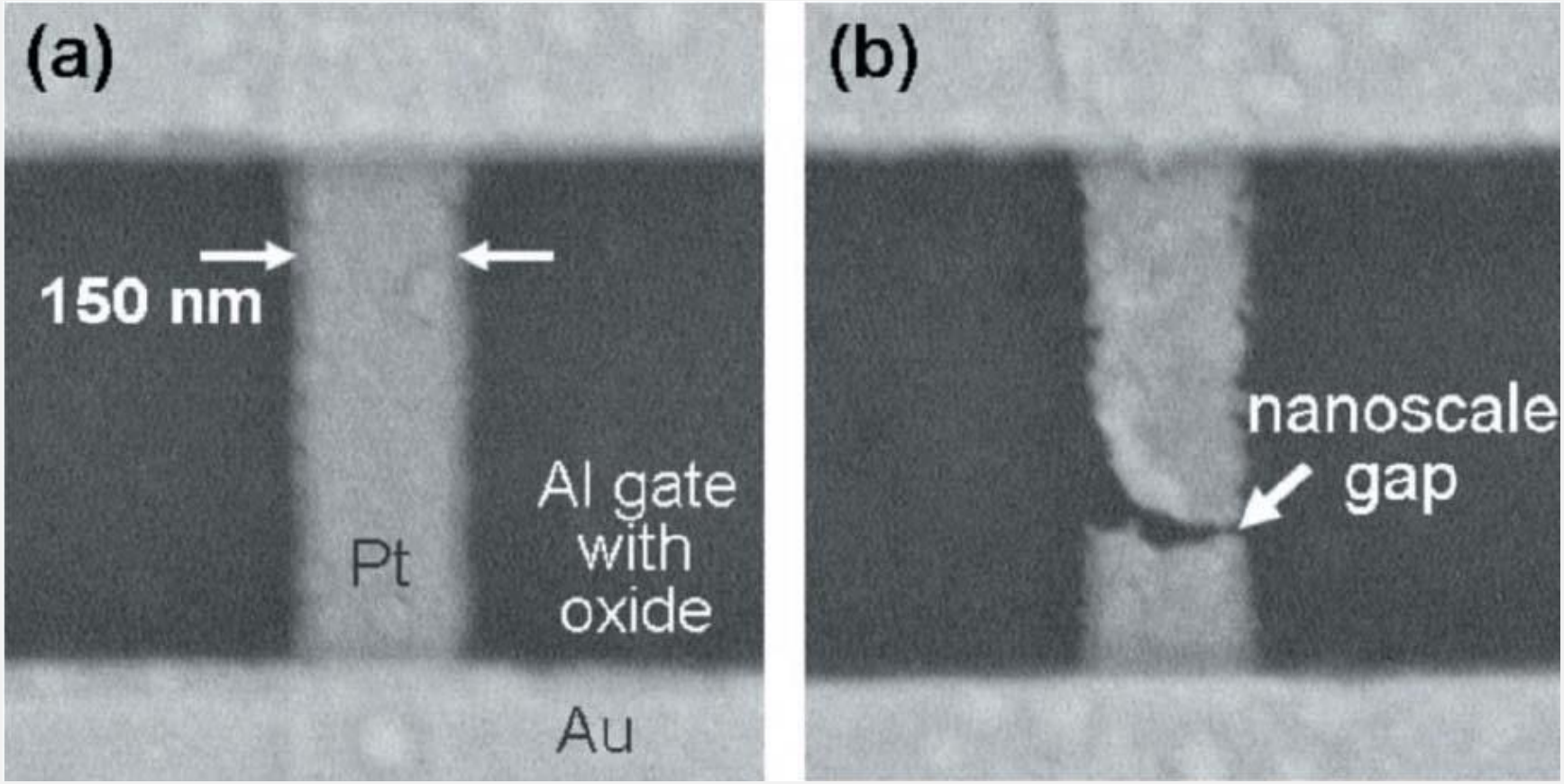




Thermal acceleration loop of electromigration

Electromigration result

Al-Cu(2-4%) prevents electromigration



Gate oxide breakdown

With scaling, gate oxide reliability becomes an issue:

– electric fields within the gate oxide grow

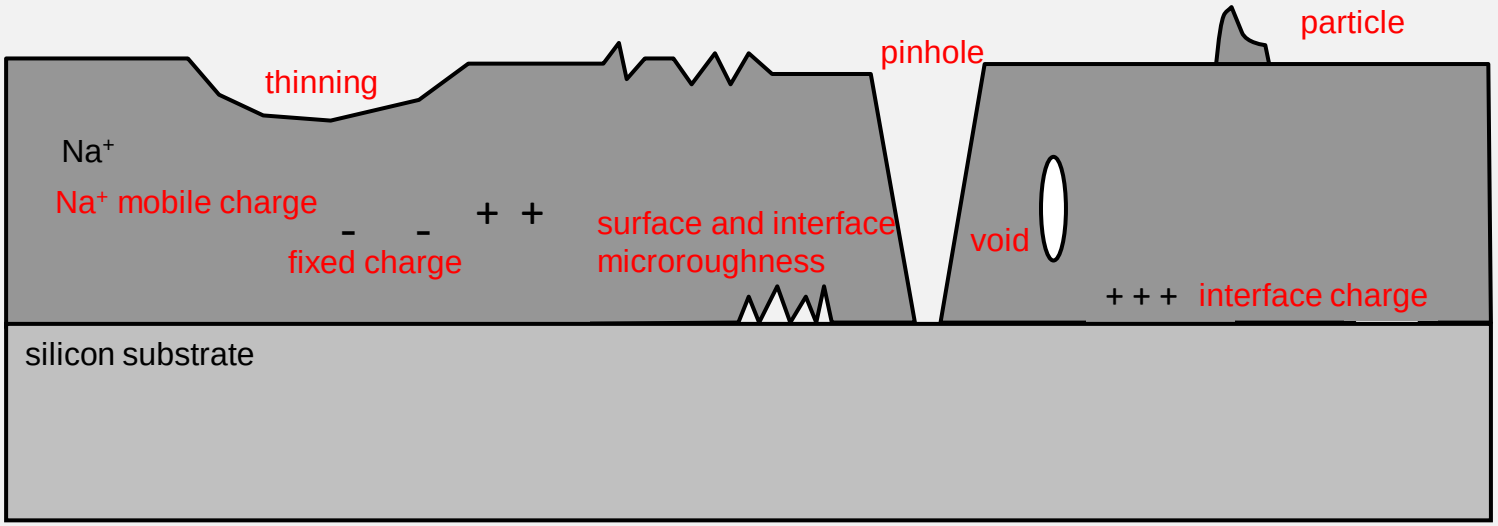
– more and more transistors on chip

Breakdown is a conduction path from the anode to the cathode through the gate oxide

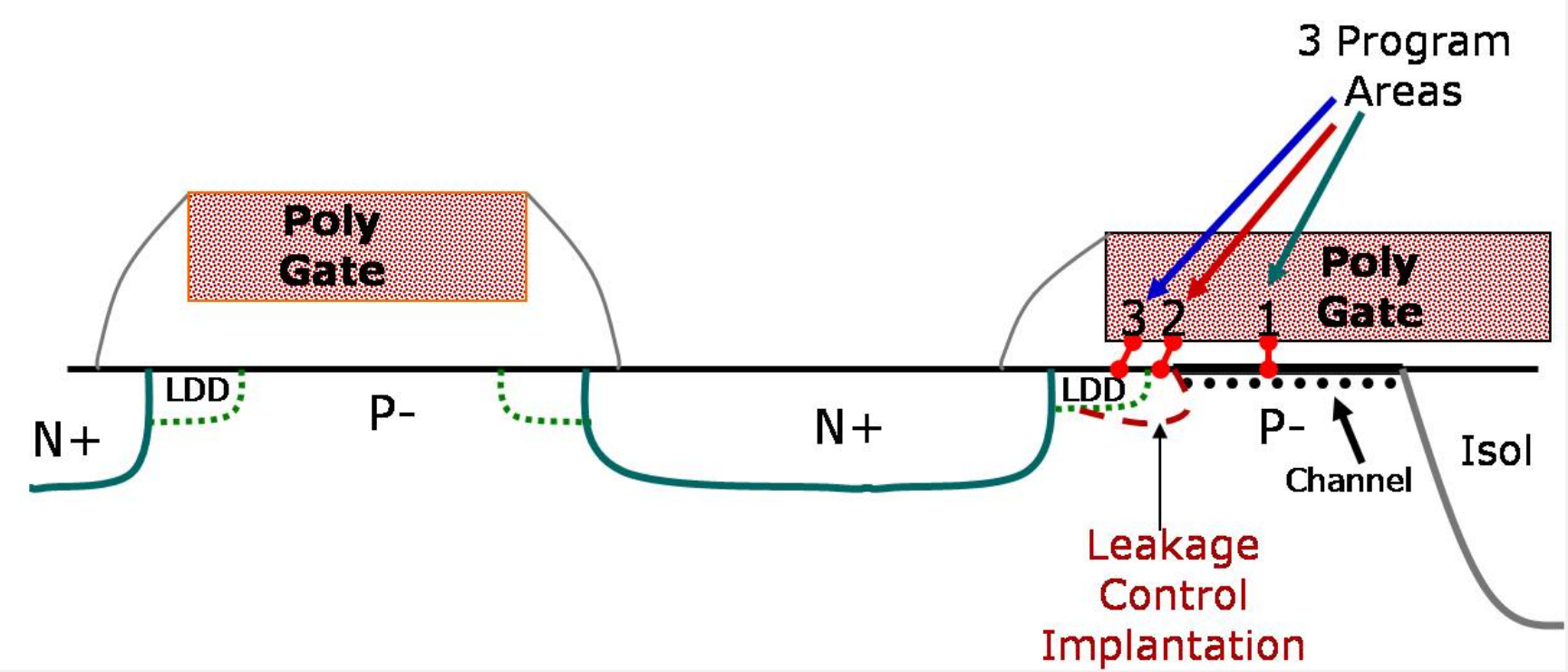
Traps allow for creation of conduction path:

- traps are defects in oxide that can trap charges

Oxide defects

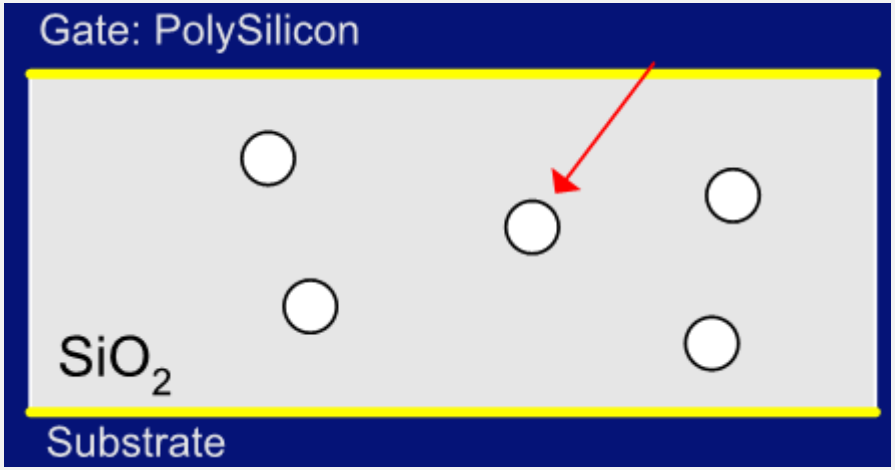


Areas with breakdown risk



Traps within gate oxide

Traps start to form in the Gate Oxide
–originally
–Non-overlapping
–Do not conduct



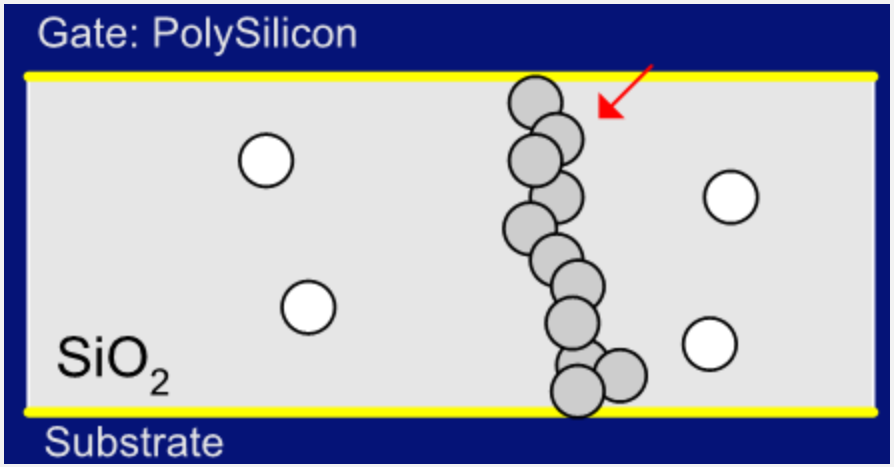
Soft breakdown

As more and more traps are created

–traps start to overlap

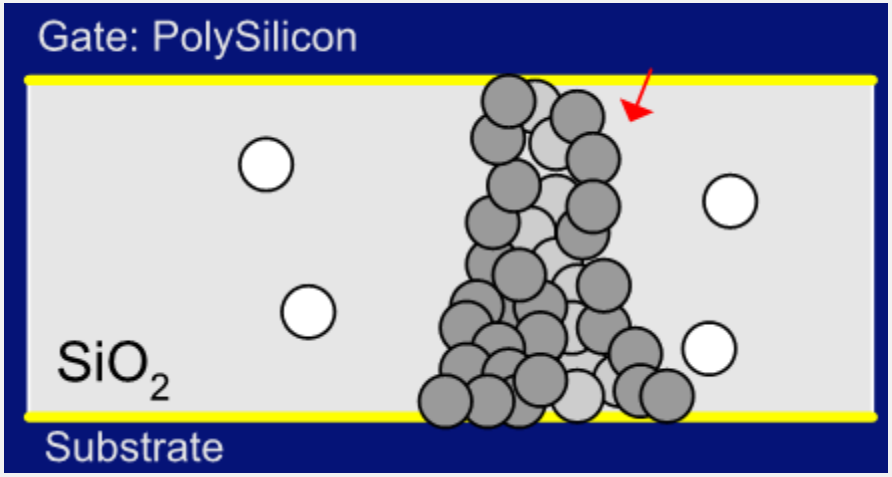
–conduction path is created

Once this conduction path is created we have Soft Breakdown (SBD) or time-dependent oxide breakdown (TDDB)



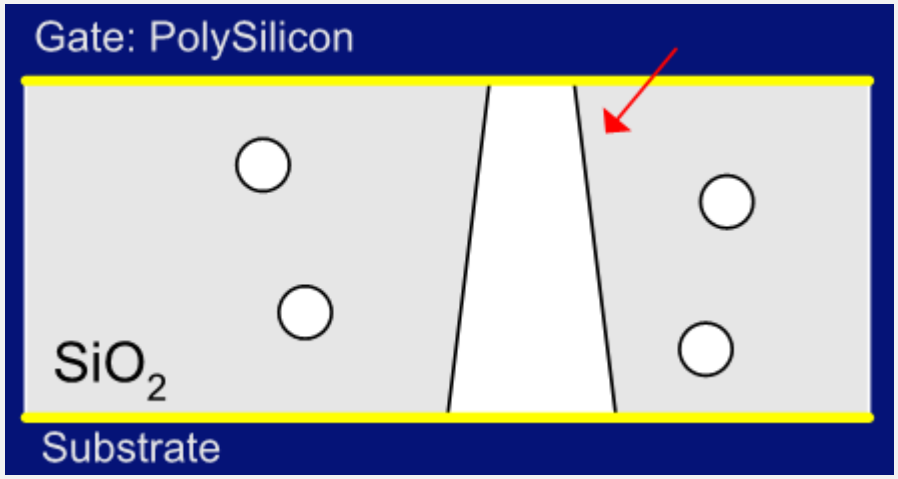
Thermal damage

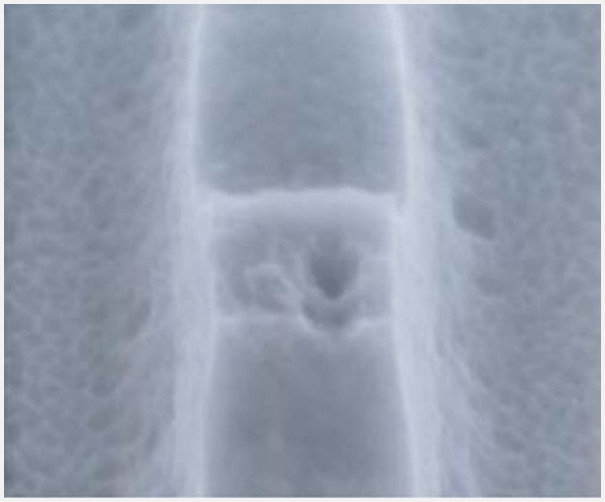
Conduction leads to heat
Heat leads to thermal damage
Thermal Damage leads to Traps
More Traps leads to more conduction



Hard breakdown

Silicon in the breakdown spots melts
Oxygen is released
Silicon Filament is formed from Gate to Substrate (Hard Breakdown)





Reliability

Reliabiliy is the ability of a system to perform its functions in routine circumstances. It is characterized by Mean Time To Failure (MTTF)

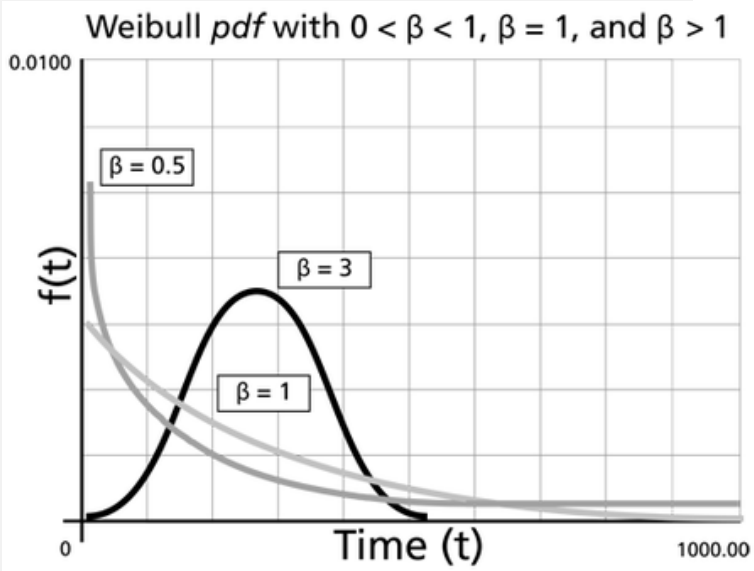
Reliability depends on:

- Chip fabrication process
- Assembly
- Environmental conditions:
  - Voltage, current density
  - Temperature, humidity, gas, dust
  - Contamination
  - Mechanical stress
  - Vibration, shock
  - Radiation, intensity of electrical and magnetic fields

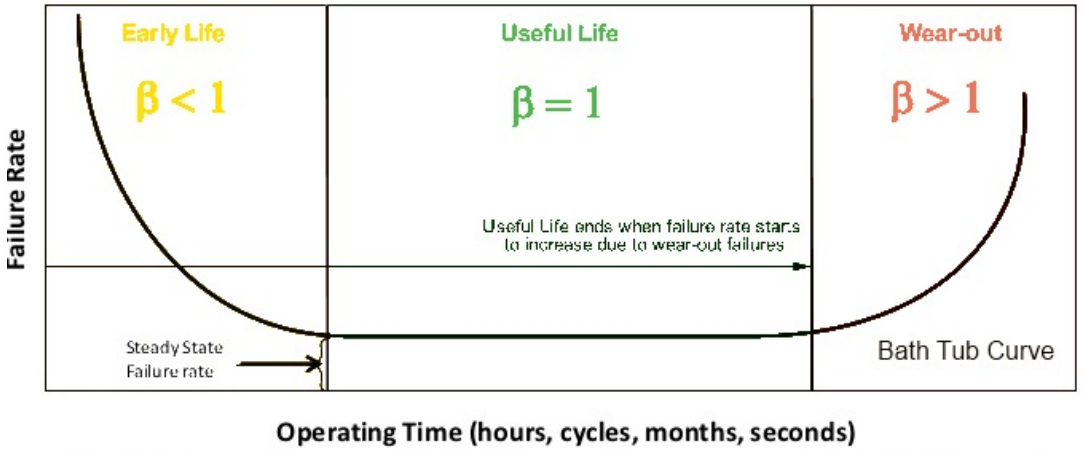
Weibull distribution of failures

Two parameters (α and β) distribution

α - scale parameter
β – shape parameter

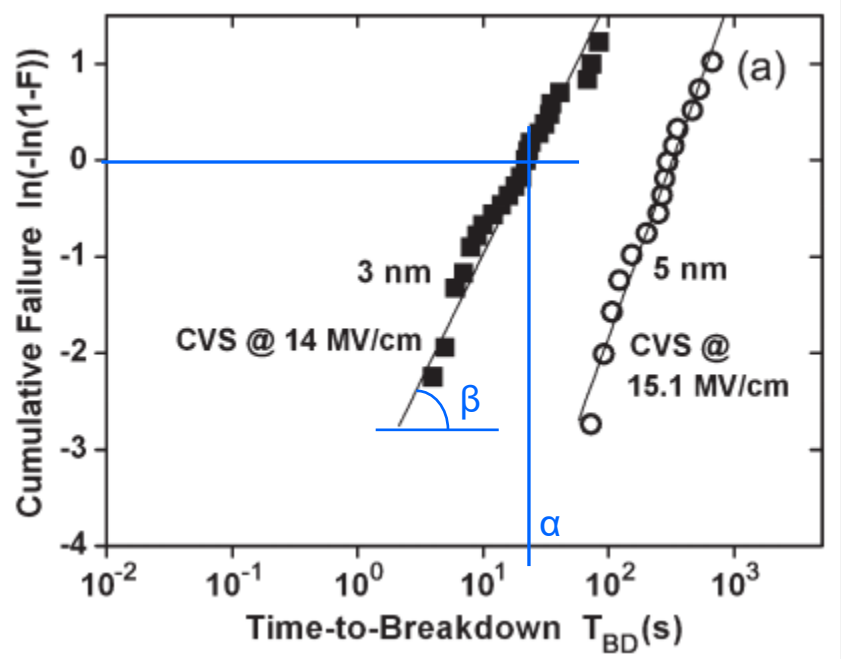


Failure Rate Curve (Bathtub Curve)

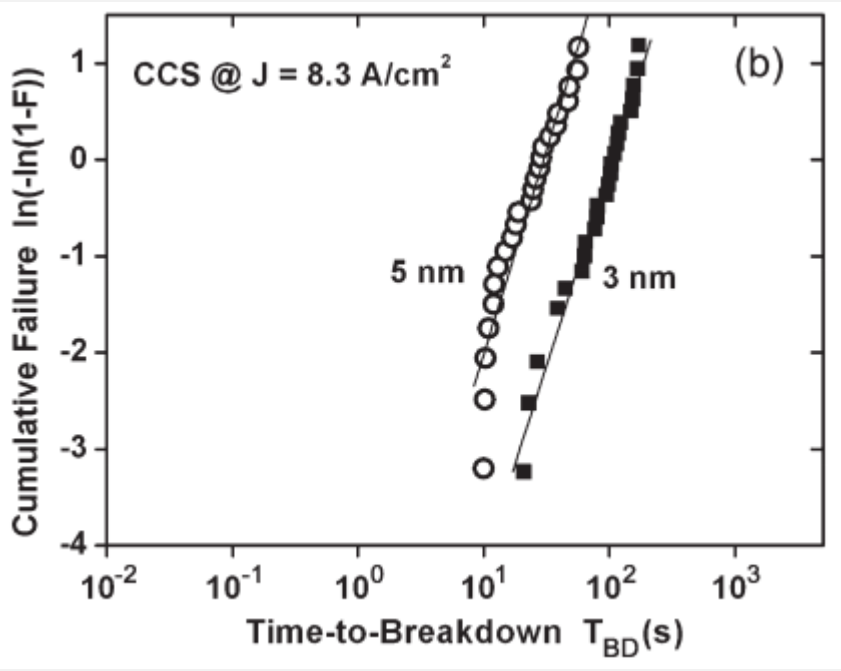


Weibull plot for gate oxide

Constant voltage



Constant charge



ln(-ln(1-*p*)), where *p*=(*i*-0.3)/(*n*+0.4), *i* is the rank of the observation

if the data follow a Weibull distribution, the points will be linear

Yield and Reliability

- Yield – chip fabrication period
  – Affects chip cost

- Reliability – chip application period
  – Affects chip lifespan

Conclusions

- Yield (defect loss) is inherent feature of the microfabrication
- Yield and reliability can be statistically analyzed and monitored
- Yield and reliability depend both on design and on processing