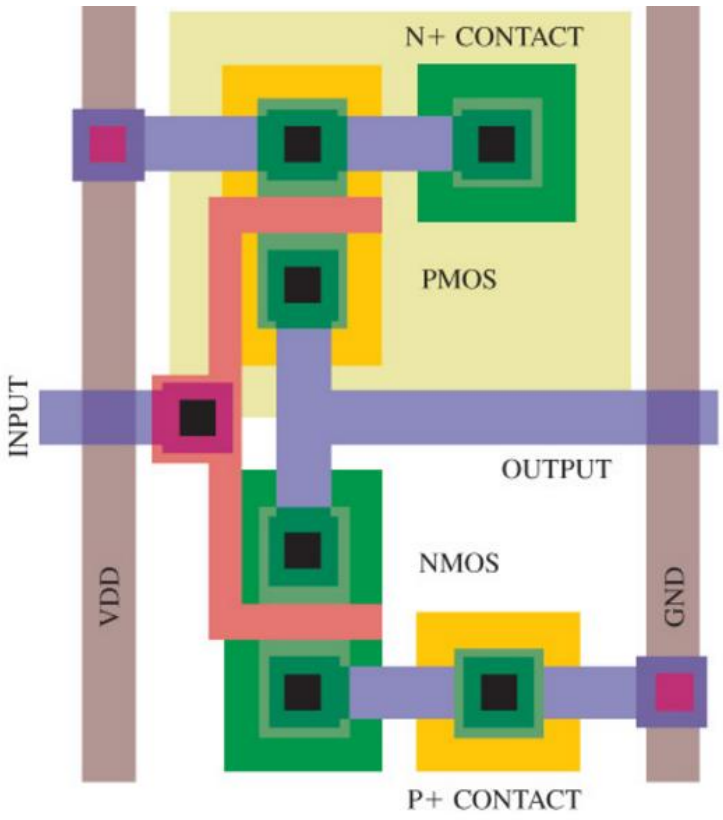
Microfabrication, Exercise 8: Yield. Economics
(return by 14.05. 2023, 10 pm Sunday)

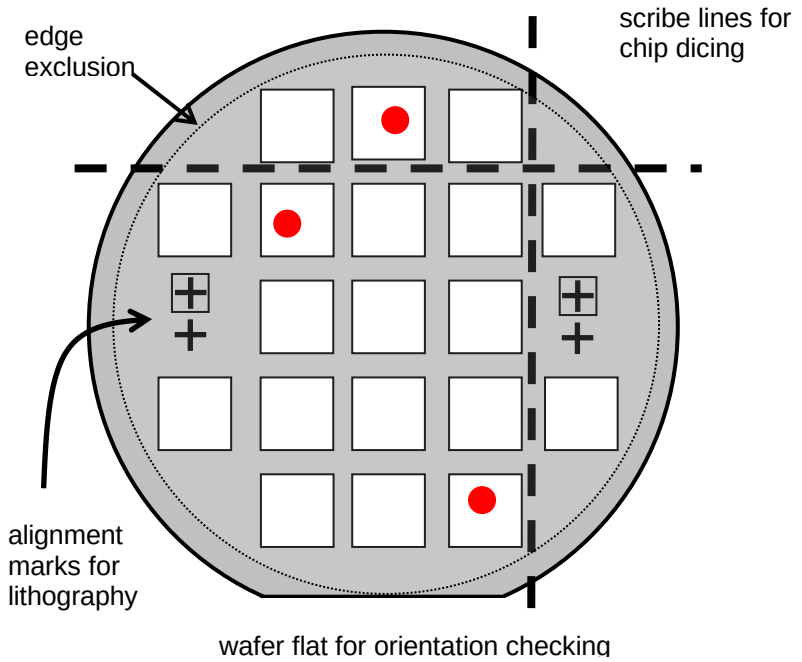
Session will be on May 16th, 9:15 o'clock.

A CMOS IC is fabricated by 5 µm process with polysilicon gate. See the given below layout of one inverter (in scale). One chip includes plenty of invertors and chip area is 8000 times larger than invertor area.



a) Using the picture above, provide an estimate for the dimensions of the chip. (0.5 p)

b) If 150 mm wafer is used, how many chips will fit on it (use the chip dimension you estimated above)? Consider all aspects that are pictured below. (0.5 p)



c) What is the processed wafer cost under the following assumptions? (1.5 p)

SSP silicon wafer cost 15 €
Metallization cost 15 €/wafer
Lithography cost 15 €/mask
Implantation cost 20 €/implantation
Thermal oxidation cost:
investment cost 6 000 000 €; 50 wafer batch size; 5 000 WPM.
operating cost 100 €/h
Silicon dry etching costs:
RIE tool investment 1 500 000€; 5 000 WPM
RIE running cost 50 €/h
Other process costs 50 €/wafer

d) Assuming defect density D = 0.5 cm^{-2}, what will be the yield of chips? Use the Poisson model and any other model! (0.5 p)

e) New invertor design with smaller linewidth was developed. Estimate new number of chips on wafer and yield if the same wafer fab is used. What happens to the cost of chips? (1 p)

Hints: 1. New defect density is 2 cm^{-2}.
2. New chip area is 1/2 of original area.