Scaling

or how changes are related to each other

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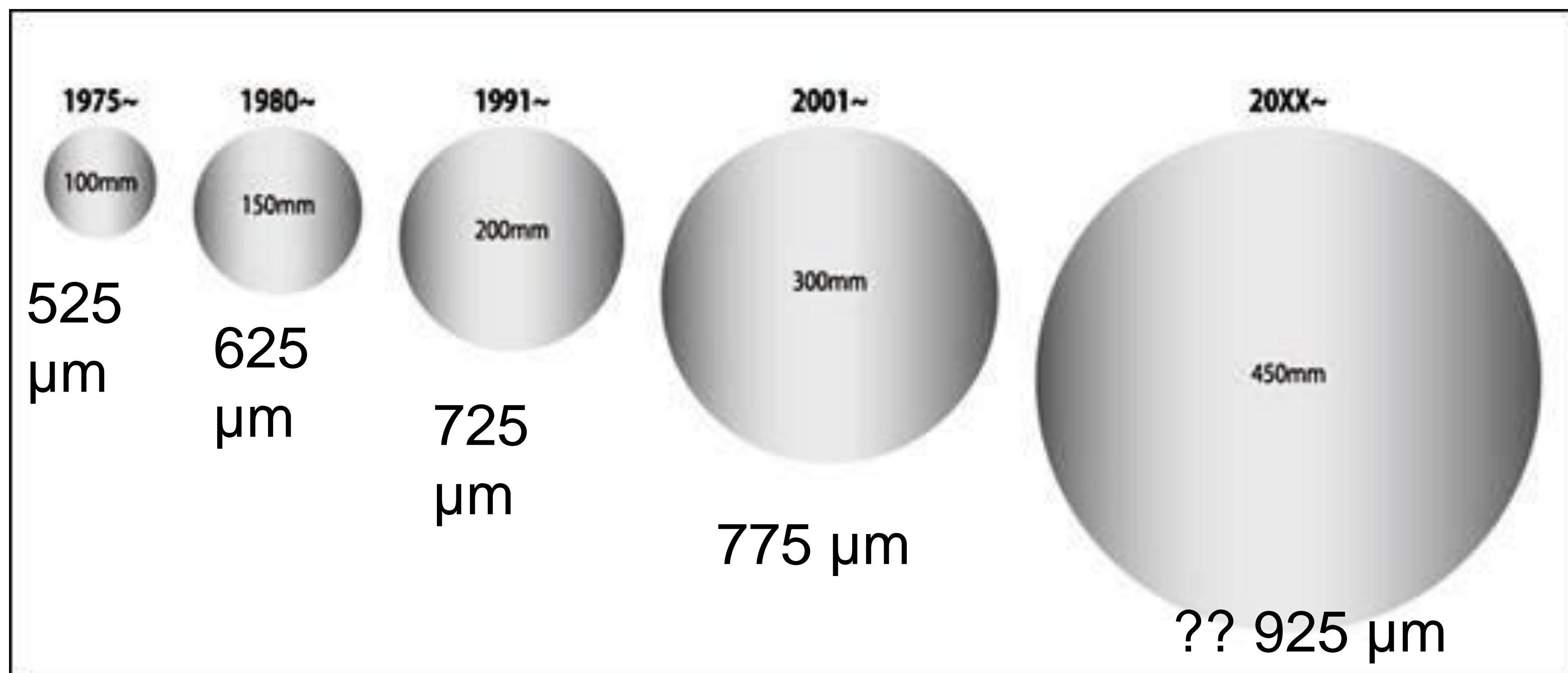
Outline

- Wafer size (and thickness) scaling
- Wafer specs scaling
- Wafer fab scaling
- Etch scaling
- Aspect ratio scaling
- CMOS oxide and junction scaling

Wafer size & thickness scaling



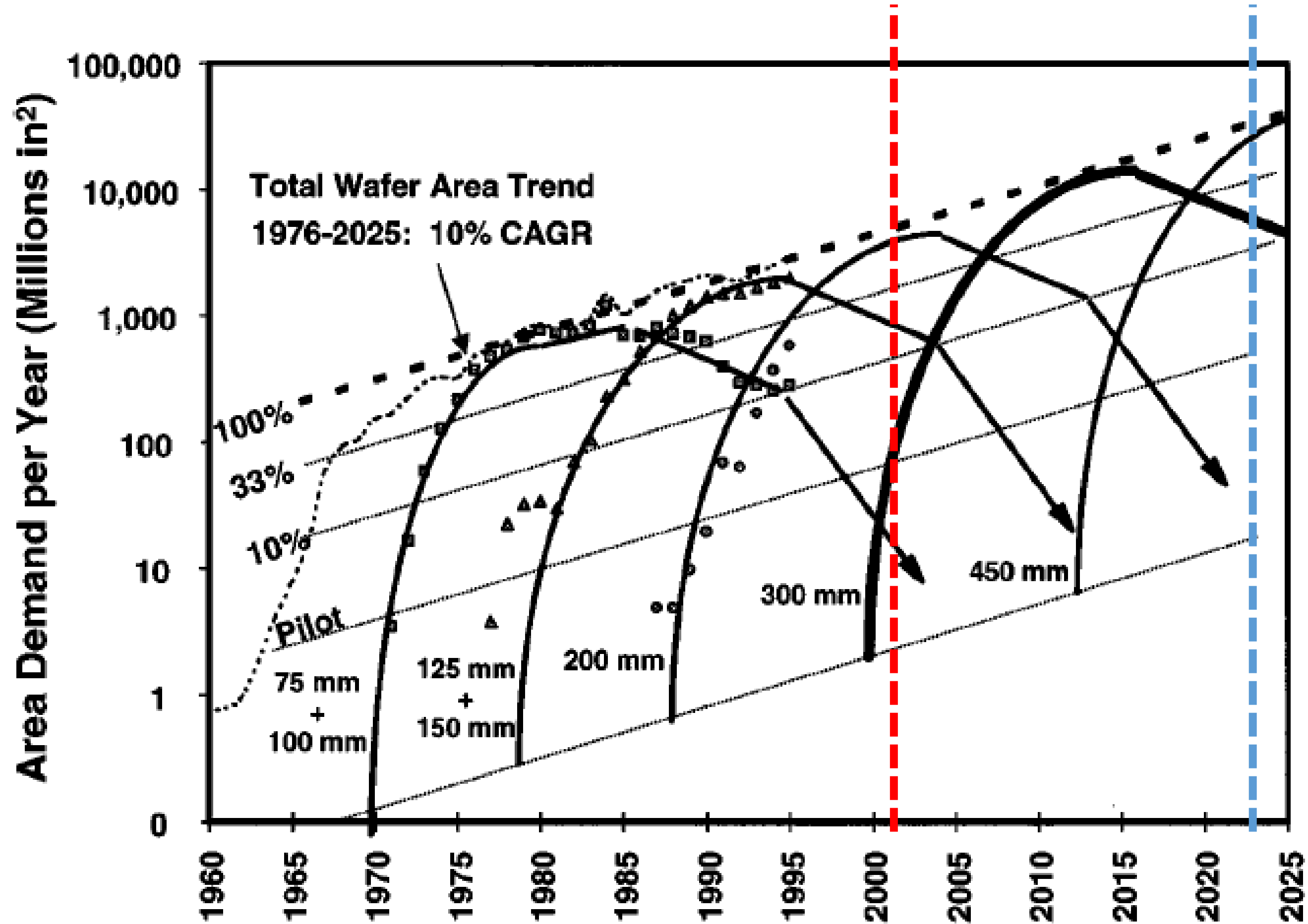
Thickness has to increase because mechanical strength (especially at high temperatures) is required.

Wafer specs scaling for CMOS

Wafer size	100	125	150	200	300	mm
Thickness	525	625	675	725	775	µm
TTV	3	3	2	1.5	1	µm
Warp	20-30	18-35	20-30	10-30	10-20	µm
Flatness	<3	<2	<1	0.5-1	0.5-0.8	µm
Oxygen	20	17	15	14	12	pmma
OISF	100-200	100	<10	none	none	cm^{-2}
Particles	10	10	5-10	10-100	50-100	#/wafer
Particle size	0.3	0.3	0.3	0.16	0.12	µm
Metals	10^{12}	10^{11}	10^{11}	$5*10^{10}$	10^{9}	atoms/cm^2

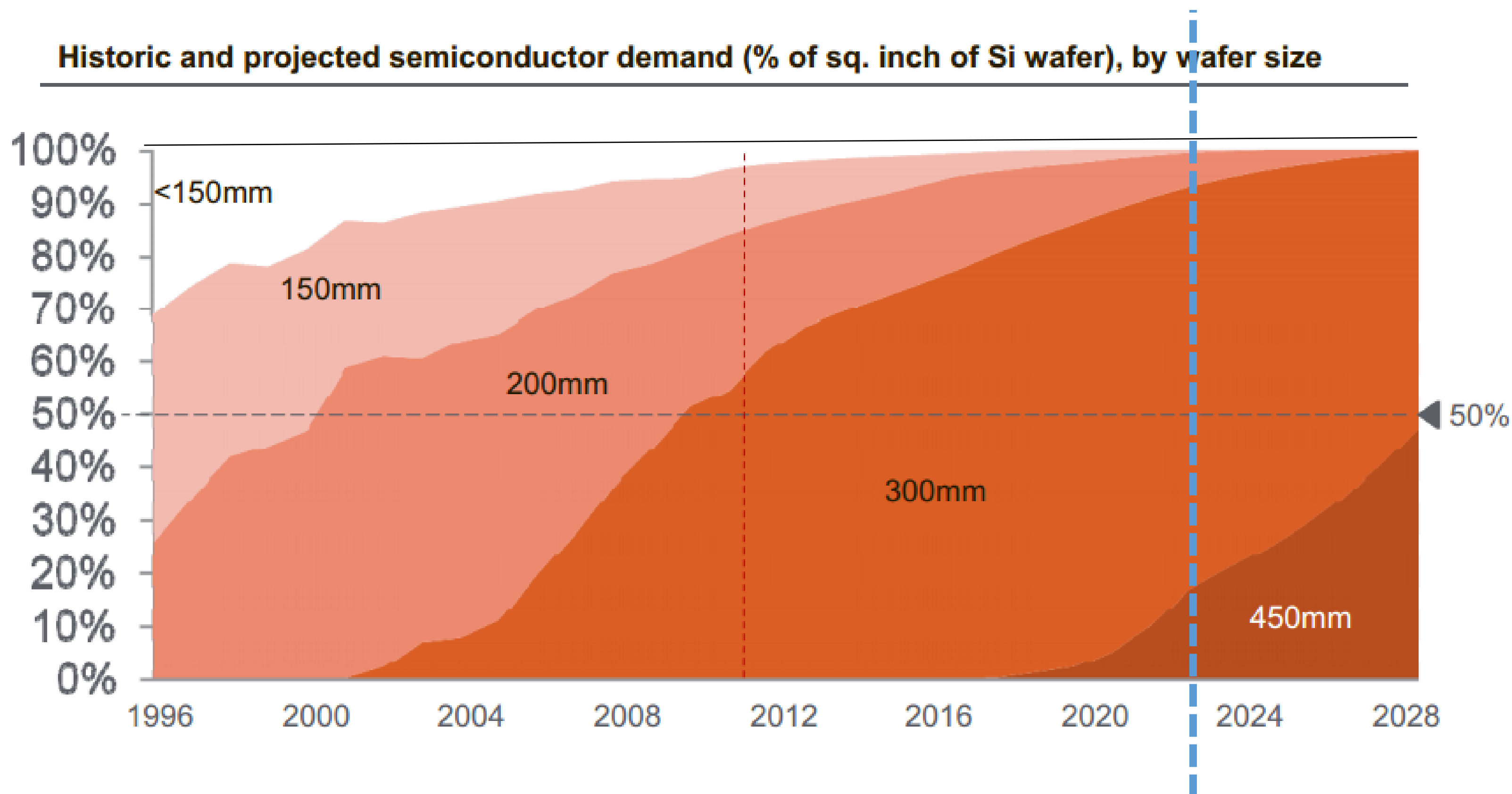
Tighter, not because of wafer size, but because smaller LWs on large wafers.

Wafer sizes (2001 prediction)



Doering, R. & Y. Nishi: Limits of integrated circuit manufacturing, Proc. IEEE Vol. 89 (2001) p. 375

Wafer sizes (2013 prediction)



https://www.extremetech.com/extreme/163372-atom-everywhere-intel-breaks-ground-on-first-450mm-fab

Making 450 mm etcher

“Maximum throughput of an etch tool is governed by two basic factors:

1) wafer load/unload time
2) etch time.

With good engineering wafer throughput is independent of wafer size, so that *chip* throughput improves as the wafer size increases.”

Chris Mack: http://www.lithoguru.com/scientist/essays/why450.html

Making 450 mm etcher (2)

"But "good engineering" is not free, and it takes work to keep the etch uniformity the same for a larger wafer.

The larger etch tools also cost more money to make. But if the tool cost does not increase as fast as the wafer area, the result is a lower cost per chip.

This is the goal, and the reason why we pursue larger wafer sizes."

Chris Mack: http://www.lithoguru.com/scientist/essays/why450.html

Cost analysis of 450 mm etcher

Wafer diameter increase of 1.5X compared with 300 mm
Wafer area increases by factor of 2.25

Because of edge die effect it is possible for the number of good chips to increase at a slightly higher amount, maybe up to a factor of 2.4.

If the cost of the etcher, the amount of fab floor space, and the per-wafer cost of process chemicals all increase by 30%, the cost per chip will change by 1.3/2.25 = 0.58.

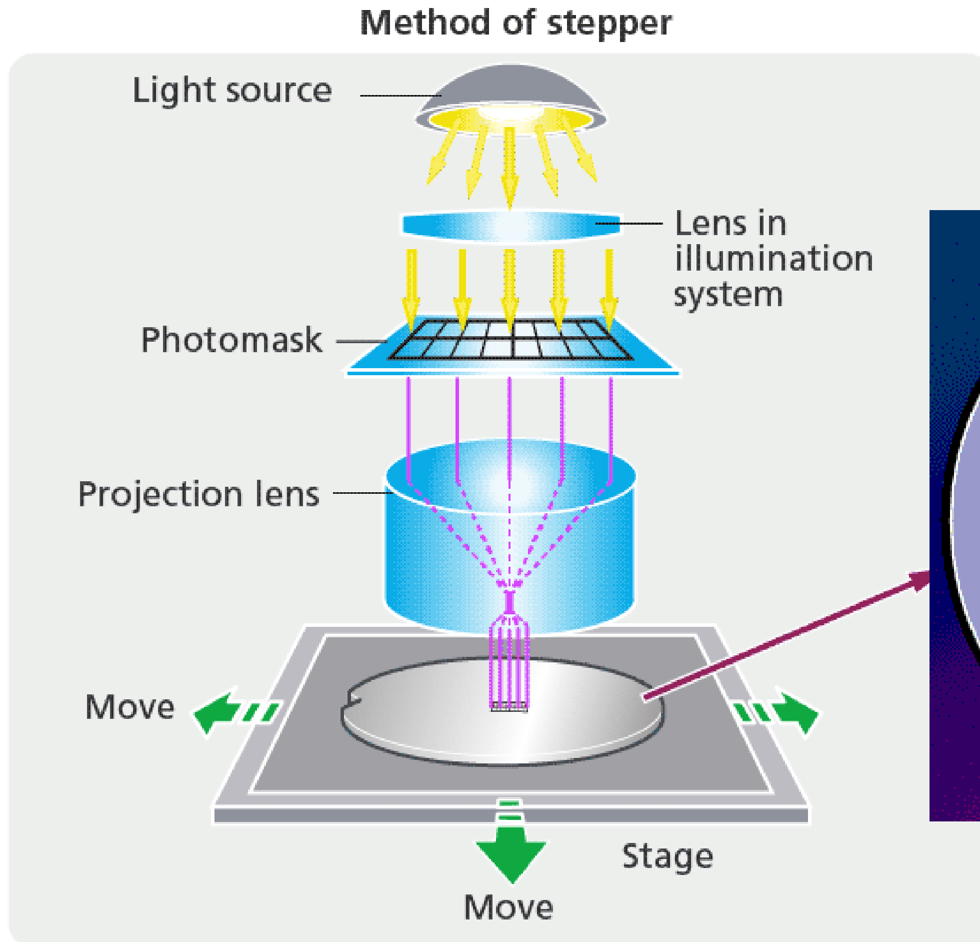
Thus, the etch cost per chip will be 42% lower.

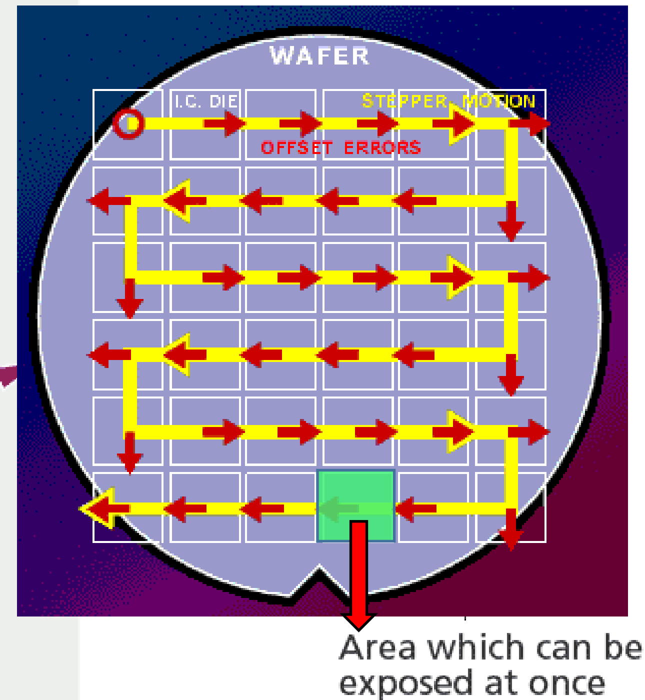
Chris Mack: http://www.lithoguru.com/scientist/essays/why450.html

Reduction stepper: ~100 exposures/wafer

Compared to proximity litho:

-smaller LW possible
-better alignment





Nikon.com

450 mm lithography

Reduction stepper litho process time consists of:

1) wafer load/unload time
2) exposure time

The load time can be kept constant as a function of wafer size, but the exposure time increases as the wafer size increases.

And since wafer load/unload time is a very small fraction of the total process time, the result for lithography is a near-constant *wafer-area* throughput (rather than the constant wafer throughput for etch) as wafer size is changed.

➔ Proportion of lithography of total costs will increase. Today 50%

Chris Mack: http://www.lithoguru.com/scientist/essays/why450.html

450mm: Why it failed.

23rd-Mar-2020

- lack of consensus of wafer fab owners
- opposition from the semiconductor equipment and materials industry
- but in the end it was the economics of Moore’s Law …
- growth in areal density in the semiconductor industry is still above the trendline after 55-years!

https://www.vlsiresearch.com/semiconductor-week/mar-23-2020#page1

Photomask cost scaling

1X litho

Min LW	Cost
3 μm	300 euros
1 μm	500 euros
1 μm	1000 euros, quality checked

Mask LW	Wafer LW	Cost
1 μm	0.2 μm	2000 euros
0.5 μm	0.1 μm	5000 euros
200 nm	40 nm	20000 euros
100 nm	20 nm	50000 euros

5X reduction litho

For a 40 mask microprocessor ➔ mask set costs $2M

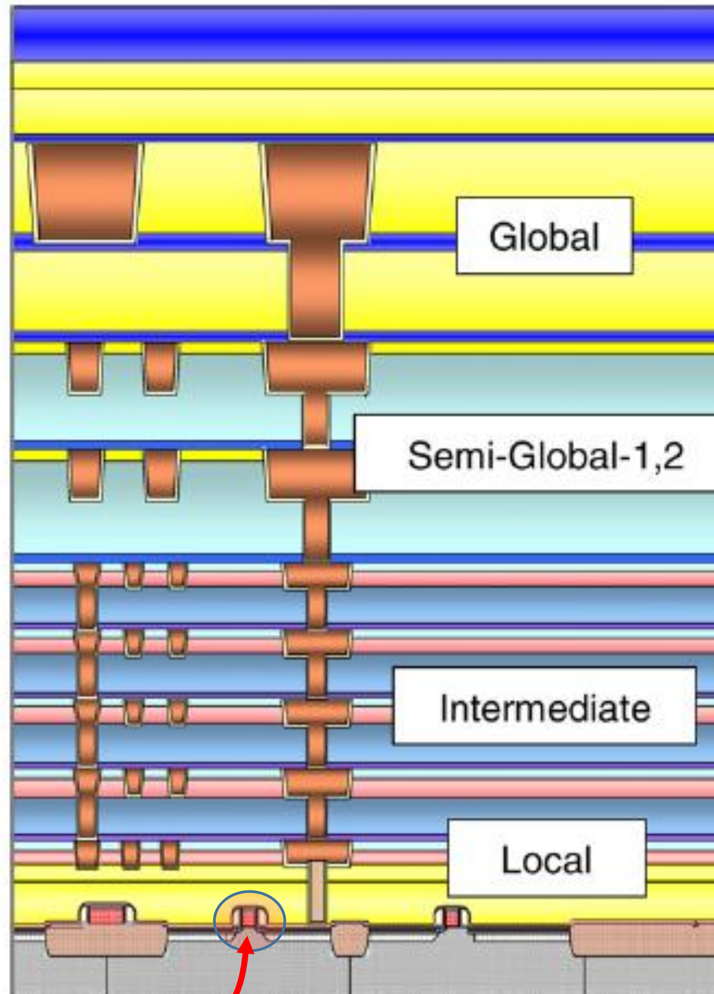
8-level IC metallization

This is ~2010 technology

Metal-8 LW
e.g. 100 nm

Metal-4 LW
e.g. 50 nm

Transistor
gate
linewidth
e.g. 30 nm



SiO2 (k=4.1)/SiN (k=7.0)

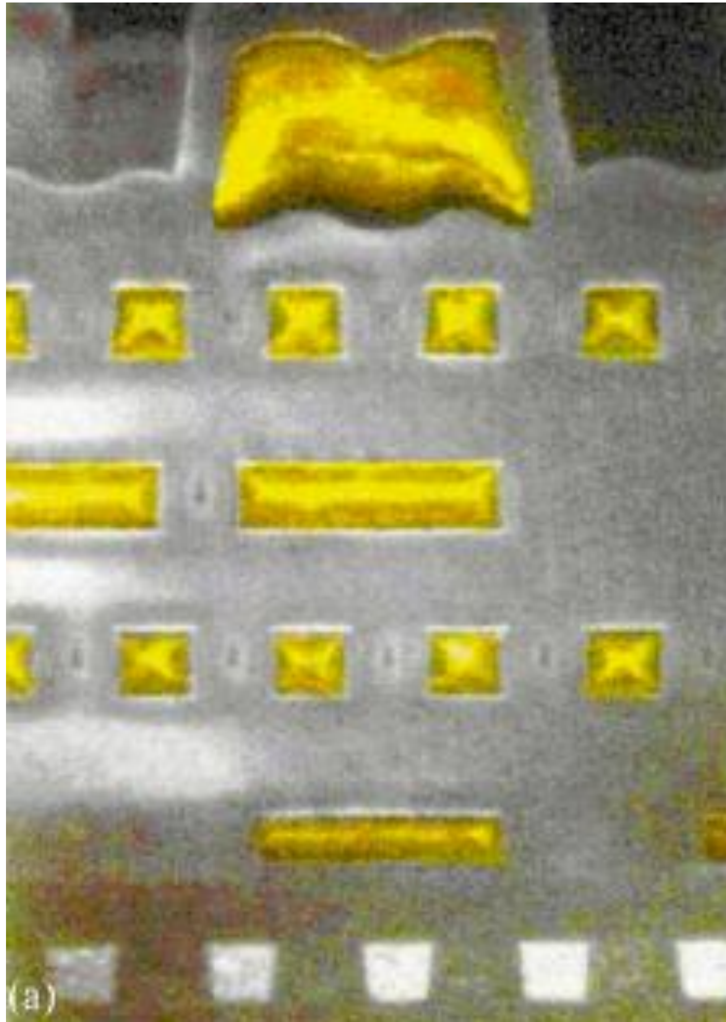
SiOC (k=2.9)/SiCN (k=4.9)

Wire:SiOC(k=3.0)/PAr (k=2.3)
Via:SiOC (k=2.3)/SiC (k=3.8)

PAr (k=2.3)

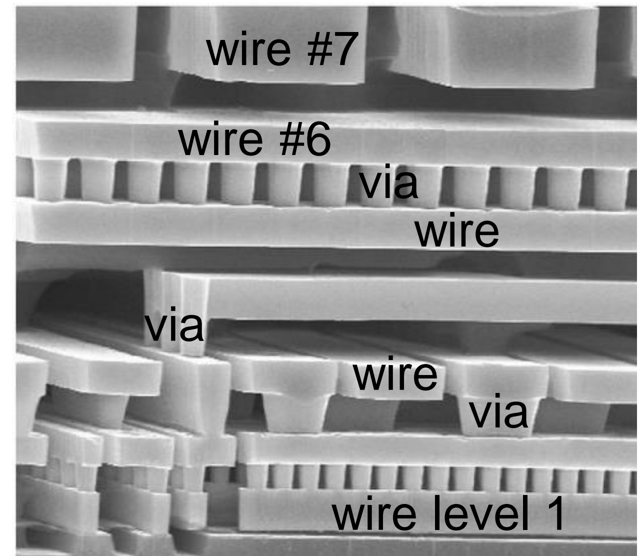
Solid-State Electronics 52 (2008) 1266–1273

Aspect ratio scaling

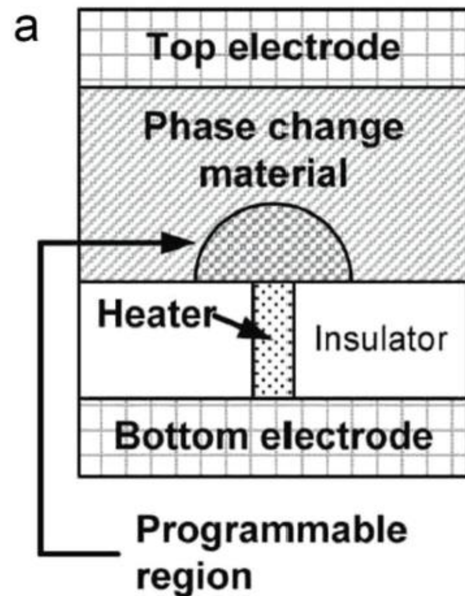


IBM

Actually, aspect ratio (height:width) does NOT scale; it has remained more or less 1:1 for decades.



Aspect ratio - nanodevices



This picture is highly schematic.

But if we know that 50 nm lithography linewidth is used to make it, we can make some good guesses:

Heater is clearly the smallest structure, i.e. width 50 nm.

Aspect ratio 2:1 is realistic, so insulator thickness is 100 nm, and PCM thickness 150 nm.

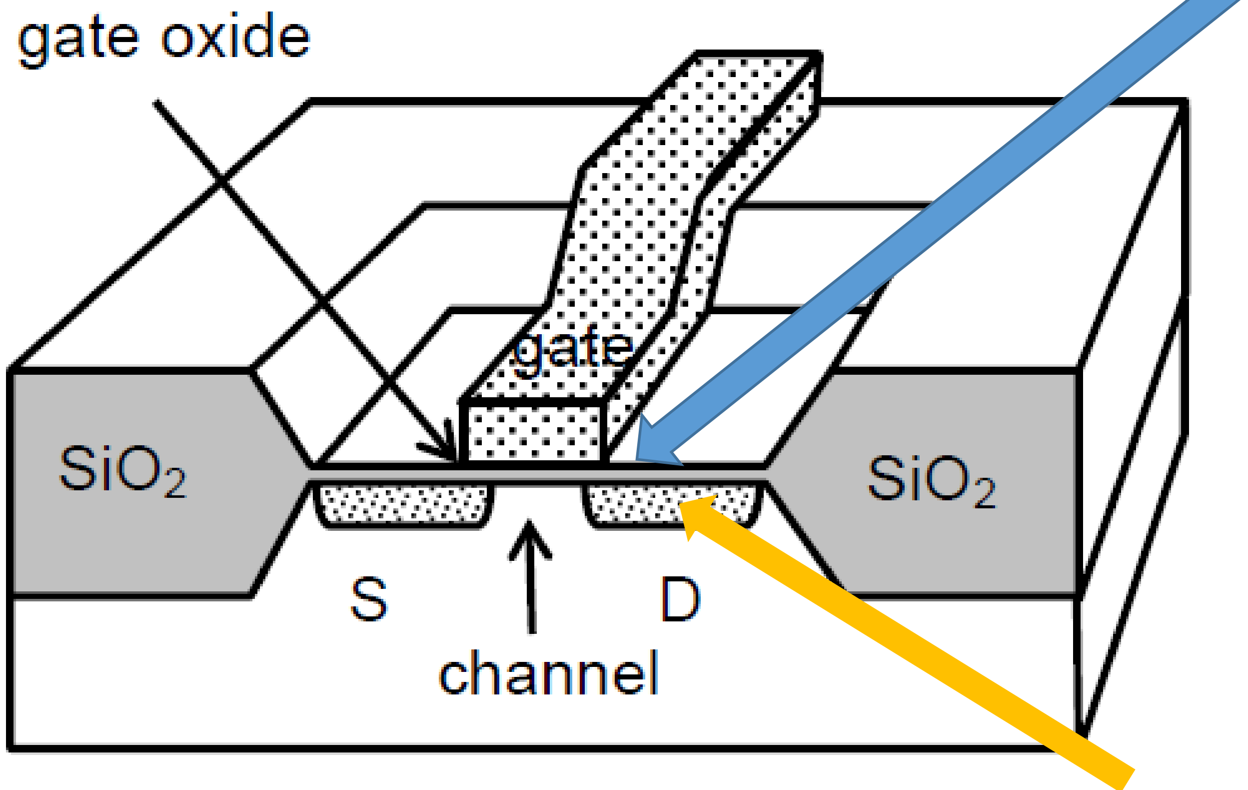
PCM = Phase Change Memory. PCM material is either crystalline or amorphous, and its resistance changes dramatically. Thermally programmed.

Etch selectivity scaling

Case 1: poly:oxide selectivity in gate etching

Case 2: contact hole etch selectivity (oxide:silicon)

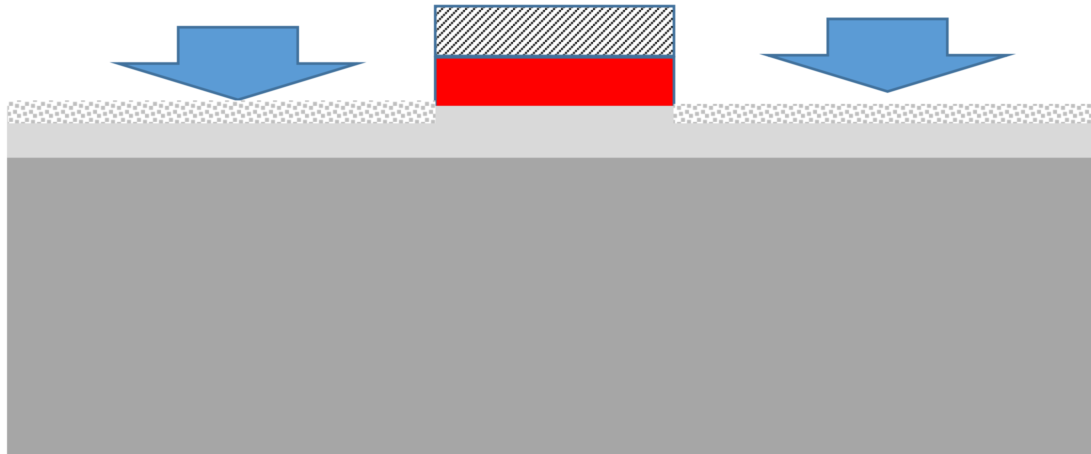
CMOS cross section



When we etch the gate, we do not want to etch thru gate oxide

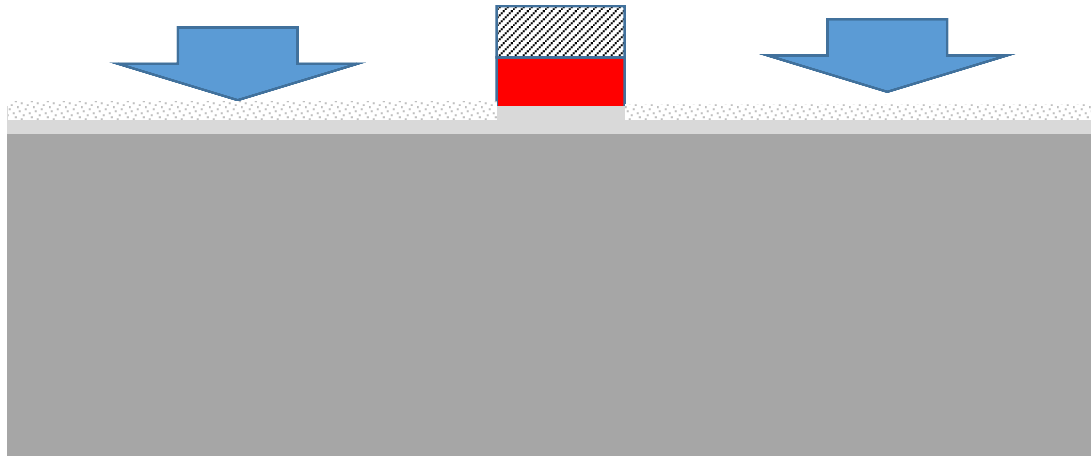
Later on, when we etch the contact holes, we must not etch thru the junction.

CMOS linewidth: 5 μm



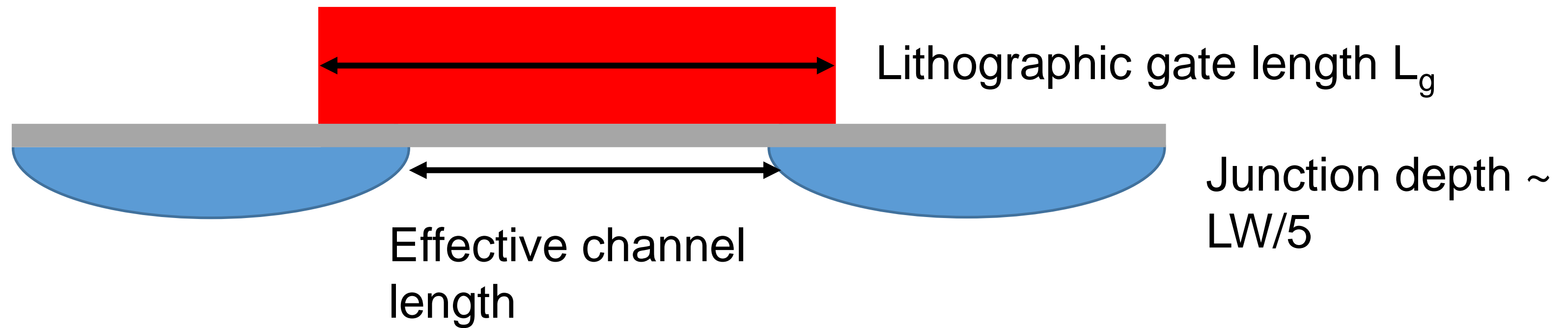
Polysilicon gate: 500 nm thick
Gate oxide thickness (LW/50) = 100 nm
Etch selectivity poly:oxide = 10:1
Overetch = 50 %
Oxide loss = nm
Oxide loss = % of original thickness

CMOS linewidth: 1 μm

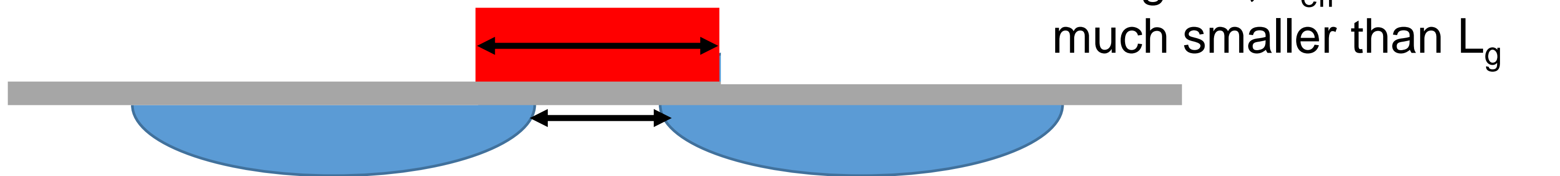


Polysilicon gate: 300 nm thick
Gate oxide thickness (LW/50) = 20 nm
Overetch = 50 %
Oxide loss = same % loss as in above,
Calculate etch selectivity poly:oxide needed to achieve this !

Junction depth scaling

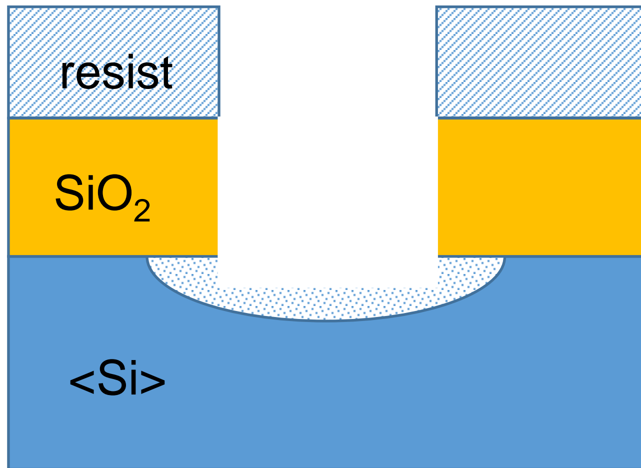


Not good, L_{eff} becomes much smaller than L_g

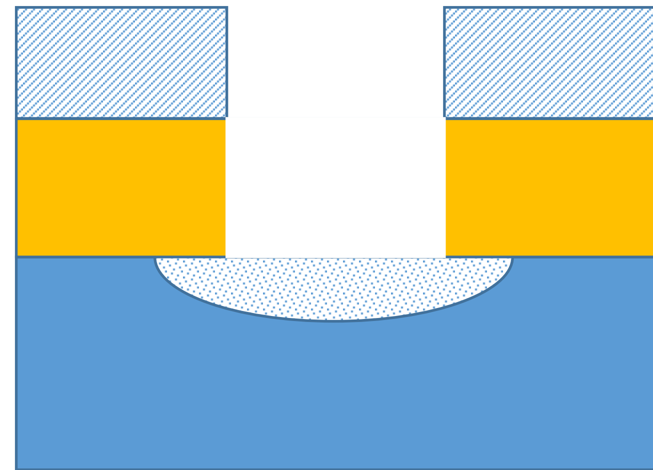


Junction depth has to be scaled when lithographic dimensions scaled.

Contact hole etch selectivity



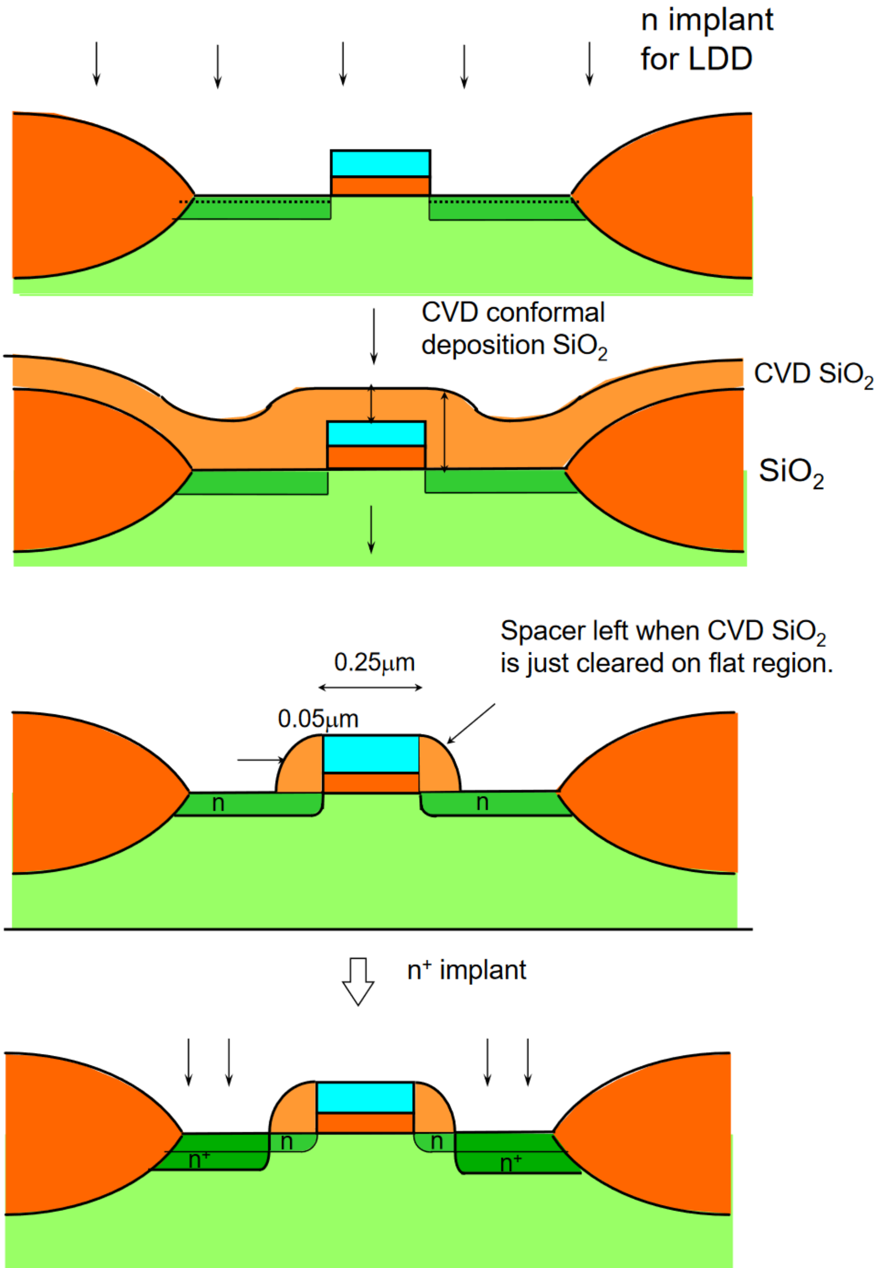
How deep can oxide etch penetrate into silicon ?



What selectivity is required if ox thickness 250 nm, ox etch rate 500 nm/min, and allowed silicon loss is 5 nm ? 30% overetch.

Etch time = 30 s

Overetch = 10 s, so 5 nm/0.16 min ≈ 30 nm/min



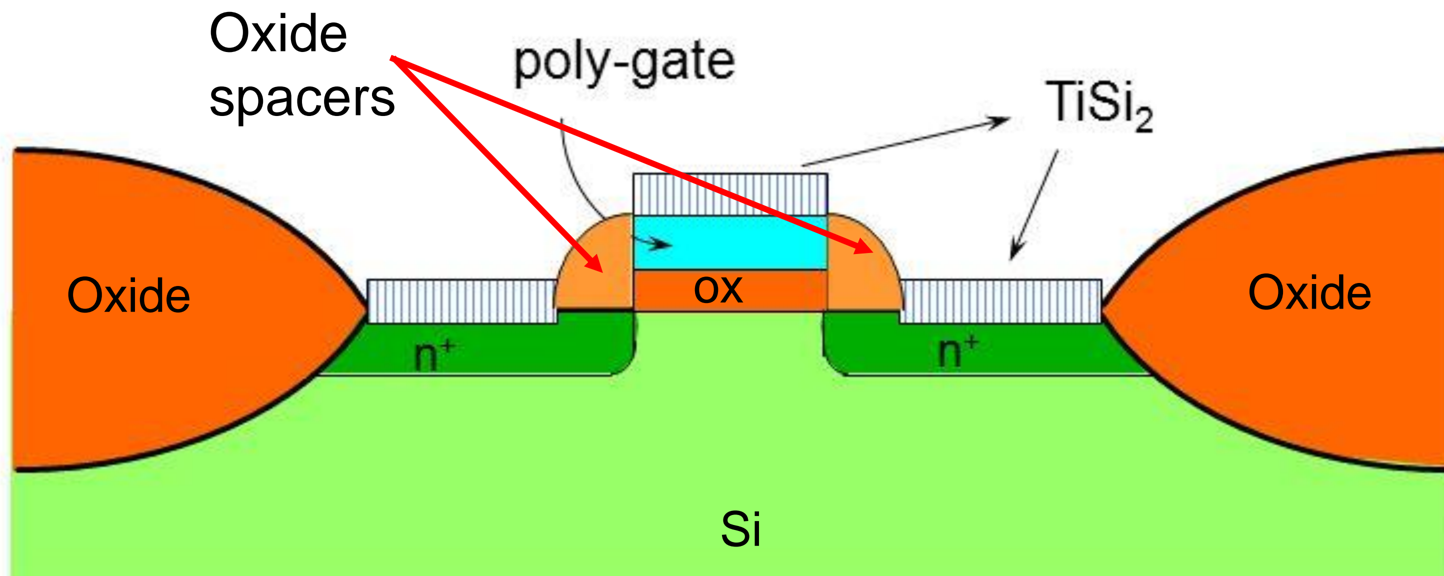
LDD:

1st implant, low dose
2nd implant, high dose

Spacer:

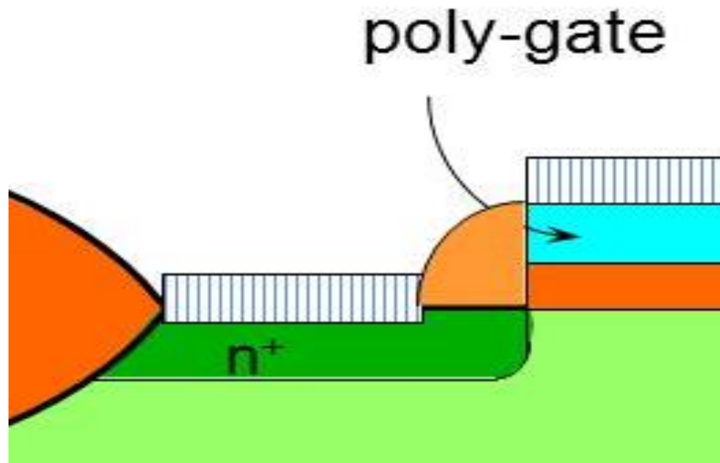
Conformal CVD deposition
Anisotropic etch

Self-Aligned Silicide Process (SALICIDE) using Ion Implantation and Metal-Si reaction



Oxide spacers are formed anisotropic plasma etch of CVD oxide over poly gate. Titanium deposition. $TiSi_2$ formation on <Si> and polysilicon alike.

Silicide thickness scaling



When junction depth is scaled down, silicide thickness must be scaled down.

If junction depth is 100 nm, silicide thickness e.g. 50 nm.

What is the original metal thickness ?

Choice of silicide

Want: low resistivity
low anneal temperature
small consumption of silicon

Silicide	Thin film resistivity (μΩcm)	Sintering temp (˚C)	Stable on Si up to (˚C)	Reaction with Al at (˚C)	nm of Si consumed per nm of metal	nm of resulting silicide per nm of metal
PtSi	28-35	250-400	~750	250	1.12	1.97
$TiSi_2$ (C54)	13-16	700-900	~900	450	2.27	2.51
$TiSi_2$ (C49)	60-70	500-700			2.27	2.51
Co_2Si	~70	300-500			0.91	1.47
CoSi	100-150	400-600			1.82	2.02
$CoSi_2$	14-20	600-800	~950	400	3.64	3.52
NiSi	14-20	400-600	~650		1.83	2.34
$NiSi_2$	40-50	600-800			3.65	3.63
WSi_2	30-70	1000	~1000	500	2.53	2.58
$MoSi_2$	40-100	800-1000	~1000	500	2.56	2.59
$TaSi_2$	35-55	800-1000	~1000	500	2.21	2.41

Take home messages

- Chip size should be as small as possible (from production efficiency; but large from functionality point of view)
- Small linewidths costlier but enable more functions.
- Big wafer size reduces costs.
- Advanced lithography is only done on large wafers.
- Large wafers are thicker because of mechanical strength.
- Thicker wafers not good for thru-wafer MEMS.
- Thin wafers good for solar, but mechanically weak.
- Usually aspect ratios are between 1:2 to 2:1.
- In nanodevices aspect ratios ~1:1
- High aspect ratios are rare, mostly in MEMS and DRAM.