Nano-CMOS and Moore's law

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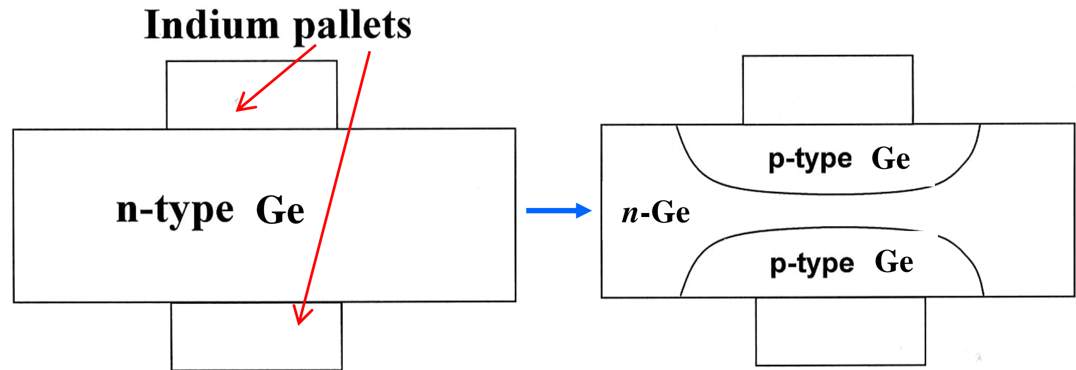
Chapter 38

Outline

- Moore's law
- Nanofabrication features
- Double patterning
- Cu metallization

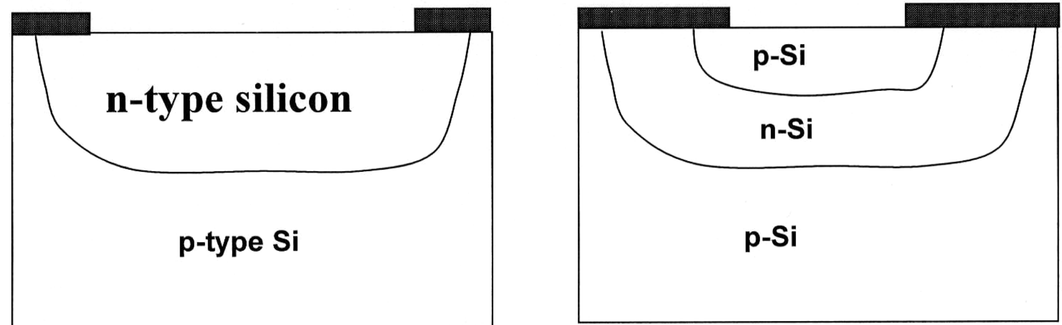
Transistor history

Bulk transistor



One chip – one transistor
Chip size 3 x 3 mm^2

Planar transistor



Semiconductor technology nodes

Scaling factor √2

- 10 µm – 1971
- 3 µm – 1975
- 1.5 µm – 1982
- 1 µm – 1985
- 0.8 µm – 1989
- 0.6 µm – 1994
- 0.35 µm – 1995
- 0.25 µm – 1998
- 0.18 µm – 1999
- 0.13 µm – 2000
- 90 nm – 2002
- 65 nm – 2006
- 45 nm – 2008
- 32 nm – 2010
- 22 nm – 2012
- 14 nm – 2014
- 10 nm – 2016
- 7 nm – 2018
- 5 nm – 2020
- 3 nm – 2022

Number of transistors per chip

Number of transistors

1.E+11
1.E+10
1.E+09
1.E+08
1.E+07
1.E+06
1.E+05
1.E+04
1.E+03
1.E+02
1.E+01
1.E+00

1950 1960 1970 1980 1990 2000 2010 2020

24 months
36 months
18 months

DRAM
Early Logic
Intel X86
NAND

IA2-90
4Gb
16Gb
8Gb
2Gb
512Mb
1Gb
IA2-65
256Mb
128Mb
1Gb
Core
64Mb
Intel IA64
P4-90
16Mb
PIII
PP
IA
IA2
4Mb
PII
1Mb
Pnt
P4-130
256Kb
486
P4-180
64Kb
386
8008
8086
286
8080
8088
256Kb SRAM
1Kb
16Kb
4Kb
8085
1st MOS IC
4004
Mosiac
Flip Flop
1st IC
Op Amps
RTL 907

http://www.icknowledge.com/trends/trends.html

Transistor Count Trends

Transistor Count Trends

Transistors per Die

1.0E+12
1.0E+11
1.0E+10
1.0E+9
1.0E+8
1.0E+7
1.0E+6
1.0E+5
1.0E+4
1.0E+3
1.0E+2

71 73 75 77 79 81 83 85 87 89 91 93 95 97 99 01 03 05 07 09 11 13 15 17 19

DRAM
NAND Flash (3D)
NAND Flash (2D)
Apple APU
Intel PC MPU
Intel Server MPU
Nvidia GPU

Sources: Intel, SIA, Wikichip, IC Insights

Moore’s law

- The number of components per IC doubles every 18 -24 months.
- Introduced in 1965
- Does not depend on technology
- Reflects development of mankind, i.e., technology in general sense

Number of mask layers

Number of Mask Layers

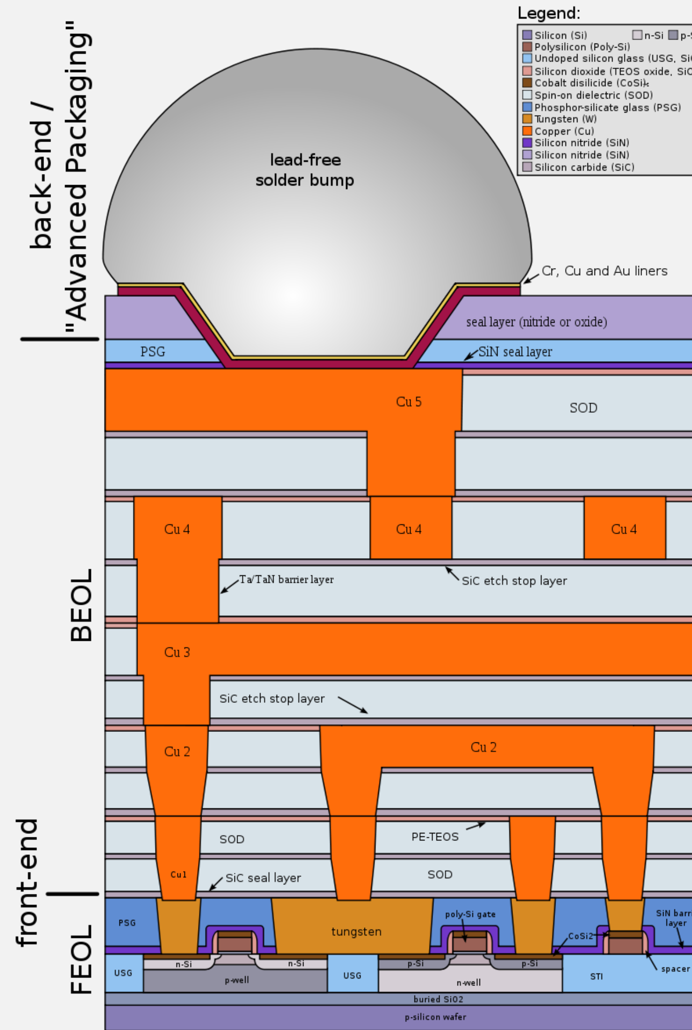
50
40
30
20
10
0

SiGe
CMOS Logic
DRAM
BiCMOS Logic
Flash
eDRAM
Bipolar
SRAM
PMOS/NMOS Logic

1960 1970 1980 1990 2000 2010 2020

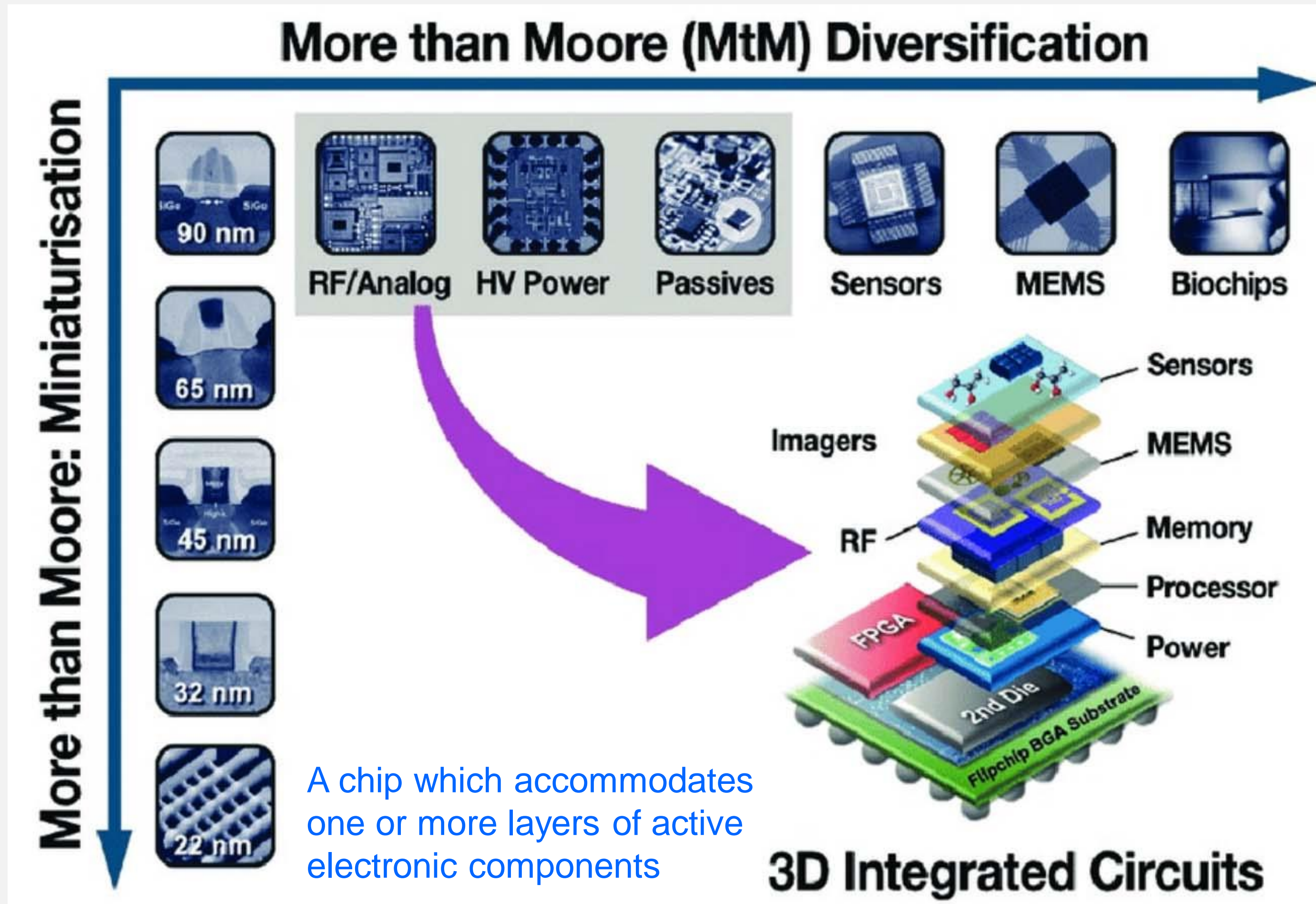
http://www.icknowledge.com/trends/trends.html

CMOS chip, as built in the early 2000s



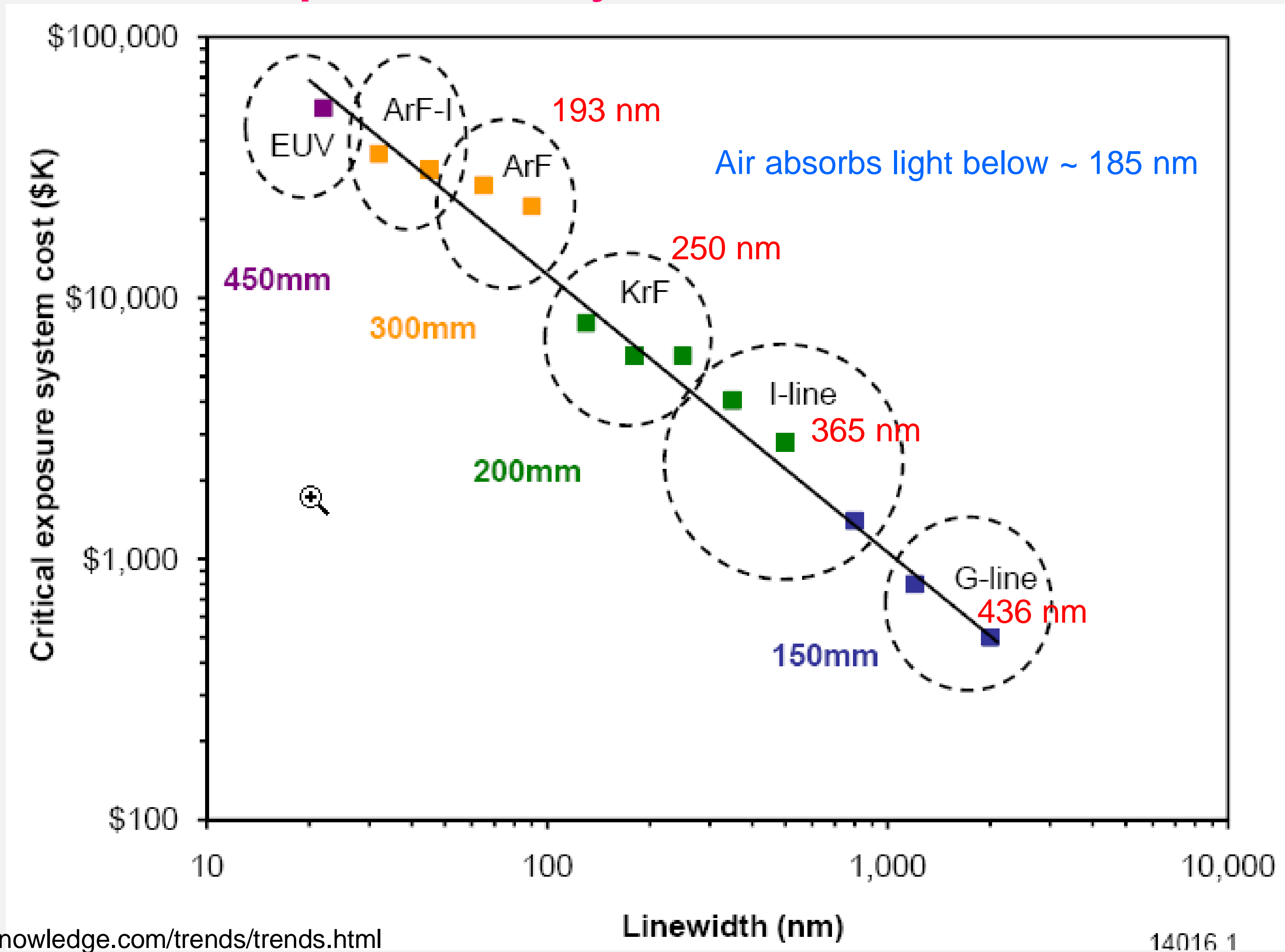
Integrated circuit - Wikipedia

3D integrated circuits



Falub, Claudiu, 2018/01/19
Innovating the Soft Magnetics for Tomorrow's RF Passive Devices

Exposure system cost



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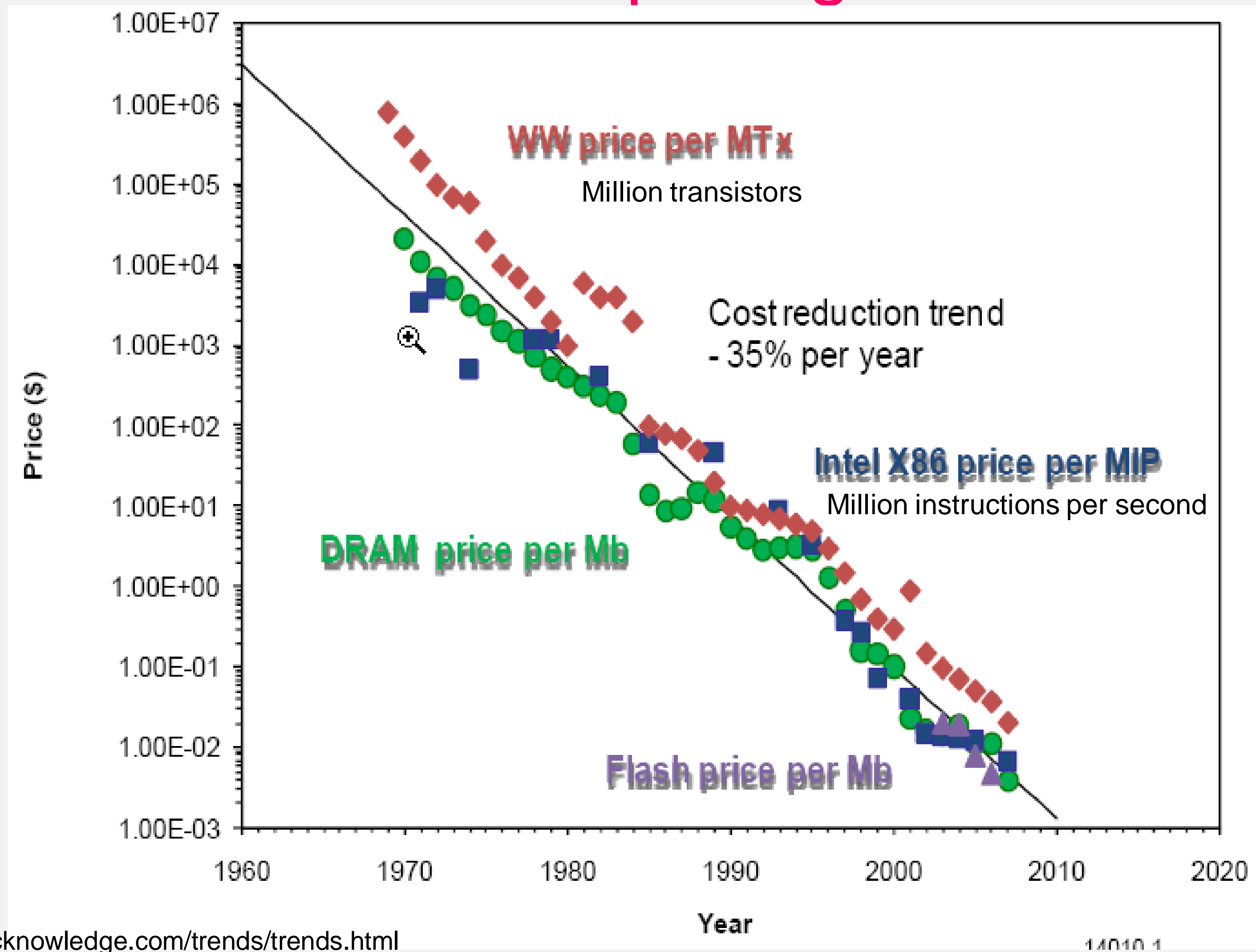
Product pricing



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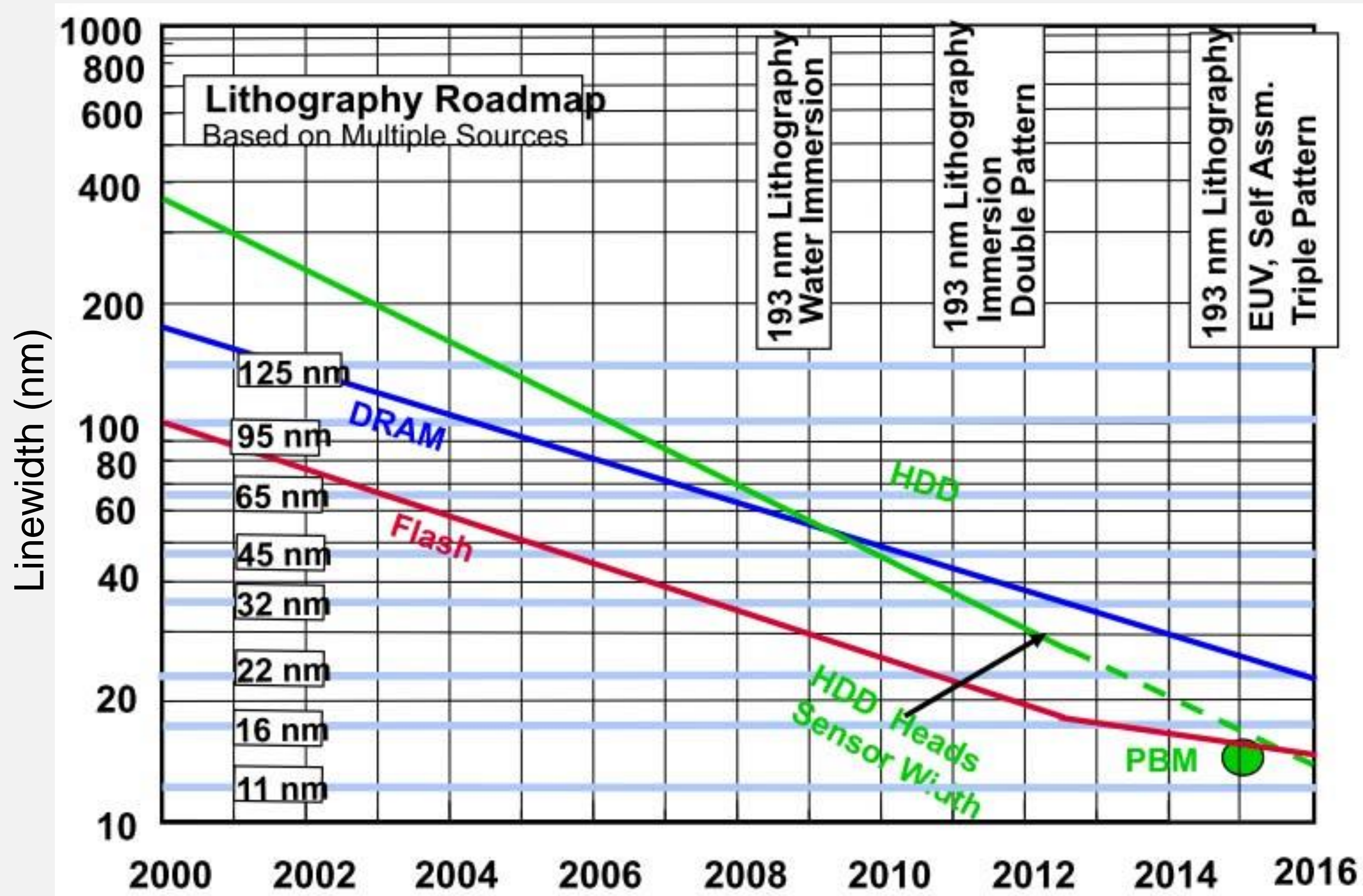
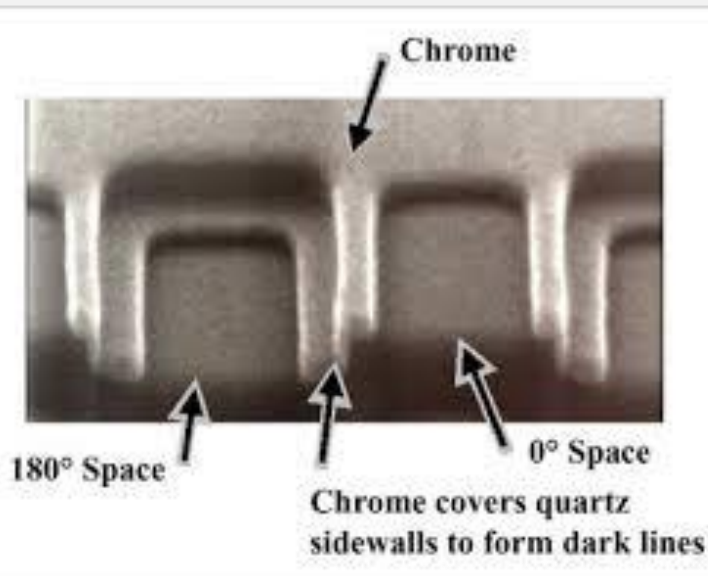
Microlithography trends

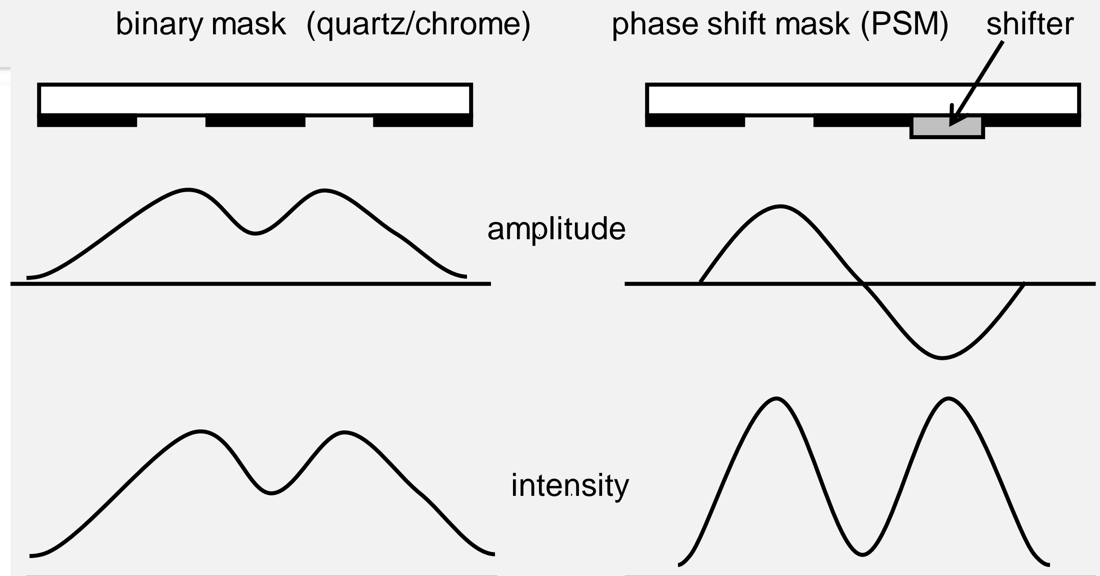


ITRS Roadmap 2012

Phase shift mask (PSM)

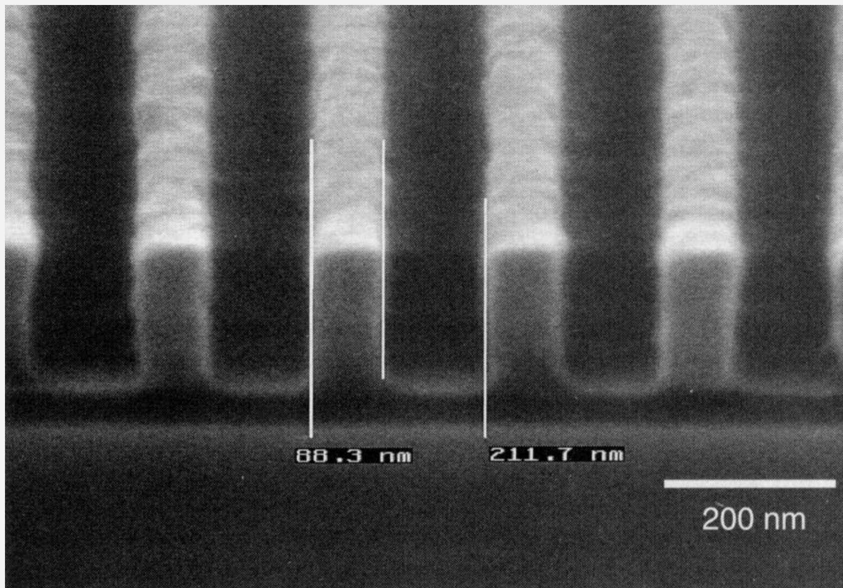
- Phase shift for light traveling:
  - in the air for a distance L is
    $\Phi = 2\pi L/\lambda$,
  - in the phase shifter material with index of refraction "n",
    $\Phi = 2\pi nL/\lambda$.
- For 180 degree phase shift, $\Delta\Phi = 180^0$, the condition for shifter thickness is given by
  $L\,(n\text{-}1) = \lambda/2$



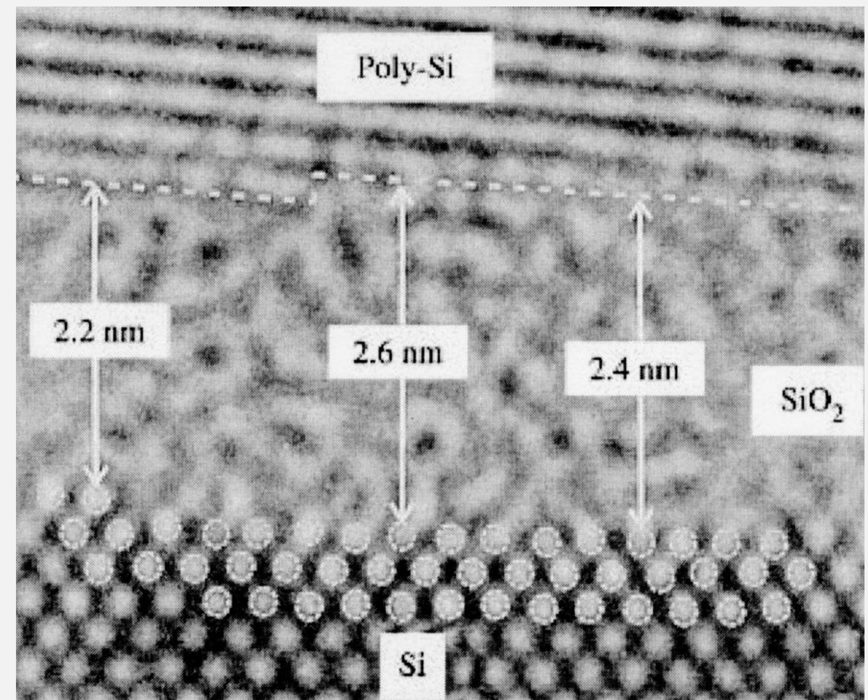


PSM application and quantized SiO_2

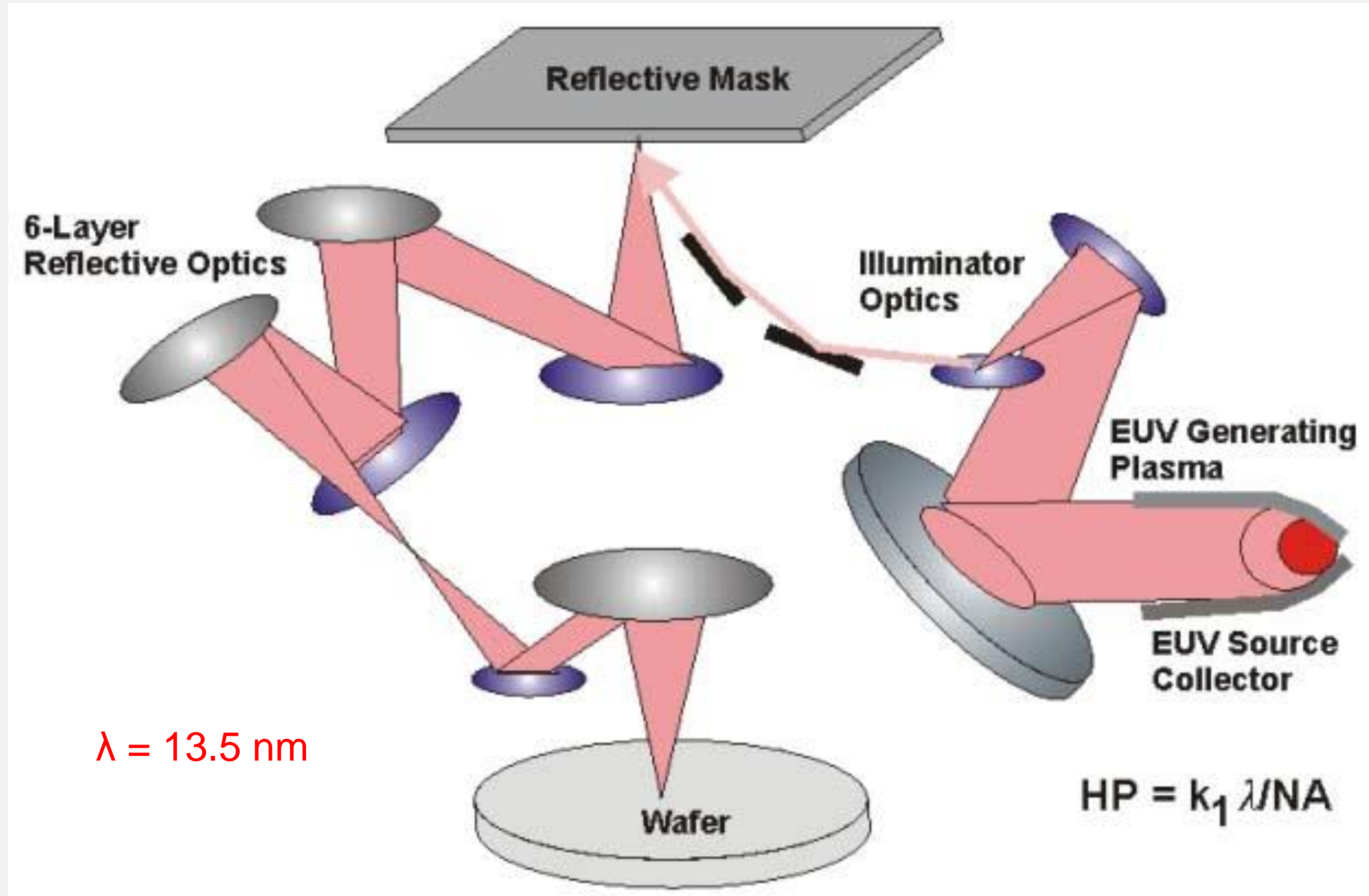
Linewidth λ/2, λ=193nm



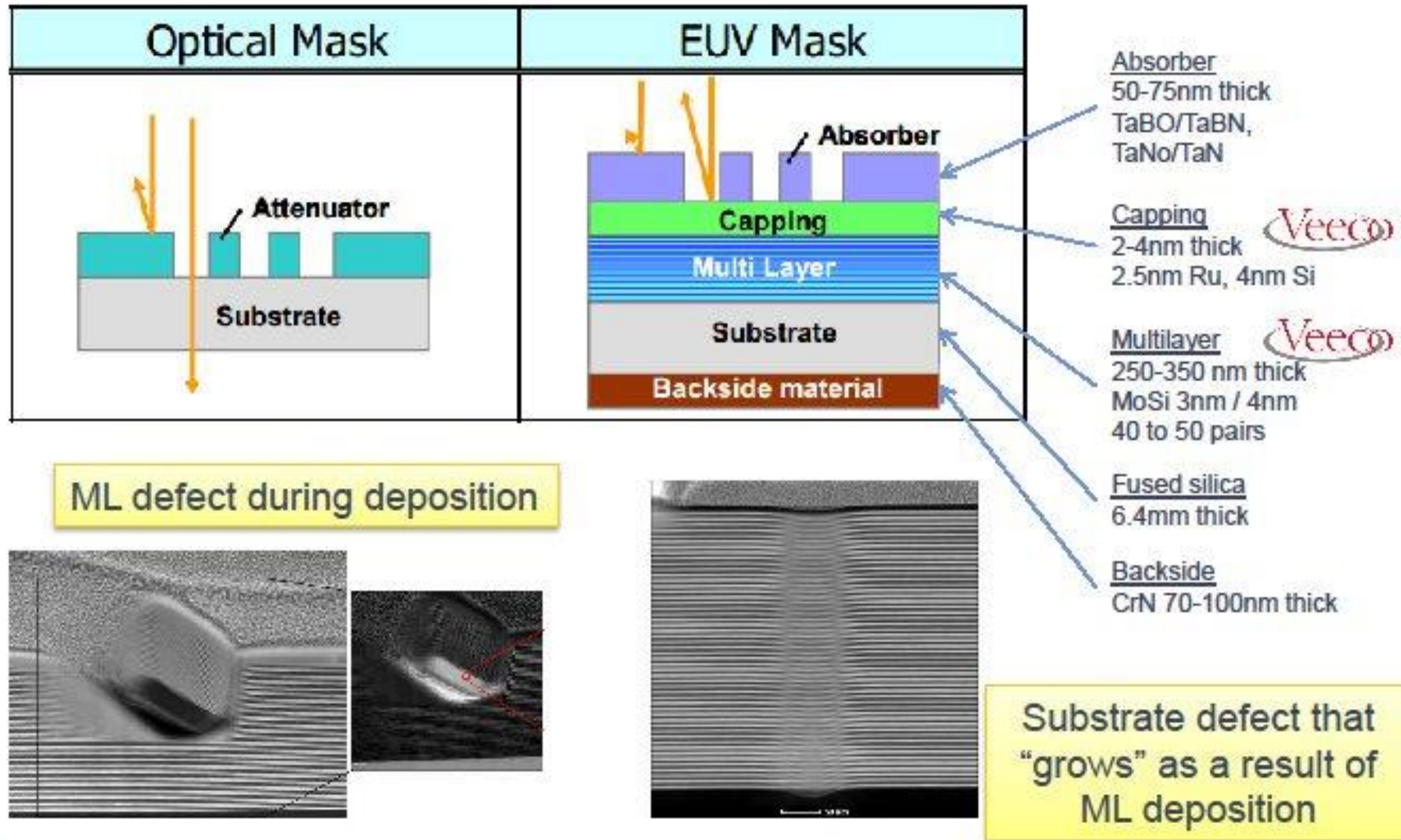
Quantized gate oxide thickness



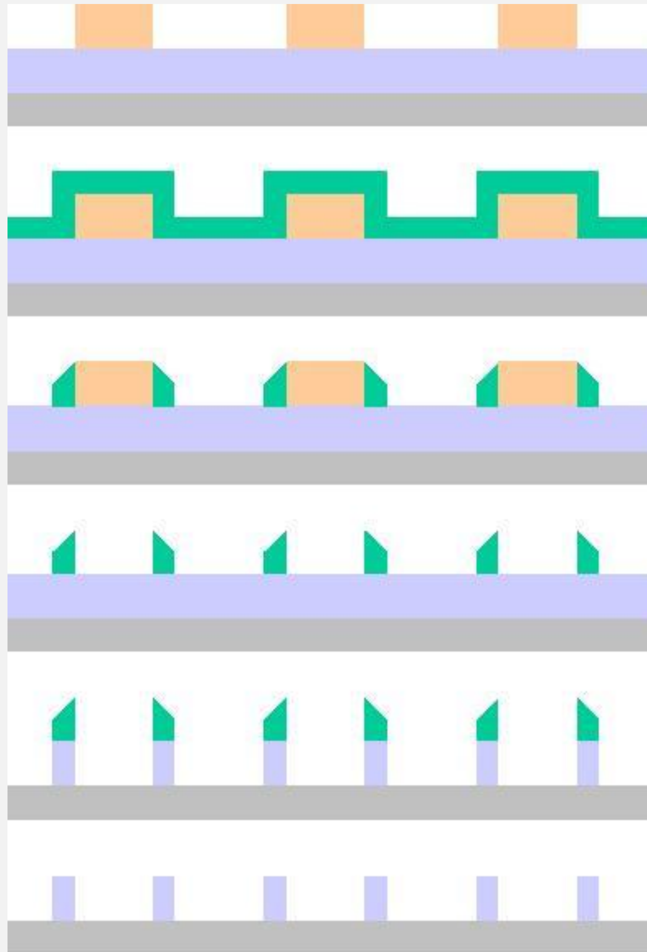
EUV, starts 2020



EUV mask



Double patterning



first pattern – PR mask

CVD or ALD deposition

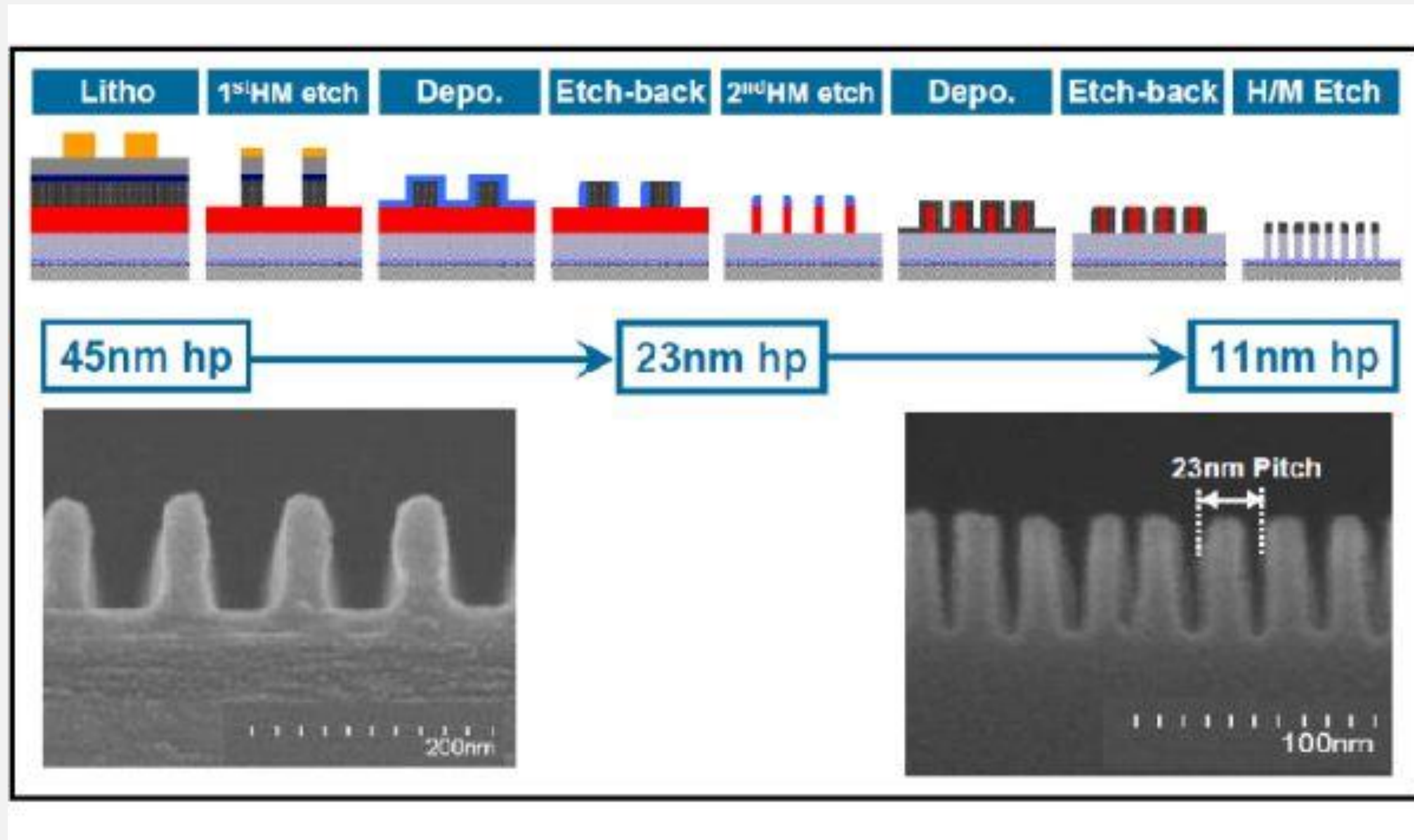
spacer formation by RIE

first pattern (PR) removal

etching with spacer mask

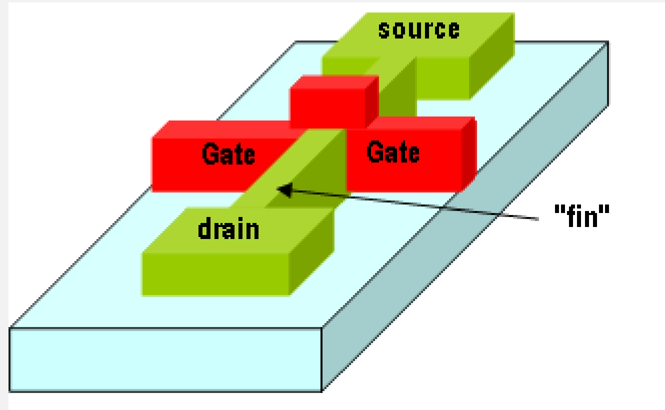
spacer residues removing

Multiple (triple) patterning I

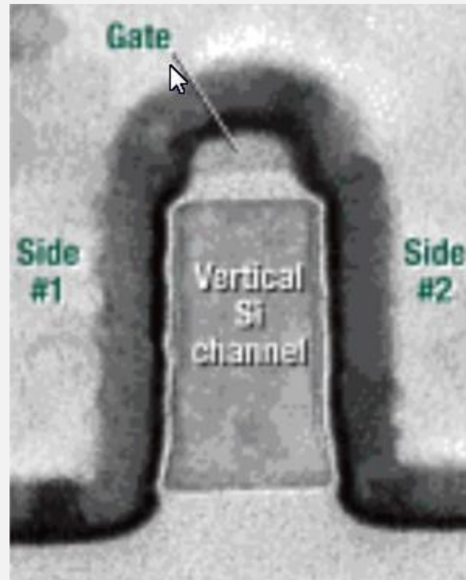


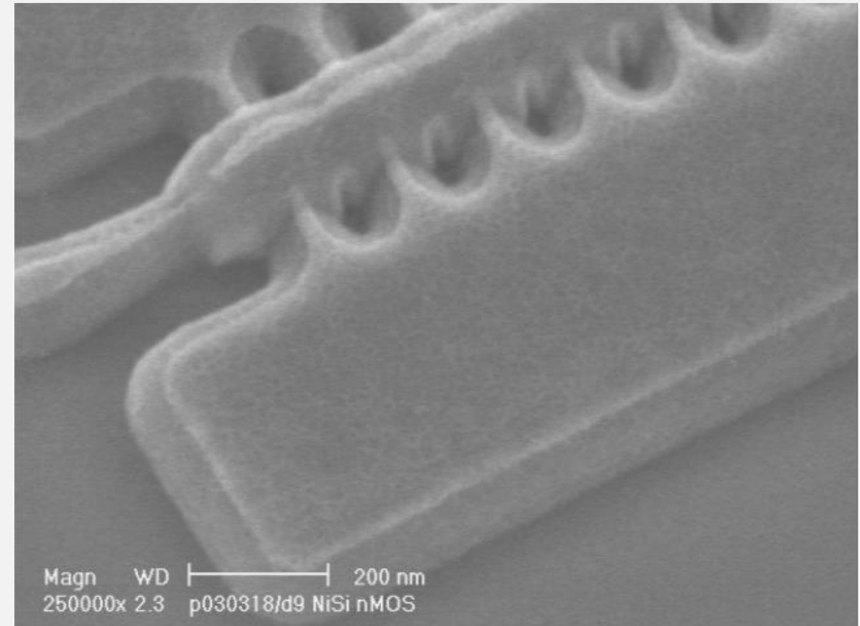
HM – hard mask

FinFET



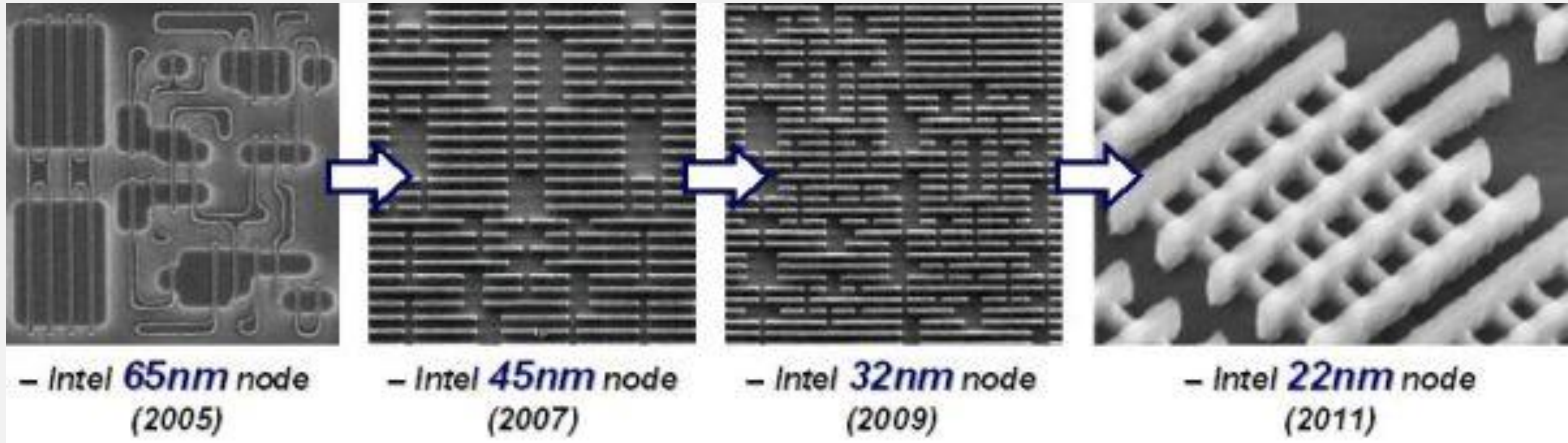
14 nm FinFET: Two levels of air-gap-insulated interconnects at 80 and 160nm minimum pitches. Eight layers of 52nm pitch interconnects embedded in low-k dielectrics. 15 levels of Cu interconnect

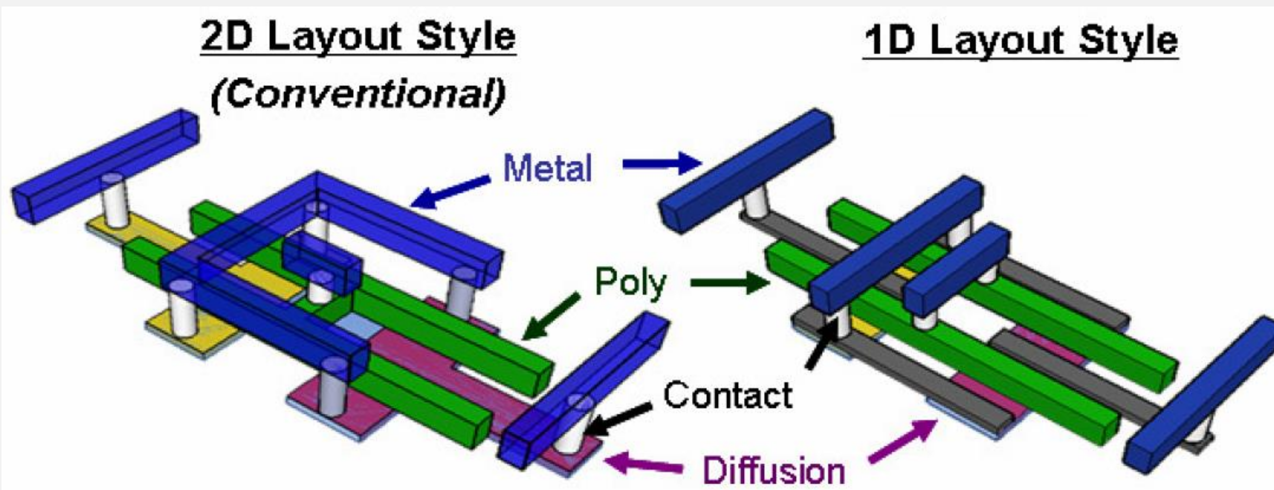




32 nm – the last node with planar FETs

1-D gridded layout



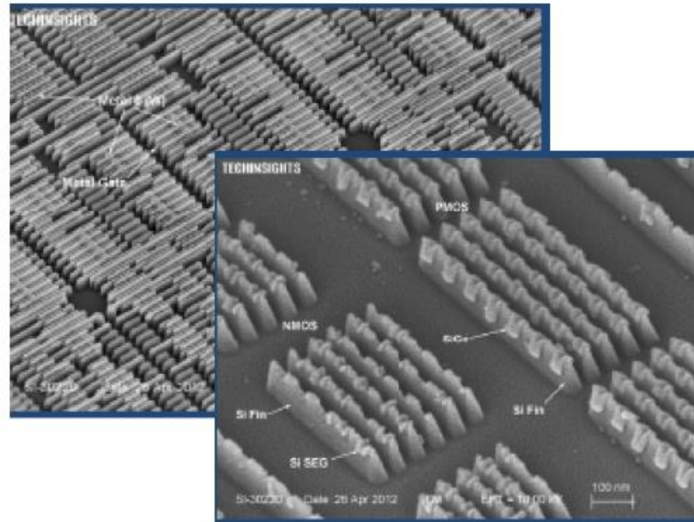


The vertical fins (9nm) of Intel's tri-gate transistors passing through the gates

David K. Lam et al., Multibeam Corporation and Tela Innovations

Multiple patterining II

FinFET Formation – Scalable to 10nm w/o EUV



*TechInsights, Intel Ivybridge

Self Aligned Double Patterning
With Cut Mask for Fin and Gate

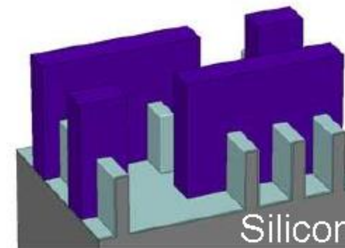
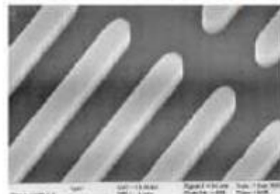
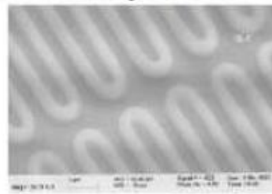


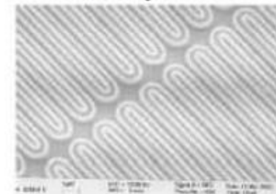
Photo-lithographically defined sacrificial structures



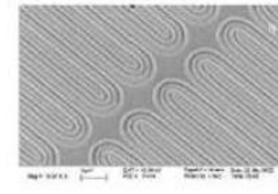
1st Spacers



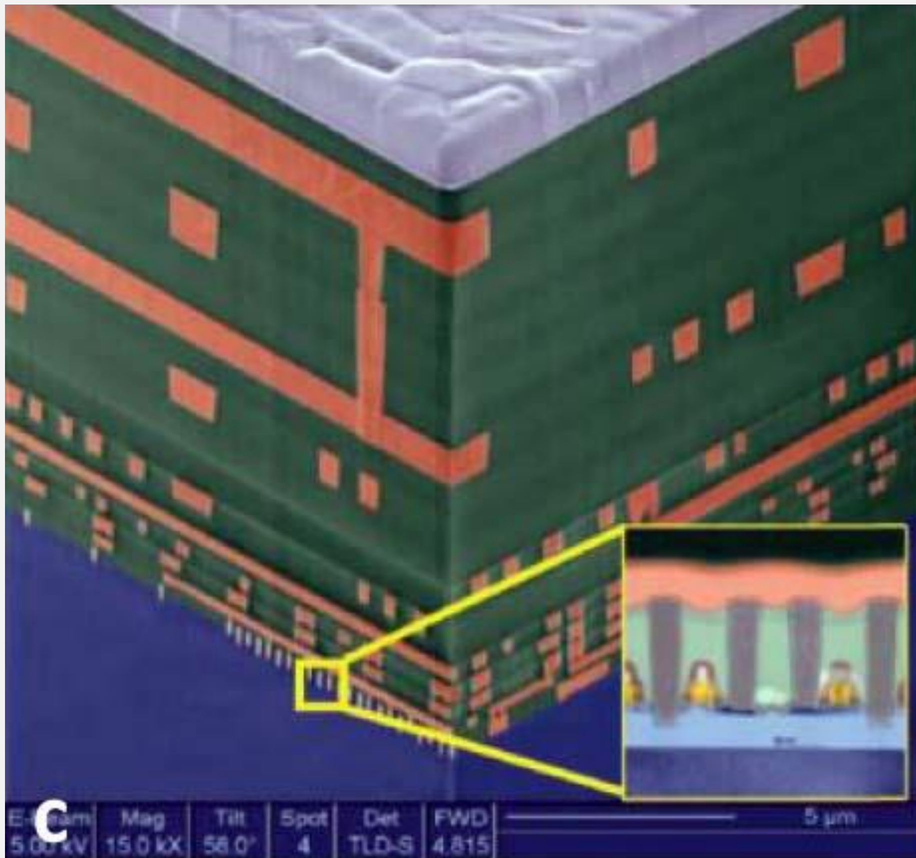
2nd Spacers

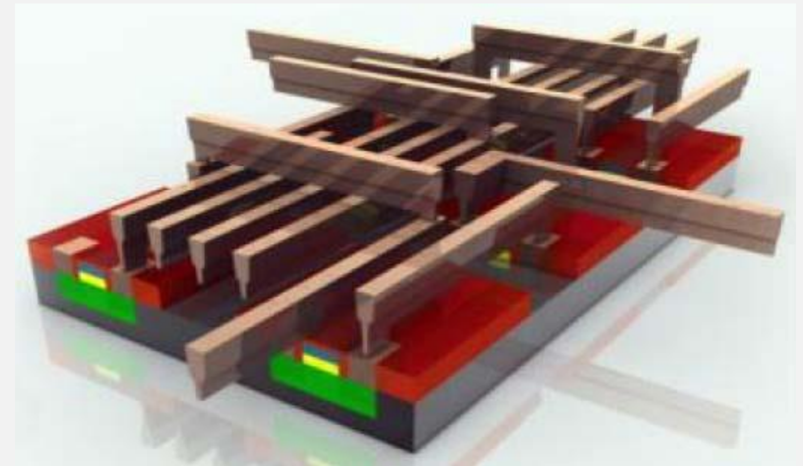


3rd Spacers



Cu metallization





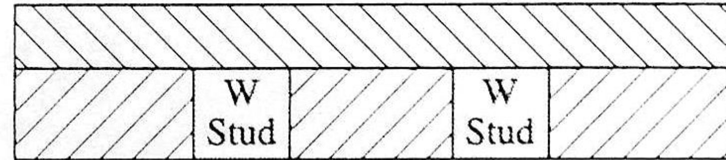
www.intel.com

Issues with Cu metallization

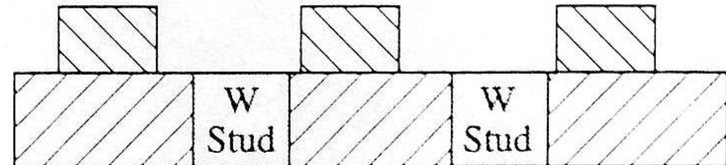
- Adhesion to dielectric
- Diffusion in (and reacion with) dielectric
- Compatibility to lower level metallization
- Deposition
- Etching / patterning CMP
- Contamination on the chip
- Contamination in the equipment

Metal-CMP planarization (damascene)

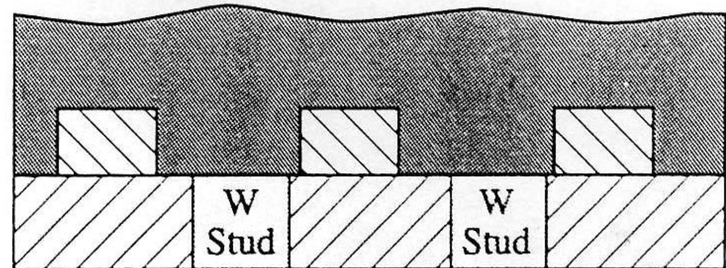
Oxide deposition



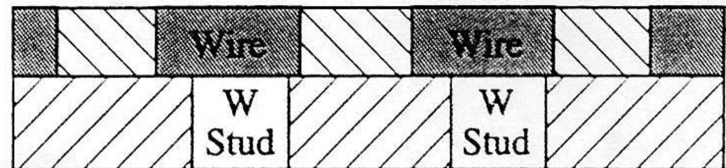
Wire litho, oxide RIE



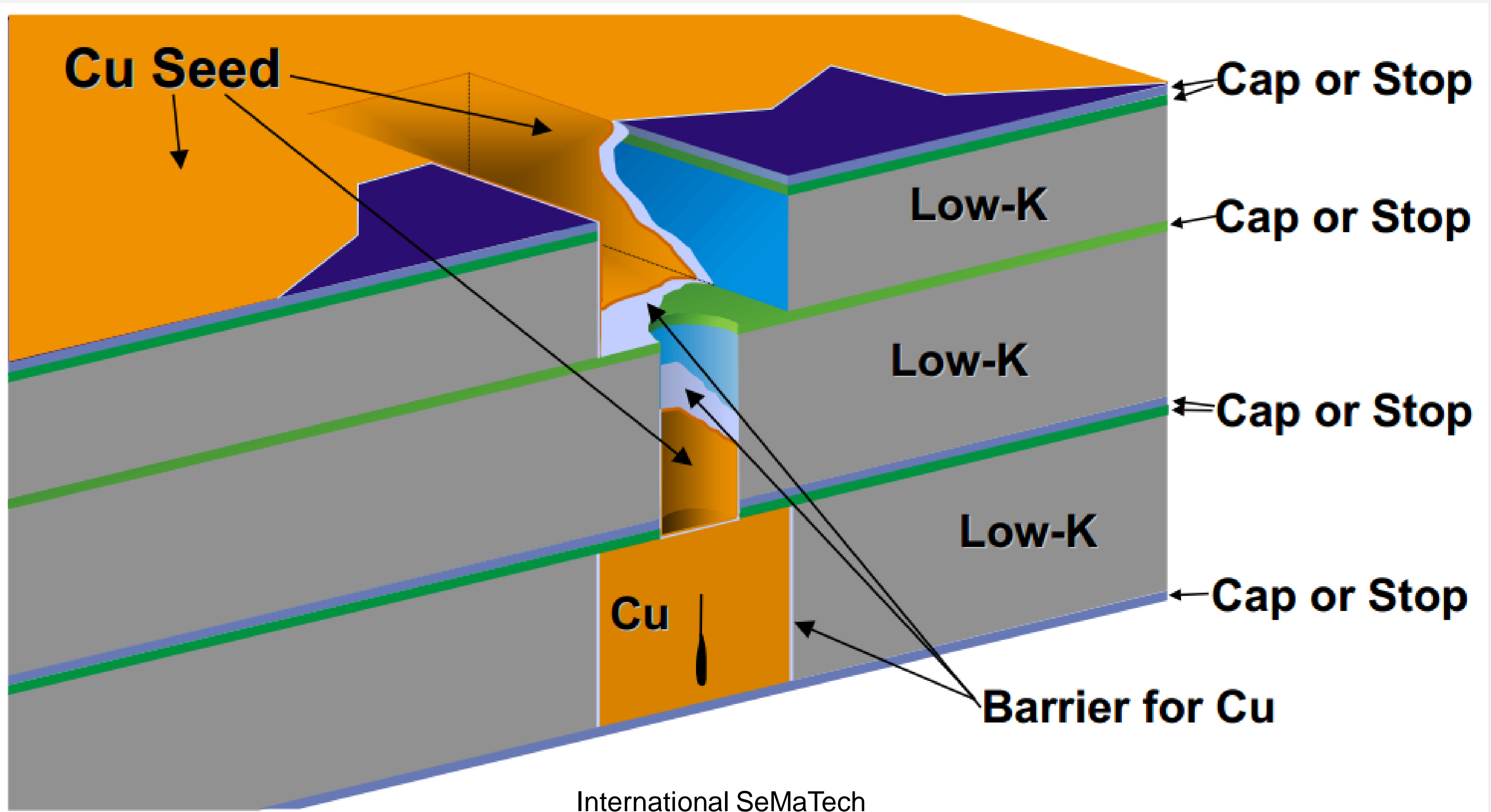
Metal stack depostion



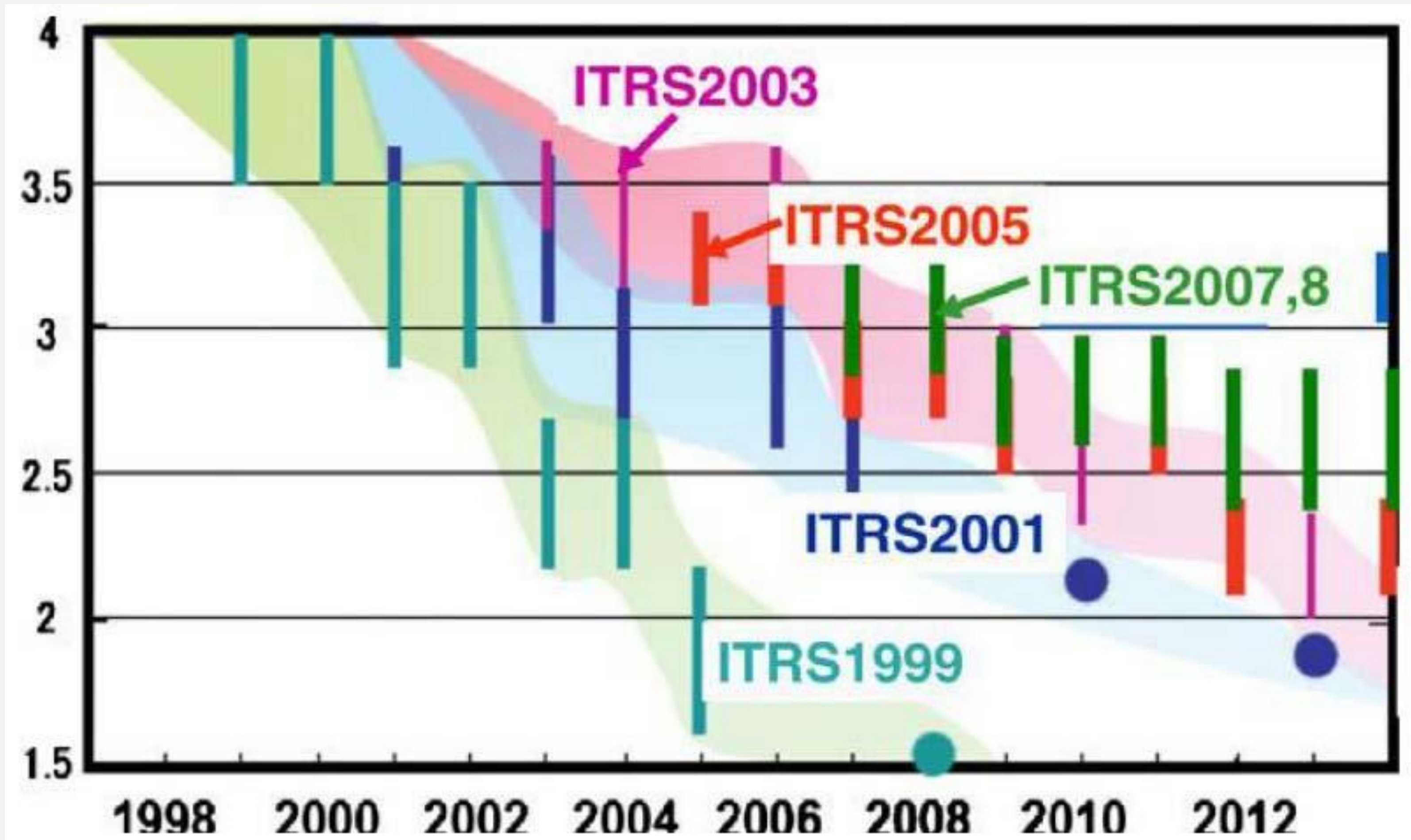
Metal CMP



Dual damascene unit structure



Low-K is hard…



Low-k materials

Oxide Derivatives

F-doped oxides (CVD)	$k = 3.3\text{-}3.9$
C-doped oxides (SOG, CVD)	$k = 2.8\text{-}3.5$
H-doped oxides (SOG)	$k = 2.5\text{-}3.3$

Organics

Polyimides (spin-on)	$k = 3.0\text{-}4.0$
Aromatic polymers (spin-on)	$k = 2.6\text{-}3.2$
Vapor-deposited parylene	$k \sim 2.7$
F-doped amorphous carbon	$k = 2.3\text{-}2.8$
Teflon/PTFE (spin-on)	$k = 1.9\text{-}2.1$

Highly Porous Oxides

Xerogels/Aerogels	$k = 1.8\text{-}2.5$

Air

$k = 1$

How long can this scaling continue ?

- If all goes as predicted by Moore's law, in 2059, the 100th birthday of the integrated circuit, we will have:
- 2.5 Å minimum linewidth
- 0.04 Å gate oxide thickness
- 2 mV operating voltage
- 64 exabit DRAMs (exa = 10^{18})