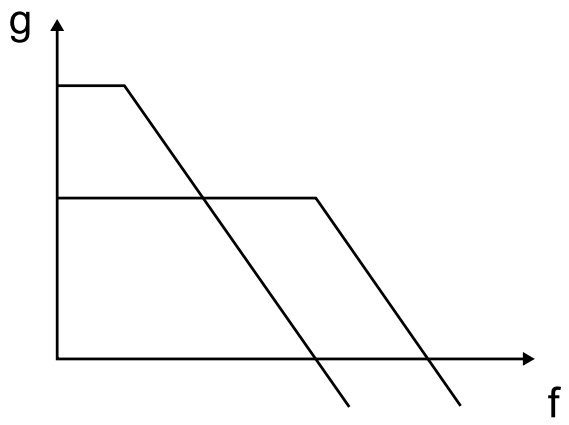
ELEC-E3530

Integrated Analog Systems L5 Nonidealities in SC-circuits

Non-idealities in SC integrators

- charge transfer error
- error charges from switches
- noise
- PSRR



Charge transfer error

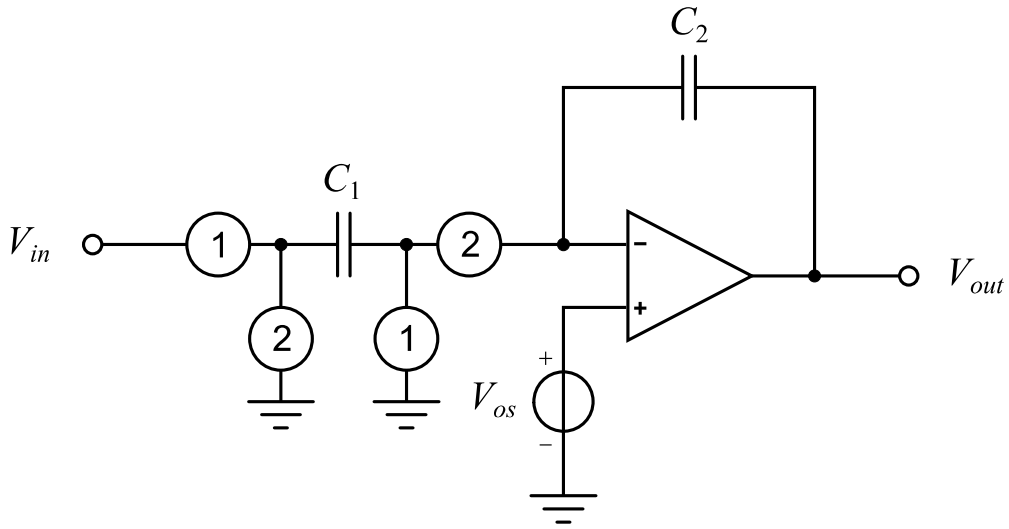
- static error
- dynamic error

Caused by:
- amplifier gain
- amplifier bandwidth
- amplifier current drive capability (slewing)
- amplifier internal poles (doublet's)
- parasitic capacitors
- channel charge of switches
- clock feedthrough in switches

Results in:
- offset
- gain error
- distortion noise

Fully differential configuration

Amplifier offset-voltage in SC integrators

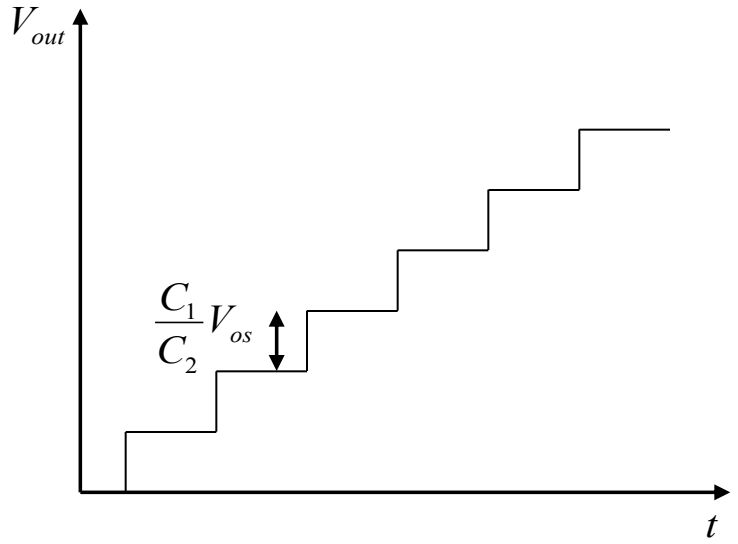


$$\Delta Q_2 = C_1\left(V_{in} - V_{os}\right) = C_1 V_{in} - C_1 V_{os}$$

$$\Delta V_{out} = \frac{\Delta Q_2}{C_2} = \frac{C_1}{C_2}\left(V_{in} - V_{os}\right)$$

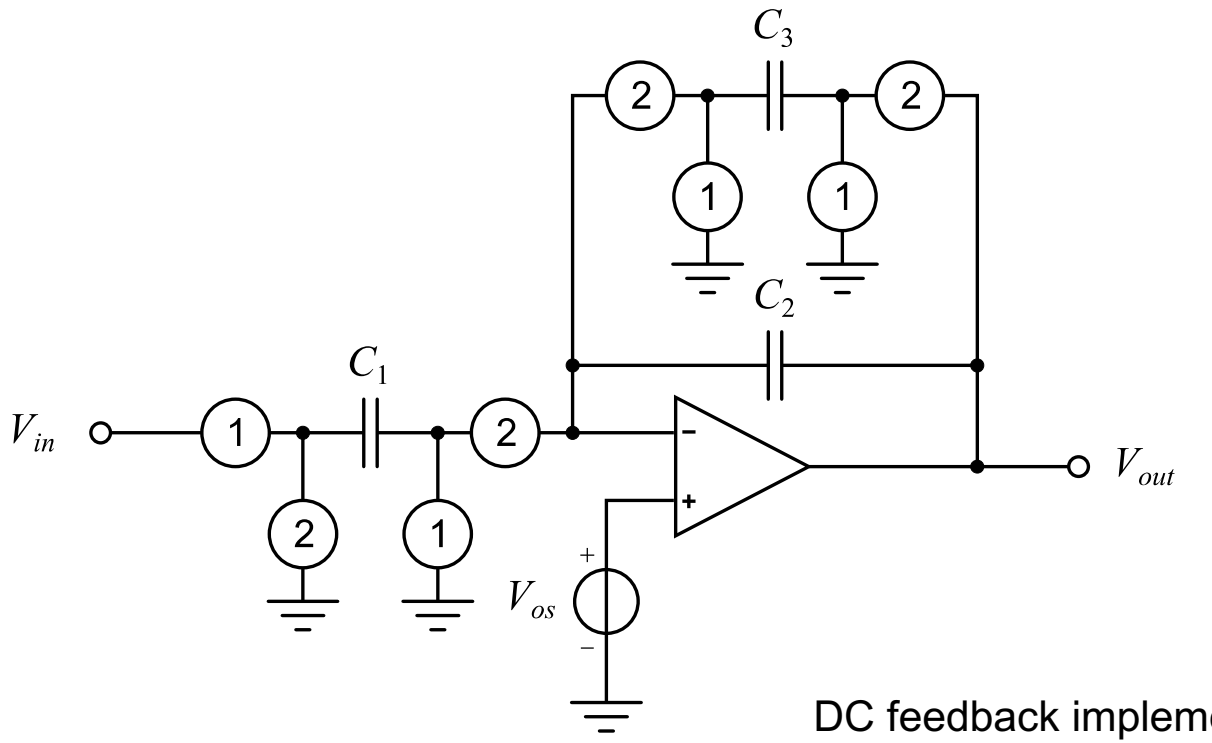
$$ol.\,V_{in} = 0$$

During every clock-cycle a charge packet of $\Delta Q_2 = -C_1 V_{OS}$ is transferred into the integrating capacitor C_2



$\Rightarrow$The accumulated charge will drive the output to either of the supplies and the amplifier saturates $\Rightarrow$ DC-feedback is needed!

SC integrator with DC feedback

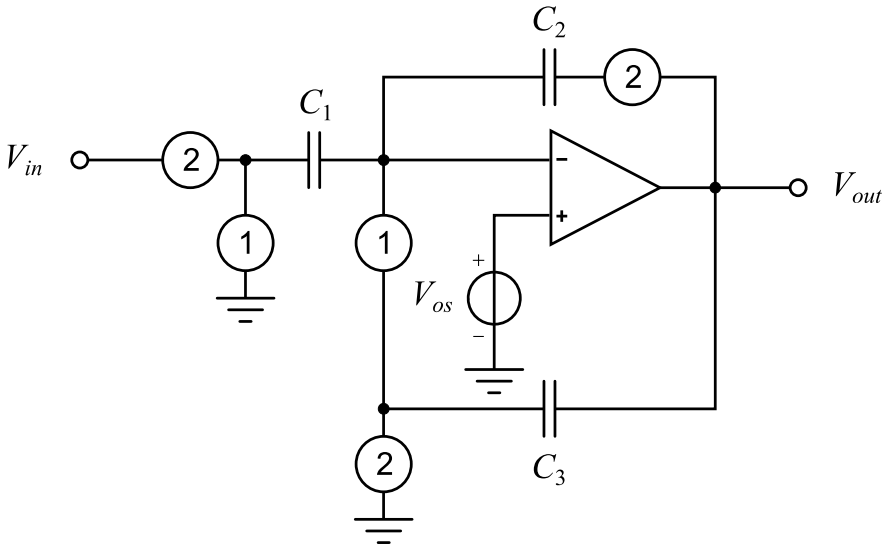


DC feedback implemented with a switched capacitor C_3.
Now the integrator output offset is limited to

assume $V_{in} = 0 \Rightarrow$

$$V_{out} = \frac{C_1}{C_3} \cdot V_{os}$$

Offset free SC integrator



Phase ϕ_1: offset is pre-sampled by C_1

Phase ϕ_2: input voltage is sampled by C_1 and charge C_1 V_{in} is transferred to C_2

Charge transfer equation:

$$\Delta Q_2 = -C_1\left(V_{in} - V_{os}\right) - \Delta Q_1$$

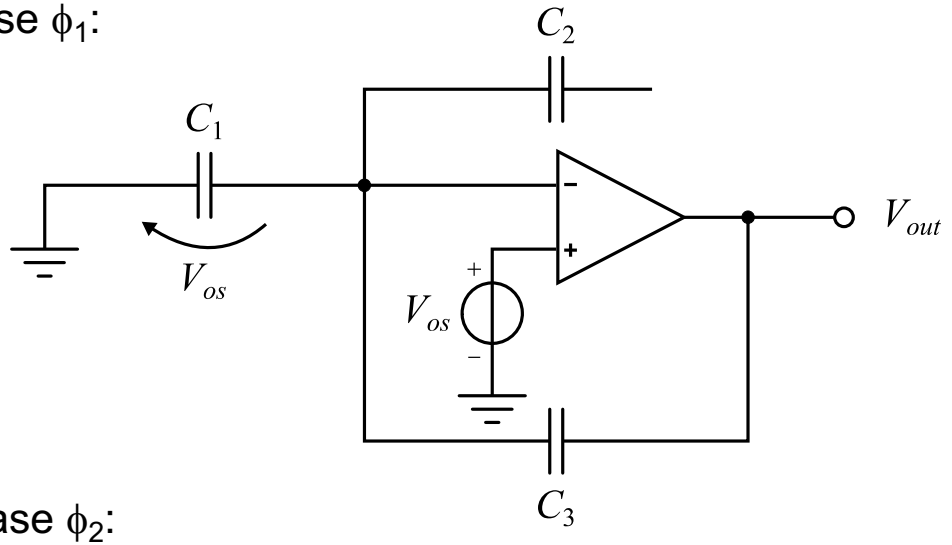
$$\Delta Q_2 = -C_1 V_{in} + \Delta Q_1 - C_1 V_{os}$$

$$= -C_1 V_{in}$$

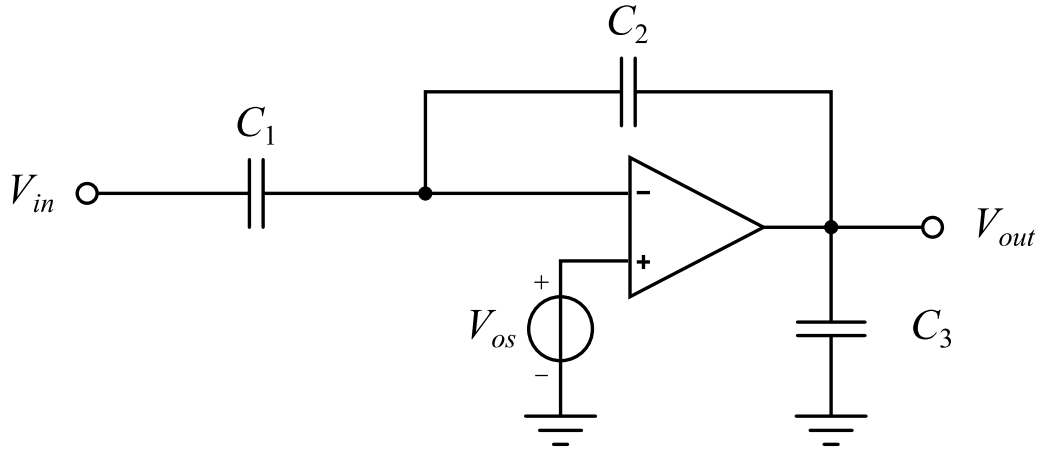
$$\Delta V_{out} = \frac{\Delta Q_2}{C_2} = -\frac{C_1}{C_2} \cdot V_{in}$$

offset charge is not transferred into C_2

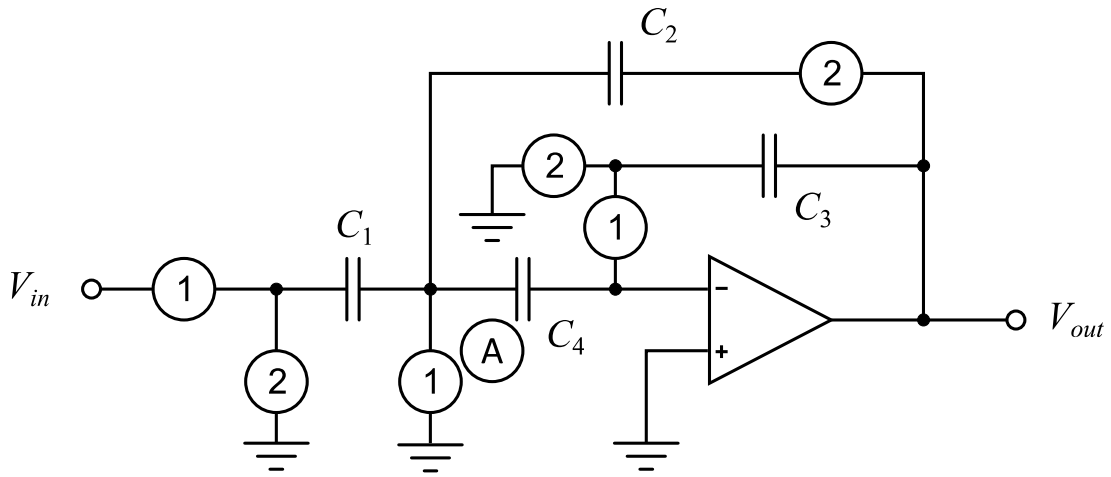
Phase ϕ_1:



Phase ϕ_2:



Offset free SC integrator

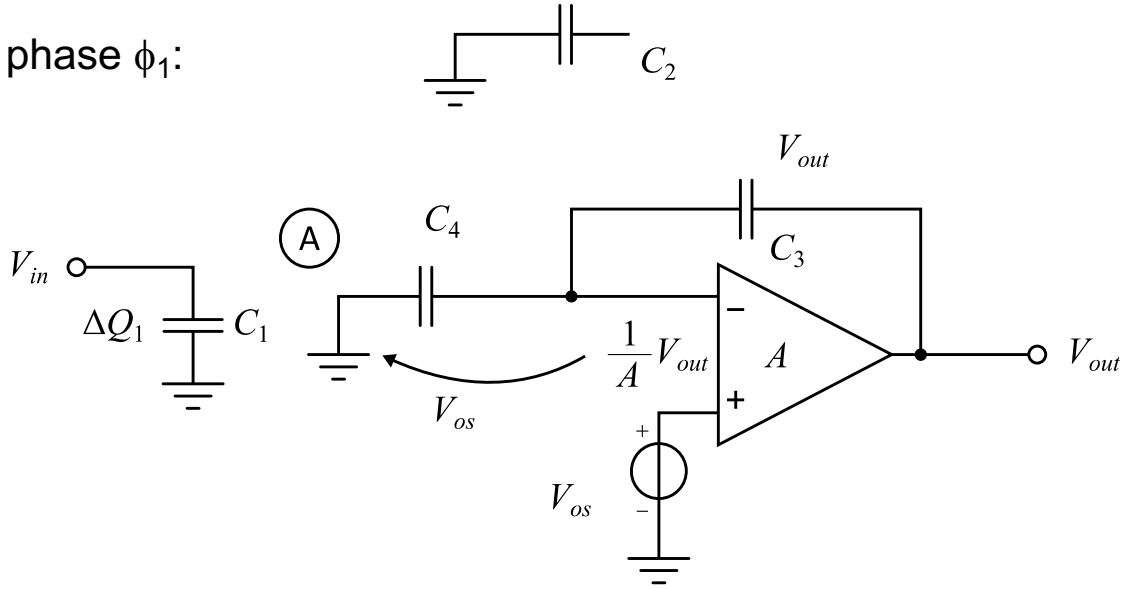


Node Ⓐ is offset compensated virtual ground.
C1 samples against node Ⓐ ⇒ offset eliminated

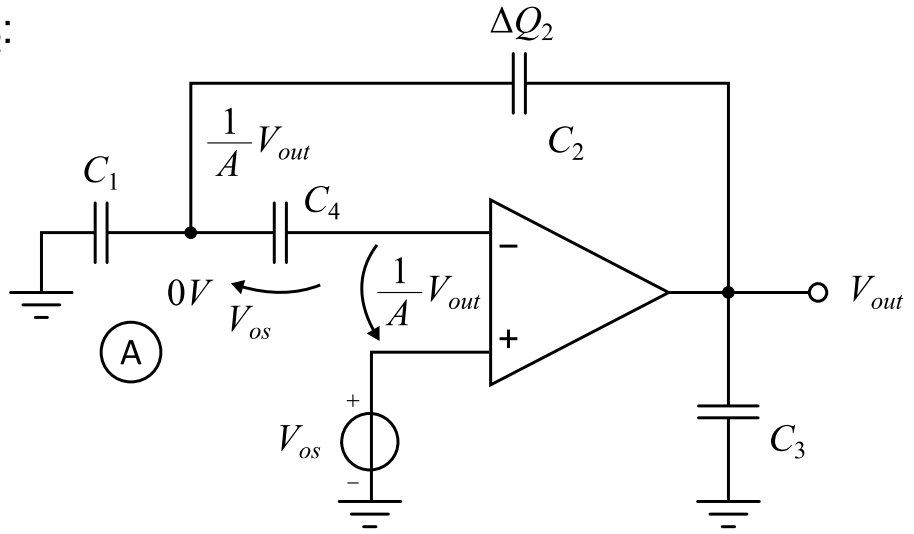
$\Delta Q_2 \equiv \Delta Q_1 = C_1 V_{in}$ exactly!

No charge transfer error!
Also gain error is eliminated!

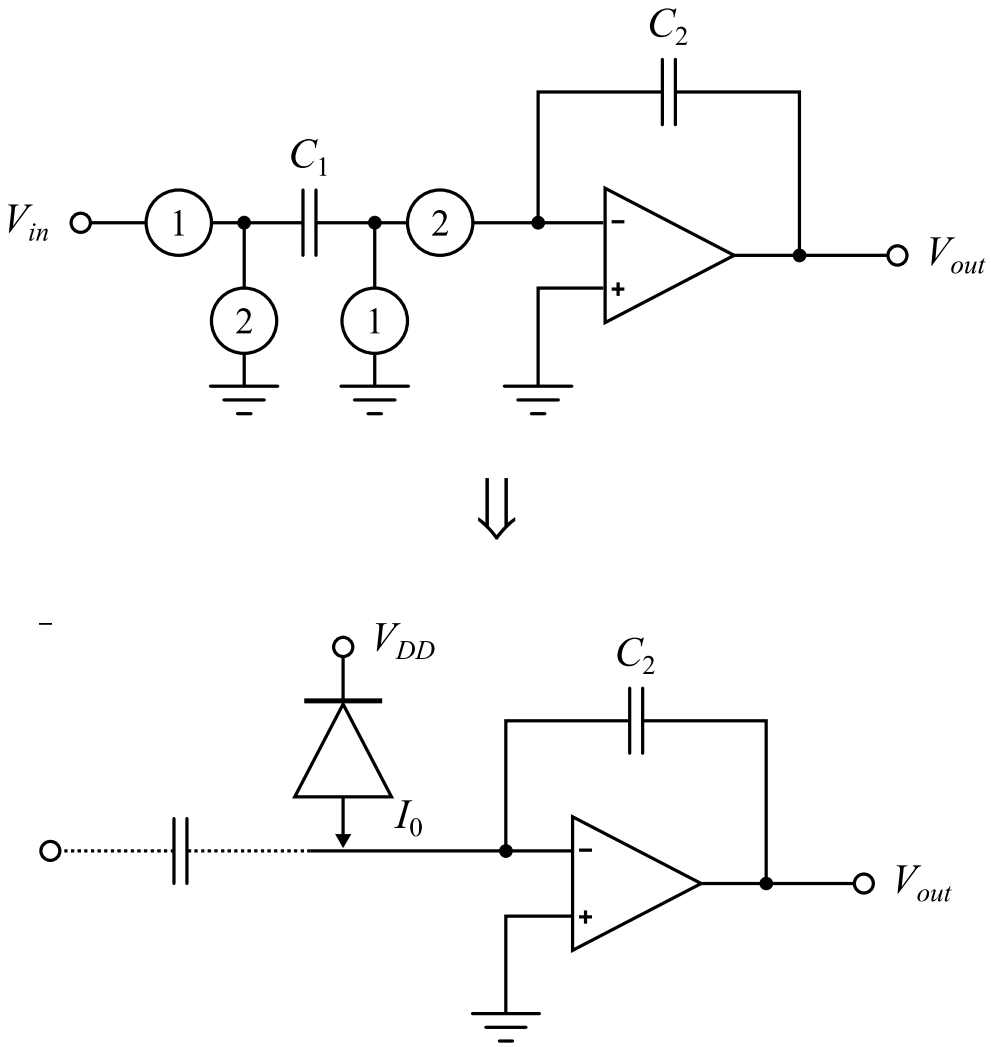
phase ϕ_1:



phase ϕ_2:



Leakage currents of switches



Leakage current I_0 charges C_2

Change of charge in C_2 during one clock-cycle

$$\Delta Q = I_o \cdot T$$

Voltage droop in C_2

$$\Rightarrow \Delta V_{C2} = \frac{\Delta Q}{C_2} = \frac{I_o \cdot T}{C_2} = \frac{I_o}{f_{CLK} C_2}$$

Leakage current causes offset!

Example

$I_o = 1pA$

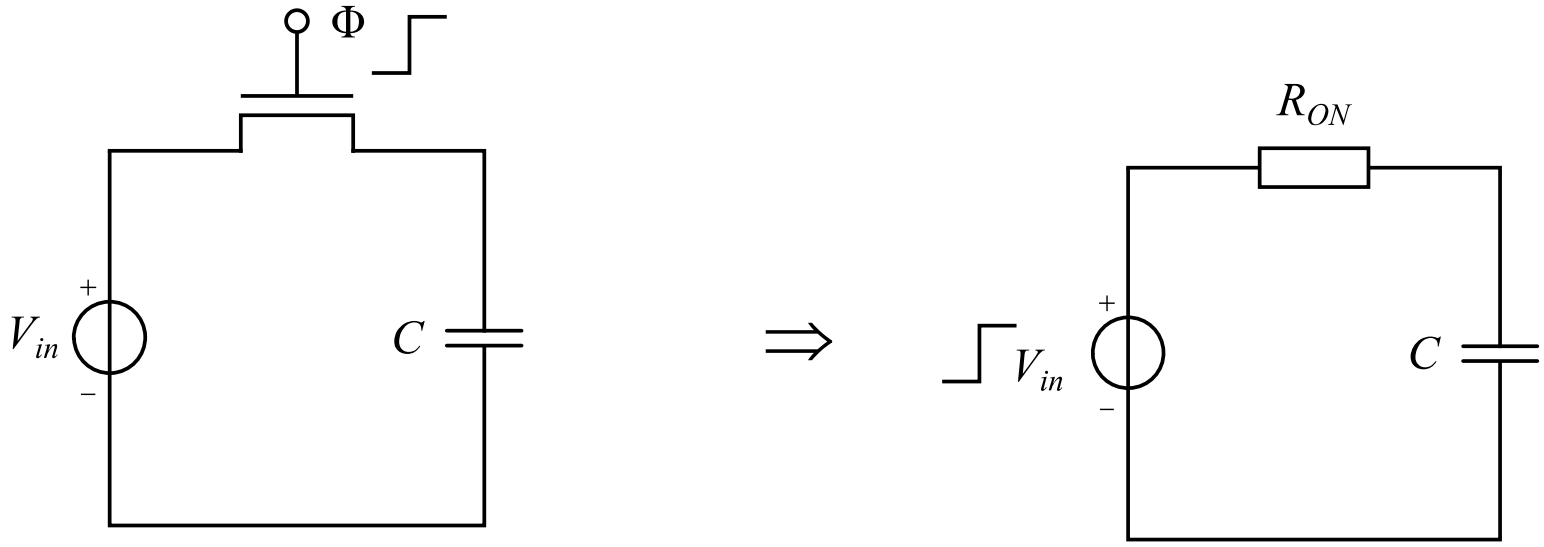
$C_2 = 5pF \quad \Rightarrow V_{OS} = 0{,}5mV$

$f_{CLK} = 1kHz$

I_o doubles every 10˚C rise of temperature!

@100˚C $\Rightarrow V_{OS} = 50mV$!!

Error due to switch on-resistance



Settling during sampling the input

$$V_C = V_{in}\left(1 - e^{-t/R_{ON}C}\right)$$

Sampling time $t = \frac{T}{2}$; $f_{CLK} = \frac{1}{T}$

$$\Rightarrow V_C = V_{in}\left(1 - e^{-T/2R_{ON}C}\right)$$

The error in charge transfer is

$$\Delta V = V_{in} e^{-T/2R_{ON}C}$$

$$\varepsilon = \frac{\Delta V}{V_{in}} = e^{-T/2R_{ON}C}$$

Example:

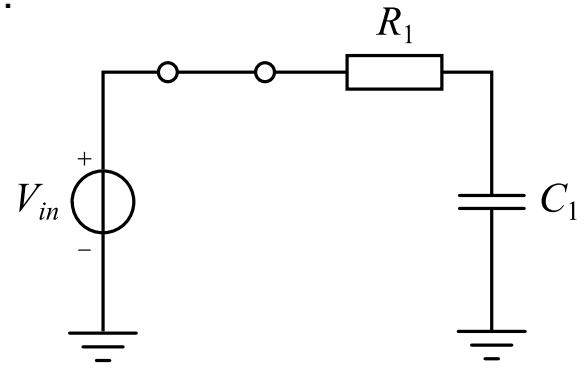
$$\varepsilon < 0{,}1\% \Rightarrow \frac{T}{2RC} < 5$$

$$\Rightarrow \frac{1}{2RC} > 5 \cdot f_{CLK}$$

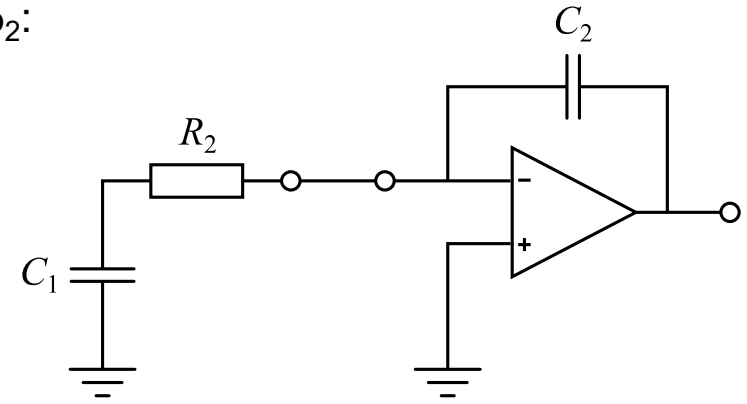
$$\left.\begin{array}{l} f_{CLK} = 1MHz \\ C = 5pF \end{array}\right\} \Rightarrow R_{ON} < 40k\Omega$$

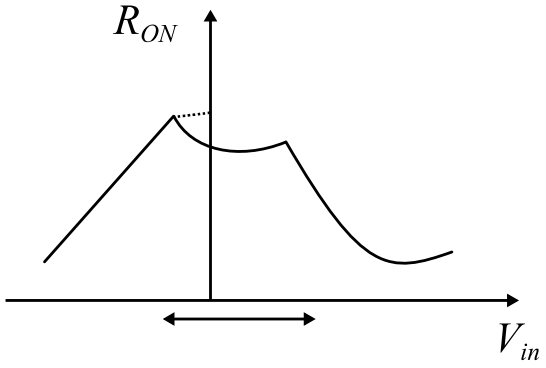
Switch on-resistances in SC integrator

phase ϕ_1:



phase ϕ_2:





Phase ϕ_1:

$$V_1(nT) = V_{in}(nT)\left(1 - e^{-T/2R_1C_1}\right) \qquad T_{ov} = \frac{1}{f_{clk}}$$

Phase ϕ_2:

$$\Delta q(nT + T/2) = C_1 v_1(nT)\left(1 - e^{-T/2R_2C_1}\right)$$

$$\Rightarrow \Delta v_{out} = \Delta q / C_2 = v_{out}(nT + T) - v_{out}(nT)$$

Z-domain transfer function:

$$H(z) = \frac{-\left(1 - e^{-T/2R_1C_1}\right)\left(1 - e^{-T/2R_2C_1}\right)\frac{C_1}{C_2}}{z - 1}$$

$$R_1 = R_2 = R$$

$$\Rightarrow \varepsilon = 1 - \left(1 - e^{-T/2RC_1}\right)^2 \approx 2e^{-T/2RC_1}$$

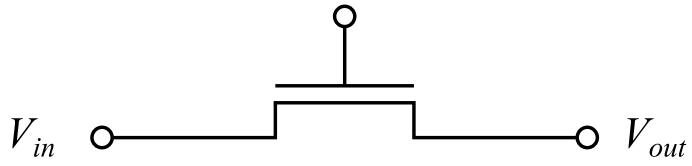
Example:

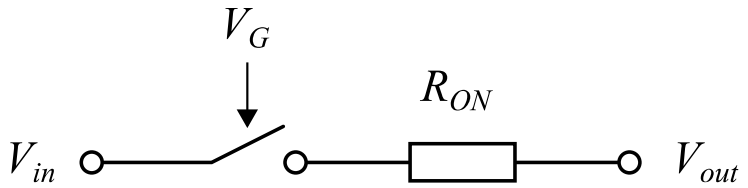
$$\varepsilon \le 10^{-4} \ldots 10^{-3} \Rightarrow \left(\frac{RC_1}{T}\right)^{-1} = \left(\frac{t_R}{T}\right)^{-1} \approx 7 \ldots 10$$

$$C_1 = 5pF \quad f_c = 1MHz$$

$$R_{on} \approx 20k\Omega$$

MOS-switch





1. Switch open, $V_{GS} < V_T$

$$\Rightarrow R_{ON} = \infty$$

2. Switch closed, $V_{GS} > V_T$, V_{DS} small

$\Rightarrow$ transistor in linear region

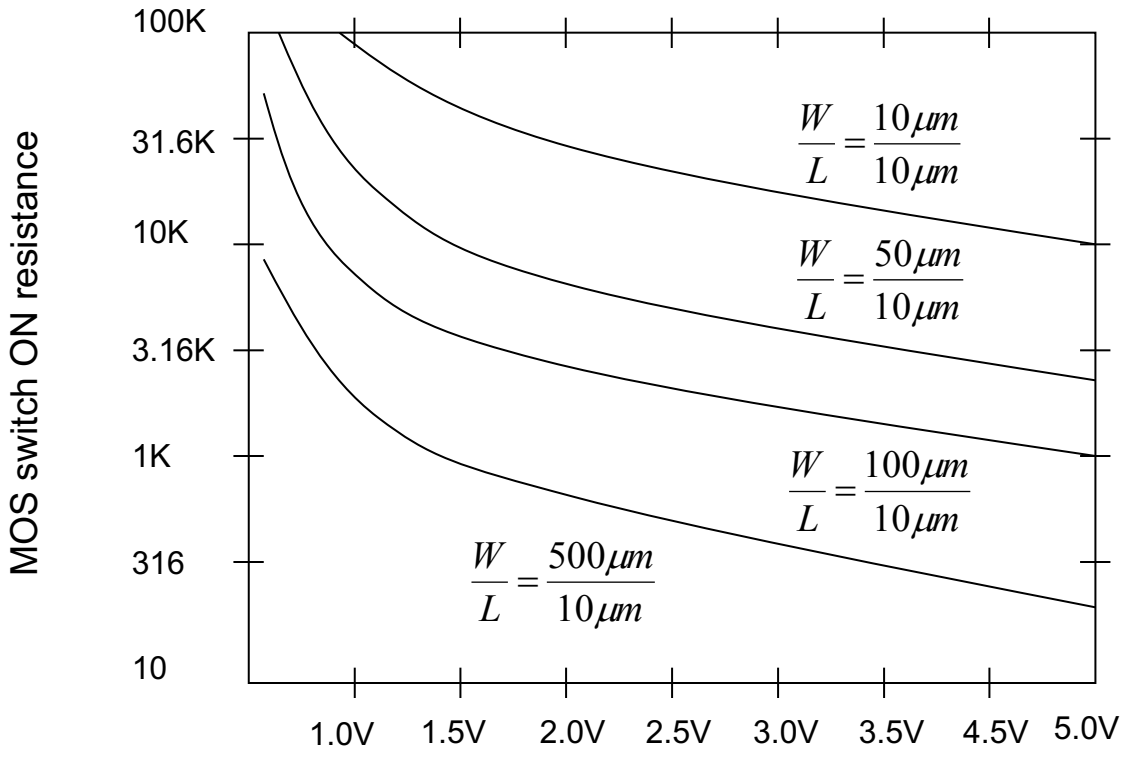
$$\frac{1}{R_{ON}} = \frac{\partial I_D}{\partial I_{DS}} = \mu C_{OX} \frac{w}{L}\left(V_{GS} - V_T\right)$$

$$R_{ON} = \frac{1}{\mu C_{OX} \frac{w}{L}\left(V_{GS} - V_T\right)} \qquad 200\Omega \ldots 200k\Omega$$

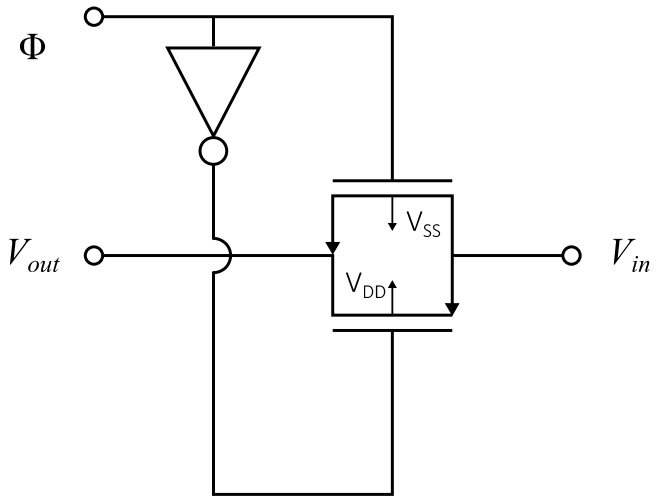
- gate impedance infinite
- gate-capacitance causes clock-feedthrough
- C_{par} to substrate
- V_{in}, V_{out} limited

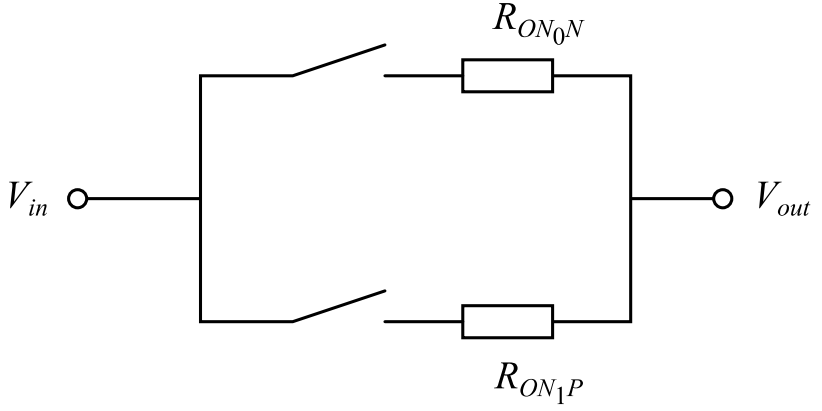
  ($V_{GS} = V_G - V_{in} > V_T$, $V_{DD} - V_{in} > V_T \Rightarrow V_{DD} - V_T > V_{in}$)

MOS-switch ON-resistance



CMOS-switch





Symmetrical design:

$$R_{ON_0N} \approx R_{ON_1P}$$

$$\left|V_{GSN} - V_T\right| = \left|V_{GSP} - V_T\right|$$

$$\left(\frac{w}{L}\right)_P \mu_P = \left(\frac{w}{L}\right)_N \mu_N$$

$$\Rightarrow \frac{\left(\frac{w}{L}\right)_P}{\left(\frac{w}{L}\right)_N} = \frac{\mu_N}{\mu_P} \quad (\sim 2{,}5)$$

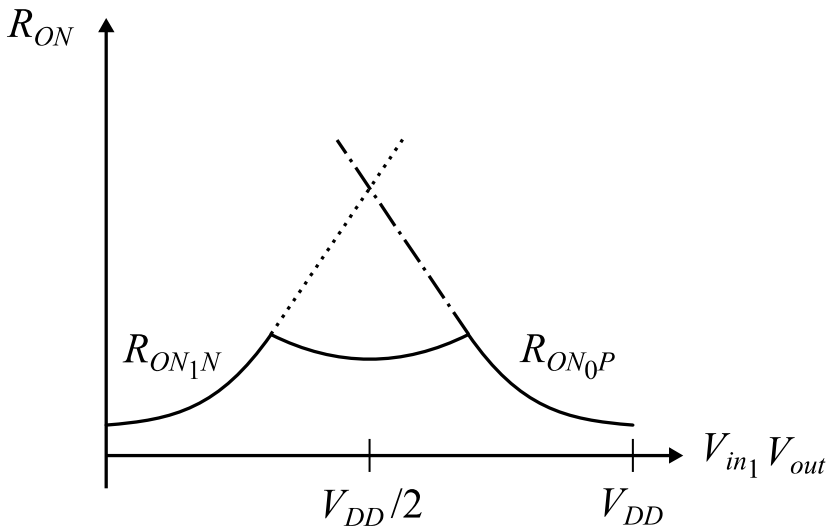
Not limited signal swings
(only by V_{DD}, V_{SS})

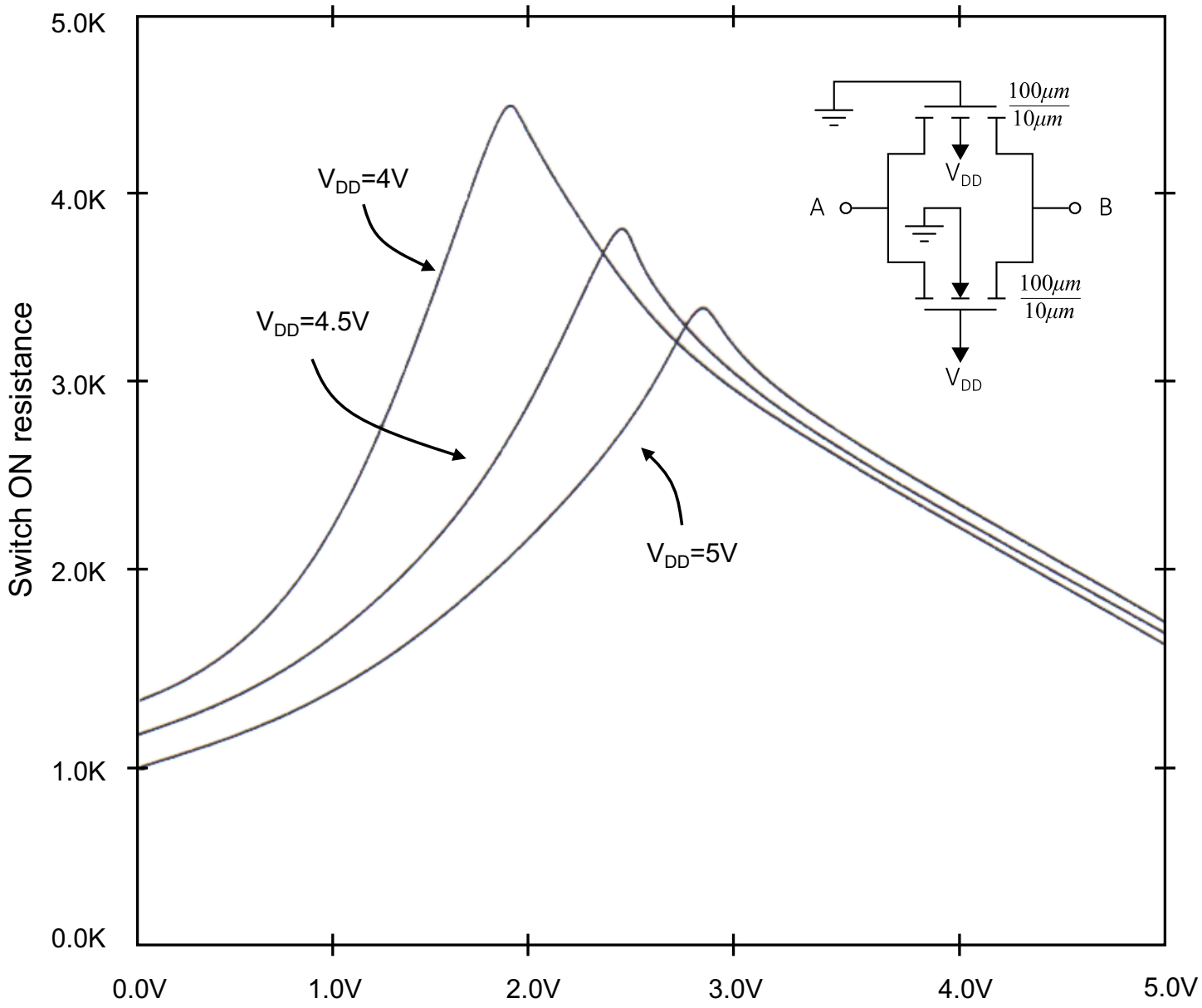
$$\frac{1}{R_{ON}} = \frac{1}{R_{ON_0N}} + \frac{1}{R_{ON_1P}}$$

$$R_{ON} = \frac{R_{ON_0N} \cdot R_{ON_1P}}{R_{ON_1P} + R_{ON_1P}}$$

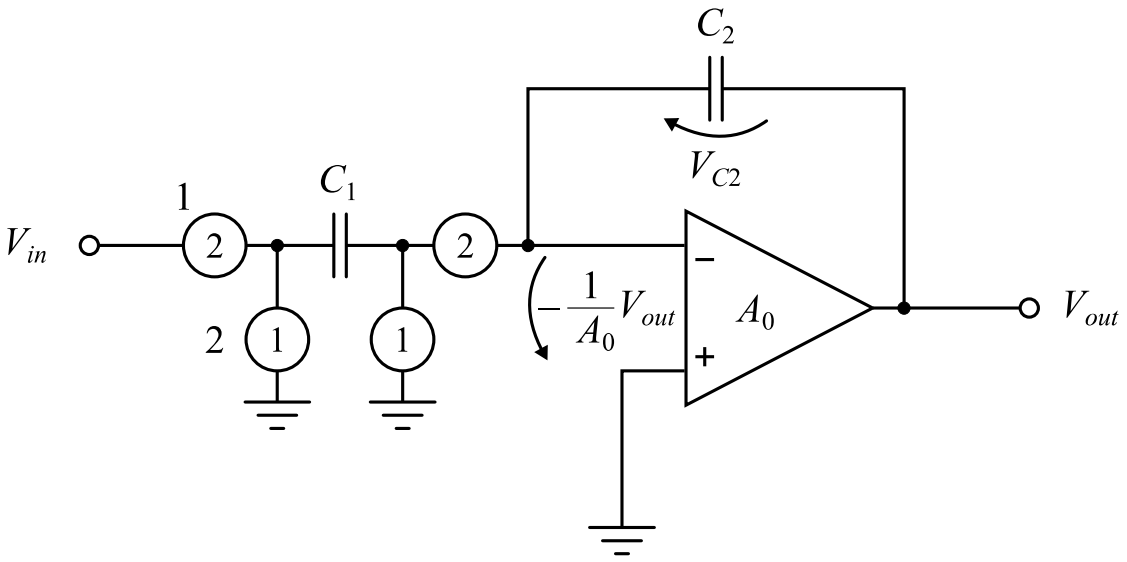
$$V_{in,CM} = V_{out} \sim \frac{V_{DD}}{2}$$

half way between supplies




5.0K
4.0K
3.0K
2.0K
1.0K
0.0K
Switch ON resistance
0.0V
1.0V
2.0V
3.0V
4.0V
5.0V
V_{DD}=4V
V_{DD}=4.5V
V_{DD}=5V
$\frac{100\mu m}{10\mu m}$
V_{DD}
A
B
$\frac{100\mu m}{10\mu m}$
V_{DD}

Effect of amplifier finite gain in SC integrator



Output voltage including finite amplifier gain

$$V_{out}(nT) = V_{C2}(nT) - \frac{1}{A_o}V_{out}(nT)$$

Charge transfer:

$$C_2\left[V_{C2}(nT) - V_{C2}(nT-T)\right] + C_1\left[V_{in}(nT) + \frac{1}{A_o}V_{out}(nT)\right] = 0$$

Apply z-transformation:

$$V_{out}(z) = V_{C2}(z) - \frac{1}{A_o}V_{out}(z)$$

$$C_2\left[V_{C2}(z) - z^{-1}V_{C2}(z)\right] + C_1\left[V_{in}(z) + \frac{1}{A_o}V_{out}(z)\right] = 0$$

Transfer function in z-domain

$$H(z) = \frac{V_{out}(z)}{V_{in}(z)} = \frac{-(C_1/C_2)\left[1+(1+C_1/C_2)/A_o\right]^{-1}z}{z-(1+1/A_o)/\left[1+(1+C_1/C_2)/A_o\right]}$$

when $A_o \Rightarrow \infty \Rightarrow$ we obtain ideal integrator in z - domain i.e.

$$H_i(z) = \frac{-(C_1/C_2)z}{z-1}$$

Finite amplifier gain A_0 causes gain and phase error

Insert $z = e^{j\omega t}$ into $H(z)$

$$H\left(e^{j\omega t}\right) = \underbrace{\frac{-\left(C_1/C_2\right)e^{j\omega t/2}}{j2\sin\left(\omega t/2\right)}}_{H_i\left(e^{j\omega t}\right)} \cdot \frac{1}{1+\left(1/A_o\right)\left(1+C_1/C_2\right)-j\left(C_1/C_2\right)/2A_o\tan\left(\omega t/2\right)}$$

ideal z-domain integrator error-term

$$H\left(e^{j\omega t}\right) = H_i\left(e^{j\omega t}\right)\cdot\frac{1}{1-m(\omega)-j\theta(\omega)}$$

$m(\omega)$ = magnitude error

$\theta(\omega)$ = phase error

$$m(\omega) = -\frac{1}{A_0}\left(1+\frac{C_1}{C_2}\right)$$

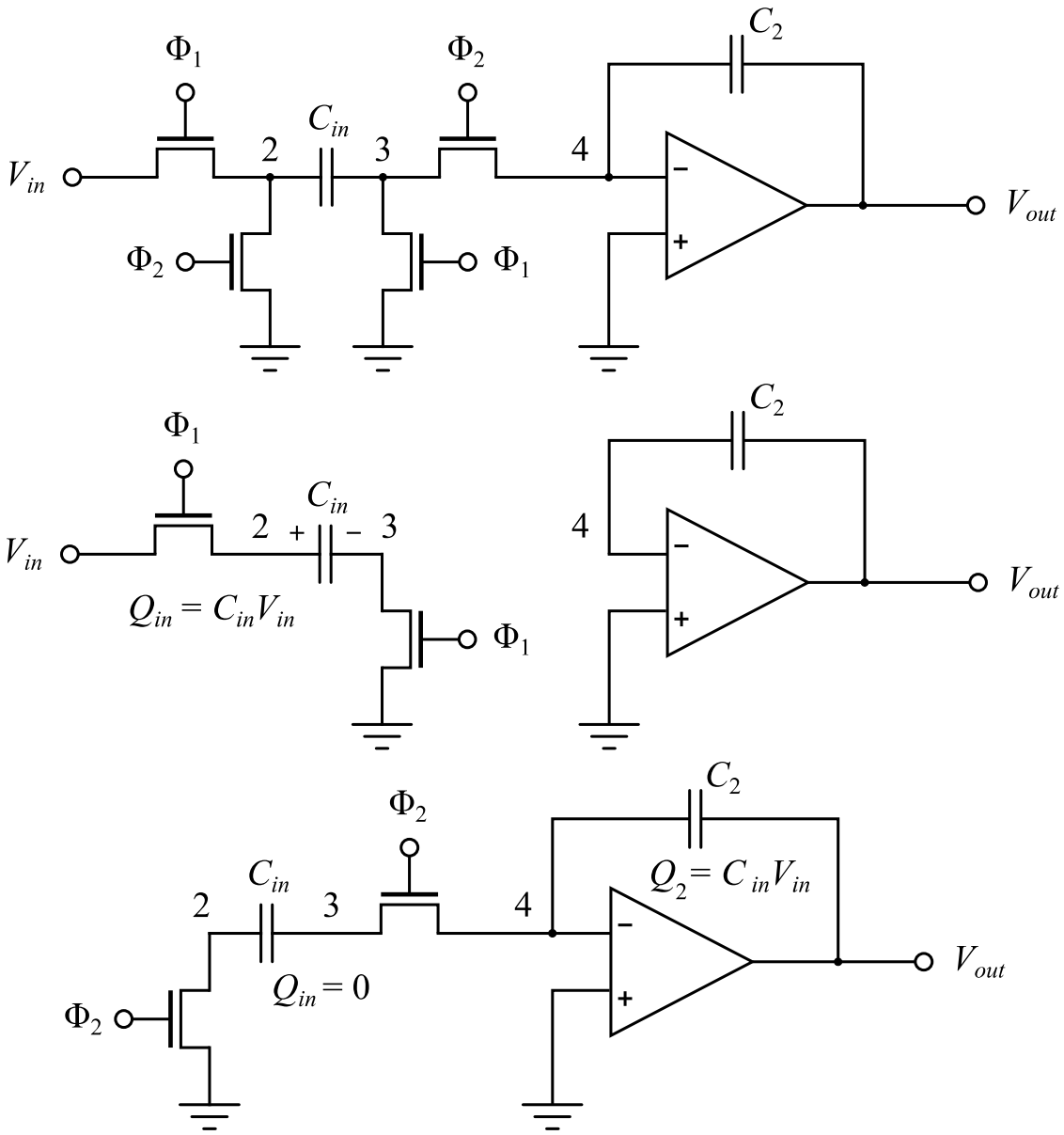
$$\theta(\omega) = \frac{C_1/C_2}{2A_0\tan\left(\omega T/2\right)} \approx \frac{C_1/C_2}{A_0\omega T}$$

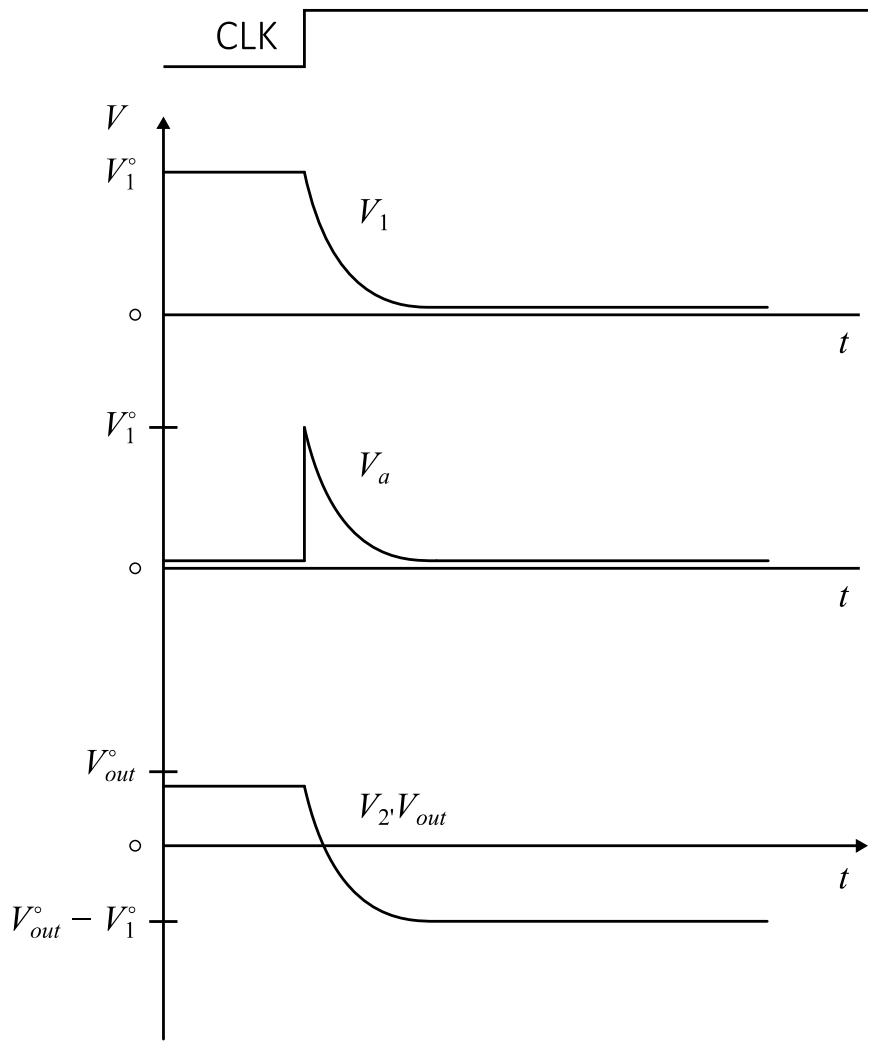
$$m(\omega), \theta(\omega)\,\alpha\,\frac{1}{A_0}$$

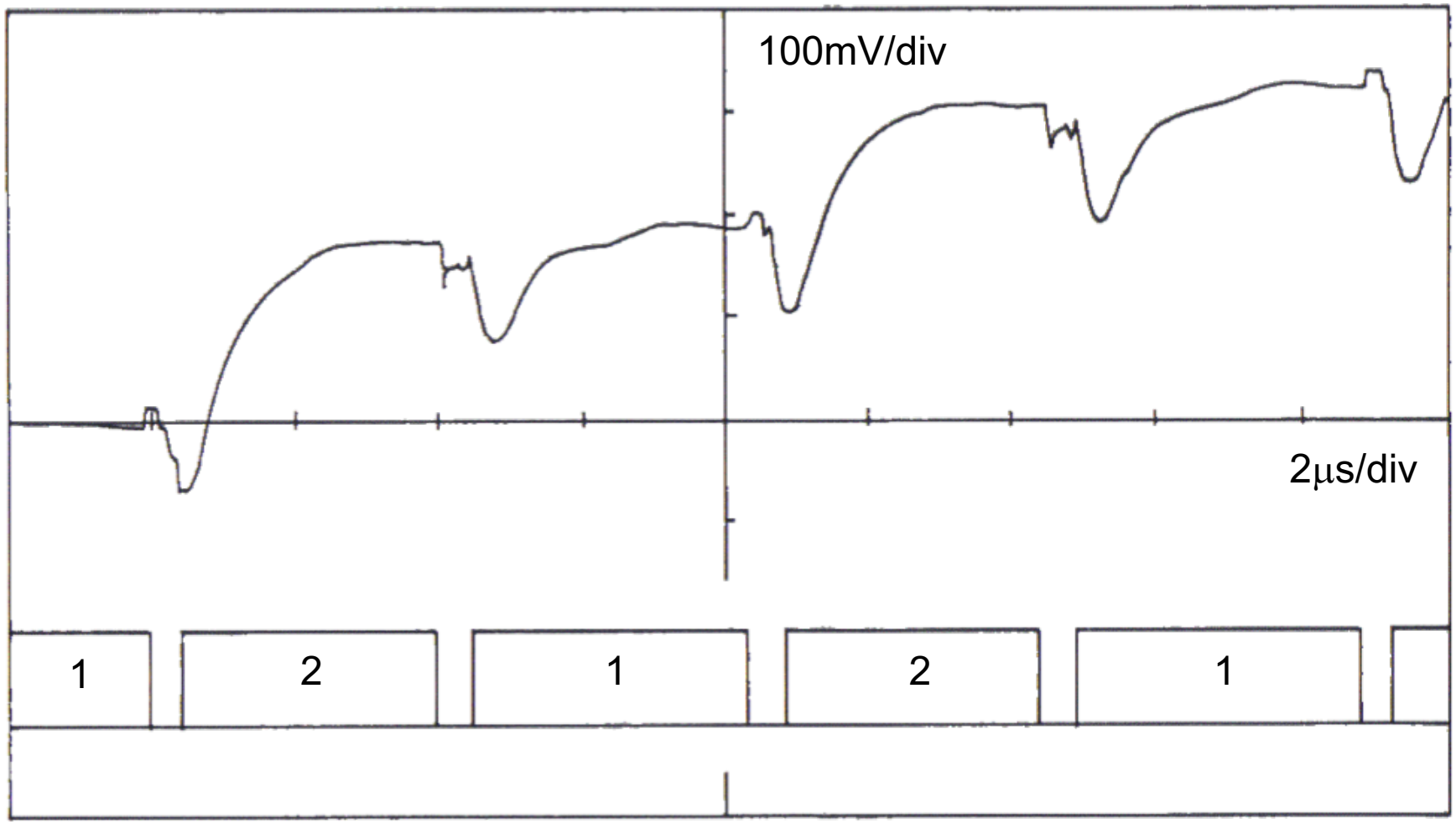
$$\left(\frac{C_1}{C_2}\right) \rightarrow \left(1+m(\omega)\right)\frac{C_1}{C_2}\,\alpha\left(1+\frac{1}{A_0}\right)\frac{C_1}{C_2}$$

$$\Rightarrow \frac{\Delta\dfrac{C_1}{C_2}}{C_1/C_2} = \frac{1}{A_0}$$

Charge transfer in SC integrator

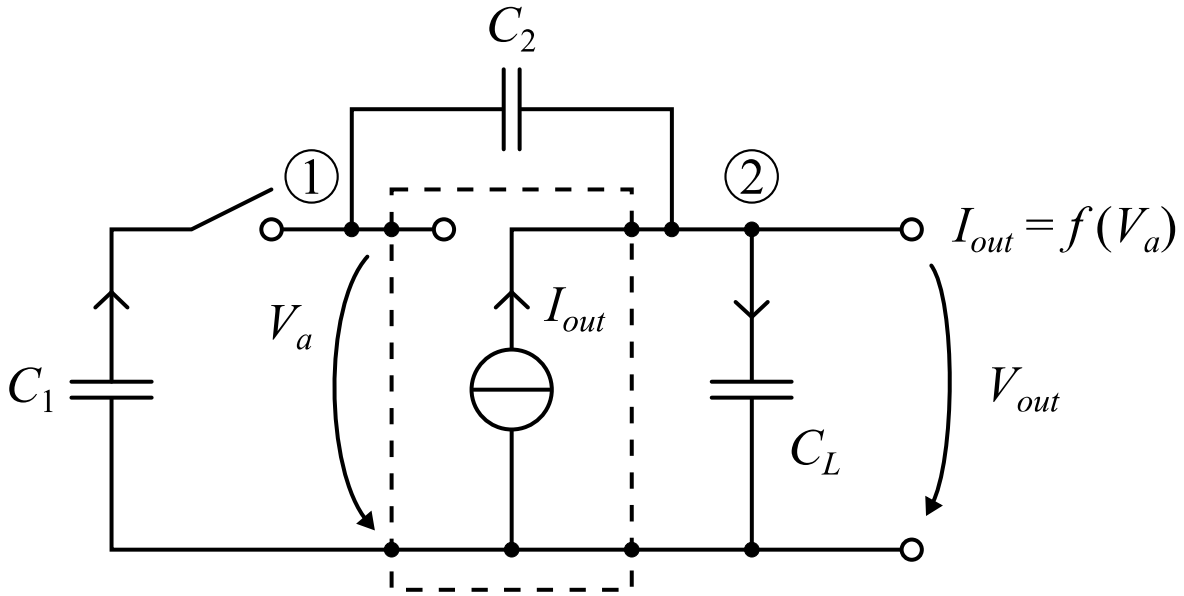






Charge transfer transient of the 4th order elliptical low-pass filter.

Charge transfer transient



The current equations for nodes ① and ② $\quad I(t) = C\dfrac{dV}{dt}$

(1) $\quad C_1 \dfrac{dV_a}{dt} - C_2 \dfrac{d(V_{OUT} - V_a)}{dt} = 0$

(2) $\quad I_{OUT}(t) - C_L \dfrac{dV_{OUT}}{dt} - C_2 \dfrac{d(V_{OUT} - V_a)}{dt} = 0$

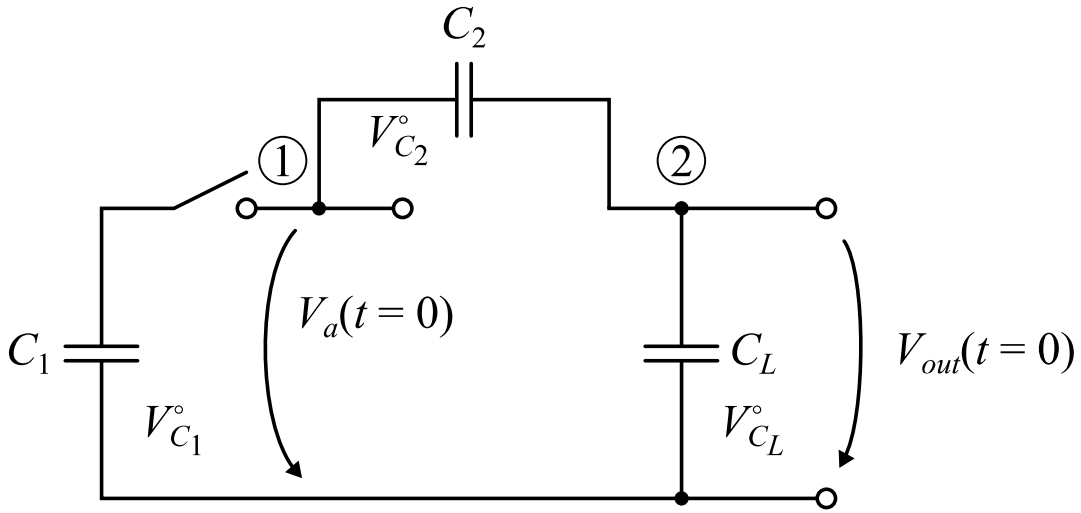
eliminating $\dfrac{dV_{OUT}}{dt} \Rightarrow$ we obtain charge transfer equation

$$\boxed{\frac{C_1C_2 + C_LC_1 + C_LC_2}{C_2} \cdot \frac{dV_a}{dt} + I_{OUT}(t) = 0}$$

$V_{OUT}(t)$ is solved from eq. (1)

$$\boxed{V_{OUT}(t) = V_{OUT}(t=0) + \frac{C_1 + C_2}{C_2}\left[V_a(t) - V_a(t=0)\right]}$$

Calculation of initial voltages $V_a(t=0)$ and $V_{OUT}(t=0)$



Before switching the capacitor voltages are

$$V^{\circ}_{C1}\ , V^{\circ}_{C2}\ \text{and}\ V^{\circ}_{CL}$$

After closing the switch the equilibrian is obtained between the charges of the capacitors

$$V_{C2} + V_a(t=0) = V_{OUT}(t=0)$$

Charge balance at nodes ① and ②

$$\Delta Q_{C1} = -\Delta Q_{C2}$$
$$-\Delta Q_{C2} = \Delta Q_{CL}$$

To obtain this a charge transfer between the capacitors occur

(1) $C_1\left(V^{\circ}_{C1} - V_a(t=0)\right) = C_2 V^{\circ}_{C2} + C_2\left(V_a(t=0) - V_{OUT}(t=0)\right)$

(2) $C_L\left(V^{\circ}_{CL} - V_{OUT}(T=0)\right) = C_2 V^{\circ}_{C2} + C_2\left(V_a(t=0) - V_{OUT}(t=0)\right)$

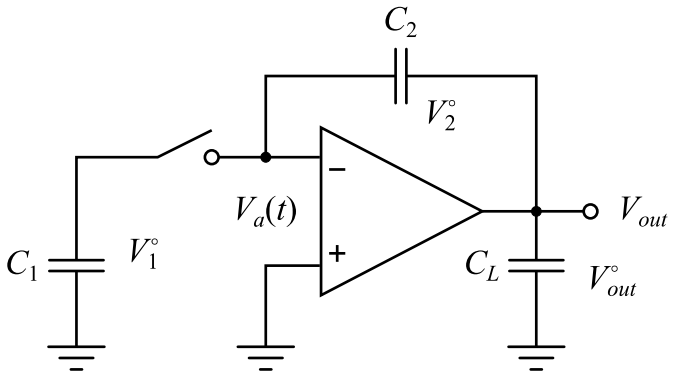
From these we solve the initial conditions

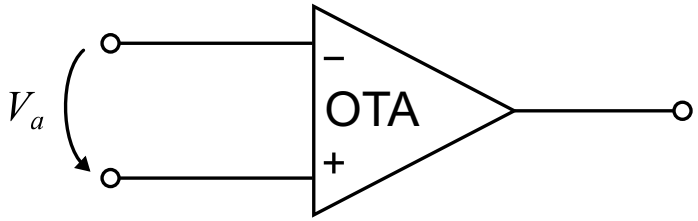
$$V_a(t=0)\ \text{and}\ V_{OUT}(t=0)$$

$$V_a(t=0) = -\frac{C_1C_2 + C_1C_L}{C_1C_L + C_1C_2 + C_2C_L} v^{\circ}_{C1} + \frac{C_2C_L}{C_1C_2 + C_1C_L + C_2C_L}\left(v^{\circ}_{CL} - v^{\circ}_{CL}\right)$$

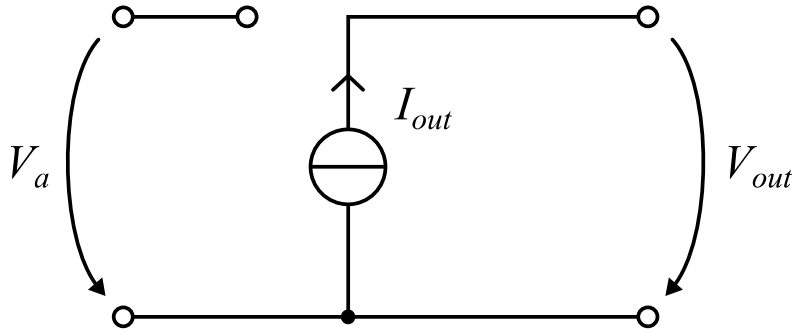
$$V_{out}(t=0) = \frac{C_1C_L + C_2C_L}{C_1C_L + C_1C_2 + C_2C_L} v^{\circ}_{CL} + \frac{C_1C_2}{C_1C_2 + C_1C_L + C_2C_L}\left(v^{\circ}_{C2} - v^{\circ}_{C1}\right)$$

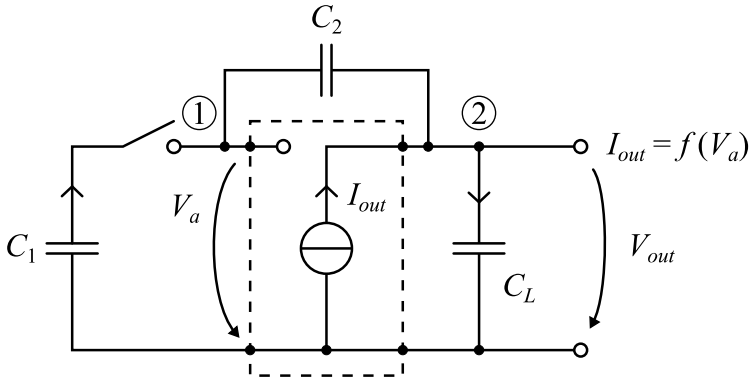
Model of OTA-amplifier (voltage controlled current-source)



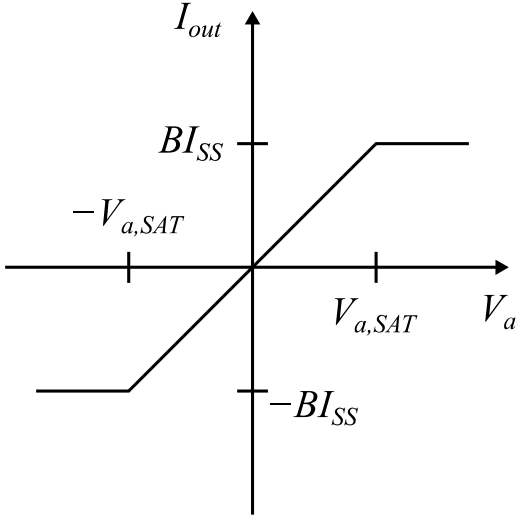


Voltage controlled current-source





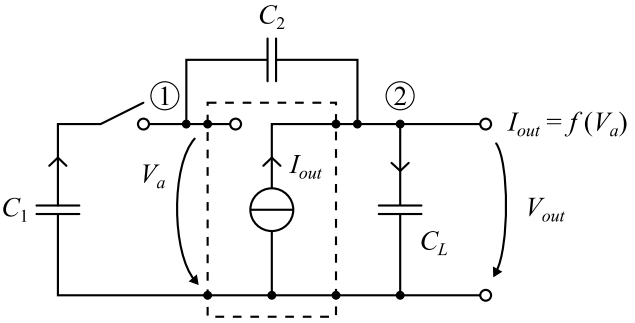
OTA transfercurve



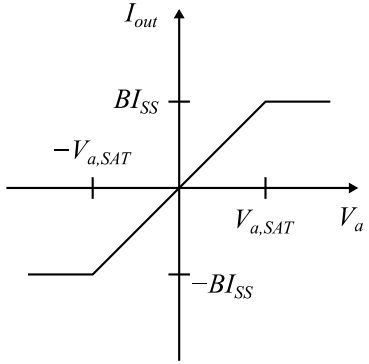
OTA output current:

$$I_{out} = \begin{cases} -BI_{SS}; V_a < V_{a,SAT} \\ g_m V_a; -V_{a,SAT} < V_a < V_{a,SAT} \\ BI_{SS}; V_a > V_{a,SAT} \end{cases}$$

(Depending on V_a regions of operation: linear and slewing)



OTA transfer curve:



OTA output current:

$$I_{out} = \begin{cases} -BI_{SS}; V_a < V_{a,SAT} \\ g_m V_a; -V_{a,SAT} < V_a < V_{a,SAT} \\ BI_{SS}; V_a > V_{a,SAT} \end{cases}$$

I Small-signal settling (linear):

assume $|V_a(t_0)| < V_{a,SAT} \Rightarrow I_{OUT}(t) = g_m V_a(t)$

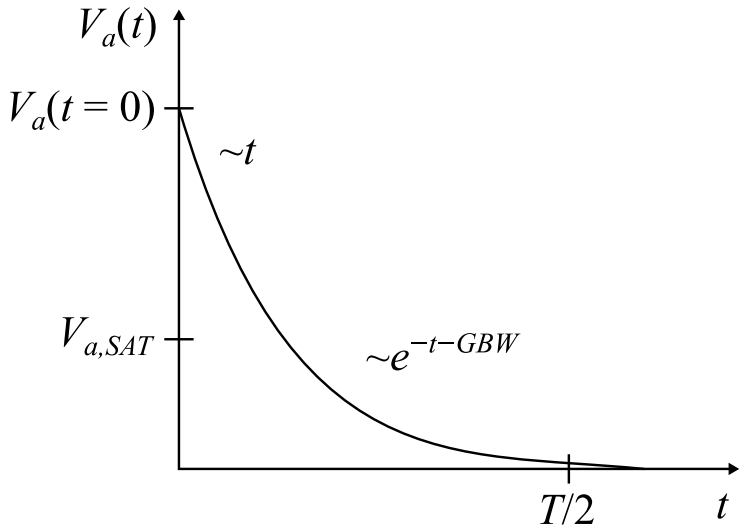
$$\frac{C_1C_2 + C_LC_1 + C_LC_2}{C_2} \cdot \frac{dV_a(t)}{dt} + g_m V_a(t) = 0$$

solving $V_a(t)$:

$$\boxed{V_a(t) = V_a(t=0)\exp\left(-\frac{g_m}{C_{L,eff}} \cdot t\right)} \quad ; C_{L,eff} = \frac{C_1C_2 + C_LC_1 + C_LC_2}{C_2}$$

$$\frac{g_m}{C_{L,eff}} \alpha GBW$$

$$|V_a(t)| = V_a(0)e^{-GBW \cdot t}$$



II Settling with slewing:

assume $|V_a(t_0)| > V_{a,SAT} \Rightarrow I_{OUT}(t) = (\pm) BI_{SS}$

$$\frac{C_1C_2 + C_LC_1 + C_LC_2}{C_2} \cdot \frac{dV_a(t)}{dt} (\pm) BI_{SS} = 0$$

solving $V_a(t)$:

$$\boxed{V_a(t) = V_a(t=0) (\mp) \frac{B \cdot I_{SS}}{C_{L,eff}} \cdot t} \quad ; SR = \frac{B \cdot I_{SS}}{C_{L,eff}}$$

slew-period:

$$|V_a(T_{SR})| = V_{a,SAT} = |V_a(t=0)| - \frac{B \cdot I_{SS}}{C_{L,eff}} \cdot T_{SR}$$

$$\Rightarrow \boxed{T_{SR} = \frac{|V_a(t=0)| - V_{a,SAT}}{B \cdot I_{SS}} \cdot C_{L,eff}}$$

linear settling after slewing

$|V_a(t)| < V_{a,SAT}$ i.e. $t > T_{SR}$

$$V_a(t) = V_{a,SAT} \exp\left(-\frac{g_m}{C_{L,eff}} \cdot (t - T_{SR})\right)$$

Charge transfer error

Relative charge transfer error:

$$\varepsilon = \frac{\Delta Q(t=\infty) - \Delta Q(T)}{\Delta Q(t \to \infty)}$$

$$\Delta Q(t \to \infty) = C_{in} V_{in}$$

I assume $|V_a(t=0)| < V_{a,SAT}$

$$\Delta Q(t \to \infty) - \Delta Q(T) = C_{in} \cdot V_a(T) = C_{in} V_a(t=0) e^{\frac{-g_m}{C_{L,e}} \cdot T}$$

$\approx V_{in}$

Error with small signal settling

$$\Rightarrow \left[\varepsilon = \frac{C_{in} V_{in}}{C_{in} V_{in}} \cdot e^{\frac{-g_m}{C_{L,e}} \cdot T} = e^{\frac{-g_m}{C_{L,e}} \cdot T} \right] \quad (\not\propto V_{in}) \qquad T = \frac{1}{2 f_{CLK}}$$

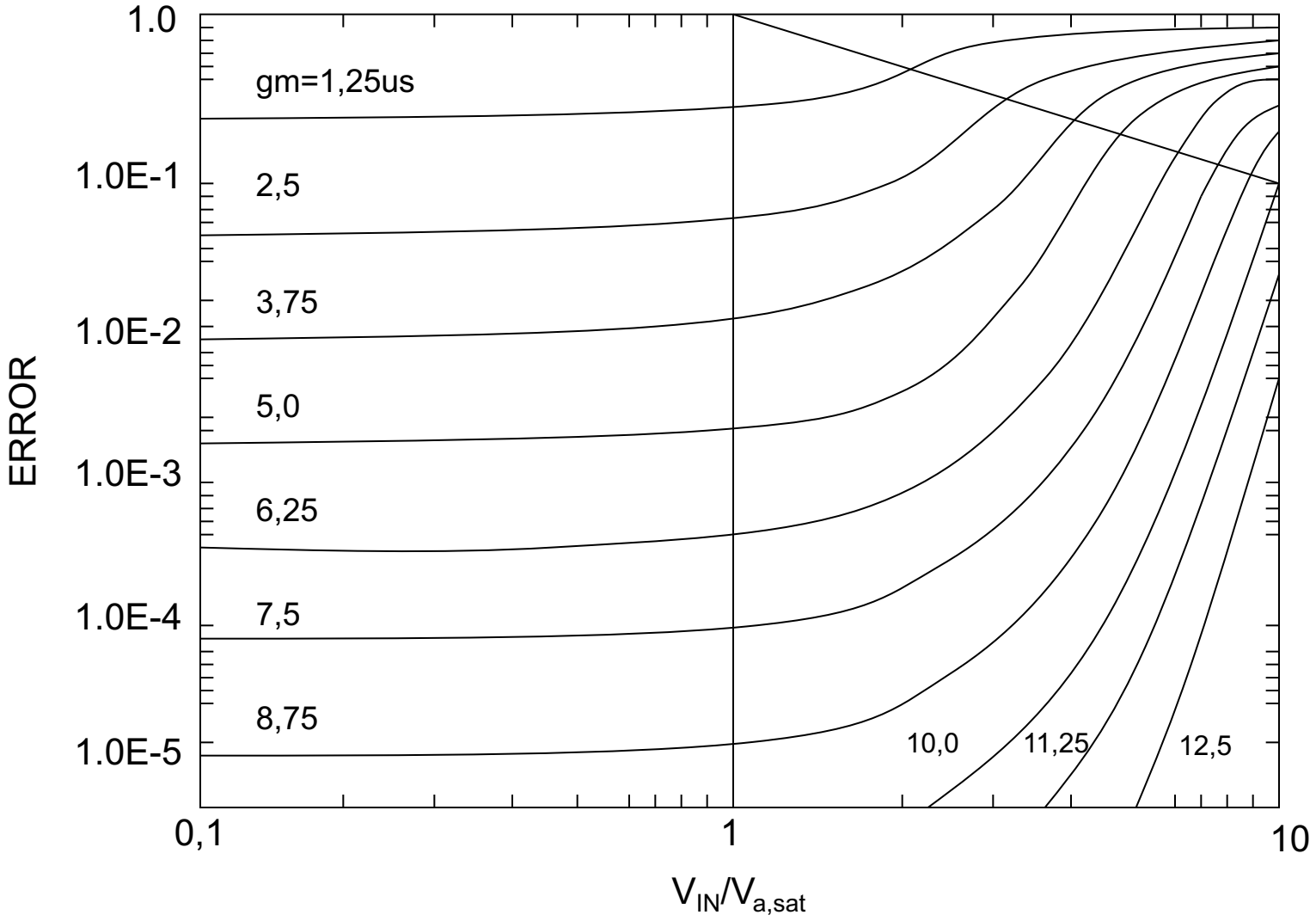
$\Rightarrow$ Only gain error i.e. linear settling-mode!

II error with slewing

assume $|V_a(t=0)| > V_{a,SAT}$

$$\Rightarrow \varepsilon = \frac{C_{in} V_{a,SAT}}{C_{in} V_{in}} \cdot e^{\frac{-g_m}{C_{L,e}} \cdot (T - T_{SR})}$$

$T_{SR} = f(V_{in}) \Rightarrow$ Slewing causes non-linearity!



Charge transfer error with the conventional OTA.

SC integrator transfer function including linear charge transfer error

$$\Delta Q_{C2} = C_1 v_{in}(nT)\left(1 - e^{-\frac{g_m}{C_{L,e}} \cdot T/2}\right) \qquad ; f_{CLK} = \frac{1}{T}$$

$$\Rightarrow \Delta V_{OUT} = \frac{\Delta Q_{C2}}{C_2} = v_{OUT}(nT + T) - v_{OUT}(nT)$$

$$\frac{C_1}{C_2} v_{in}(nT)\left(1 - e^{-\frac{g_m}{C_{L,e}} \cdot T/2}\right) = v_{OUT}(nT + T) - v_{OUT}(nT)$$

Perform z-transformation

$$\frac{C_1}{C_2} v_{in}(z)\left(1 - e^{-\frac{g_m}{C_{L,e}} \cdot T/2}\right) = v_{OUT}(z) \cdot z - v_{OUT}(z)$$

$$\Rightarrow H(z) = \frac{v_{OUT}(z)}{v_{in}(z)} = \frac{C_1}{C_2} \frac{\left(1 - e^{-\frac{g_m}{C_{L,e}} \cdot T/2}\right)}{z - 1}$$

Linear error causes only gain error!
Slewing causes also phase error!!

Non-ideal amplifiers in biquad

Magnitude error m(ω) causes only capacitor ratio error in the integrators.

Ideal integrator:

$$H(s)=\frac{-1/c}{s}$$

Non-ideal integrator:

$$H(s)=\frac{-(1+m)/c}{s+\delta i}$$

In the SC integrator:

$$H_{SC}(s)=\frac{-(1+m)\frac{C_1}{TC_2}}{s+\delta i}=\frac{-\frac{1}{T}\cdot\left(\frac{C_1}{C_2}\right)'}{s+\delta i}$$

Thus magnitude error causes the shift of the pole and cut-off frequency, which can be compensated by predistorting the capacitor ratio

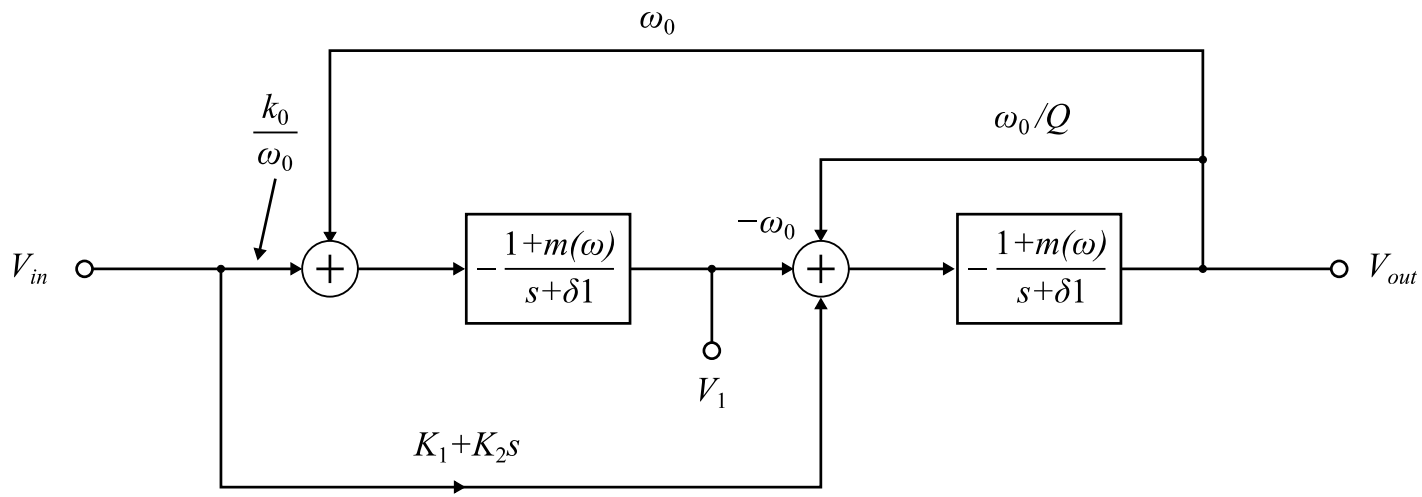
$$\frac{C_1}{C_2}\rightarrow(1+m)\frac{C_1}{C_2}$$

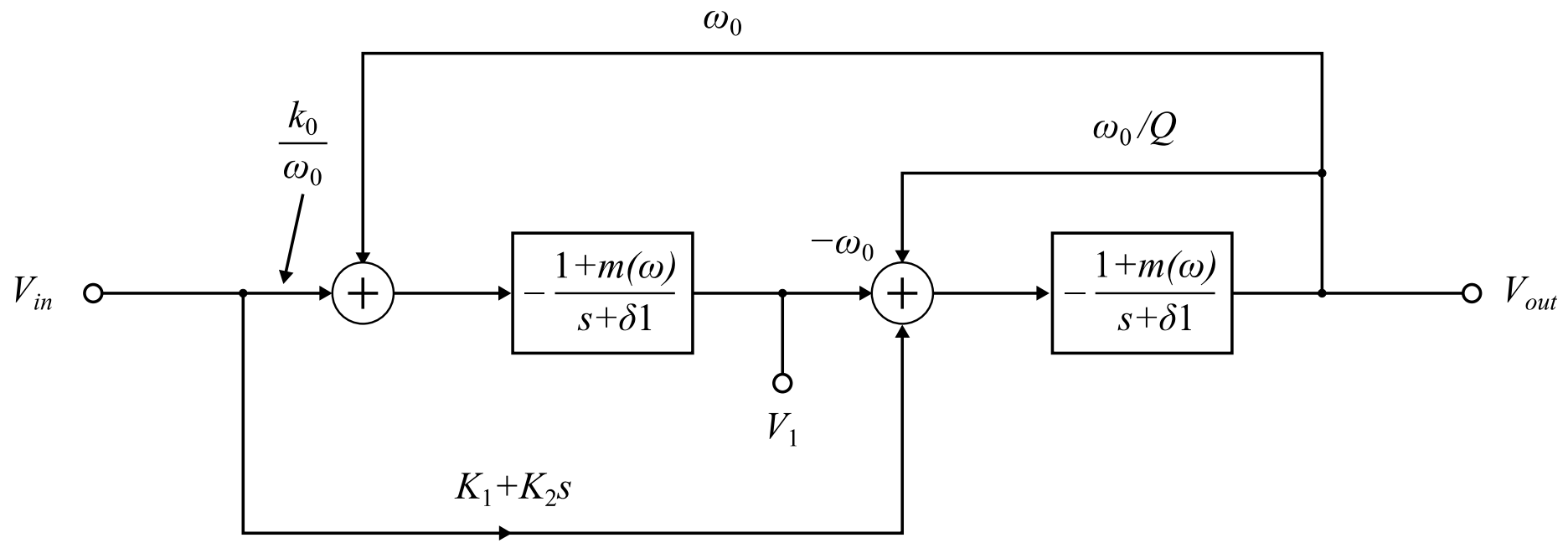
For amplifier finite gain:

$$m\sim\frac{1}{A_0}\Rightarrow\omega_p'\simeq\left(1-\frac{1}{A_0}\right)\omega_p$$

$$A=60dB=1000$$

$$\Rightarrow\frac{\Delta\omega_p}{\omega_p}\approx 0{,}1\%$$




ω_0
$\frac{k_0}{\omega_0}$
ω_0/Q
V_{in}
$-\frac{1+m(\omega)}{s+\delta 1}$
$-\omega_0$
$-\frac{1+m(\omega)}{s+\delta 1}$
V_{out}
V_1
$K_1+K_2 s$

Phase error due to amplifier finite gain (from integrator analysis):

$$\text{phase error } \theta(\omega): \qquad H(S) \cong -\frac{\frac{C_1}{C_2 T}}{S + \frac{C_1}{C_2 A_o T}}$$

integrator is lossy and has a pole

$$\delta i = \frac{C_1 / C_2}{A_o T}$$

To analyse the biquad's performance we insert the lossy integrator into the SFG

$$\frac{1}{S} \rightarrow \frac{1}{S + \delta_i}$$

Now the state equations are

$$(1) \qquad V_1(S) = -\frac{1}{S + \delta_{i1}} \left[\omega_o V_{OUT}(S) + \frac{K_o}{\omega_o} V_{in} \right]$$

$$(2) \qquad V_{OUT}(S) = -\frac{1}{S + \delta_{i2}} \left[(K_1 + K_2 S) V_{in} + \frac{\omega_o}{Q} V_{OUT}(S) - \omega_o V_1(S) \right]$$

From these we may solve the transfer function $\frac{V_{OUT}}{V_{in}}$ with the lossy integrations

The poles are given by the denomitors, which is

$$S_p^2 + \left(\frac{\omega_o}{Q} + \delta_{i1} + \delta_{i2} \right) S_p + \left(\omega_o^2 + \frac{\omega_o \delta_{i1}}{Q} + \delta_{i1} \delta_{i2} \right) = 0$$

with the ideal amplifiers :

$$S^2 + \frac{\omega_o}{Q} S + \omega_o^2 = 0$$

Thus the phase error distorts the pole Q

$$\frac{\omega_o}{Q'} \sim \frac{\omega_o}{Q} + \delta_{i1} + \delta_{i2}$$

with ideal integrator $\omega_o = \frac{C_1}{TC_2}$

$$\Rightarrow \frac{\delta_{i1}}{\omega_o} = \frac{1}{A_o}$$

dividing with

$$\frac{1}{Q'} \sim \frac{1}{Q} + \frac{\delta_{i1}}{\omega_o} + \frac{\delta_{i2}}{\omega_o}$$

$$\boxed{\frac{1}{Q'} \sim \frac{1}{Q} + \frac{2}{A_o}}$$

Example : $\left.\begin{matrix} Q = 15 \\ A = 1000 \end{matrix}\right\} \Rightarrow Q' = 14.56$

Effect on the pass - band gain at center frequency

$$S \cong j\omega_o \qquad S^2 \simeq \omega_o^2$$

the denominator is given by

$$S^2 + \left(\frac{\omega_o}{Q}\right)S + \omega_o^2 \approx \frac{\omega_o}{Q} \cdot S \qquad H(S \approx j\omega_o)\alpha \frac{1}{\frac{\omega_o \cdot S}{Q}}$$

At center frequency the gain depends on the Q - factor

$$H(S \sim j\omega_o)\alpha \frac{1}{Q}$$

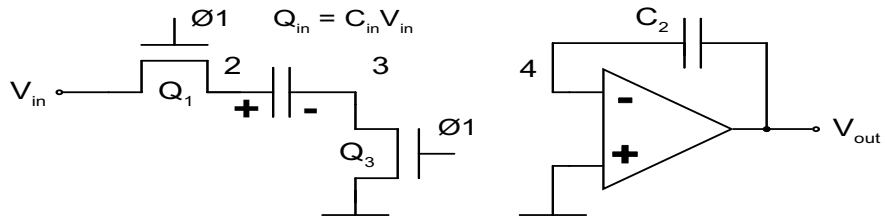
The error in Q - factor causes errors in the gain

$$\Rightarrow \varepsilon = \frac{\left|H'(S = j\omega_o)\right|}{\left|H(S = j\omega_o)\right|} \approx \frac{Q}{Q'}$$

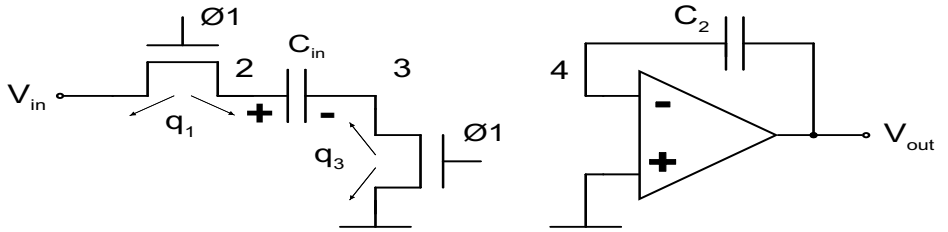
$$\Rightarrow \Delta\alpha[dB] = 20\log\left(\frac{Q}{Q'}\right) = 20\log\left(1 + 2\frac{Q}{A_o}\right)$$

Example : $\left.\begin{array}{l} Q = 15 \\ A = 1000 \end{array}\right\} \Rightarrow \Delta\alpha = 0{,}26dB$

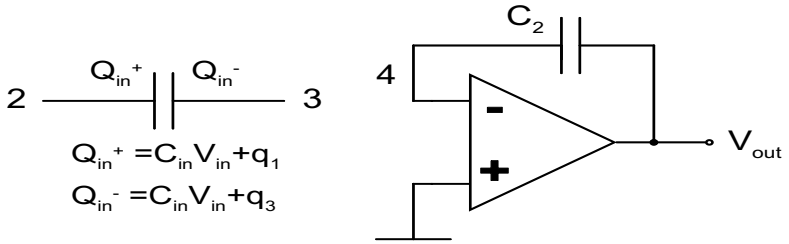
Release of switch transistor channel charge in SC integrator:



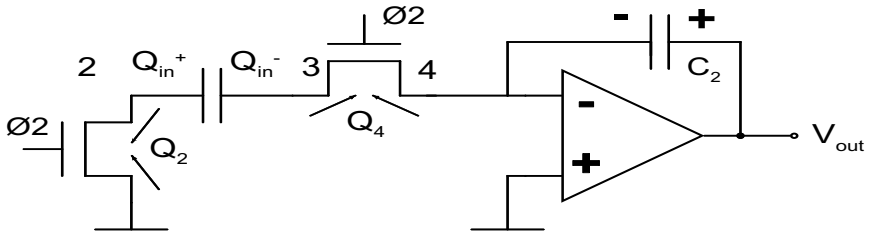
a) holding phase



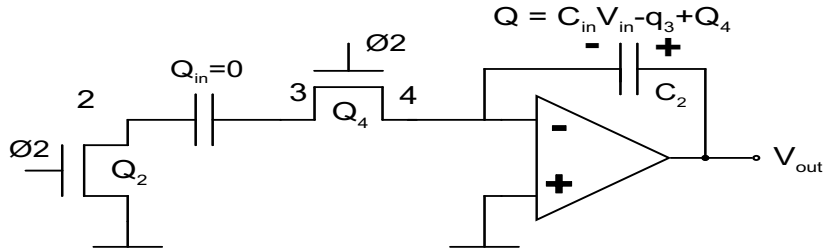
b) closer of SW1 and SW3



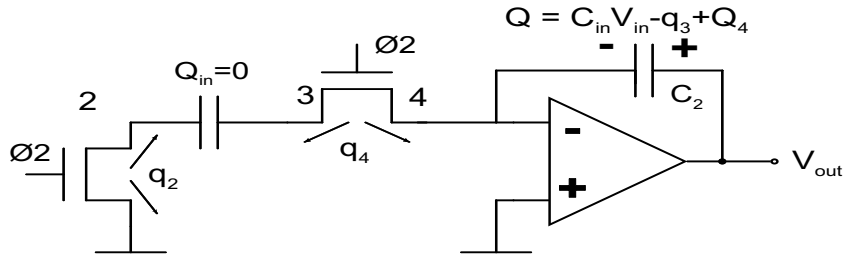
c) non-overlap period between holding and integrating phases



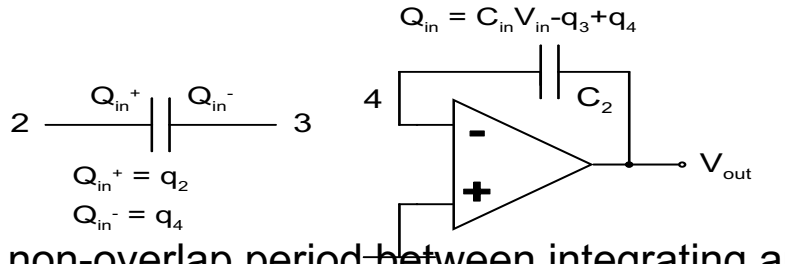
d) opening of SW2 and SW4



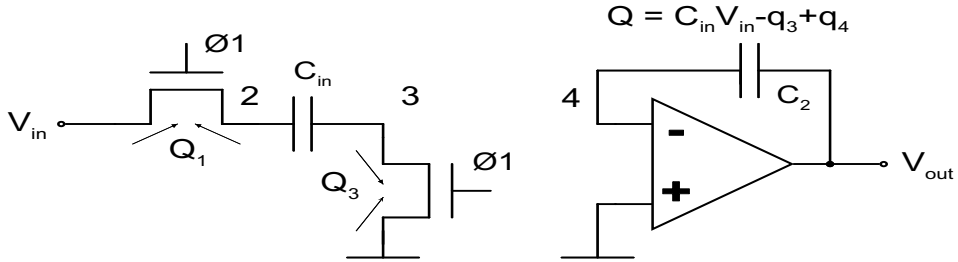
e) integrating phase



f) closer of SW2 and SW4

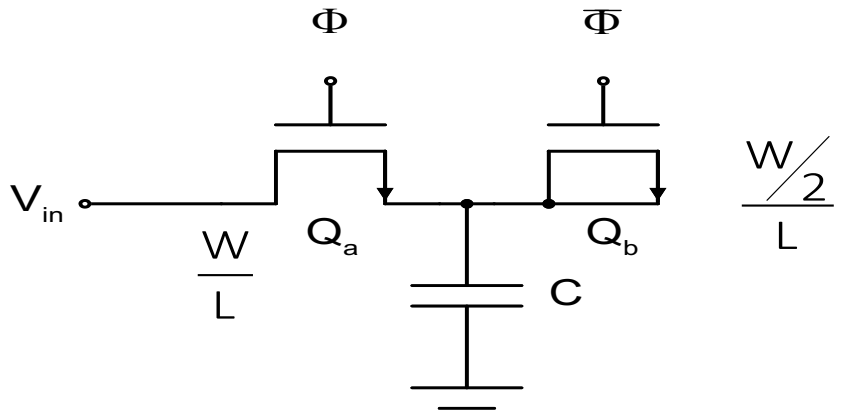


g) non-overlap period between integrating and holding phases

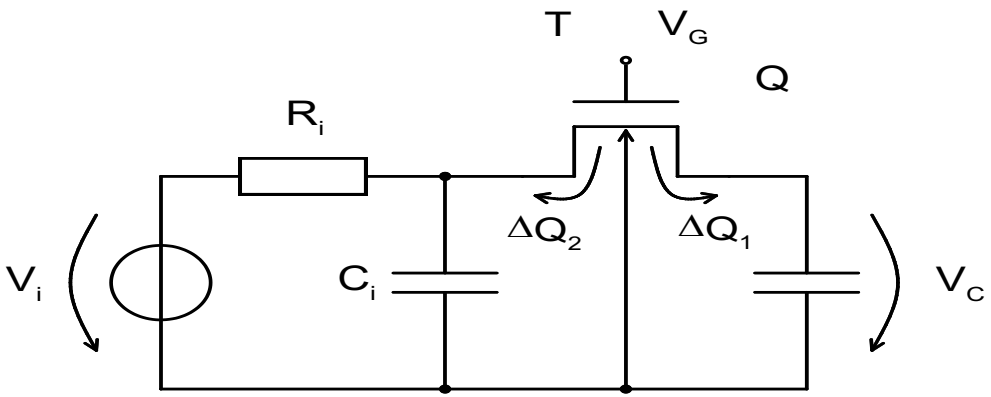


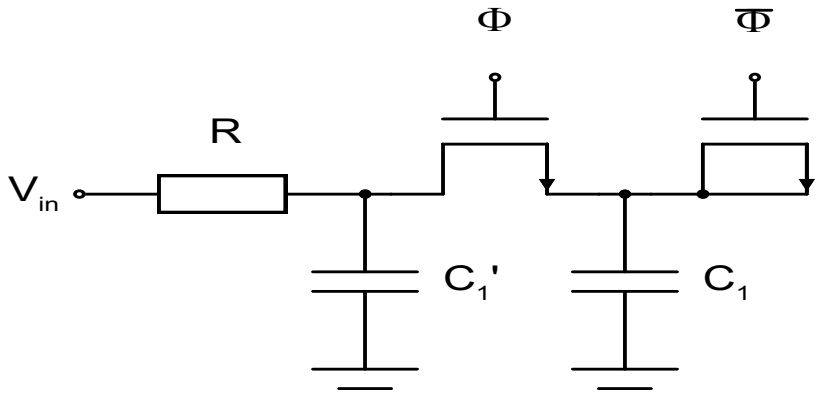
d) opening of SW3 and SW3

Cancellation of switch channel charge with a half sized transistor



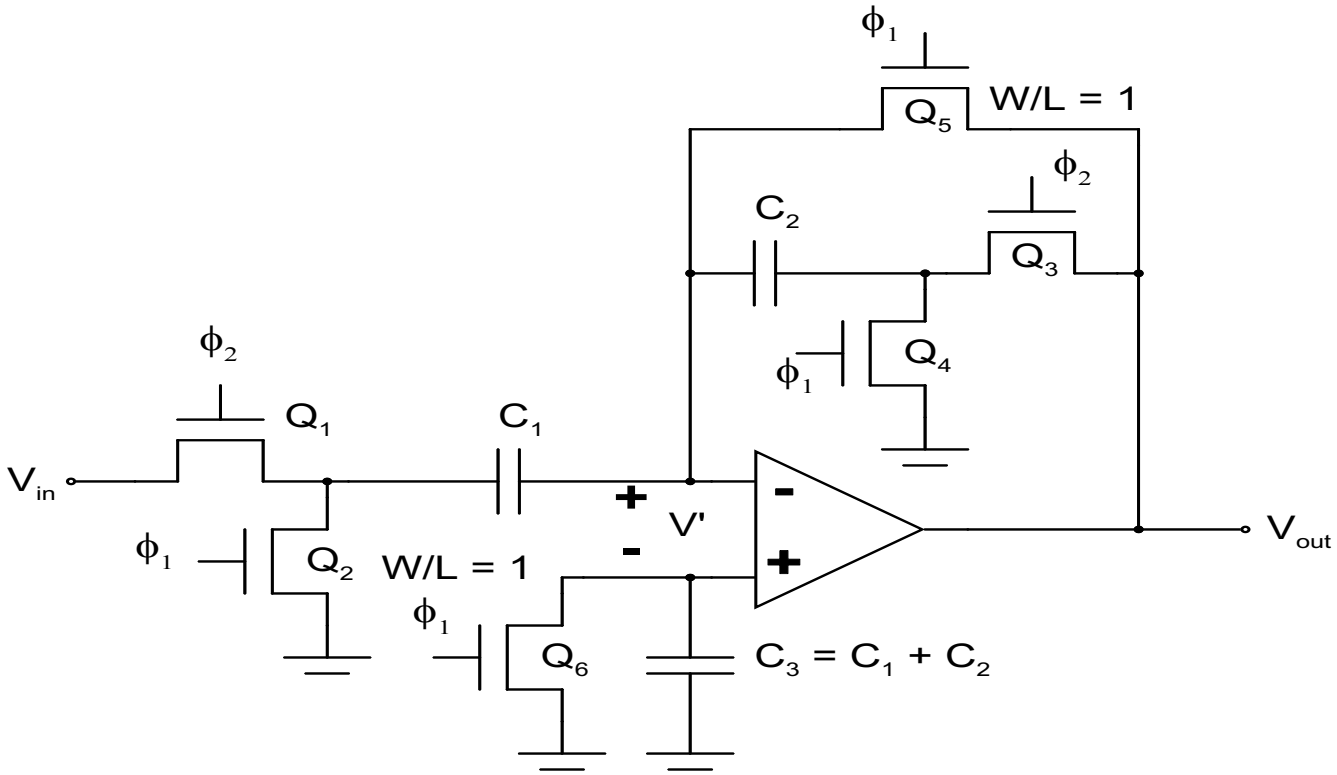
Equalization of termination impedances of the switch transistor



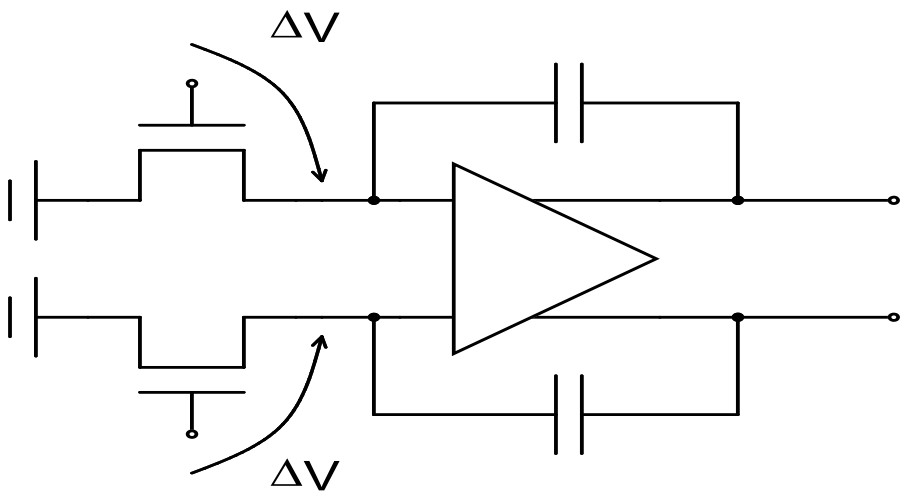


Cancellation of switch charge with fully-differential circuit topology

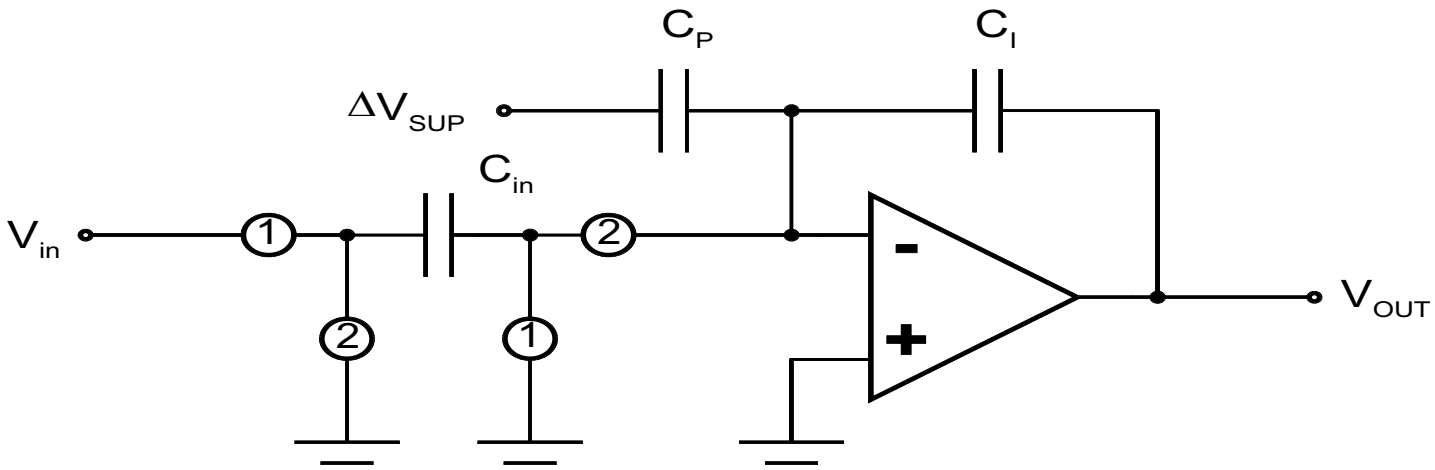
Semi-differential circuit using transistor Q_6 to cancel Q_5 channel charge:



Fully-differential circuit where channel charge of equal sized switch transistors appers as a common-mode disturbance:



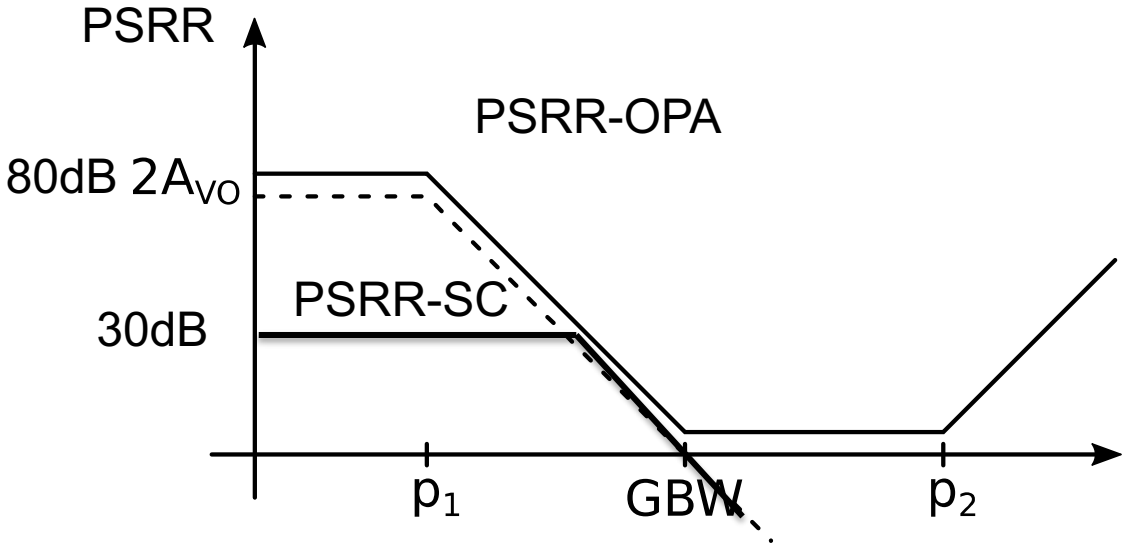
The SC-integrator model for the system PSRR_analysis



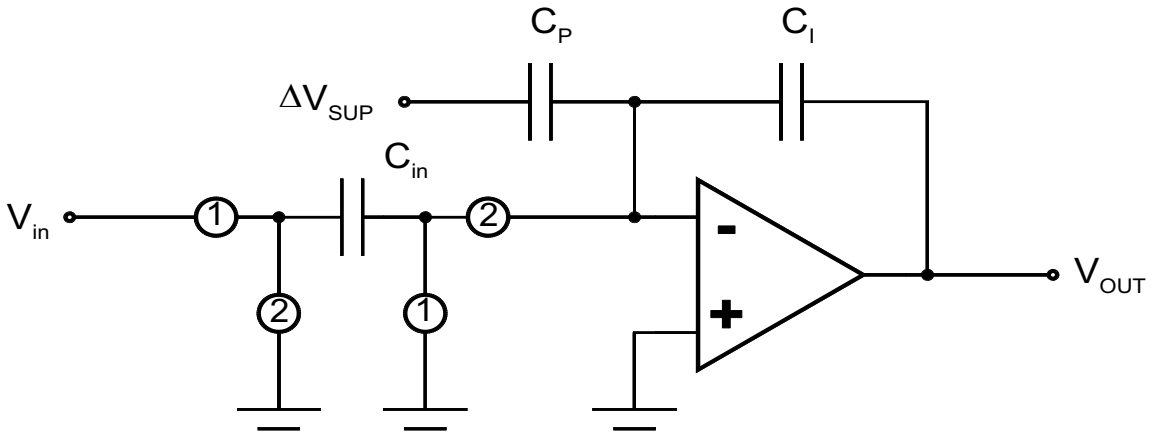
$$V_{OUT}(z) = \frac{z^{-1}}{1-z^{-1}} \frac{C_{in}}{C_I} V_{in} + \frac{C_P}{C_I} \Delta V_{SUP}$$

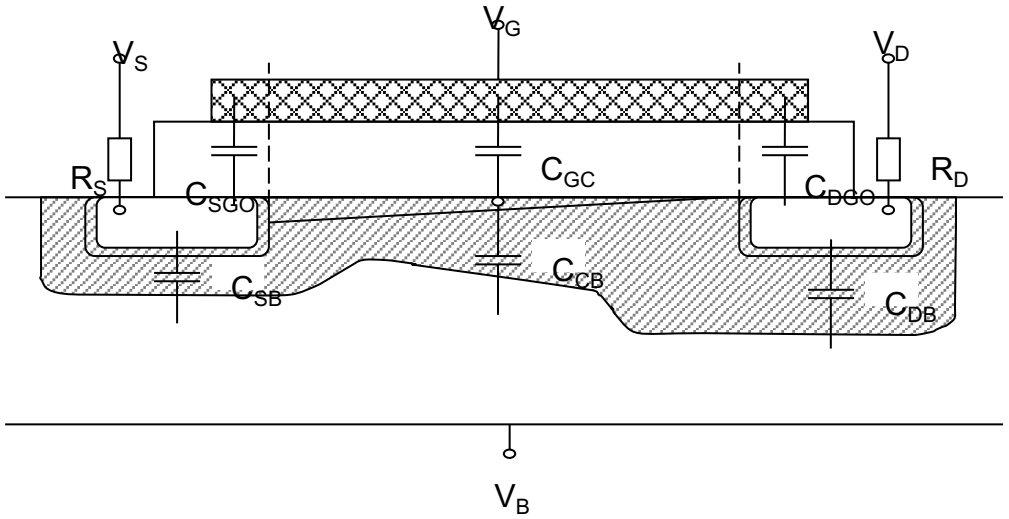
Parasitic capacitor C_P is order of tens of femtofarads
Integrator capacitor C_I is order of picofarads

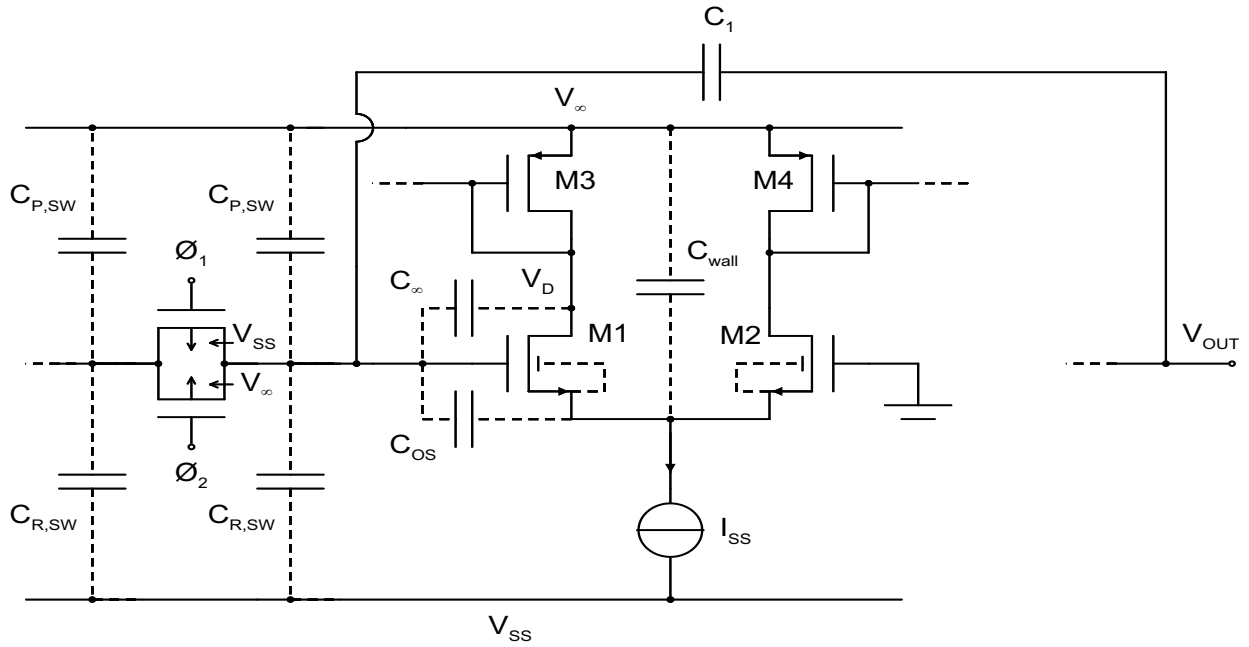
=>PSRR is reduced into order of 30-40 dB!
(Amplifier PSRR is better than 80dB)

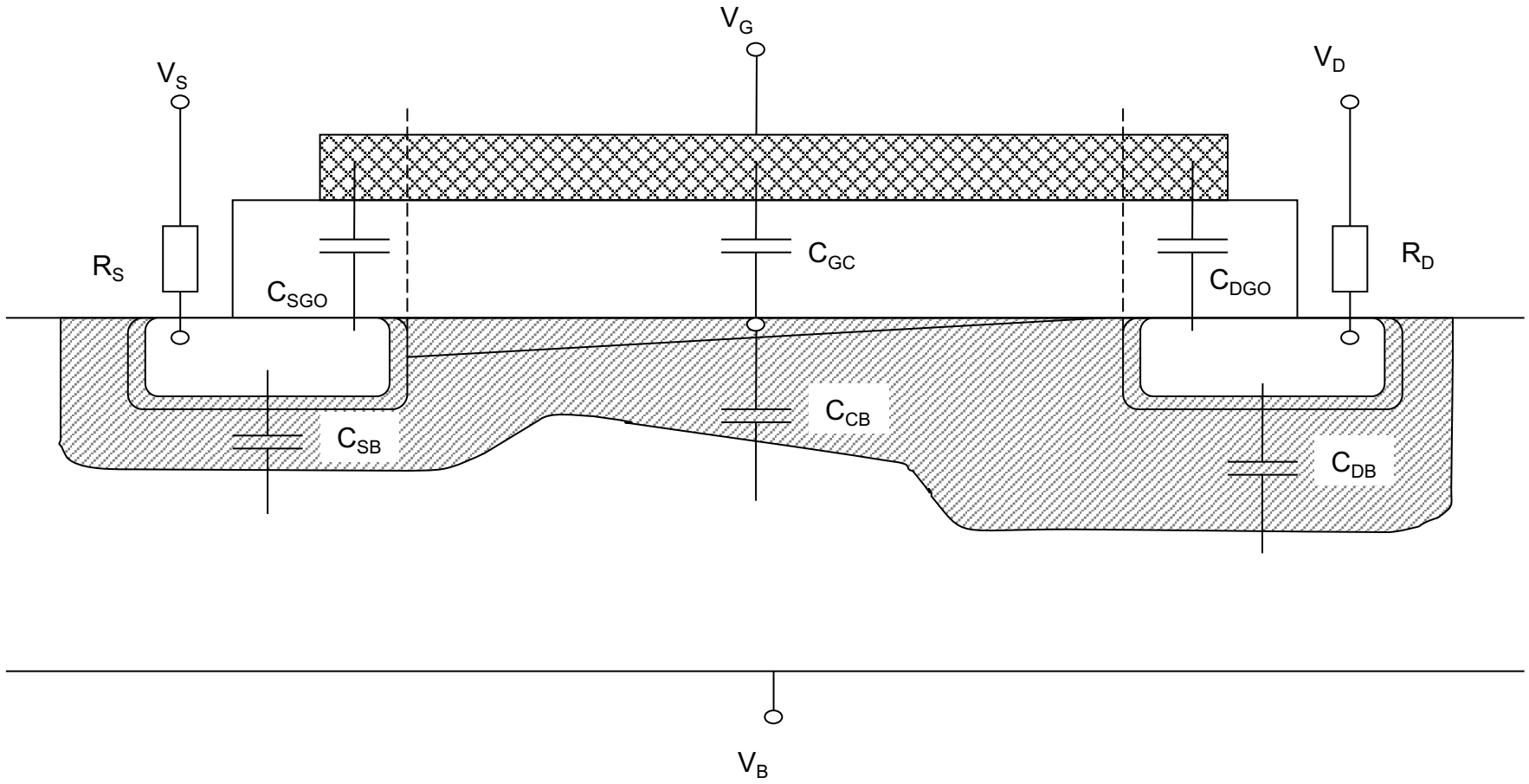


The model for the power supply coupling in the SC-integrator







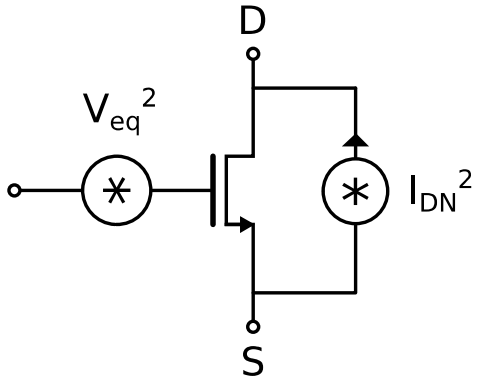

V_G
V_S
V_D
R_S
R_D
C_{SGO}
C_{GC}
C_{DGO}
C_{CB}
C_{SB}
C_{DB}
V_B

Noise in SC-circuits

1) Amplifier have a) thermal noise (broad-band) and b) 1/f-noise (low-frequency)

Resistivity of conductive channel causes thermal noise

$$\frac{\partial I_{DN}^{\ 2}}{\partial f} = \frac{8}{3} kT g_m$$

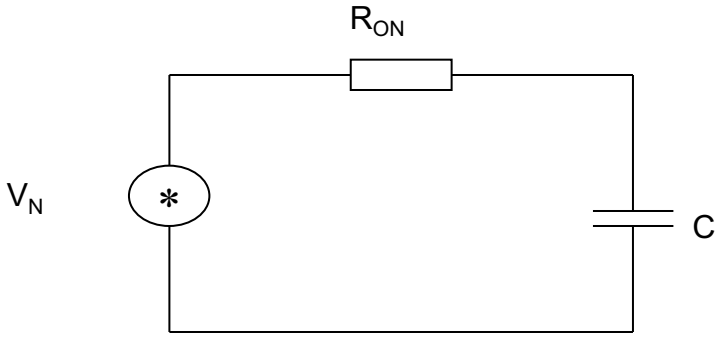


Charge traps in oxide-silicon surface are slow causing 1/f-noise

$$\frac{\partial V_{GN}^{\ 2}}{\partial f} = \frac{B}{fW \cdot L}$$

2) Switches has noise due to R_{ON} whose the noise density is

$$S_R(\omega) = 4kT\ R_{ON}$$



The noise power is obtained by integrating over the noise bandwidth.

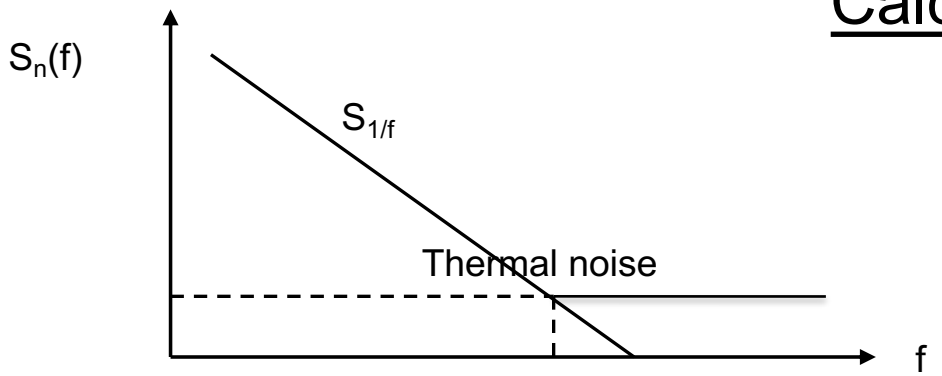
$$N_R = \int_{-\infty}^{\infty} S_R(\omega) H_{RC}^2(\omega) d\omega = \int_{-\infty}^{\infty} S_R(\omega) \frac{1}{1 + (\omega/\omega_{3dB})} d\omega$$

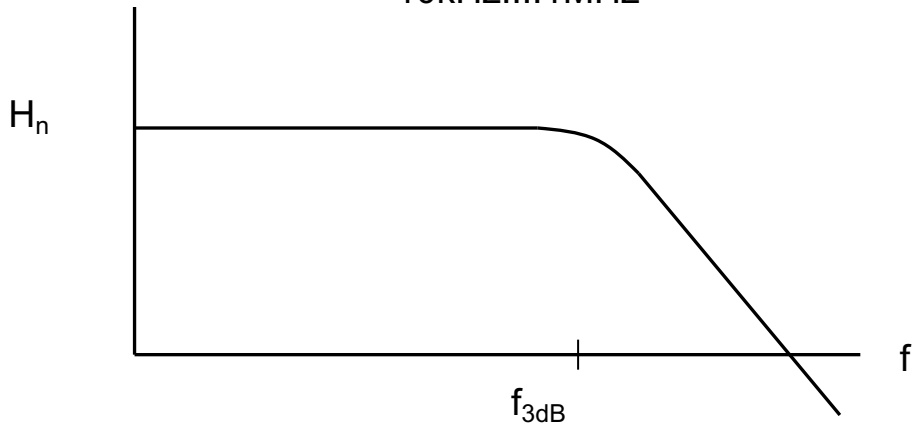
$$= \frac{kT}{C}$$

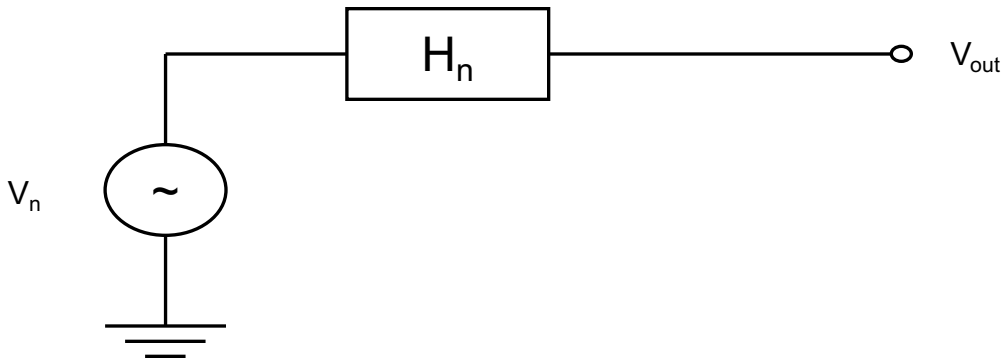
$$\Rightarrow \omega_{3dB} = \frac{1}{R_{ON} C}$$

Also the off-switch is noisy but the bandwidth is so narrow that it is meaningless.

Calculation of noise power







Amplifier noise density: $$S_{eq} = \left[\frac{8kT}{3g_m} + \frac{KF}{2fC_{OX}WLK'}\right]$$

Thermal noise — 1/f-noise

Noise power is obtained by integrating the noise density over the BW:

$$V_n^2 = \int_0^\infty S_\omega(f)|H_n(f)|^2 df + \int_0^\infty S_{\frac{1}{f}}(f)|H_n(f)|^2 df$$

$$\approx \int_0^{f_{3dB}} S_\omega(f)|H_n(f)|^2 df + \int_1^{f_{3dB}} S_{\frac{1}{f}}(f)|H_n(f)|^2 df$$

$$S_{\frac{1}{f}} = \frac{B}{WLf} \quad , \quad s_\omega \approx \frac{8kT}{3g_m} \quad , \quad f_{3dB} = GBW = \frac{g_m}{2\pi C_L}$$

$$H_y = \begin{cases} 1 & f < f_{3dB} \\ 0 & f > f_{3dB} \end{cases}$$

Integrated noise power over noise BW:

$$v_n^2 \simeq \frac{8kT}{3g_m} \cdot GBW + \frac{B}{WL} \cdot 1nGBW$$

$$\simeq \frac{8kT}{3C_L} + \frac{B}{WL} \cdot 1n\frac{g_m}{C_L}$$

Noise folding in the sampled system

Amplifier bandwidths (GBW) are typically 5-7 times larger than the clock frequency

=> Noise folding occurs from several side-bands increasing the noise level at the signal band