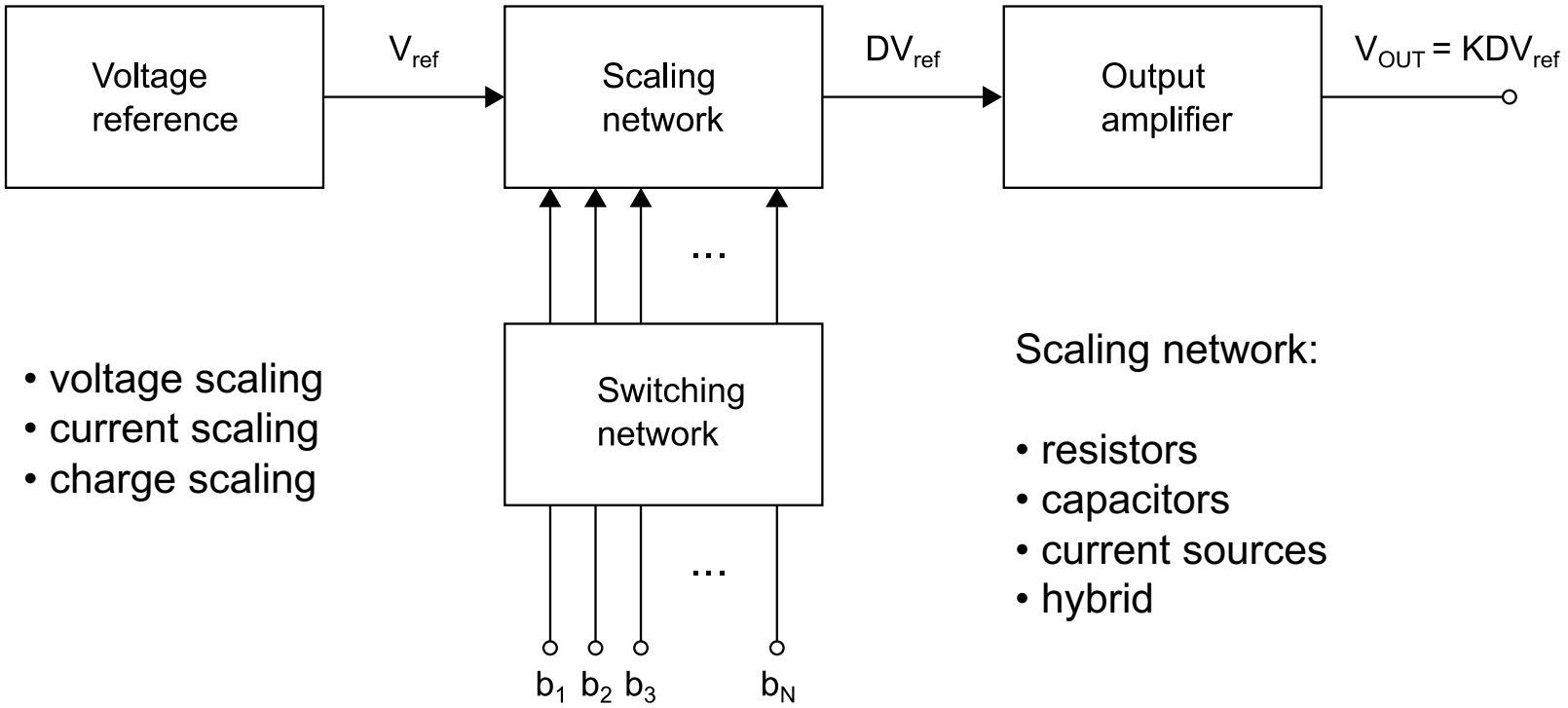
ELEC-E3530

Integrated Analog Systems
L8 Digital-to-Analog Converters

Principle block diagram of a D/A converter



- voltage scaling
- current scaling
- charge scaling

Scaling network:

- resistors
- capacitors
- current sources
- hybrid

Summary of DACs

DAC Type	Advantage	Disadvantage
Current scaling	Fast, insensitive to switch parasitics	Large element spread, nonmonotonic
Voltage scaling	Monotonic, equal resistors	Large area, sensitive to parasitic capacitance
Charge scaling	Fast, good accuracy	Large element spread, nonmonotonic

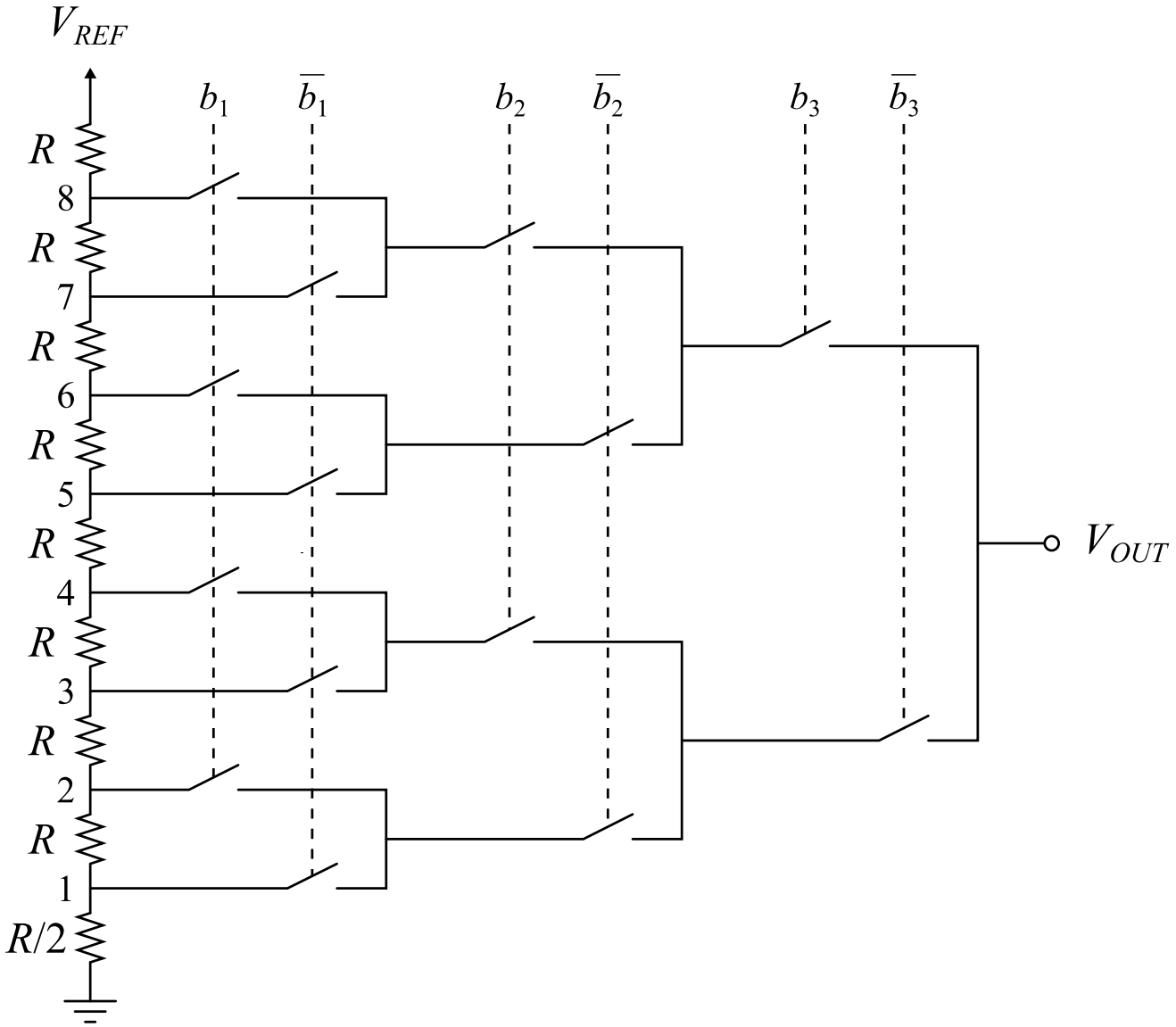
Implementation of a 3-bit voltage-scaling D/A converter

Tap voltages:

$$V_i = \frac{(i-1)R + \frac{R}{2}}{N \cdot R + \frac{R}{2}} \cdot V_{REF} = V_{OUT}$$

$$i = b_3 \cdot 2^2 + b_2 \cdot 2 + b_1$$

$$N = 2^n$$



Binary coded D/A converter

- 2^n resistors

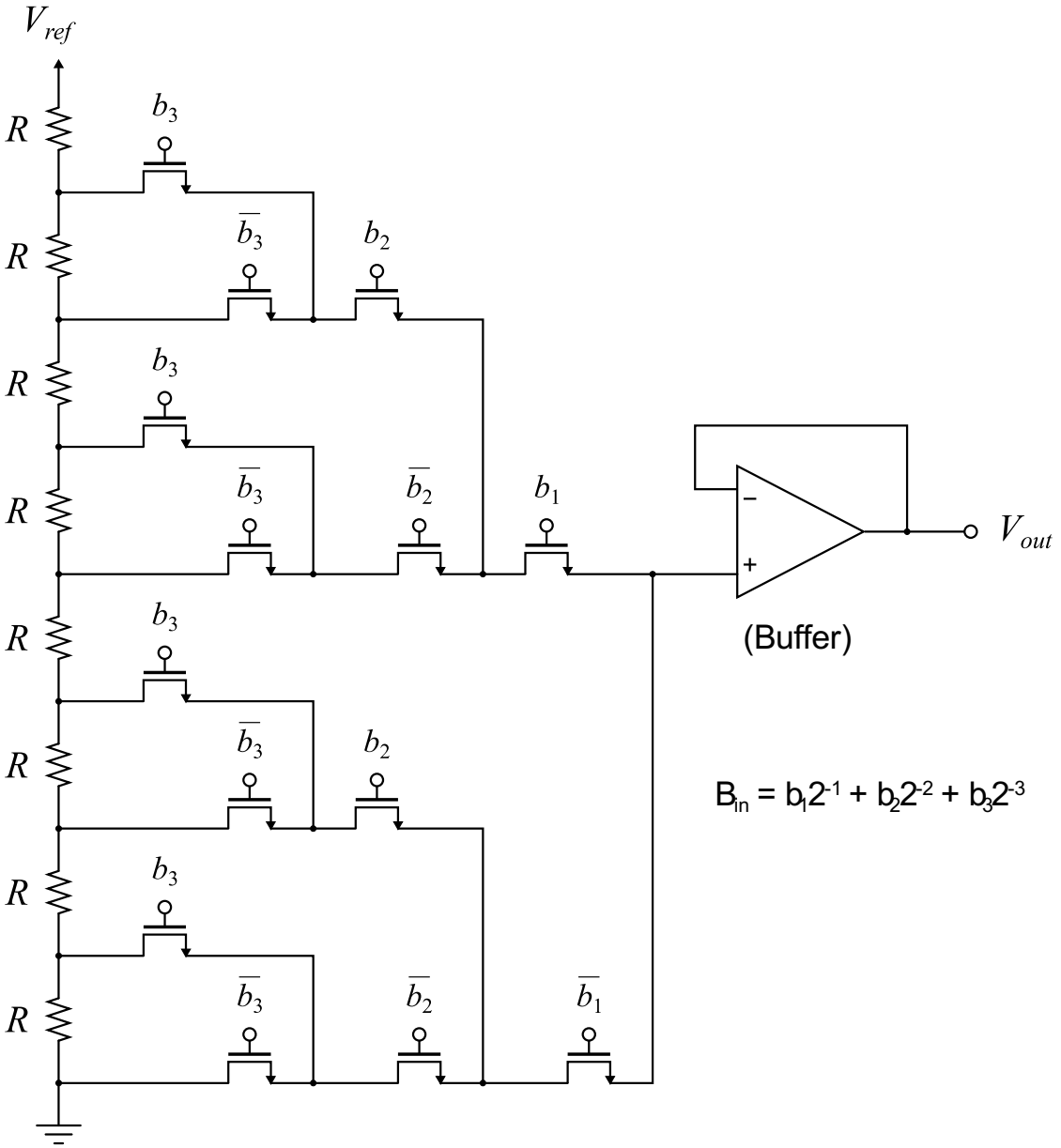
- $(2^n-1)\cdot 2$ switches

- Accuracy limited to 8 bits

- Higher accuracies common centroid geometry needed → complicated wiring

- Speed limited by number of series switches

- Glitches f. ex transition 011 →100

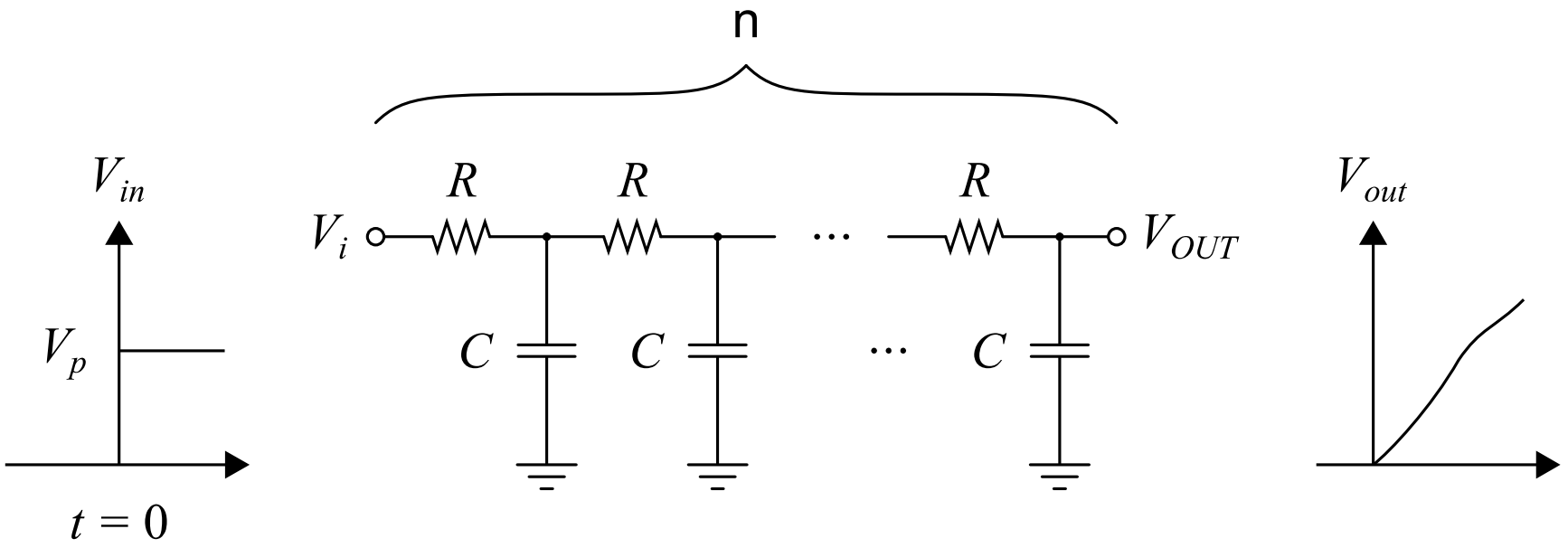


Settling of R-string D/A converter

- When switched the speed is limited by RC time constants of the switches

- Number of switches in series n

R = switch on-resistance
C = switch capacitor



$$\tau \cong RC\left(\frac{n^2}{2}\right)$$

Linear error in resistors cause integral nonlinearity

Tap voltage j assuming a linear processing error in resistivity

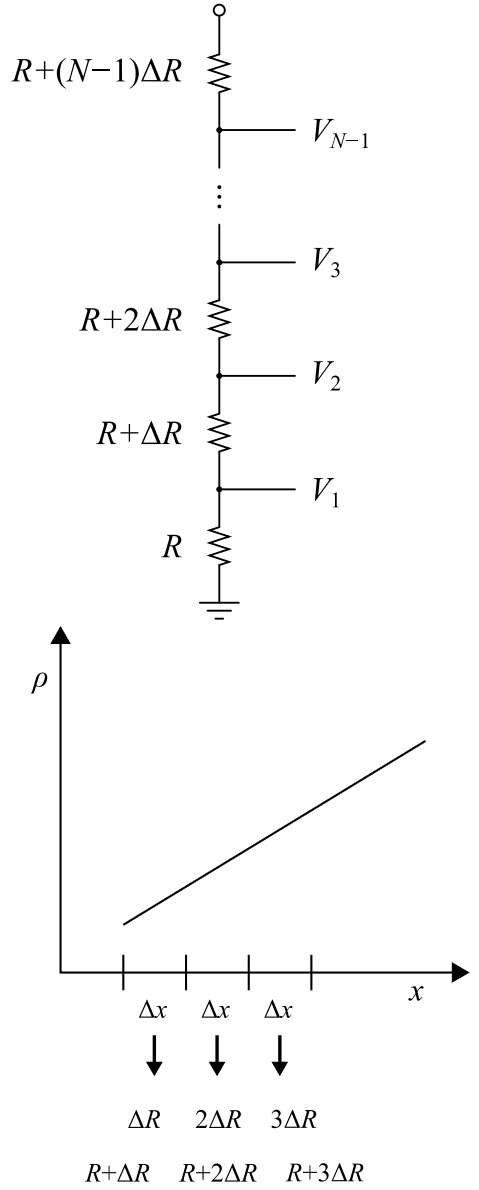
$$V_j = \frac{\sum_{K=0}^{j-1}\left(R + k\Delta R\right)}{\sum_{K=0}^{N-1}\left(R + k\Delta R\right)} V_{REF} = \frac{jR + \frac{j(j-1)}{2}\Delta R}{NR + \frac{N(N-1)}{2}\Delta R} V_{REF} \quad (1)$$

The INL profile is given by the difference between (1) and ideal tap voltage, jV_{REF}/N:

$$INL_j = \frac{j}{N} V_{REF} - \frac{jR + \frac{j(j-1)}{2}\Delta R}{NR + \frac{N(N-1)}{2}\Delta R} V_{REF} \quad (2)$$

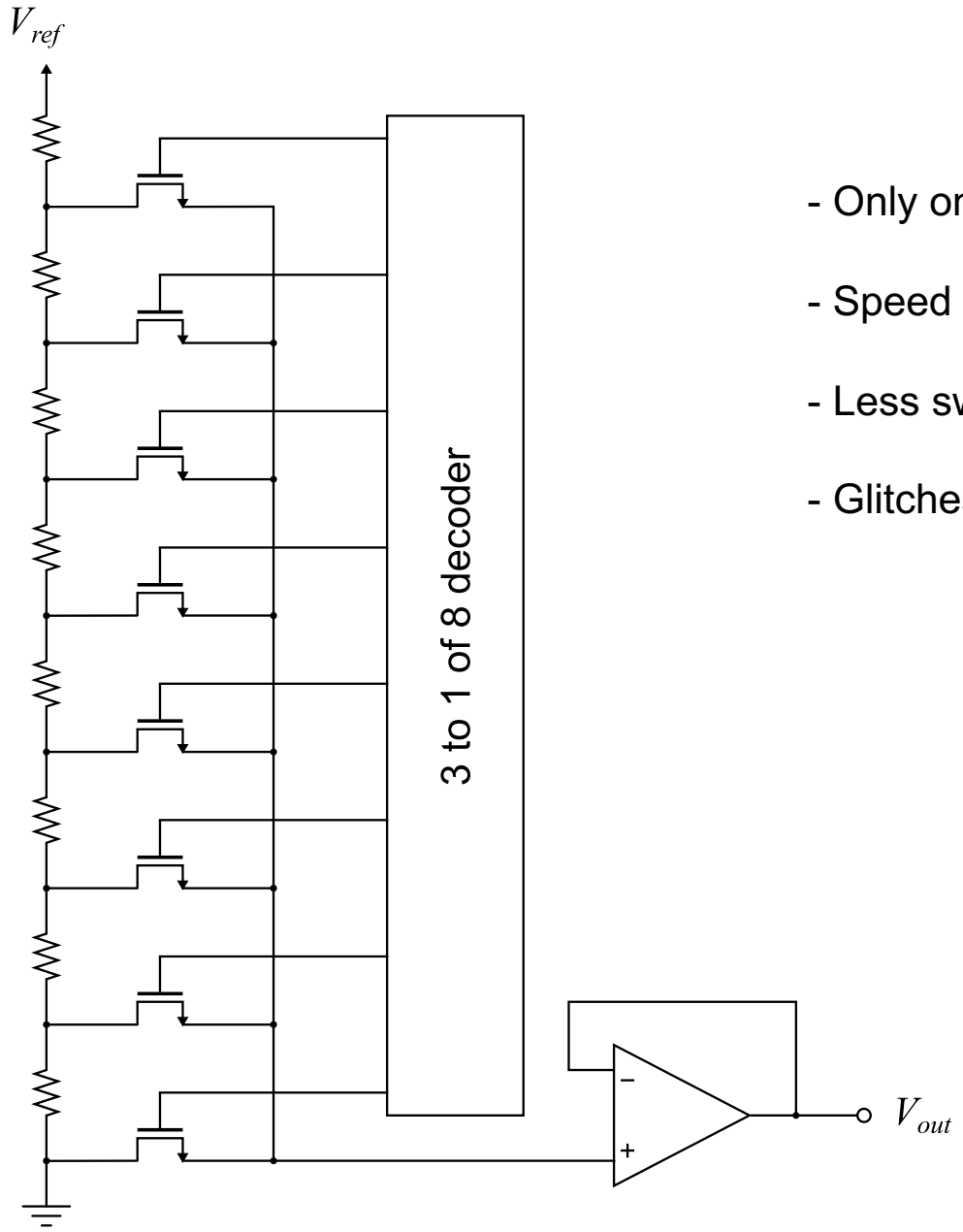
Simplifying (2) yields

$$INL_j = \frac{j(N-j)}{R + \frac{N-1}{2}\Delta R} \frac{\Delta R}{2N} V_{REF}$$



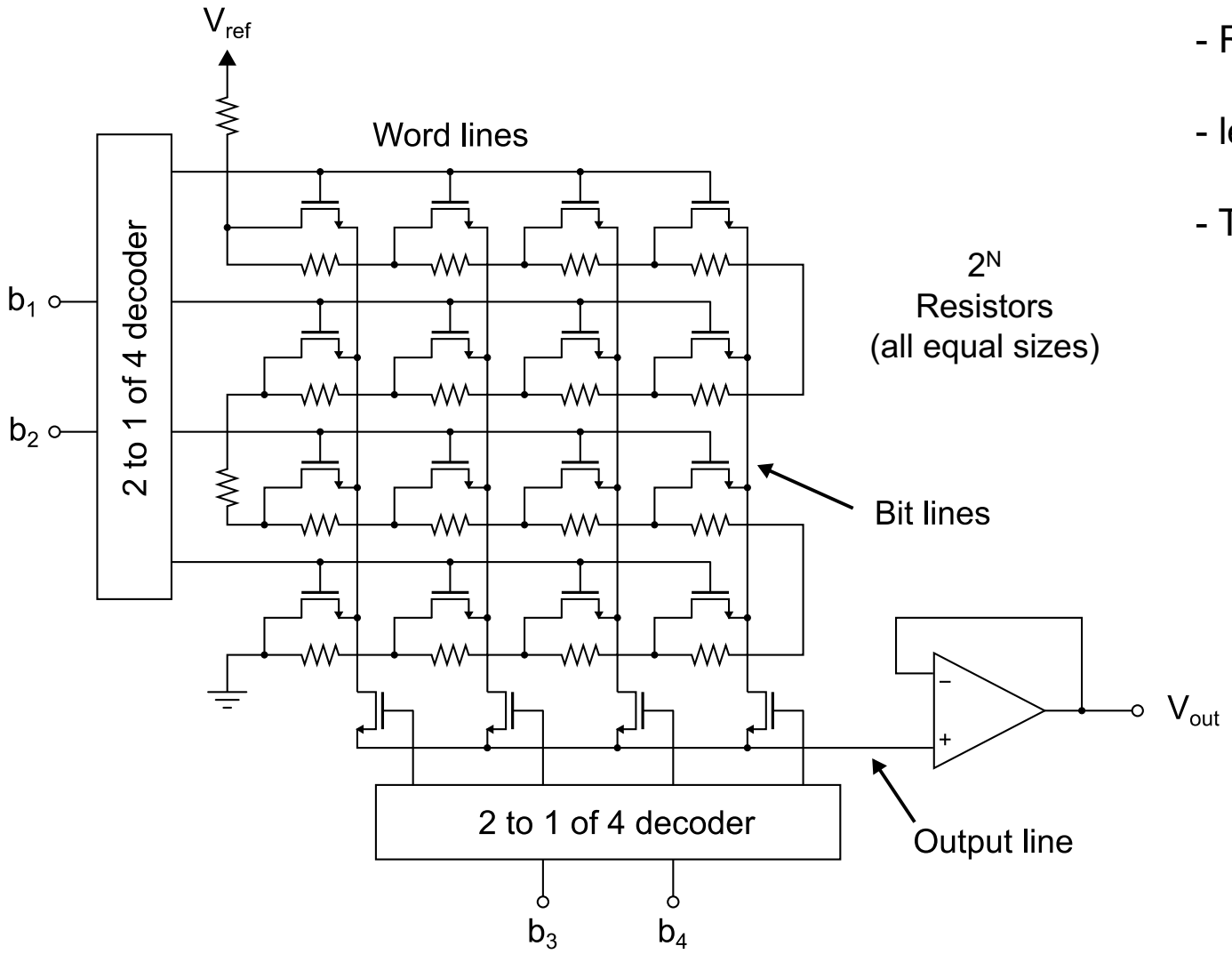
Thermometer coded D/A converter

2^N resistors
(all equal sizes)



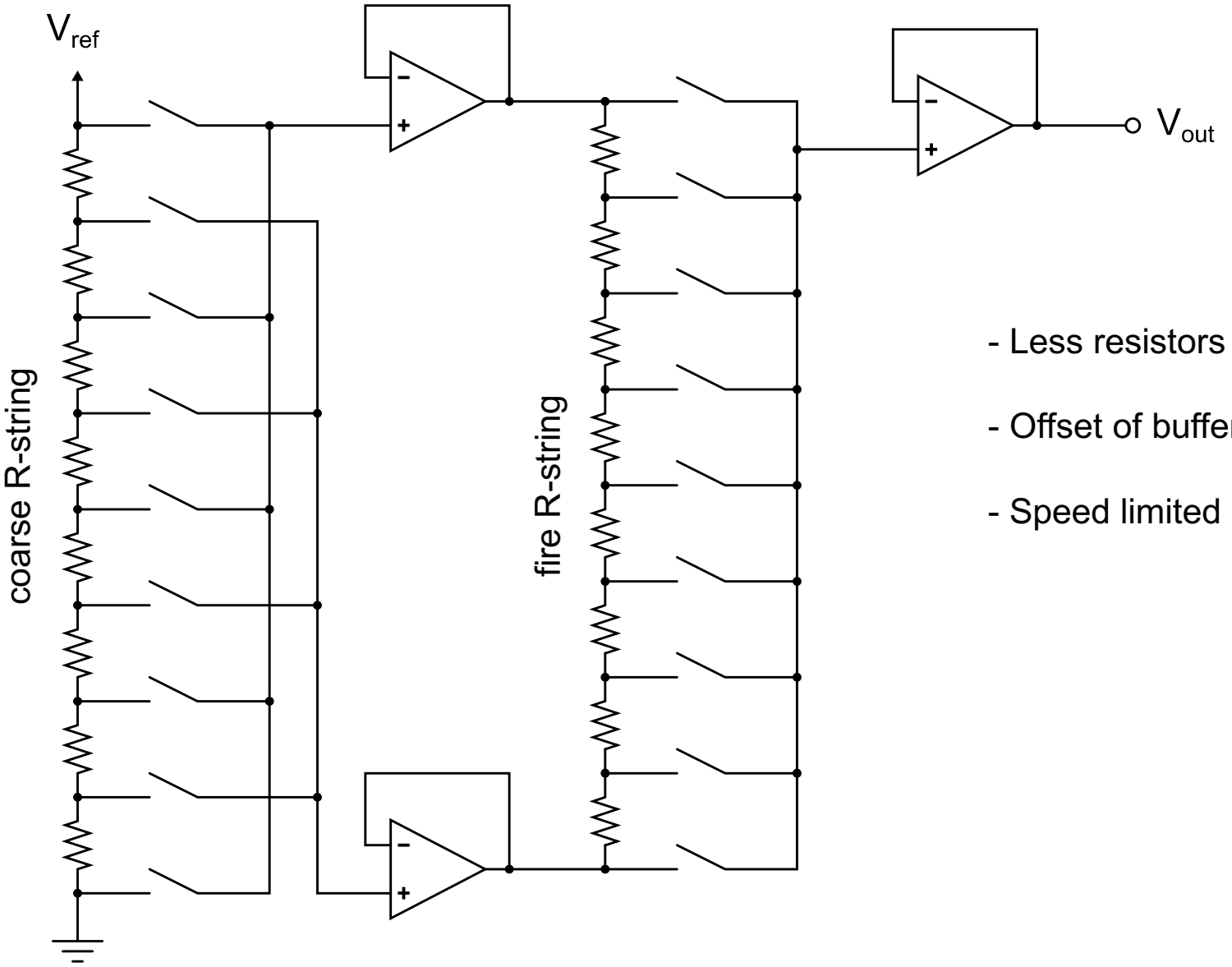
- Only one switch per tap voltage
- Speed limited by only one RC-timeconstant
- Less switches, n-to-2n decoder needed
- Glitches eliminated

A 4-bit folded resistor-string D/A converter



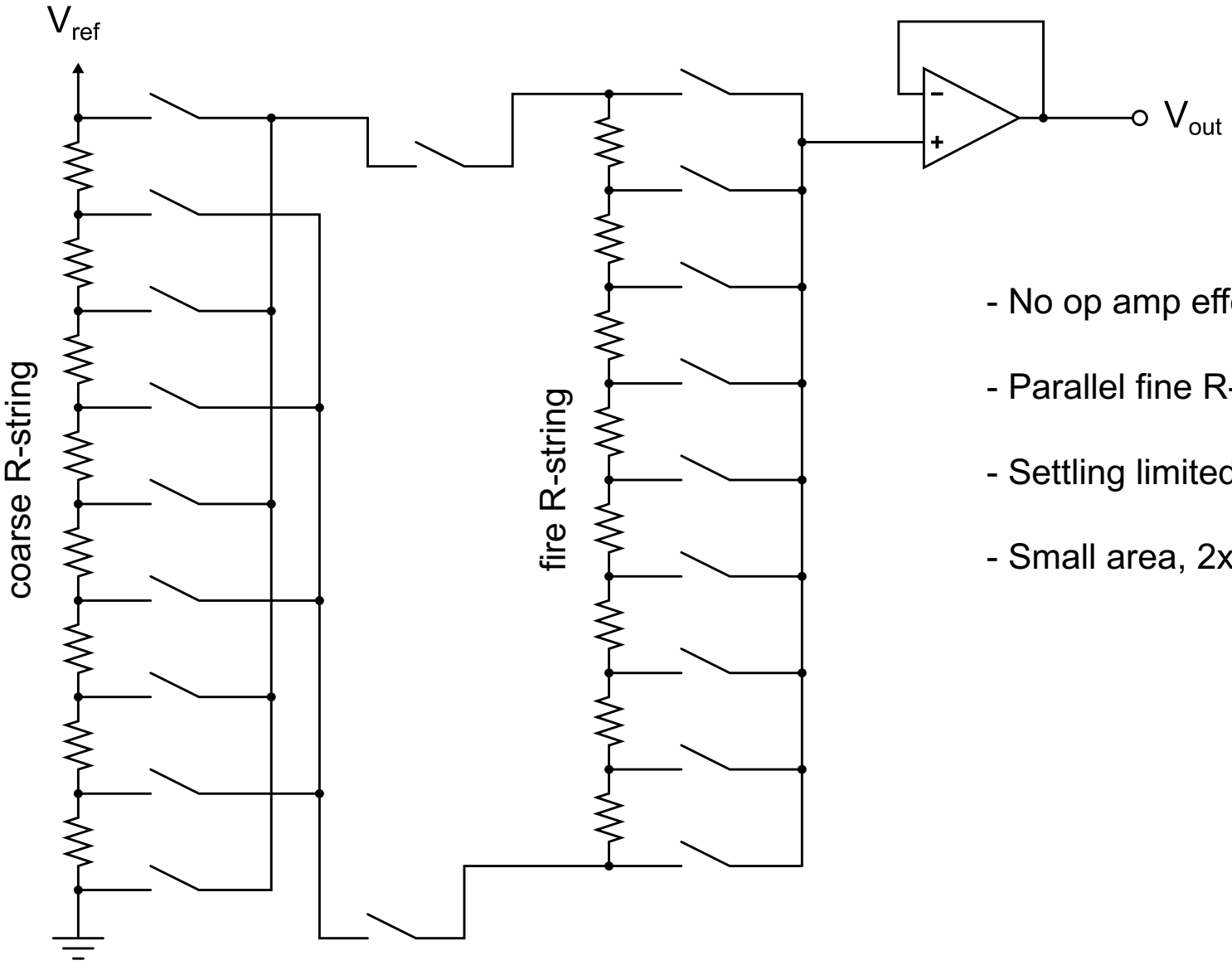
- Row and column decoders
- less complex decoders
- Two switches in series

Multiple R-string 6-bit D/A converter



- Less resistors $2x2^{N/2}$
- Offset of buffer amplifiers
- Speed limited by buffer amplifiers

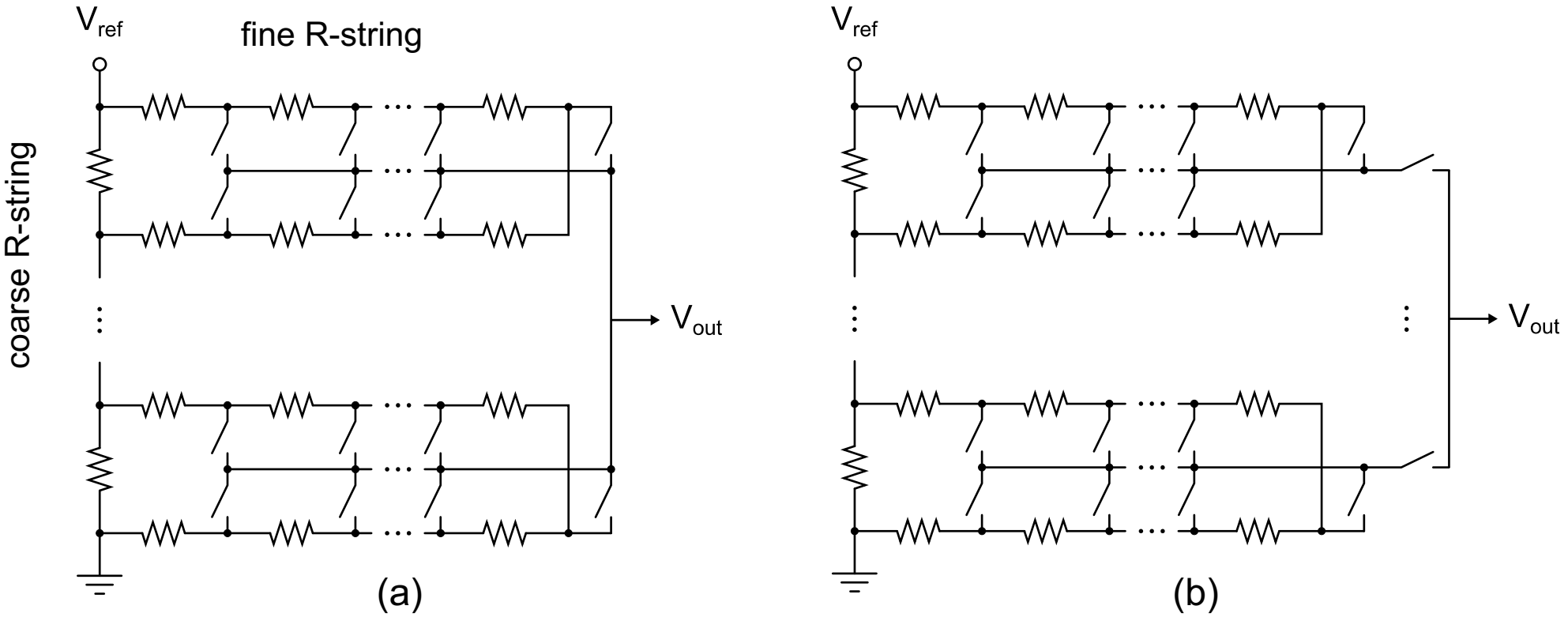
Multiple R-string 6-bit D/A converter



- No op amp effects
- Parallel fine R-string reduces the coarse tap resistor
- Settling limited by the time-constant of fine R-string
- Small area, $2x2^{N/2}$ resistors

Coarse and fine R-strings without Op Amps

Intermeshed resistor-ladder DACs with (a) one-level multiplexing and (b) two-level multiplexing.

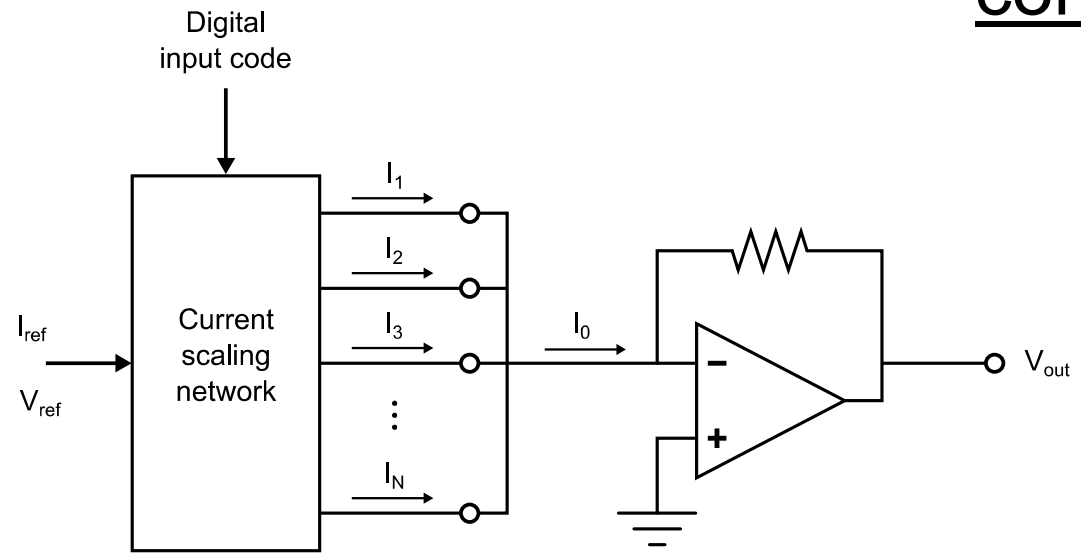


- No offset error due to op amp

- Every coarse tap resistor has a parallel fine R-string of resistors → no error due to parallel connection

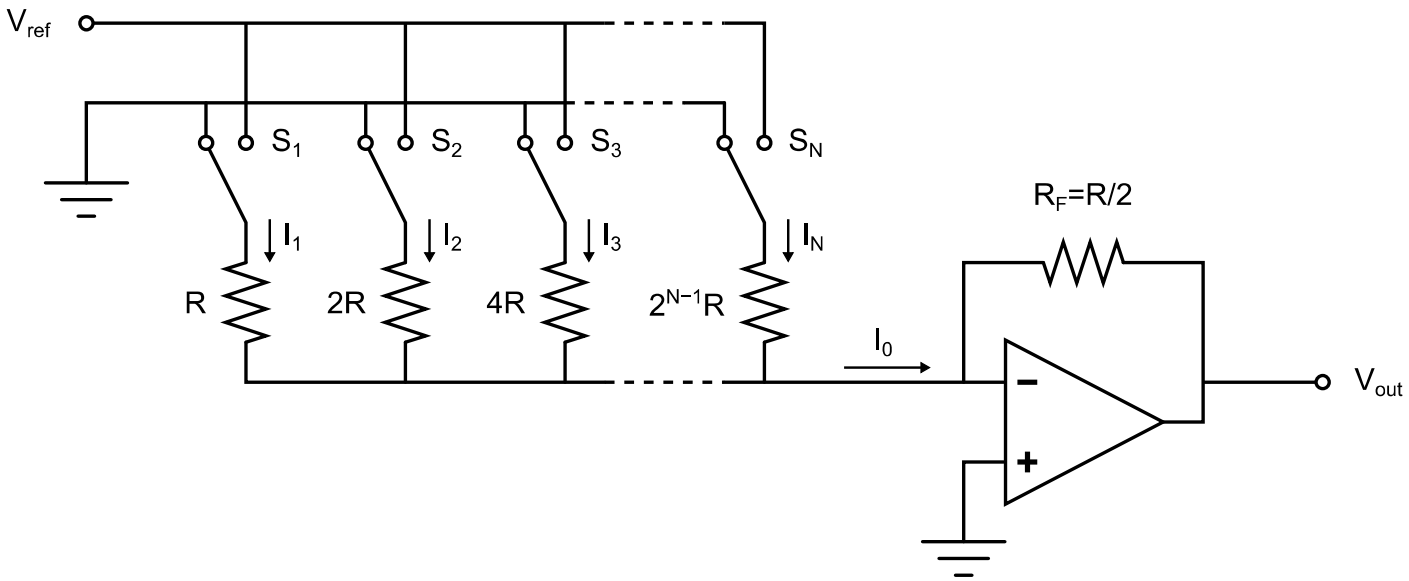
- Only one series switch low R_{ON}, many parallel switches → high C

Conceptual illustration of a current-scaling D/A converter

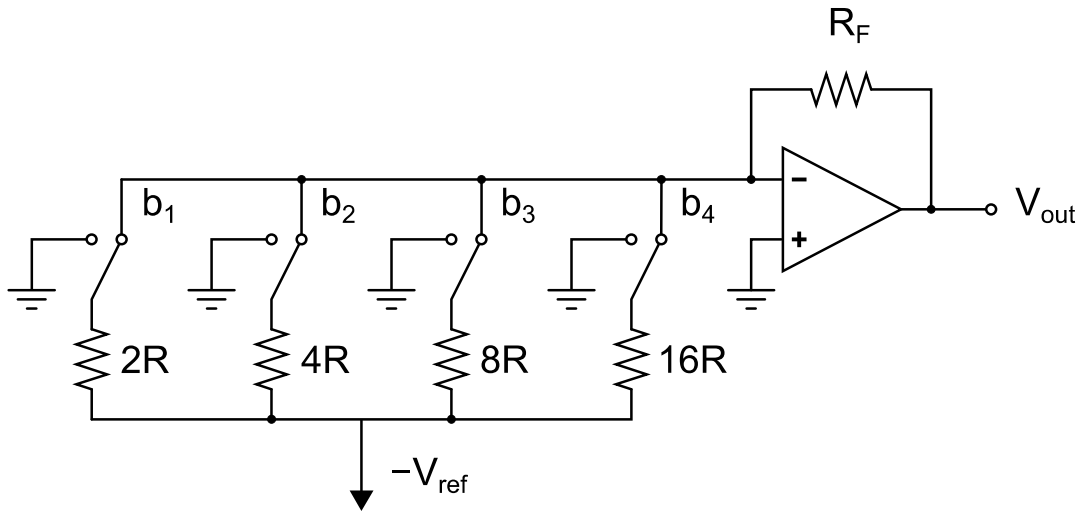


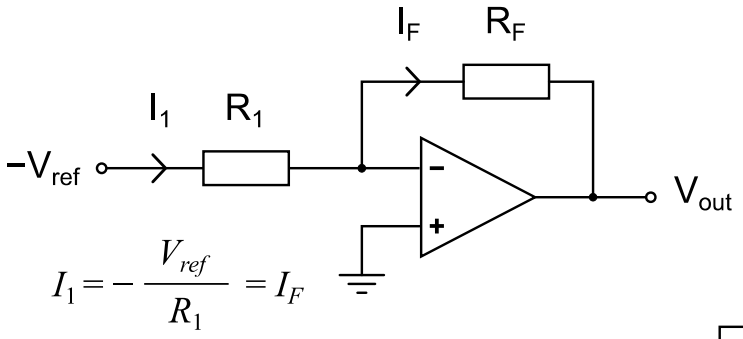
$$I_i = 2^i I_{ref}$$

Binary weighted resistors convert the V_{ref} into binary weighted currents.

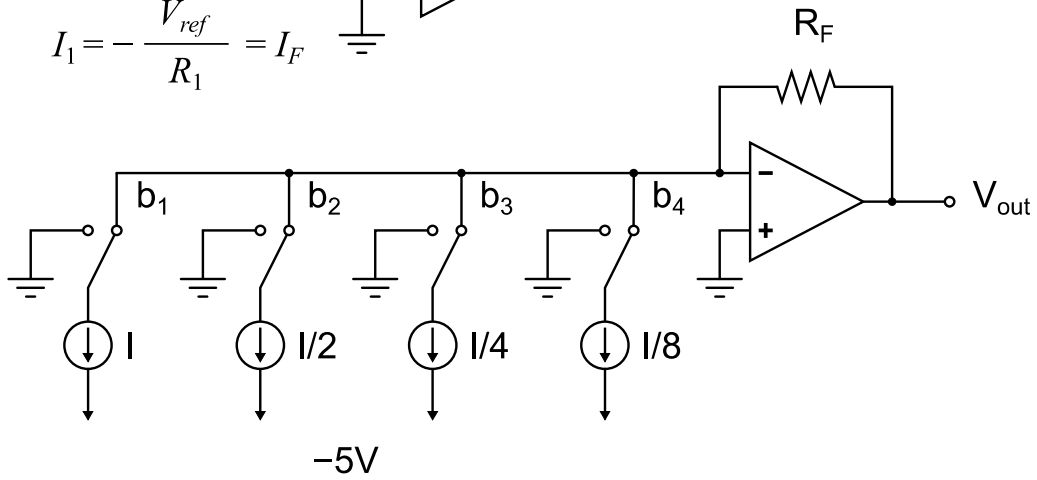


Current scaling D/A converter





$$I_1 = -\frac{V_{ref}}{R_1} = I_F$$



- Weighted currents generated with weighted resistors

$$I_i = \frac{V_{ref}}{R_i}$$

- Large resistor spread

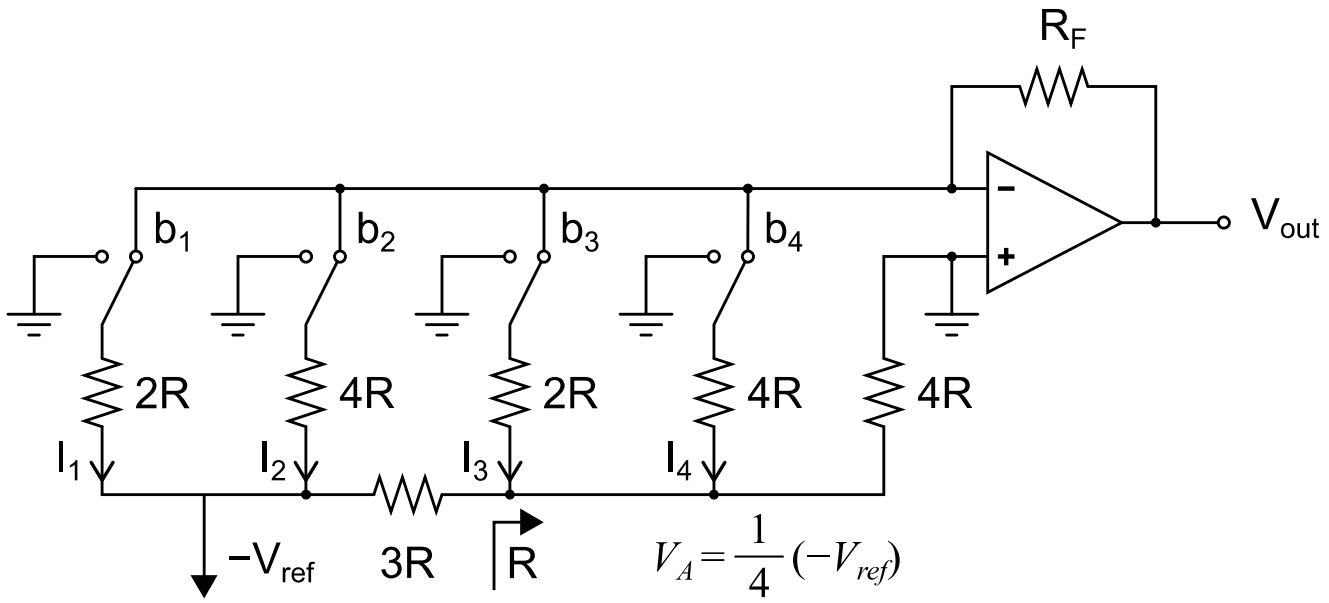
$$R_{MAX} = 2^n \cdot R_{MIN} \Rightarrow \text{large area}$$

- Switched R_{ON} in series → non-linearity

- Resistors switched between virtual ground and analog ground

- Speed limited by op amp

Voltage and current scaling



Resistor spread

$R_{MAX} = 2^{n/2} \cdot R_{MIN}$

$\Rightarrow$ reduced area

no switch in series with 3R

$\Rightarrow$ matching error

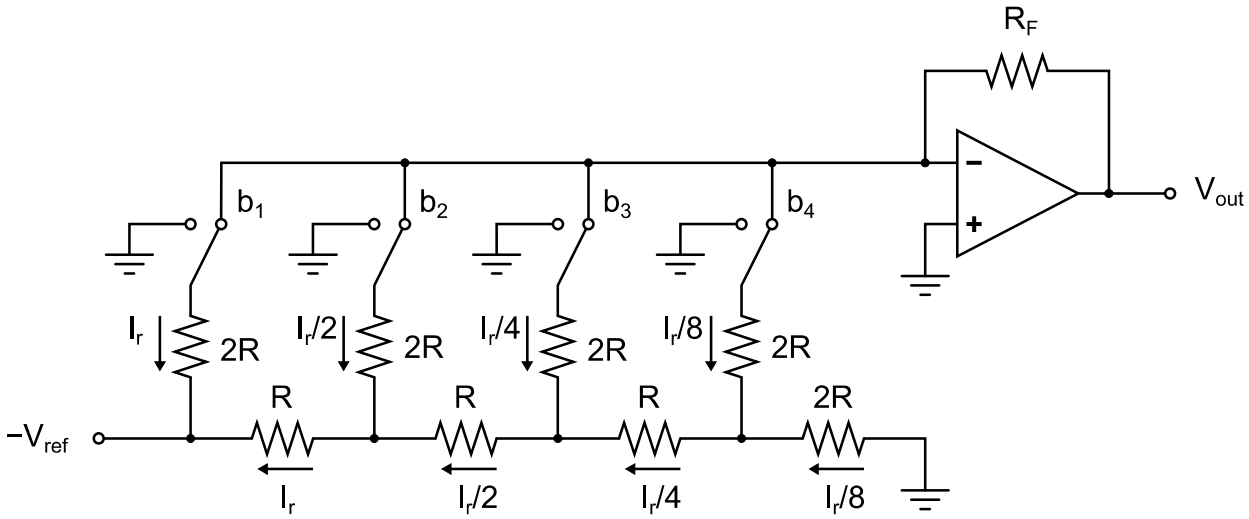
Total resistor to ground seen to the right of 3R is R = 2R||(4R||4R)

The branch currents are:

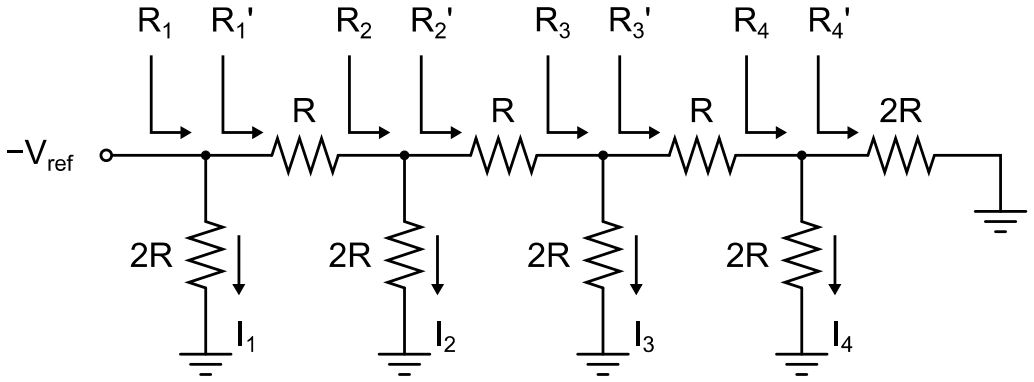
$$I_1 = \frac{-V_{ref}}{2R} \qquad I_3 = \frac{V_A}{2R} = \frac{-V_{ref}}{8R}$$

$$I_2 = \frac{-V_{ref}}{4R} \qquad I_4 = \frac{V_A}{4R} = \frac{-V_{ref}}{16R}$$

R-2R D/A converter



4-bit R-2R based D/A converter



R-2R resistance ladder

$$R_4' = 2R$$

$$R_4 = 2R \| R_4' = R$$

$$R_3' = R + R_4 = 2R$$

$$R_3 = 2R \| R_3' = R$$

$$R_2' = R + R_3 = 2R$$

$$R_2 = 2R \| R_2' = R$$

$$R_1' = R + R_2 = 2R$$

$$R_1 = 2R \| R_1' = R$$

$$I_1 = \frac{1}{2}\frac{V_{ref}}{R}$$

$$I_1' = I_1$$

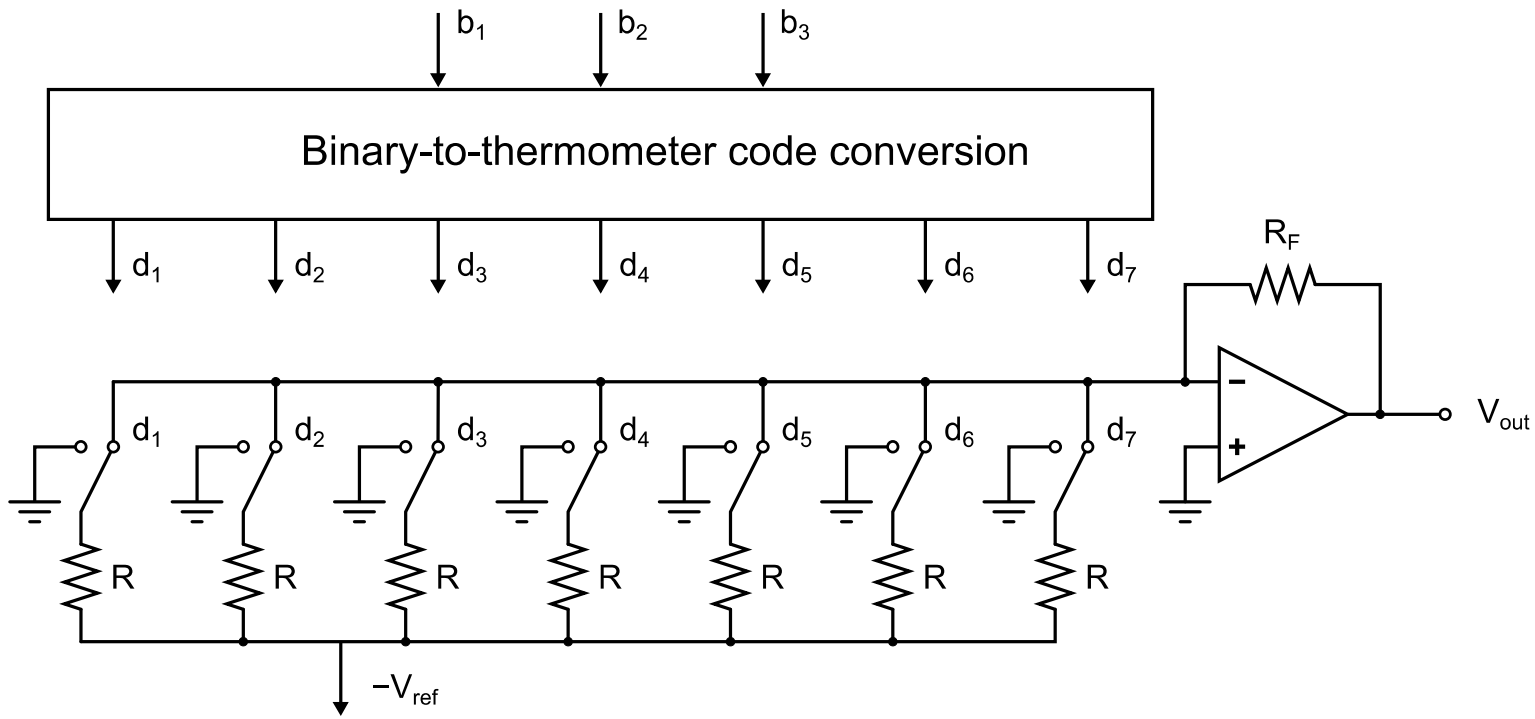
$$I_2 = \frac{1}{2} I_1' = I_2' = \frac{1}{2} I_1$$

$$I_3 = I_3' = \frac{1}{2} I_2' = \frac{1}{4} I_1$$

$$I_4 = I_4' = \frac{1}{2} I_3' = \frac{1}{8} I_1$$

- switch R_{ON} effects 2R → error

Thermometer coded current scaling D/A converter



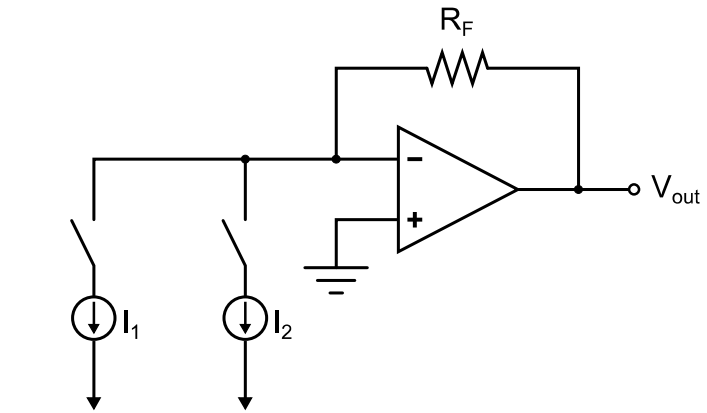
- Glitches eliminated

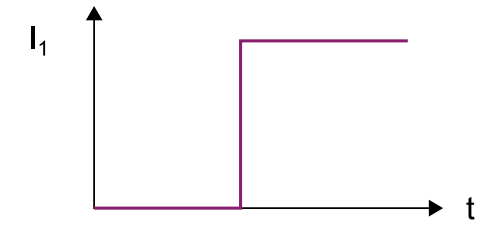
- Every resistor adds current of 1 LSB

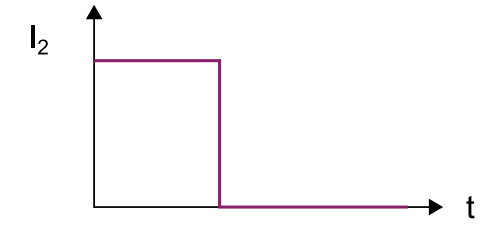
- Switches give equal error for every R → R_{ON} eliminated for first order

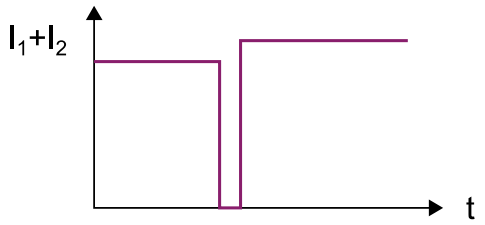
- Large n-to-1 of 2^n decoder needed → complicated wiring for switches

Binary vs. thermometer coding







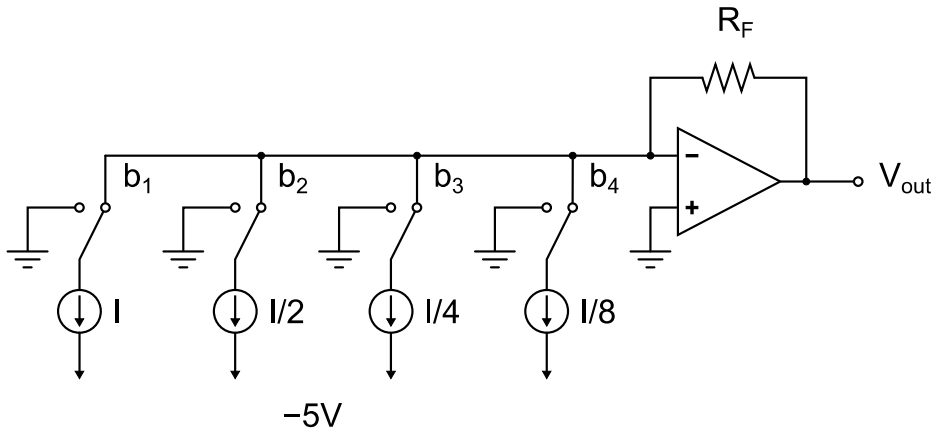


”glitch”

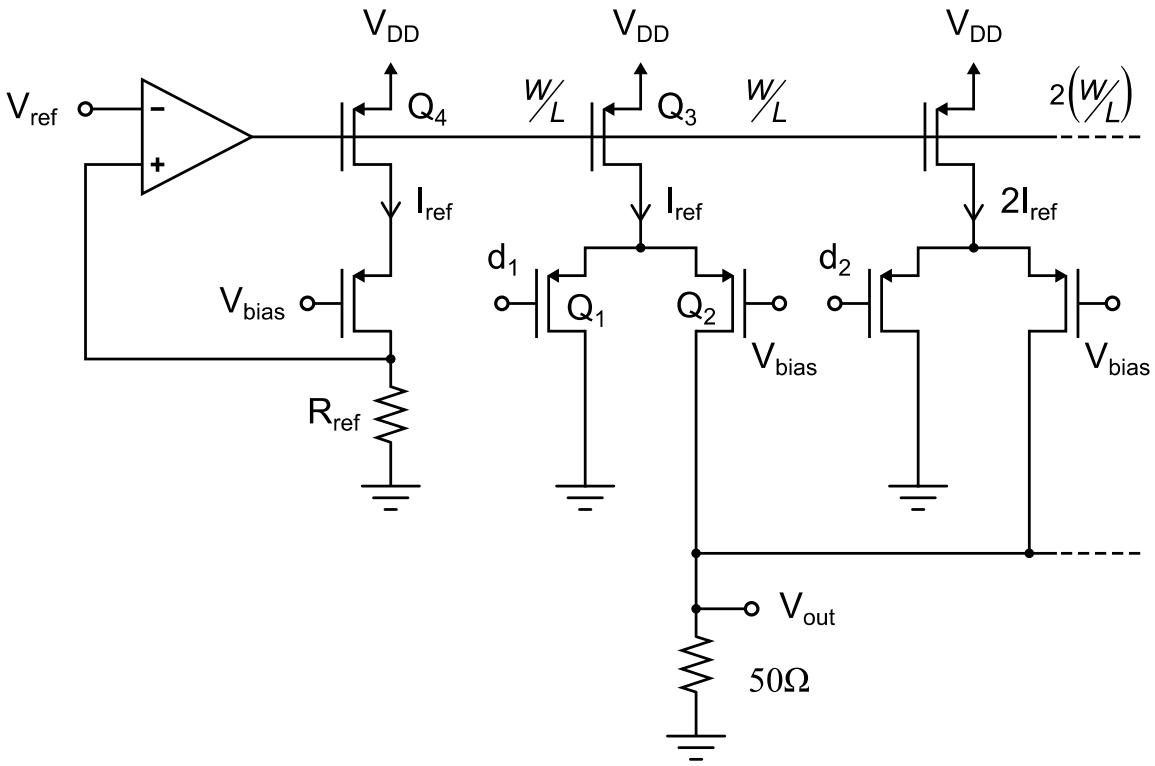
Decimal	Binary			Thermometer Code						
	b1	b2	b3	d1	d2	d3	d4	d5	d6	d7
0	0	0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	0	0	1
2	0	1	0	0	0	0	0	0	1	1
3	0	1	1	0	0	0	0	1	1	1
4	1	0	0	0	0	0	1	1	1	1
5	1	0	1	0	0	1	1	1	1	1
6	1	1	0	0	1	1	1	1	1	1
7	1	1	1	1	1	1	1	1	1	1

Glitches are code i.e. signal dependant and cause spurs in the signal spectrum.

Binary-weighted current source D/A convertor

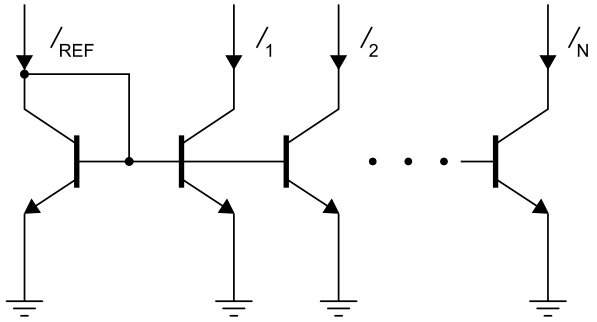


Binary-weighted current-mode D/A converter

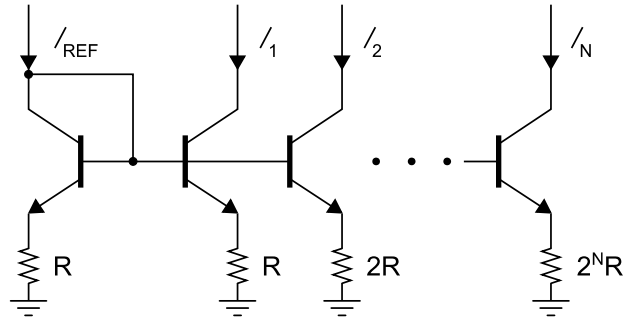


- Binary weighted currents realized with binary weighted current mirrors

- Switch transistors Q_1 and Q_2 direct the current either to V_{ss} (d_1=0) or to load reistor (d_1=1)



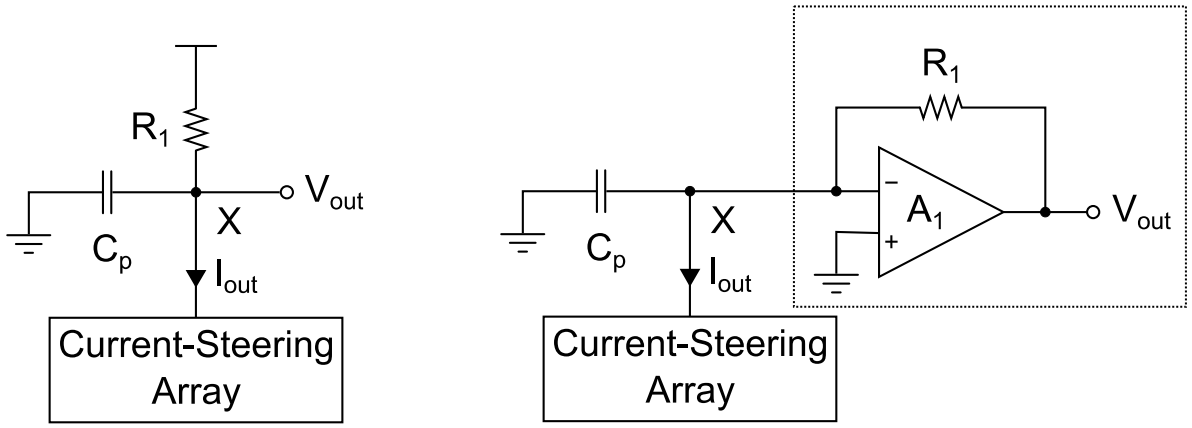
(a)



(b)

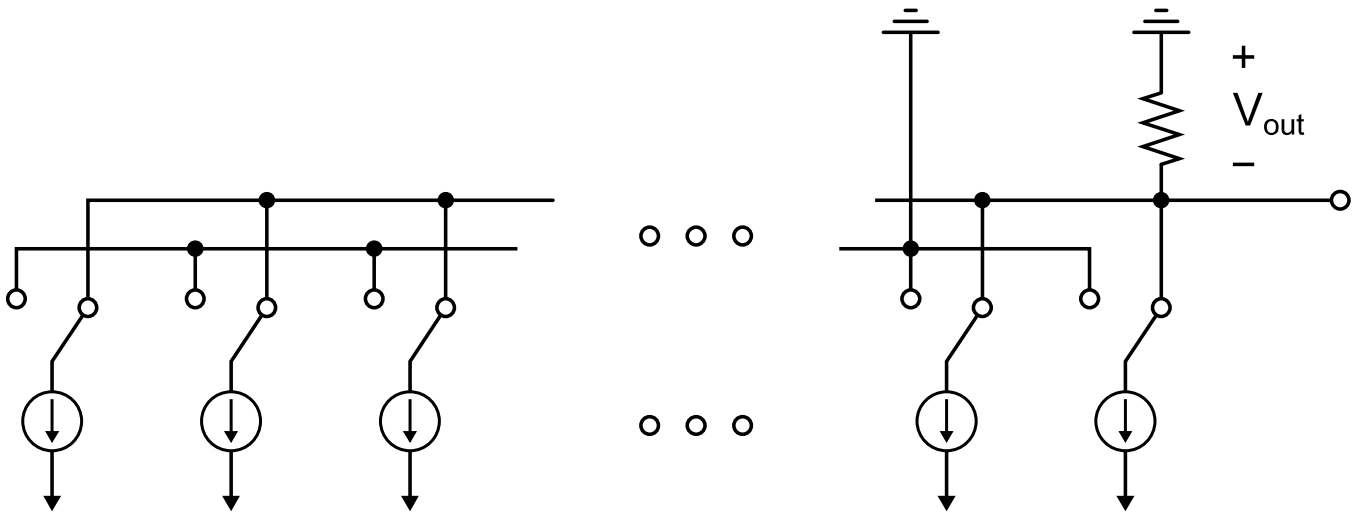
(a) Simple current replication;

(b) current replication incorporating emitter degeneration.

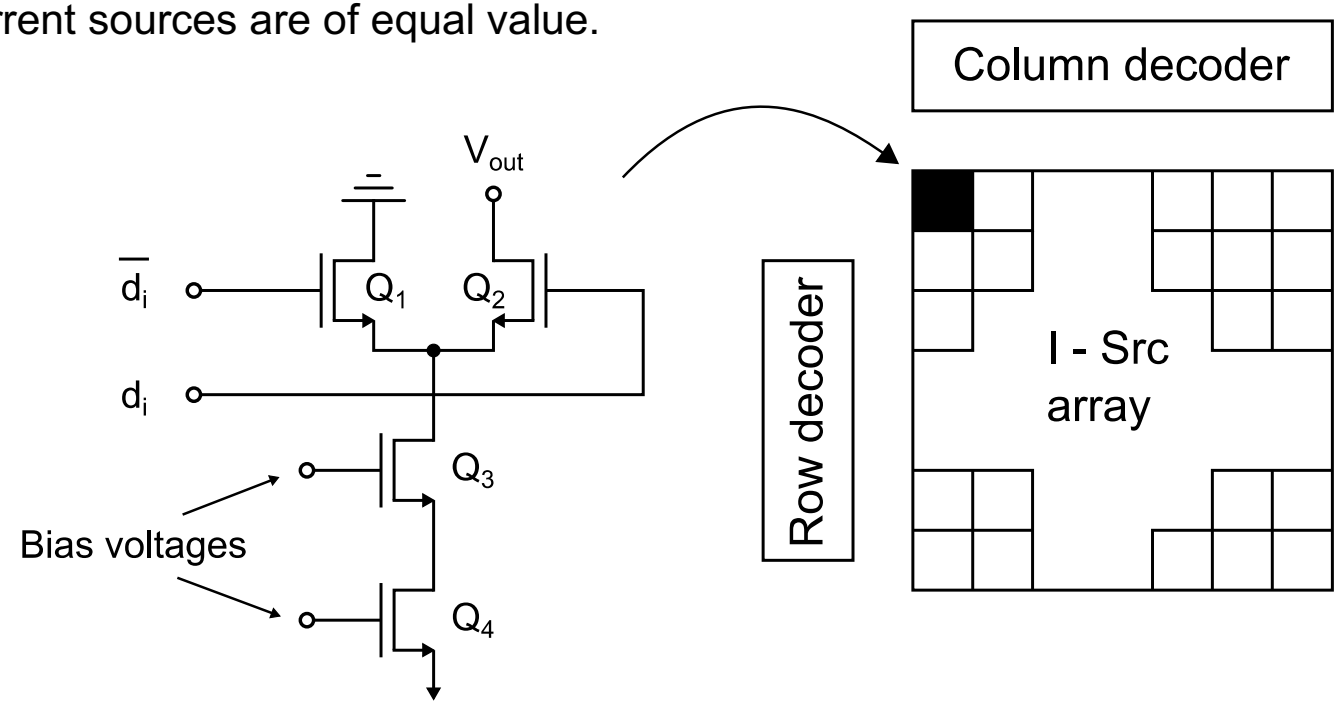


(a) (b)

Conversion of output current of an array to voltage using (a) a resistor on (b) a transimpedance amplifier.

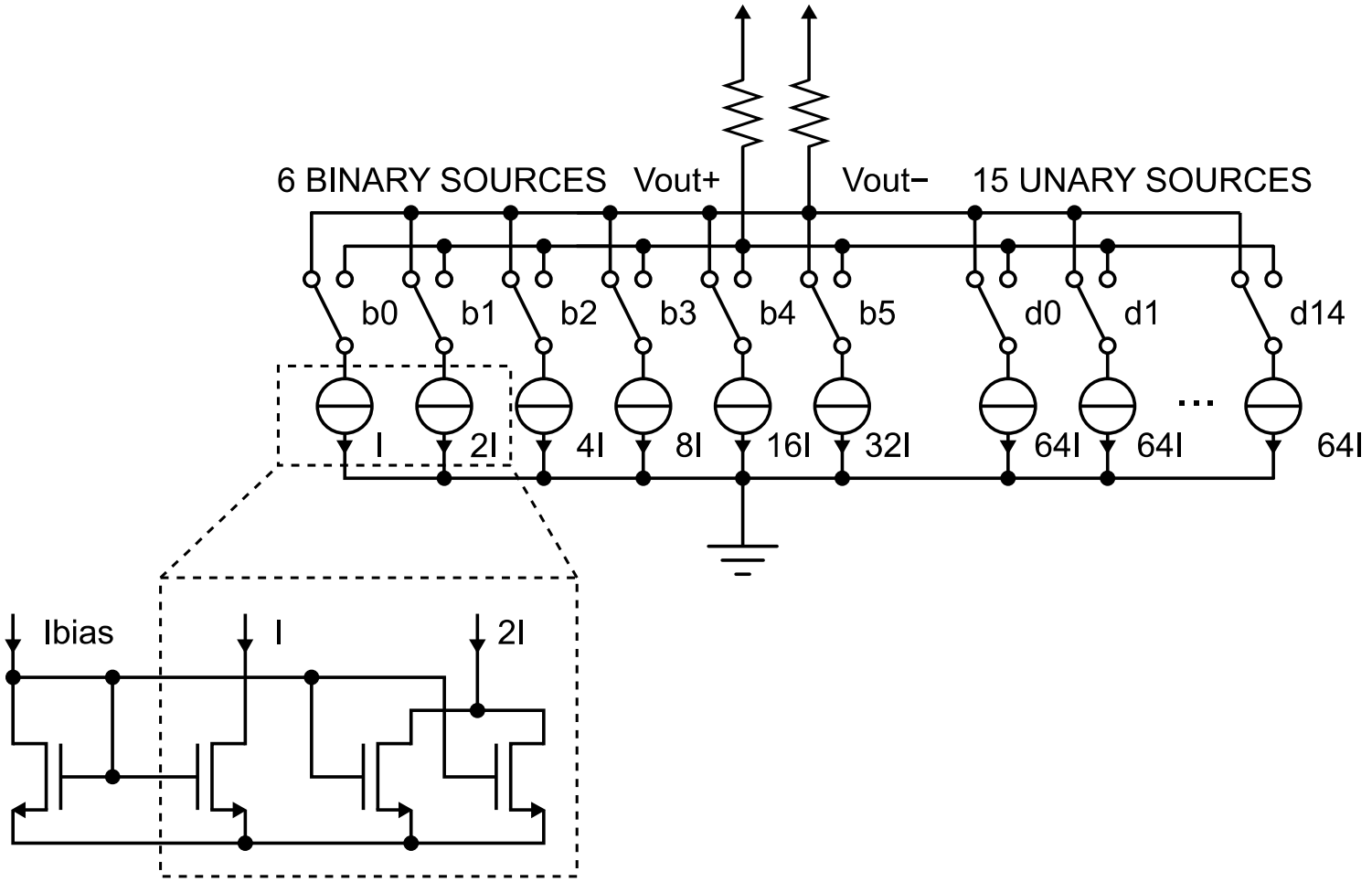


All current sources are of equal value.



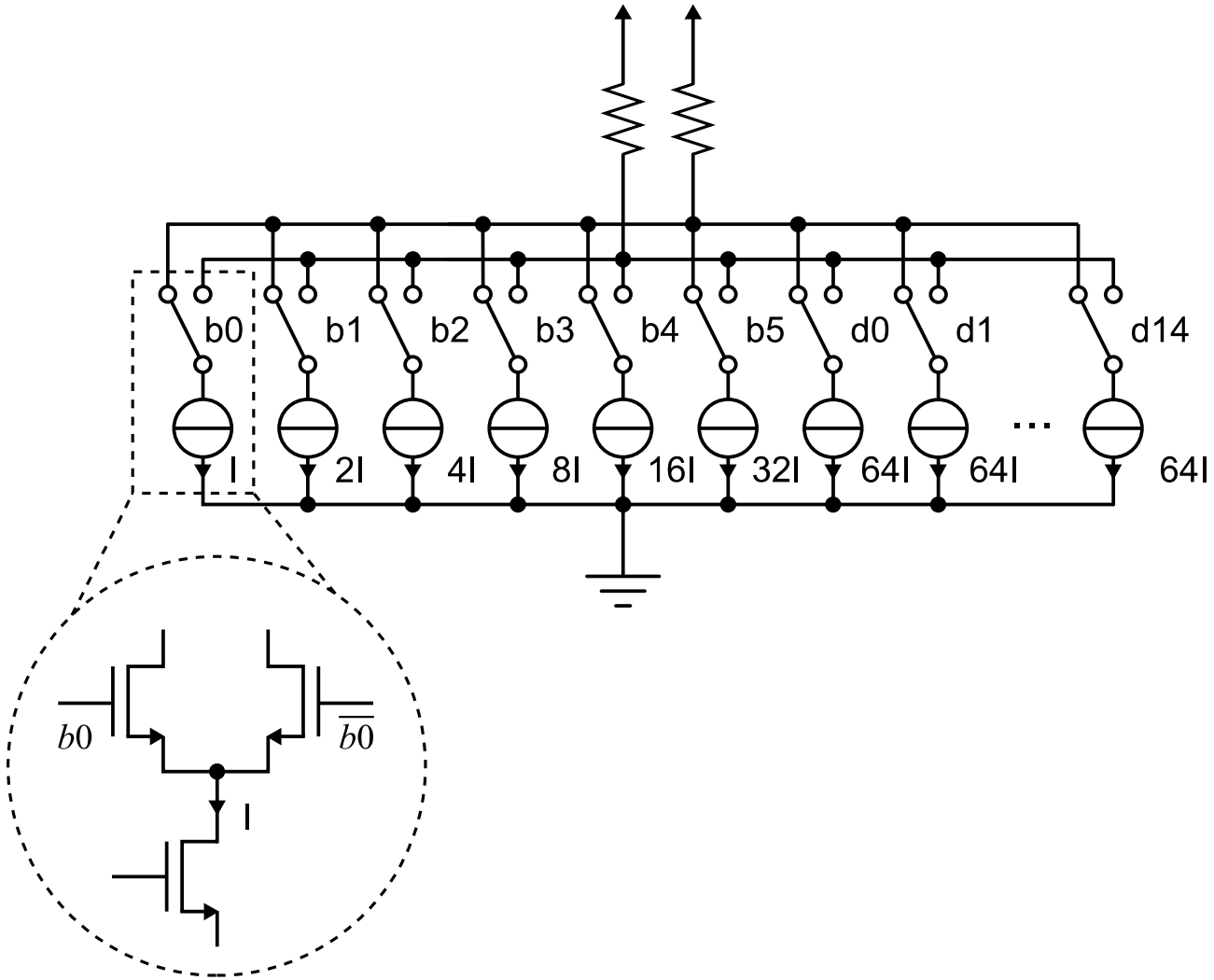
Thermometer-code current-mode D/A converter. Q_1 and Q_2 form the current switch, whereas Q_3 and Q_4 implement a cascode current source.

10-bit current-steering DAC



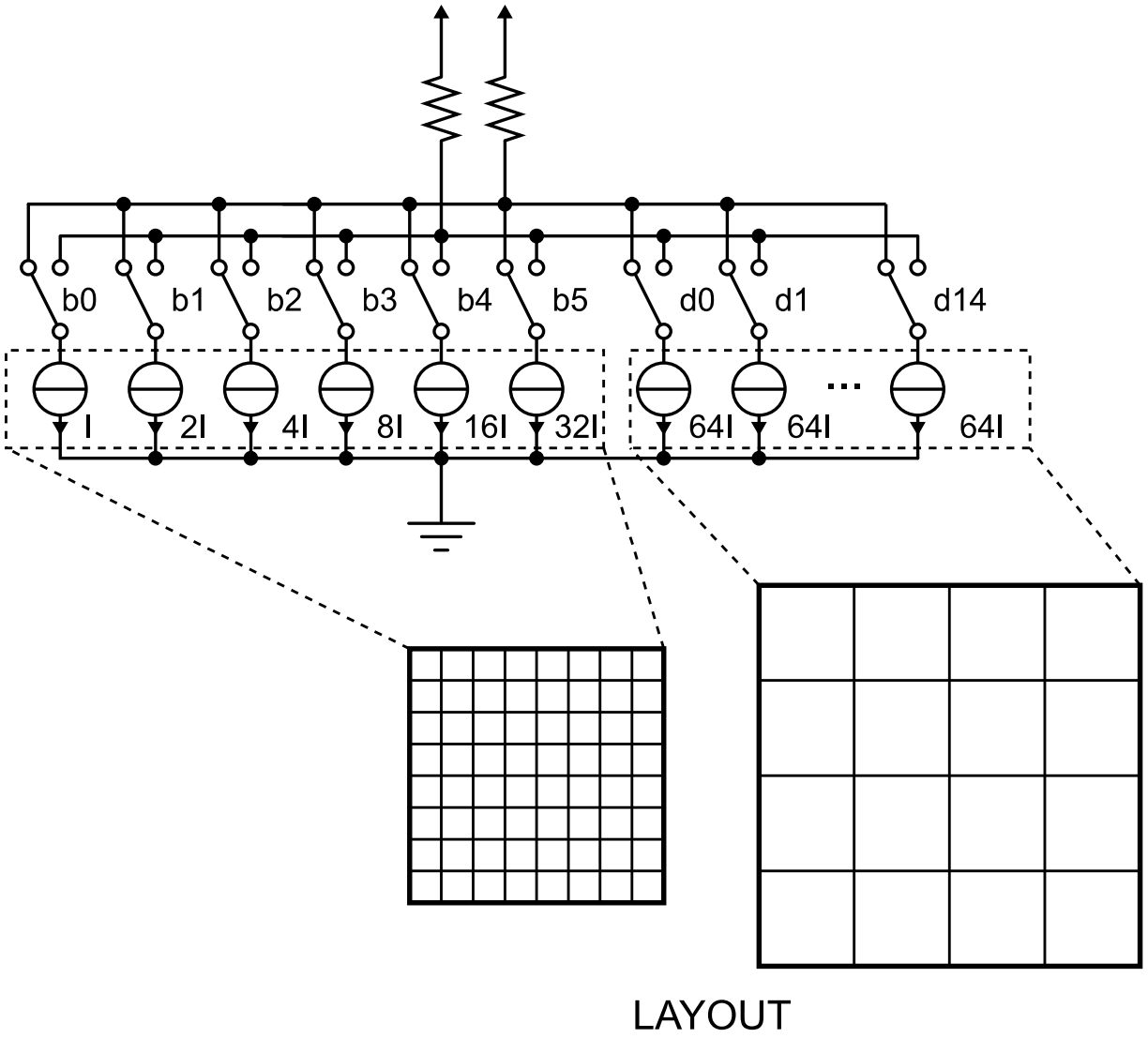
- Currents steered to output by switches controlled by digital input
- Signal current driven to load resistors
- LSBs binary weighted
- MSBs unary
  - Largest current source size and worst glitch energy reduced
- MSB bits has to be thermometer decoded
  - Decoder makes structure more complicated and consumes power and area
- Current sources constructed of unit transistors
- Biasing voltage generated from external bias current with current mirror

Current switches



- Current switches are simple source coupled pairs
- Controlling signals can be pure digital signals (input bit and its inversion)
  - Usually switches are not driven from rail to rail because quite small differential voltage is adequate
- Controlling signal generation and synchronization a key to good performance
  - Imperfect synchronization causes glitches and harmonic distortion
  - Synchronization usually done by flip-flops or latches
  - Flip-flop outputs must be buffered to achieve fast transitions
    - Sturdy inverters driving switch gates

Current source construction



LAYOUT

- Unit sources in common centroid layout to compensate for process and temperature variations on chip
  - Odd order gradients cancelled perfectly
  - Effect of even order gradients reduced by using more units
  - Unit placement and switching sequence affects INL
- MSB matrix large to improve matching
- Usage of two or more matrixes reduce the amount of units making implementation easier
- Matrixes and their bias currents have to be matched
  - Mismatch cause non-linearity

Random errors

- For a D/A converter to be fully functional, INL error has to be smaller than ½ LSB (least significant bit)

- Direct relationship exists between INL error and matching properties of used technology expressed by the relative unit current source standard deviation $\sigma(I_{LSB})/I_{LSB}$

- Parameter determines dimensions of current sources of D/A converter

$$W_{LSB}L_{LSB} = \frac{A_\beta^2}{\frac{2\sigma^2(I_{LSB})}{I_{LSB}^2}} + \frac{4A_{VT}^2}{\frac{2\sigma^2(I_{LSB})}{I_{LSB}^2}(V_{GS}-V_T)^2}$$

- Where A_β and A_{VT} are technological parameters, $(V_{GS}-V_T)$ gate overdrive voltage of current source and $\sigma(I_{LSB})/I_{LSB}$ unit current source relative standard deviation

- Convenient criterion to determine gate override voltage of current source transistor is to make two mismatches contributing about equal

Random errors

- Assuming that each unit current source has a value that follows a normal distribution, required accuracy is

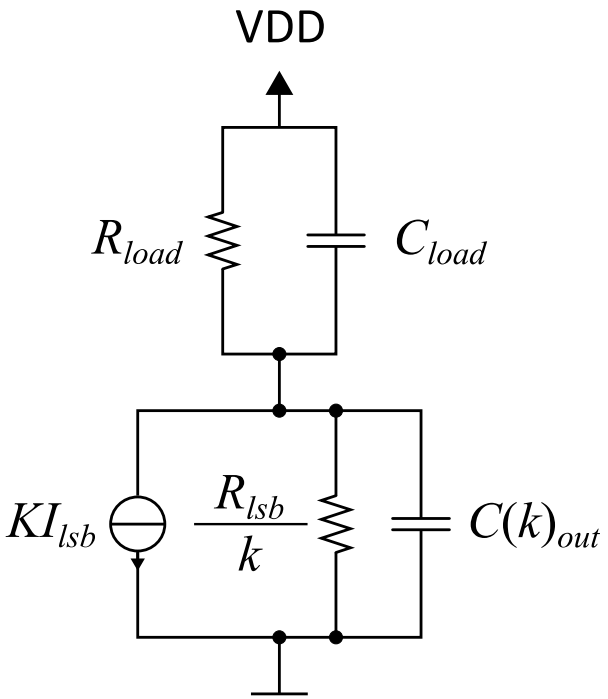
$$\frac{\sigma(I_{LSB})}{I_{LSB}} = \frac{1}{2C\sqrt{2^N - 1}}$$

where C depends only on yield requirement and N is number of bits.

- Or partially segmented architectures, INL performance is dependent on segmentation level

→ Monte Carlo simulations are therefore used to estimate INL yield as a function of unit current source standard deviation

Small signal model of D/A converter



- Output current is

$$I_{out} = \frac{I_{lsb}}{\frac{1}{k} + \frac{Z_{load}}{Z_{lsb}}}$$

where k is the digital code, Rload is the load resistance, Cload is the load capacitance, Rlsb is the LSB current source resistance, Cout is the parasitic capacitance, and Ilsb is the LSB current.

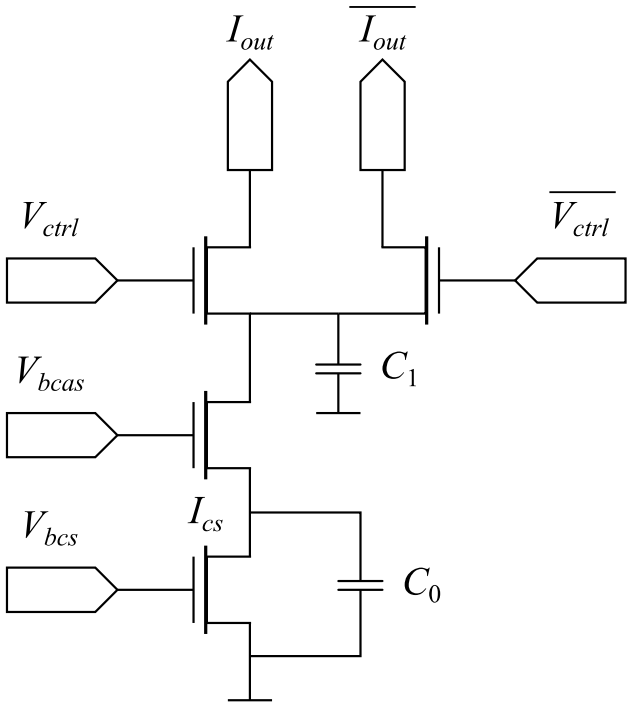
- If Z_{LSB} finite, I_{out} is a non-linear function causing harmonic distortion

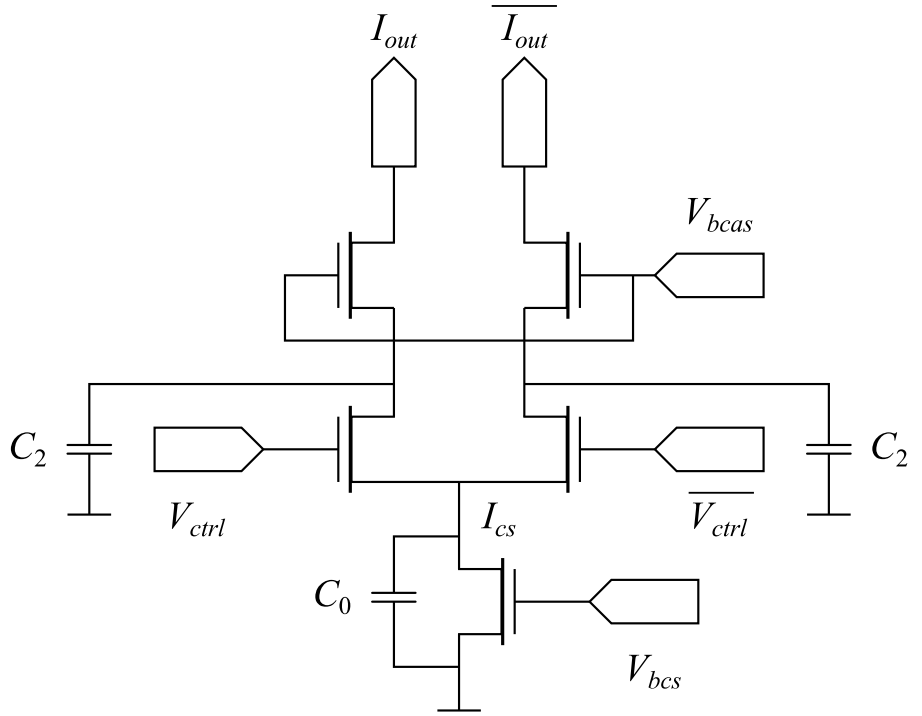
- Output current does not depend linearly on digital input code, when output impedance is finite

$$INL_{se}(k) = \frac{\frac{kZ_{load}}{1+\frac{kZ_{load}}{Z_{lsb}}} - \frac{kZ_{load}}{1+\frac{Z_{load}(2^N-1)}{Z_{lsb}}}}{\frac{Z_{load}}{1+\frac{Z_{load}(2^N-1)}{Z_{lsb}}}} I_{lsb} = \frac{Z_{load}}{Z_{lsb}} k(2^N - 1 - k) I_{lsb}$$

, where N is the number of the bits.

Cascode transistor





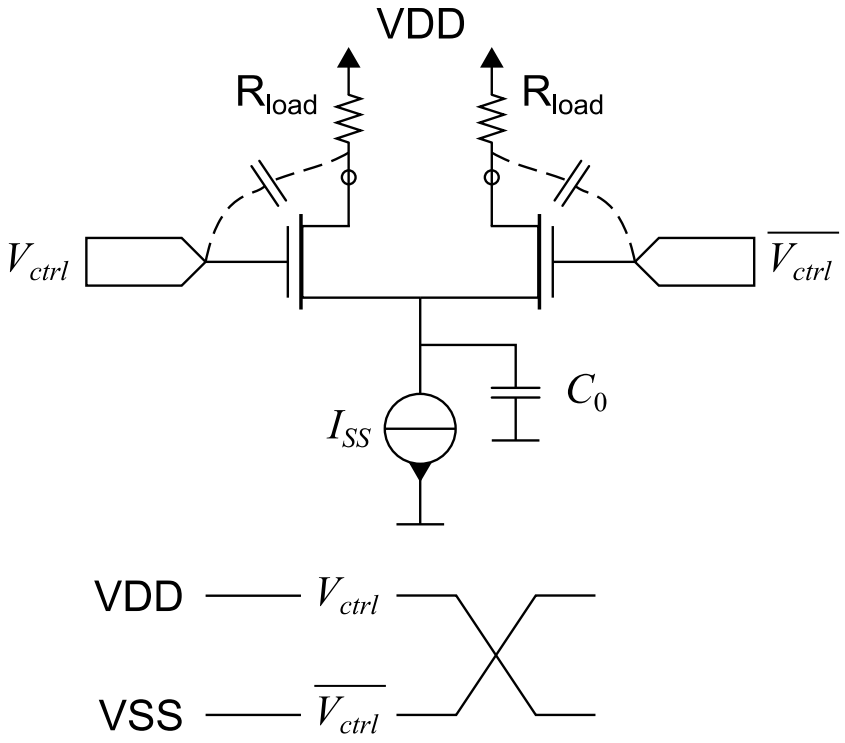
- Cascode transistor multiplies current source output impedance by their gain

- Other advantage is that cascode transistors isolate the current switches and current sources

- Two cascode transistors to enhance output impedance → additional bias voltage and reduces output voltage range

- Cascode transistors could also be added between current switches and output

Glitches reduction



A key aspect of performance of D/A converter is output glitch, which is mainly due to following effects:

1) Imperfect synchronization of control signals of current switches

→ D flip-flop or latch placed symmetrically near switches, switch drivers load matching

2) Charge and discharge of parasitic capacitances associated with current sources

→ C_0 is minimized by layout techniques and using cascode devices

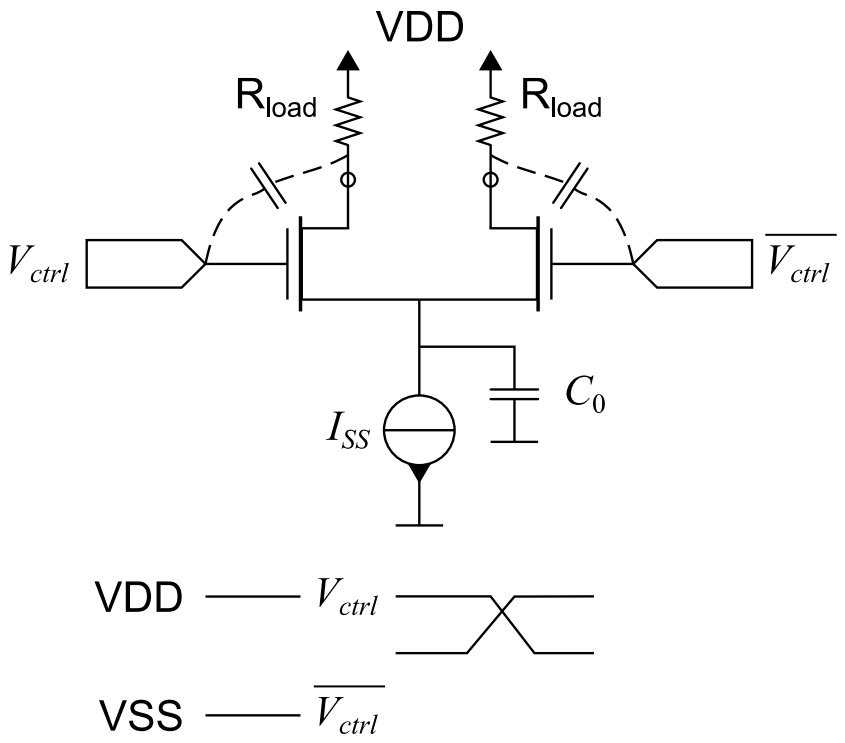
3) Feedthrough of digital input data to output

→ Low swing signals minimize capacitively coupled switching noise, dummy switches

4) Switching transistors being simultaneously in off state

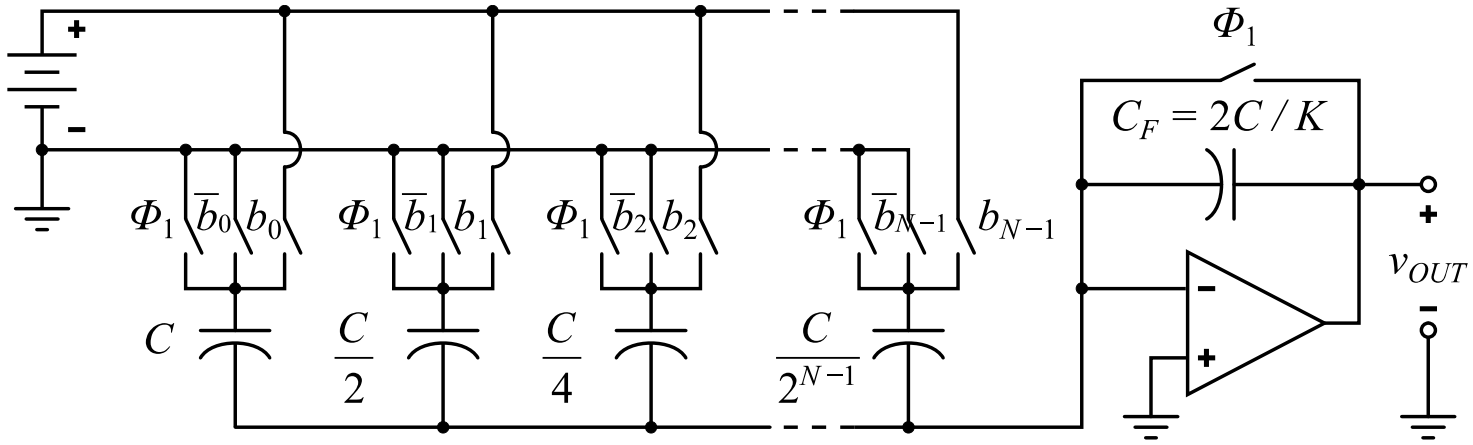
→ high crossing point signals guarantee both switch transistors do not turn off at the same time

Glitches reduction



- If both switching transistors are turned off, output node of the current source will rapidly discharge and current source will turn off
- To recover from this condition, current source must progress through the linear region and back into saturation
- The situation can, however, be improved by setting the crosspoint of the control signals at the optimum high level
- D/A converter output could be reduced by restricting the control voltage swing
- Because switches source voltage follows during the transitions control voltage (not linearly), it is possible to reduce this variation by decreasing control voltage swing
- Code dependent power supply and clock jitter → adding dummy switch drivers and switches

Binary-weighted, charge amplifier DAC implementation



1. DAC is essentially a binary-weighted charge amplifier
2. During the ϕ_1 clock phase, all capacitors are discharged to zero volts
3. Capacitors are autozeroed. During the ϕ_2 clock phase, the switch labeled b_i or $\overline{b}_i$ is closed
4. Polarity is changed by reversing the polarity of V_{REF}
5. No floating nodes
6. No terminating capacitor to make the sum equal to 2C
7. Speed limited by the op amp

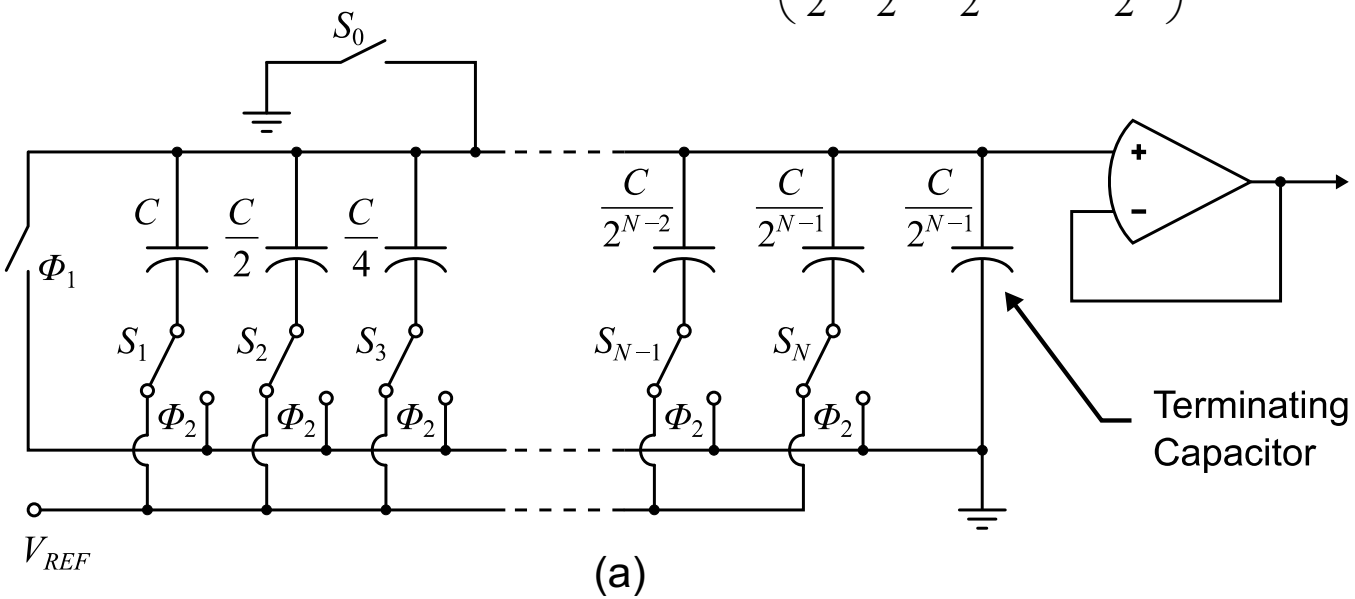
$$v_{OUT} = \frac{-K}{2C}\left(b_0 C + \frac{b_1 C}{2} + \frac{b_2 C}{2} + \cdots + \frac{b_{N-1} C}{2^{N-1}}\right) V_{REF}$$

$$= -K\left(\frac{b_0}{2} + \frac{b_1}{4} + \frac{b_2}{8} + \cdots + \frac{b_{N-1}}{2^N}\right) V_{REF}$$

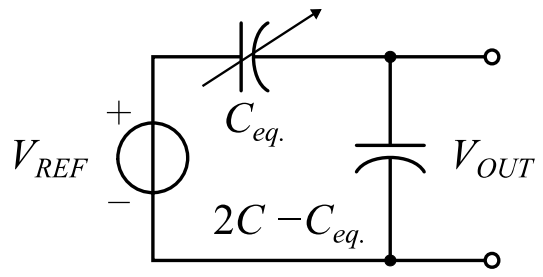
$$(V_{ref} - V_{OUT})C_{eq} = (C_{TOT} - C_{eq}) \cdot V_{OUT}$$

$$V_{REF}C_{eq} = V_{REF}\left(b_1 C + \frac{b_2 C}{2} + \frac{b_3 C}{2^2} + \cdots + \frac{b_N C}{2^{N-1}}\right) = C_{tot}V_{OUT} = 2CV_{OUT}$$

$$V_{REF}\left(\frac{b_1}{2} + \frac{b_2}{2^2} + \frac{b_3}{2^3} + \cdots + \frac{b_N}{2^N}\right) = V_{OUT}$$



(a)



(b)

(a) Charge-scaling D/A converter. Switches S_i close to V_{ref} if b_i = 1 or ground if b_i = 0 during Φ_2. All switches are connected to ground during Φ_1.

(b) Equivalent circuit of (a).

$$C_{MAX} = C - \Delta C$$
$$C_{MIN} = C - \Delta C$$

Worst-case output for the *i*th capacitor

$$v_{out}(actual) = \frac{(C \pm \Delta C)/2^{i-1}}{2C} V_{REF} = \frac{V_{REF}}{2^i} \pm \frac{\Delta C \cdot V_{REF}}{2^i C} = \frac{2^N}{2^i} \pm \frac{2^N \Delta C}{2^i C} LSBs$$

The *INL* for the *i*th-bit is give as

$$INL(i) = v_{out}(actual) - v_{out}(ideal) = \frac{\pm 2^N \Delta C}{2^i C} = \frac{\pm 2^{N-i} \Delta C}{C} LSBs$$

The worst-case occurs for i=1

$$INL = \pm 2^{N-1} \frac{\Delta C}{C} LSBs$$

The worst-case DNL for the binary-weighted capacitor arrays is found when the MSB changes.

$$v_{OUT} = \frac{C_{eq}}{(2C - C_{eq}) + C_{eq}} v_{REF}$$

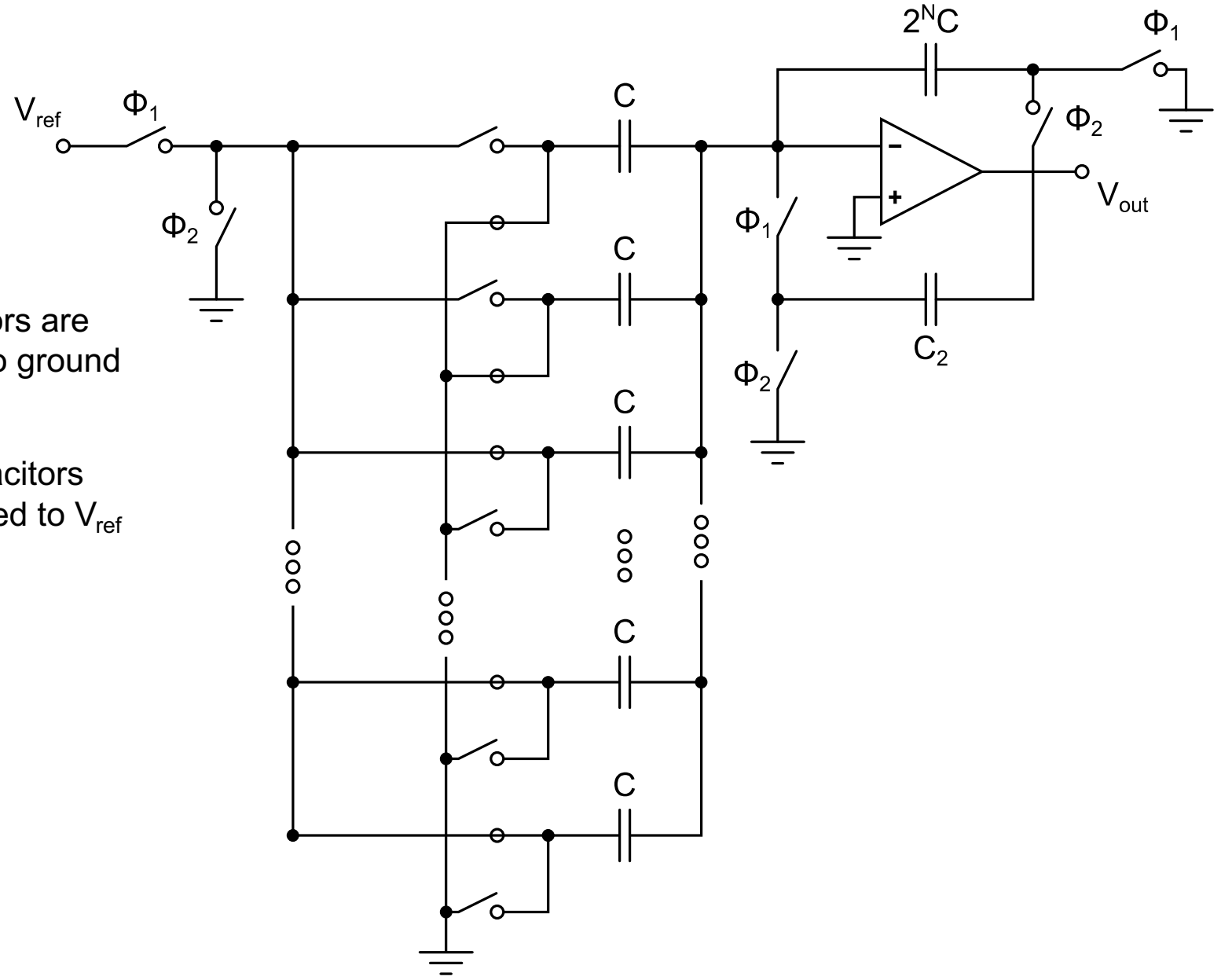
C_{eq} represents the capacitors whose bits are 1 and (2C-C_{eq}) represents the capacitors whose bits are 0. The worst-case DNL can be expressed as

$$DNL = \frac{v_{step}(\text{worst case})}{v_{step}(\text{ideal})} - 1 = \frac{v_{OUT}(1000....) - v_{OUT}(0111....)}{LSB} - 1$$

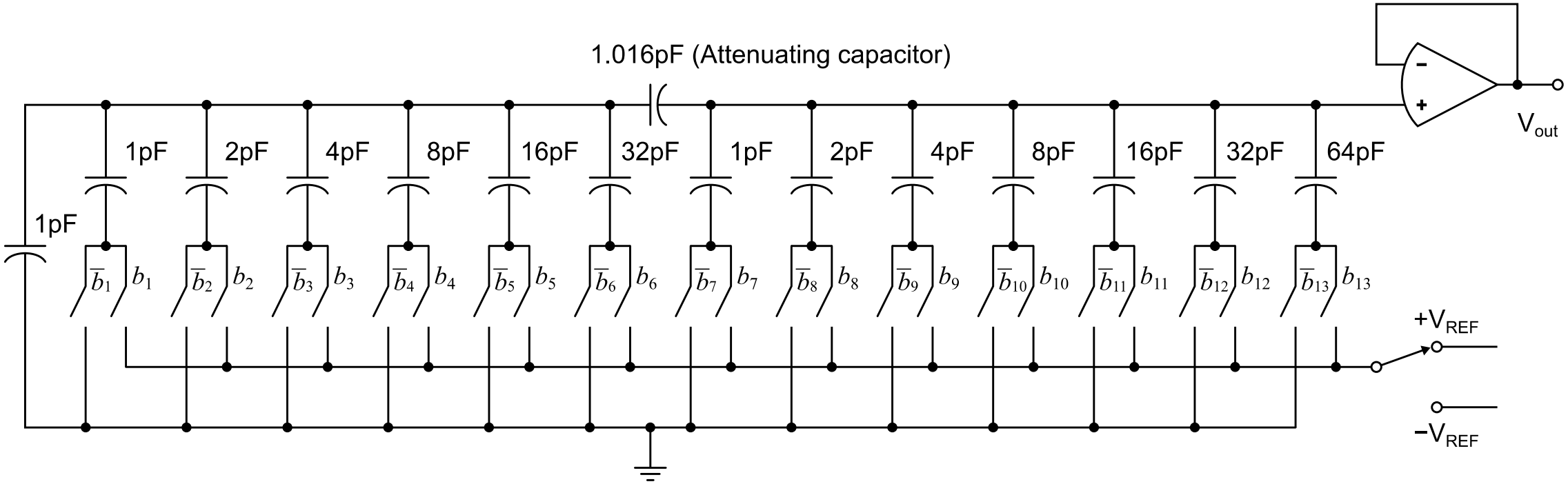
$$= \frac{\left(\frac{C + \Delta C}{(C + \Delta C) + (C - \Delta C)}\right) v_{REF} - \left(\frac{(C + \Delta C)\left(1 - \frac{2}{2^N}\right)}{(C + \Delta C) + (C - \Delta C)}\right) v_{REF}}{\frac{v_{REF}}{2^N}} - 1 = 2^N \left(\frac{C + \Delta C}{2C}\right) - 2^N \left(\frac{C - \Delta C}{2C}\right)\left(1 - \frac{2}{2^N}\right) - 1 = \left(2^N - 1\right)\frac{\Delta C}{C} LBSs$$

Top capacitors are connected to ground

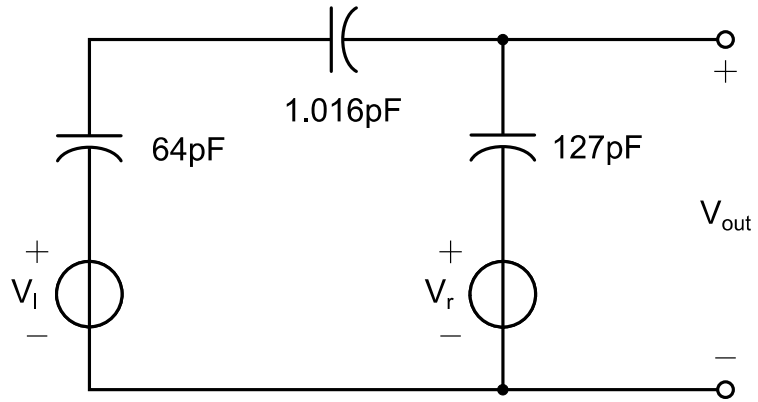
Bottom capacitors are connected to V_{ref}



Thermometer-code charge-redistribution D/A converter.

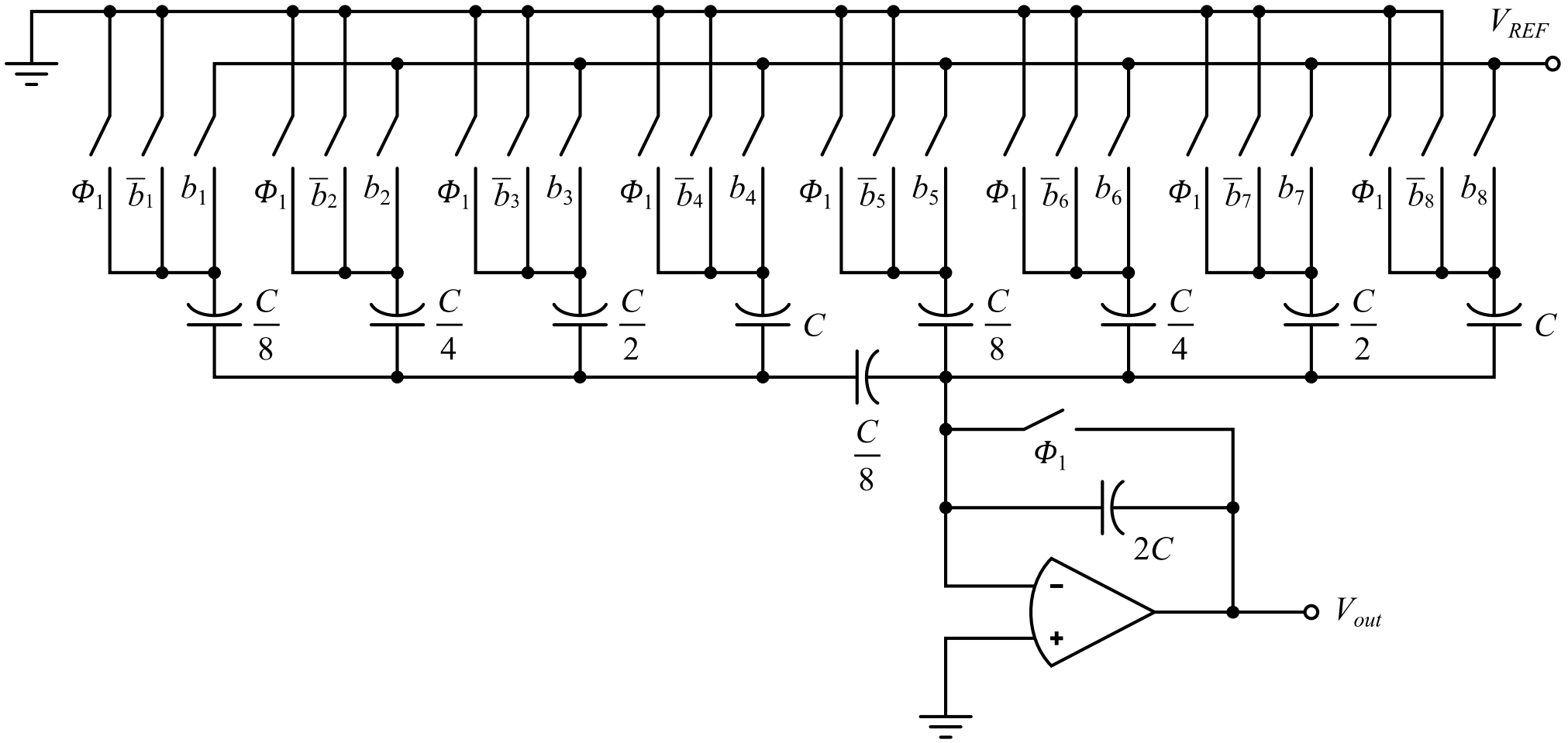


A 13-bit two-stage MDAC. Note that whether or not the ϕ_2 switches close depends upon the state of the binary variable, b_1.



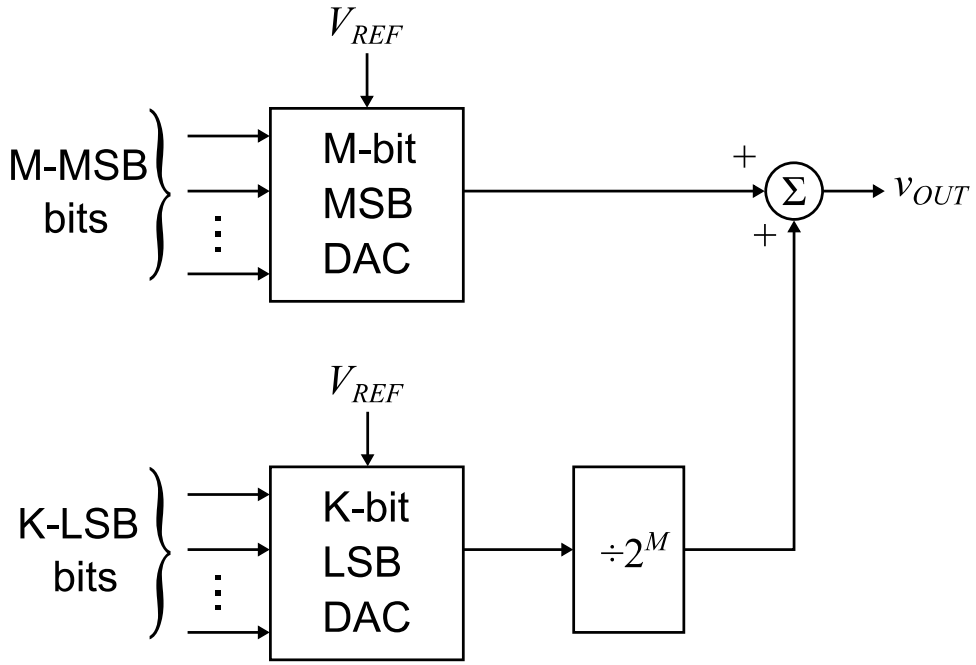
(b)

An equivalent circuit of (a).



A charge-scaling D/A converter that is insensitive to nodal-capacitive parasitics.

Combining of M-bit and K-bit subDAC to form an M+K-bit DAC

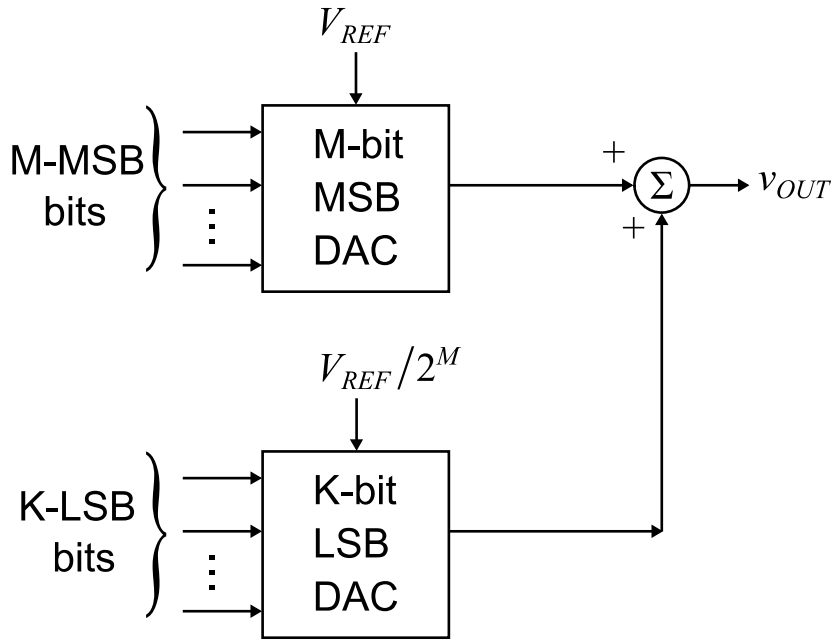


$$v_{OUT} = \left(\frac{b_0}{2} + \frac{b_1}{4} + \cdots + \frac{b_{M-1}}{2^M}\right)V_{REF} + \left(\frac{1}{2^M}\right)\left(\frac{b_M}{2} + \frac{b_{M+1}}{4} + \cdots + \frac{b_{M+K-1}}{2^K}\right)V_{REF}$$

or

$$v_{OUT} = \left(\frac{b_0}{2} + \frac{b_1}{4} + \cdots + \frac{b_{M-1}}{2^M} + \frac{b_M}{2^{M+1}} + \frac{b_{M-1}}{2^{M+2}} + \cdots + \frac{b_{M+K-1}}{2^{M+K}}\right)V_{REF}$$

Combining of M-bit and K-bit subDAC to form an M+K-bit DAC by dividing the V_{REF}

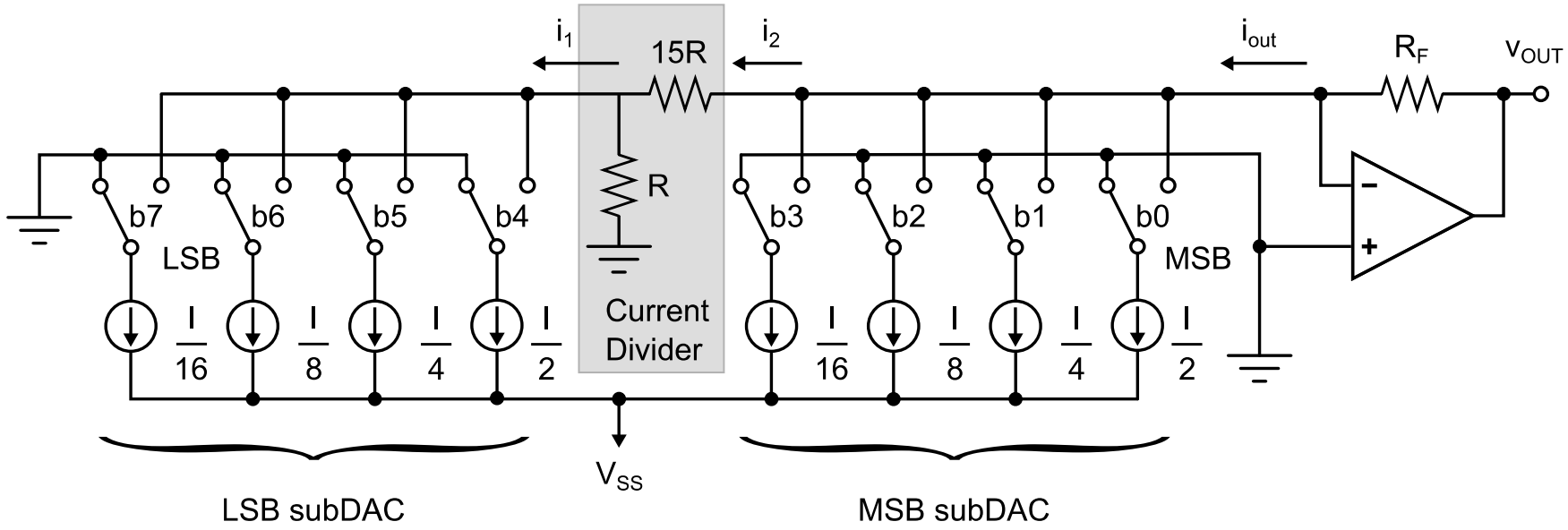


$$v_{OUT} = \left(\frac{b_0}{2} + \frac{b_1}{4} + \cdots + \frac{b_{M-1}}{2^M}\right)V_{REF} + \left(\frac{b_M}{2} + \frac{b_{M+1}}{4} + \cdots + \frac{b_{M+K-1}}{2^K}\right)\left(\frac{V_{REF}}{2^M}\right)$$

or

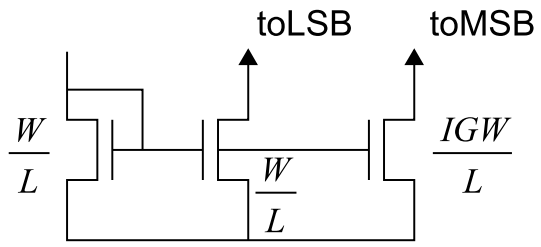
$$v_{OUT} = \left(\frac{b_0}{2} + \frac{b_1}{4} + \cdots + \frac{b_{M-1}}{2^M} + \frac{b_M}{2^{M+1}} + \frac{b_{M+1}}{2^{M+2}} + \cdots + \frac{b_{M+K-1}}{2^{M+K}}\right)V_{REF}$$

Combination of current scaling subDACs using a current divider

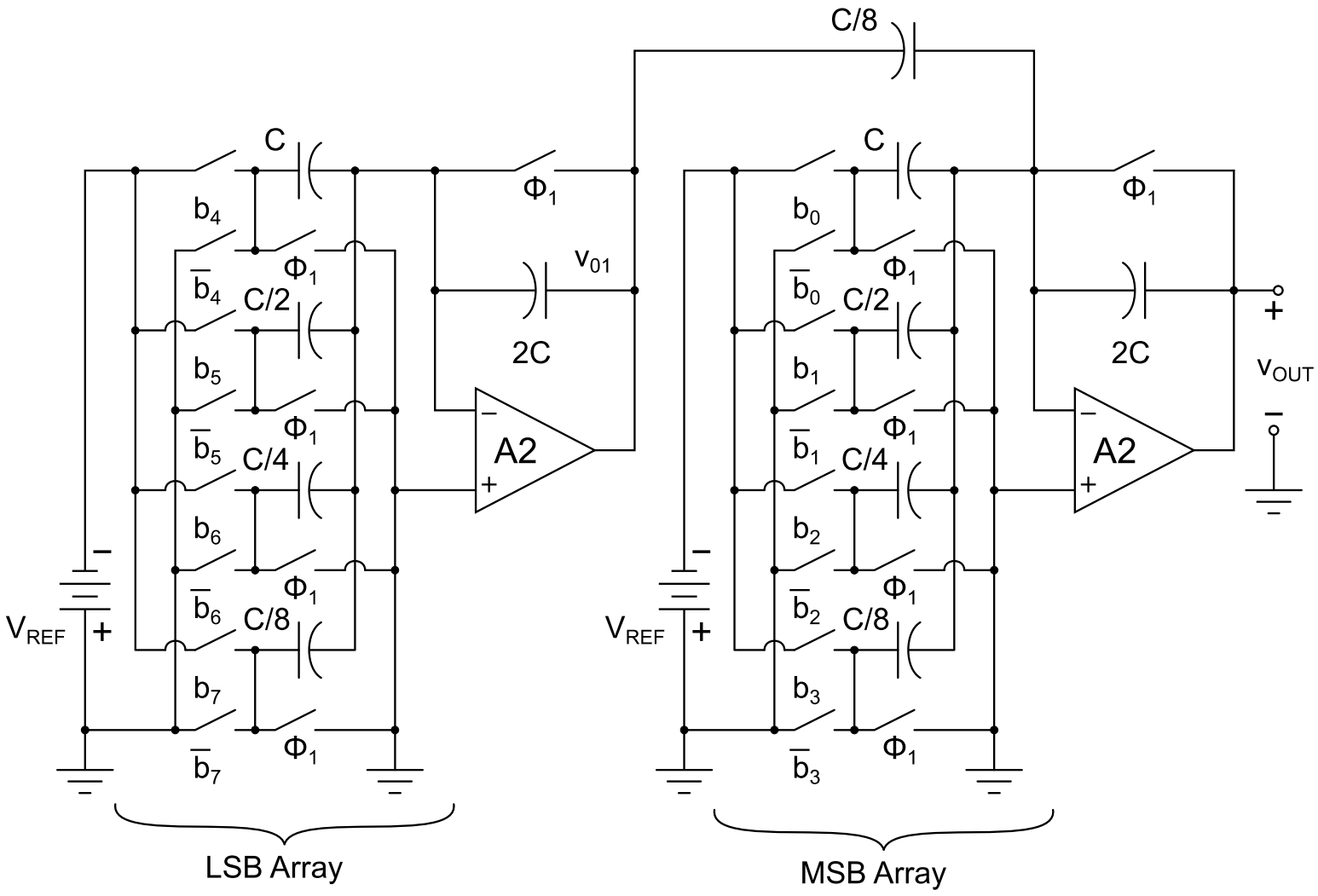


- current division by $\frac{R}{R+15R}$ for LSB subDAC
- waisted power

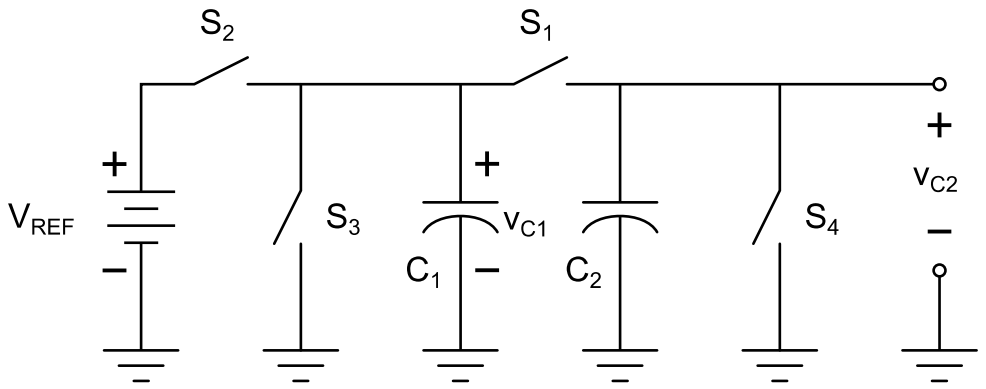
Use current multiplier between LSB and MSB current sources

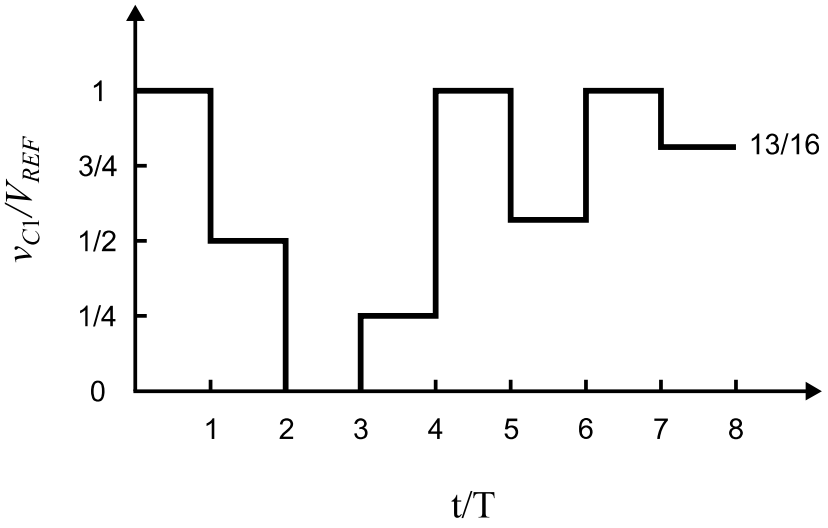


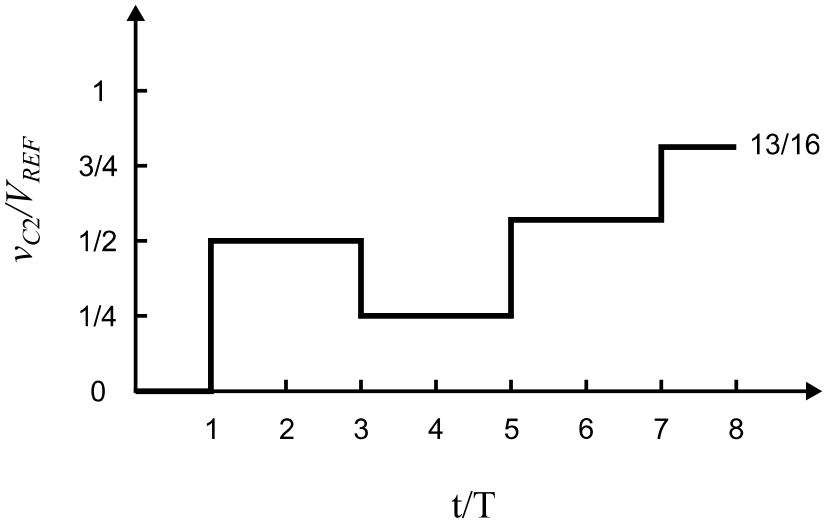
Combination of two 4-bit, binary-weighted, charge amplifier subDACs to form an 8-bit, binary-weighted



Operation of the serial charge-redistribution DAC







$$C_1 = C_2$$

$$b_0 = 1, b_1 = 1, b_2 = 0, b_3 = 1$$