ELEC-E3530

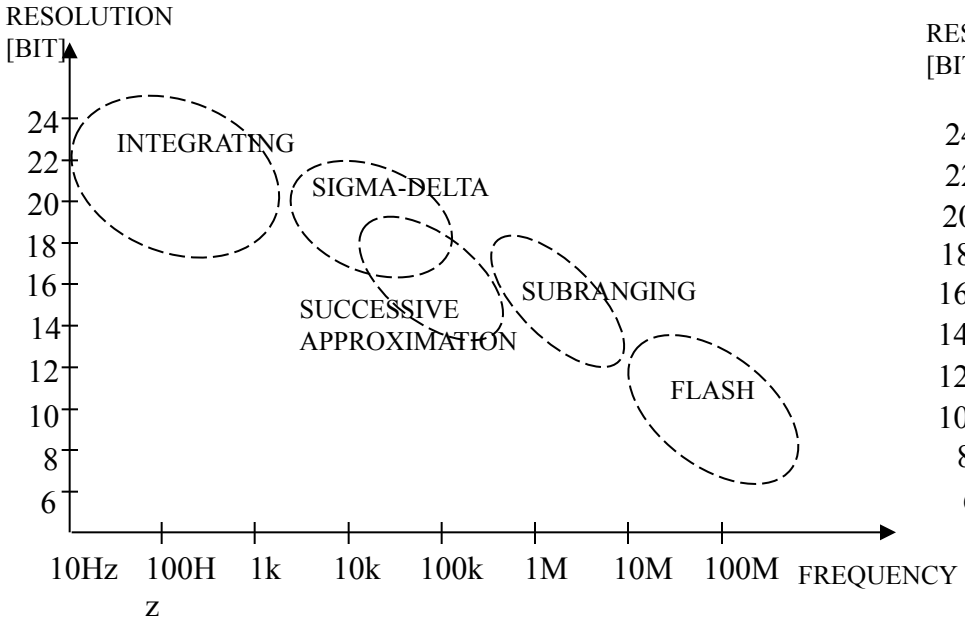
Integrated Analog Systems L9
Analog-to-Digital Converters

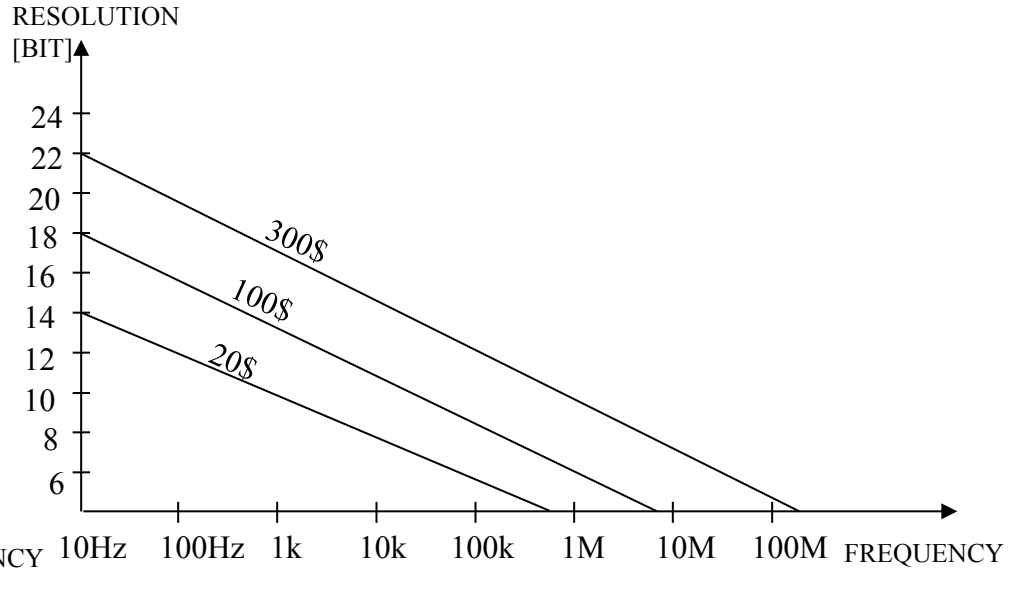
Basic Conversion Techniques

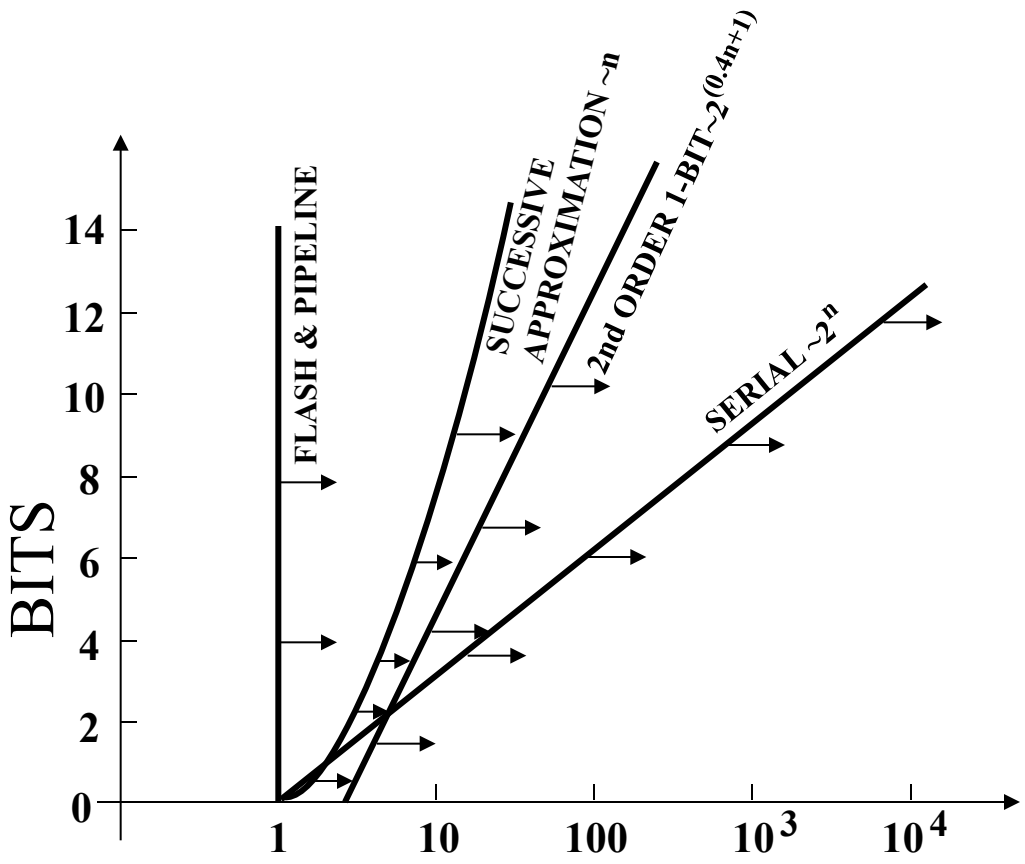
1. Serial Conversion
2. Successive Approximation Conversion
3. Parallel Conversion
4. Pipelined Converters
5. Sigma-delta

A/D Converters

Type	Speed	Resolution	Price
Integrating	0.1Hz…100Hz	18-25	5-500
Successive appr.	1kHz…100kHz	14-16	20-300
Sigma-delta	1kHz…50kHz	16-20	20-150
Subranging	100kHz…1MHz	12-16	150-500
Flash	1MHz…500MHz	6-10	100-500



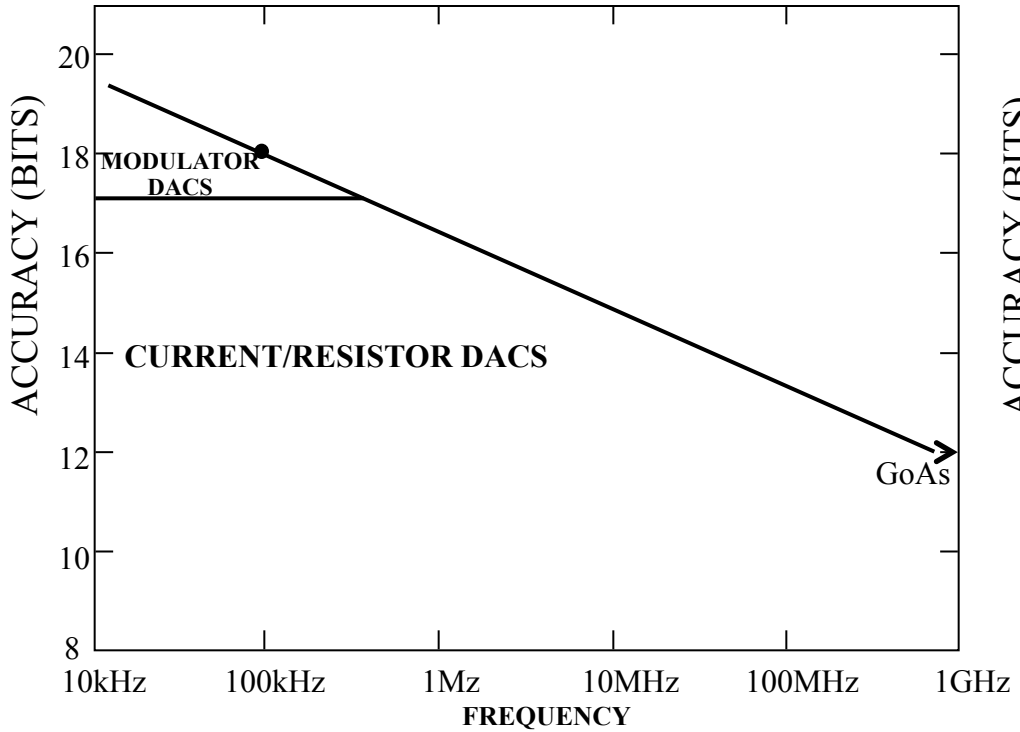




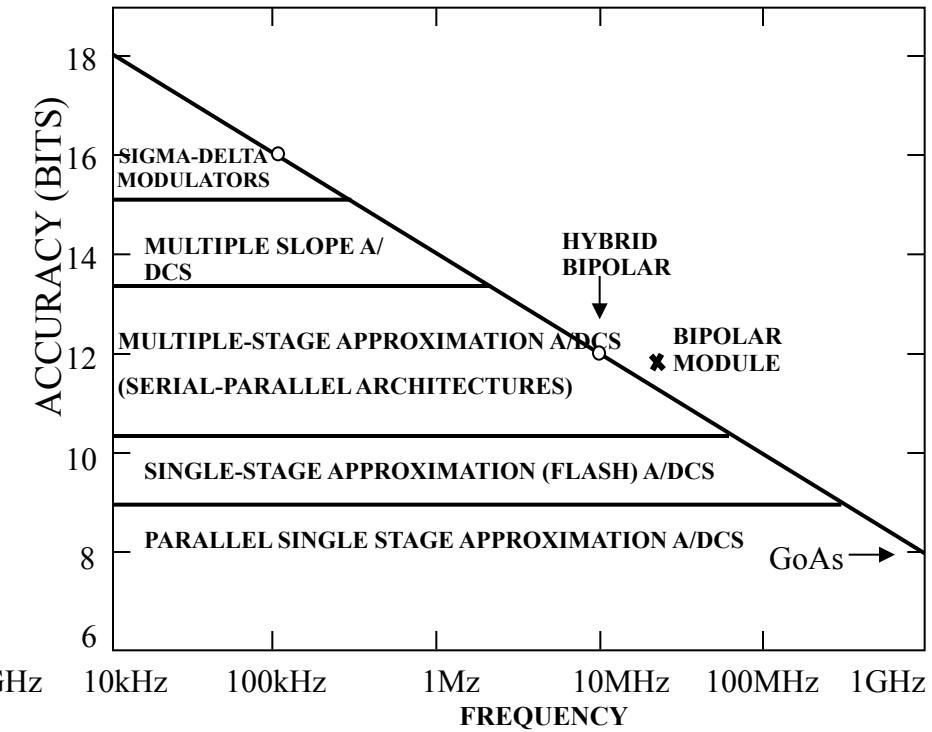
CLOCK INTERVALS

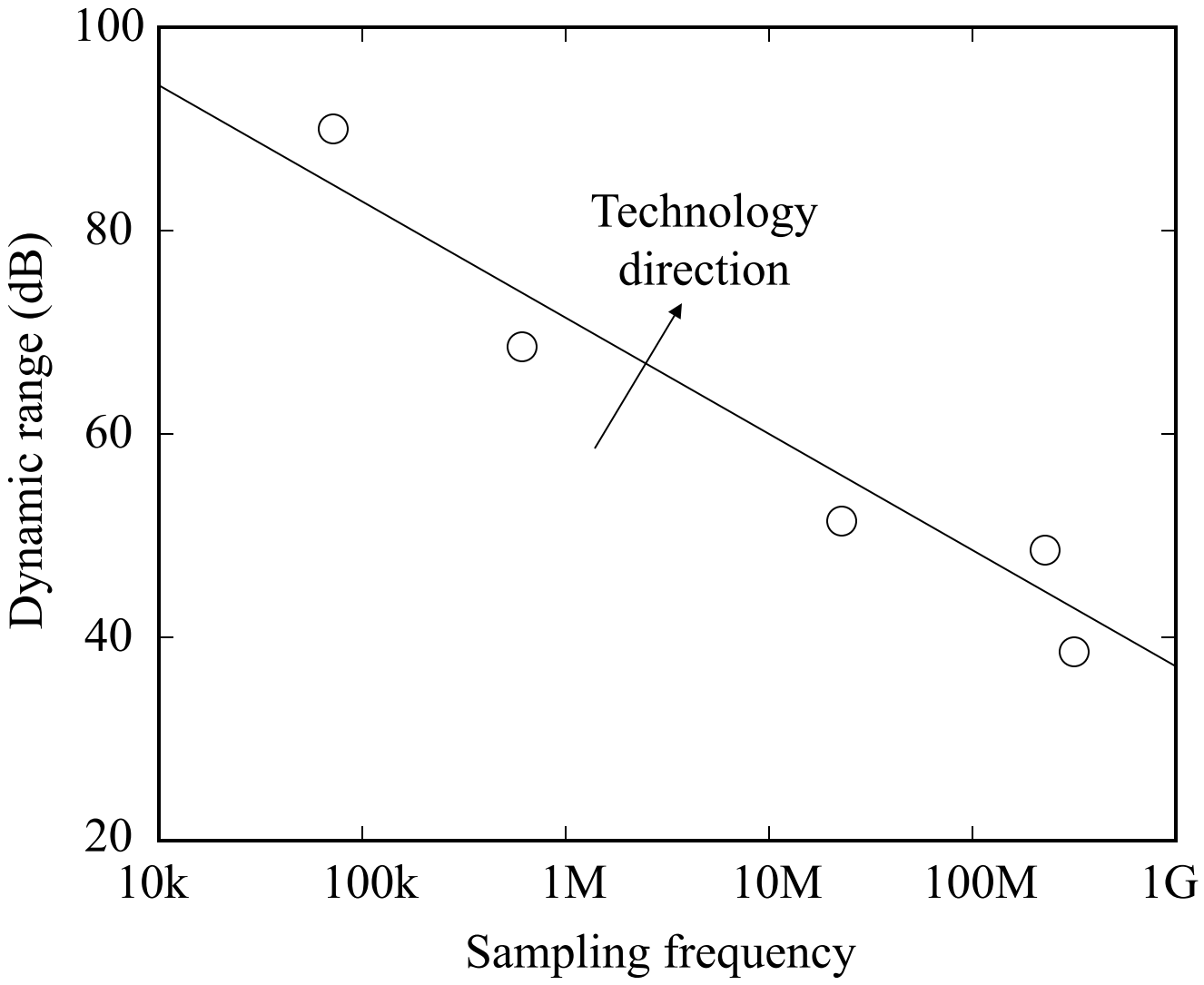
SAMPLE OUT

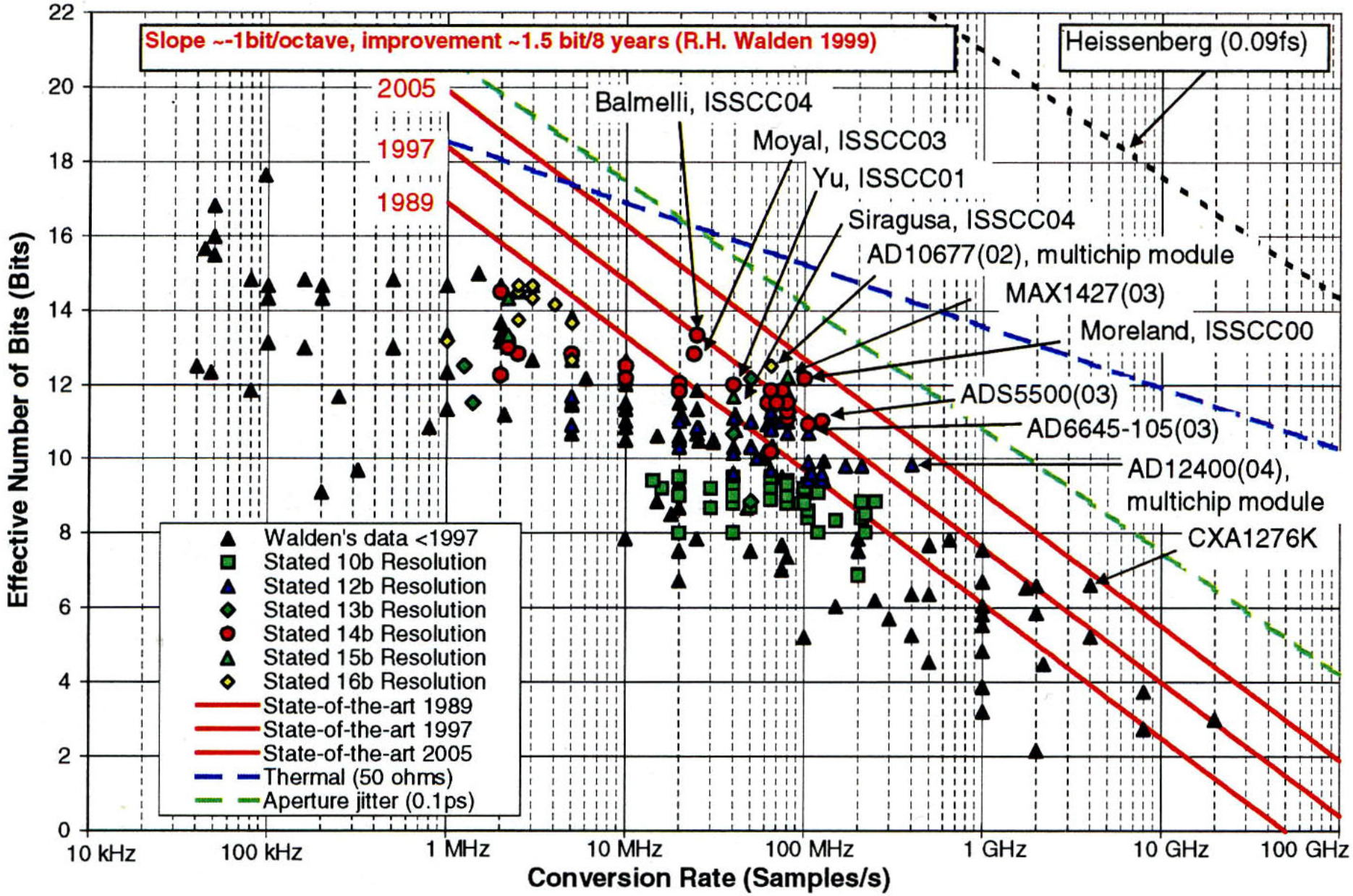
Frequency vs Accuracy Limits of Digital/Analog Converters (1989)



Frequency vs Accuracy Limits of Analog/Digital Converters (1989)




100
80
60
40
20
Dynamic range (dB)
Technology
direction
10k
100k
1M
10M
100M
1G
Sampling frequency



Survey of ADC's. Effective number of bits vs. sample rate.

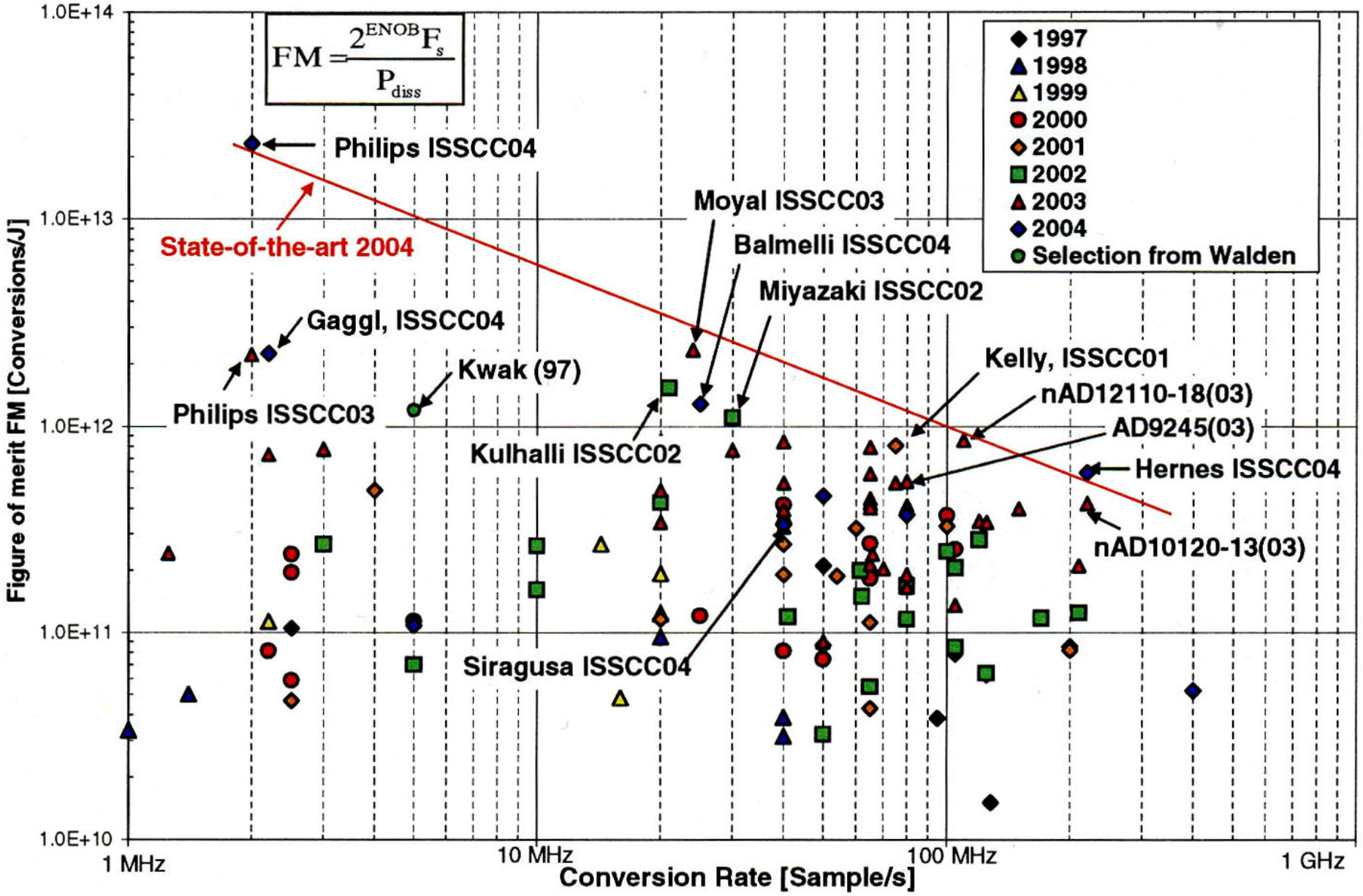
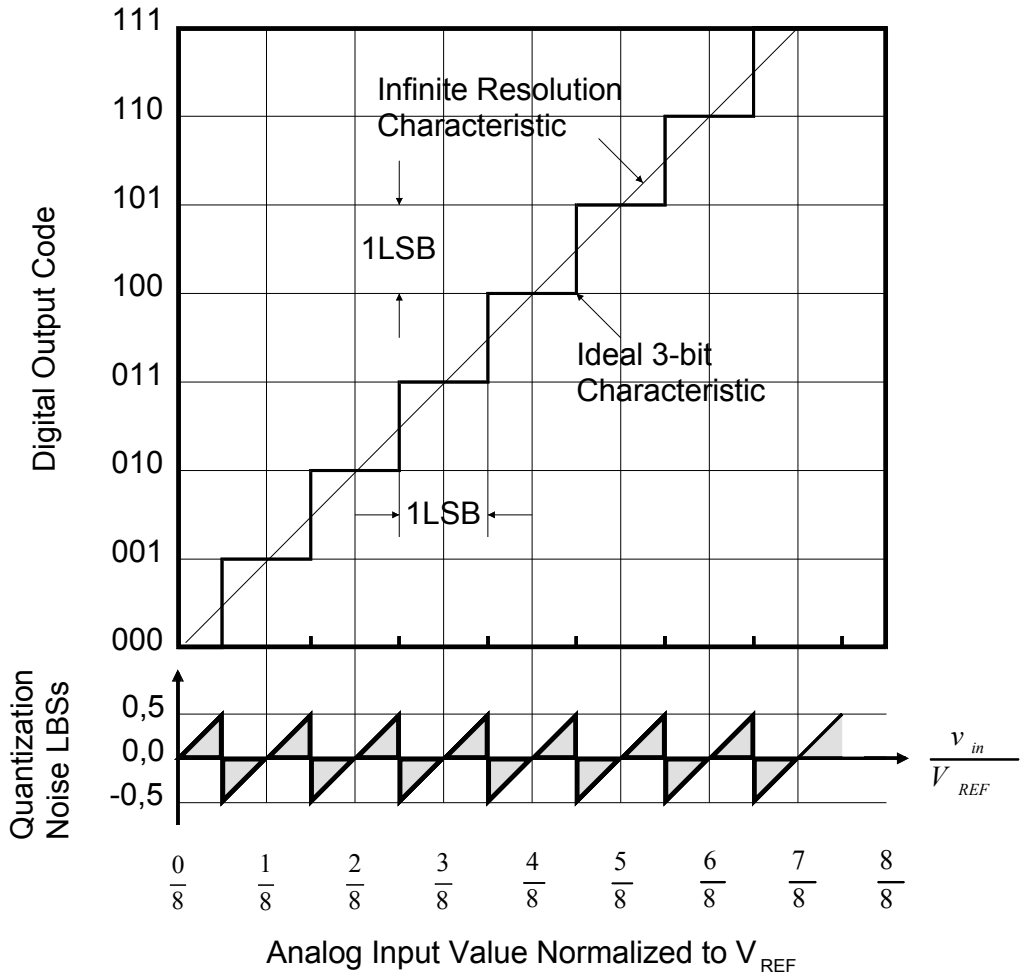


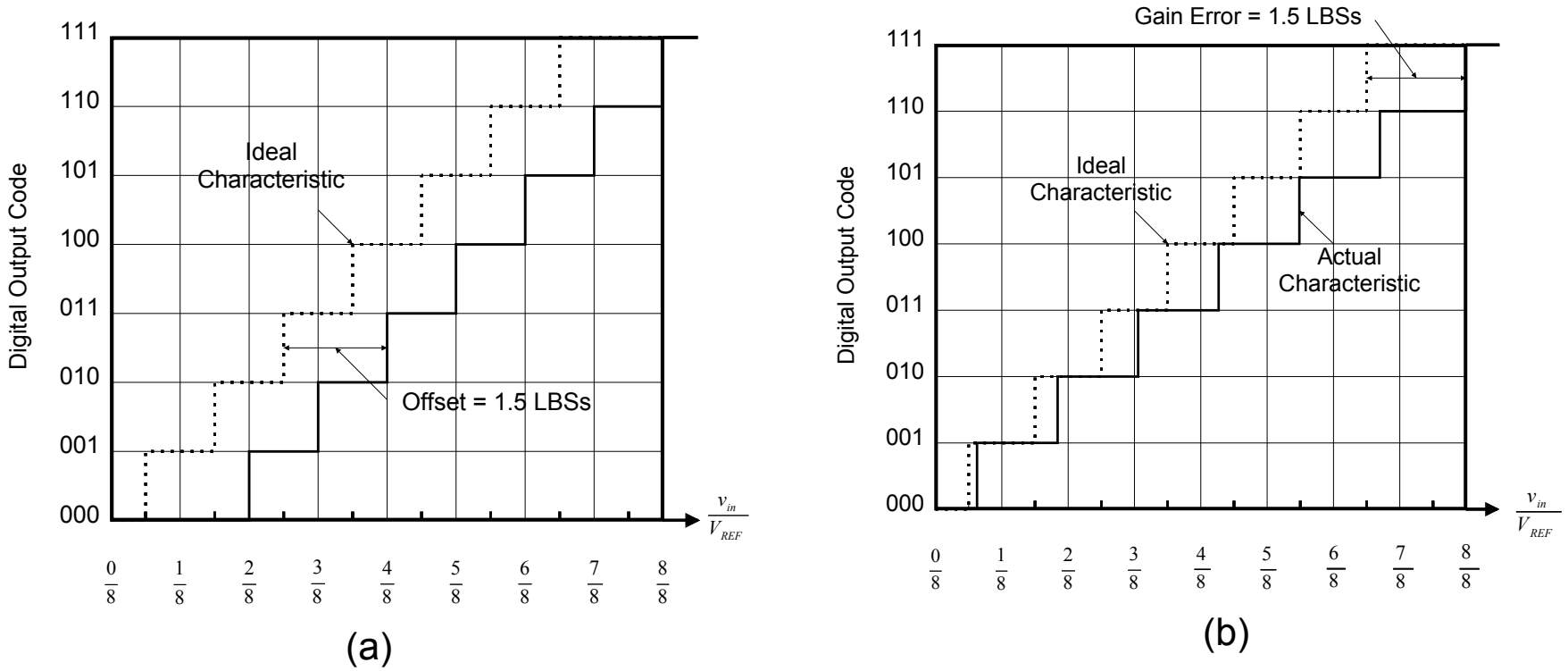
Figure of merit FM as a function of conversion rate.

Ideal input-output characteristic of a 3-bit ADC



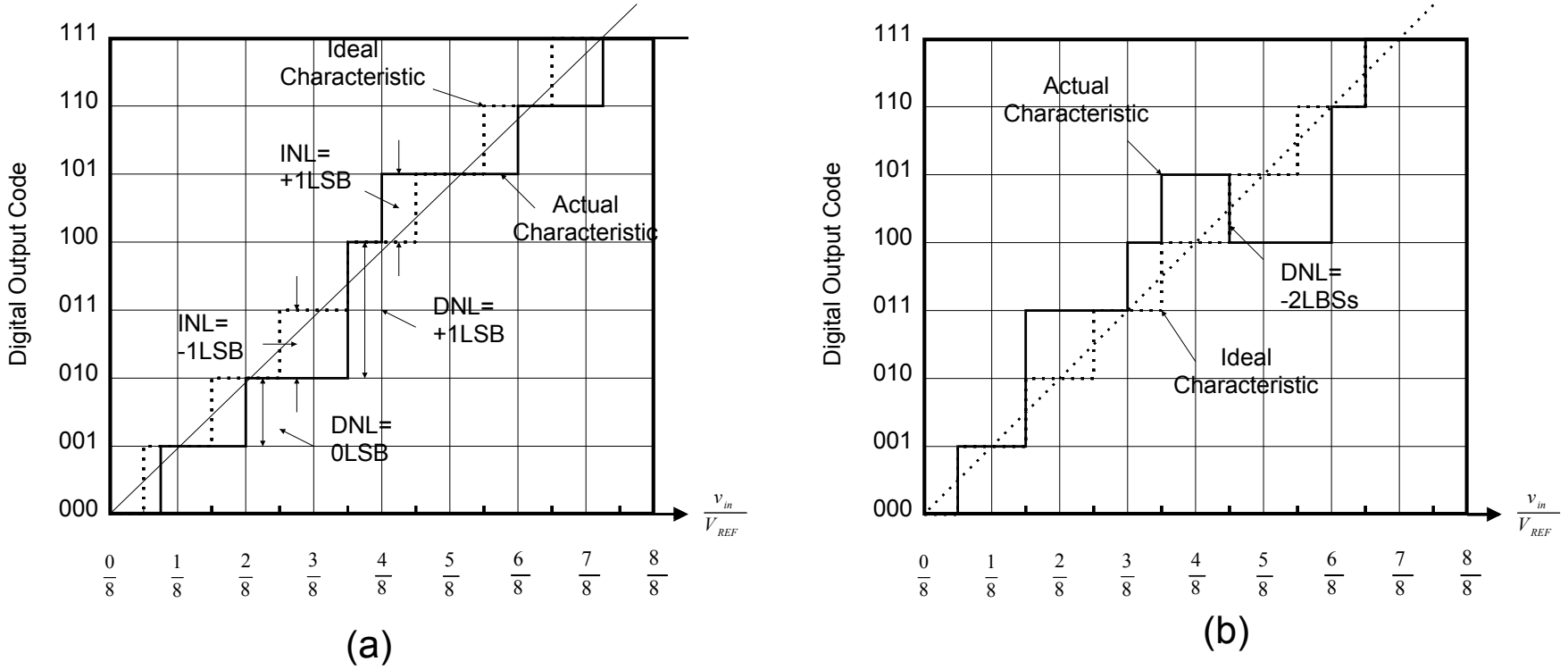
Parameters used to characterise the performance of analog-to digital converters:

- **Differential nonlinearity (DNL)** is the maximum deviation in the output step size from the ideal value of one least significant bit (LSB).
- **Integral nonlinearity (INL)** is the maximum deviation of the input/ouput characteristic from a straight line passed through its end points. The difference between the ideal and actual characteristics will be called the INL profile.
- **Offset** is the vertical intercept of the straight line passed through the end points.
- **Gain error** is the deviation of the slope of the line passed through the end points from its ideal value (usually unity).
- **Settling time** is the time required for the output to experience full-scale transition and settle within a specified error band around its final value.
- **Glitch impulse** area is the maximum area under any extraneous glitch that appears at the output after the input code changes. This parameter is also called ”glitch energy” in the literature even though it does not have an energy dimension.
- **Latency** is the total delay from the time the digital input changes to the time the analog output has settled within a specified error band around its final value. Latency may include multiples of the clock period if the digital logic in the DAC is pipelined.
- **Signal-to-(noise + distortion)** ratio (SNDR) is the ratio of the signal power to the total noise and harmonic distortion at the output when the input is a (digital) sinusoid.



(a) Example of offset error for a 3-bit ADC.

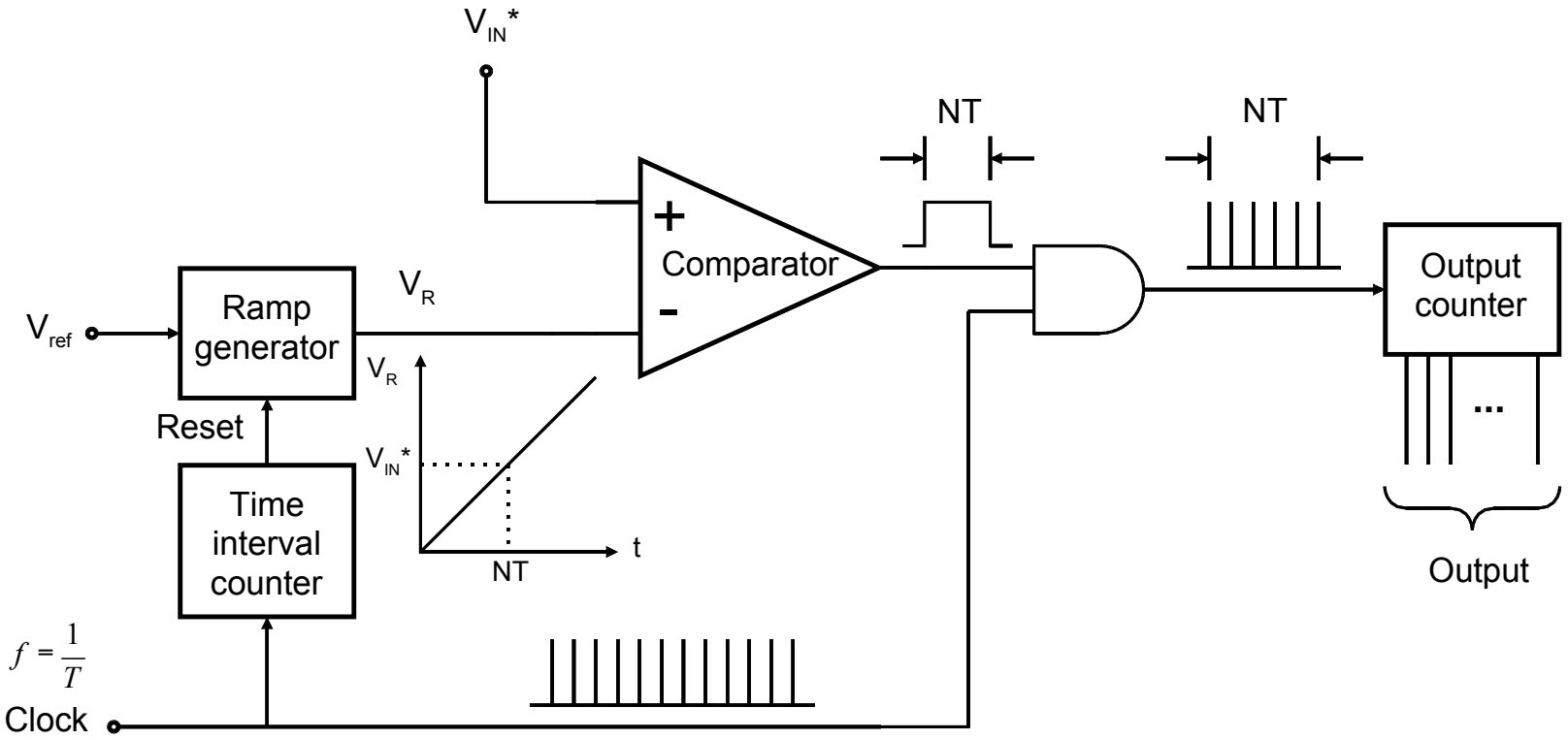
(b) Example of gain error for a 3-bit ADC.



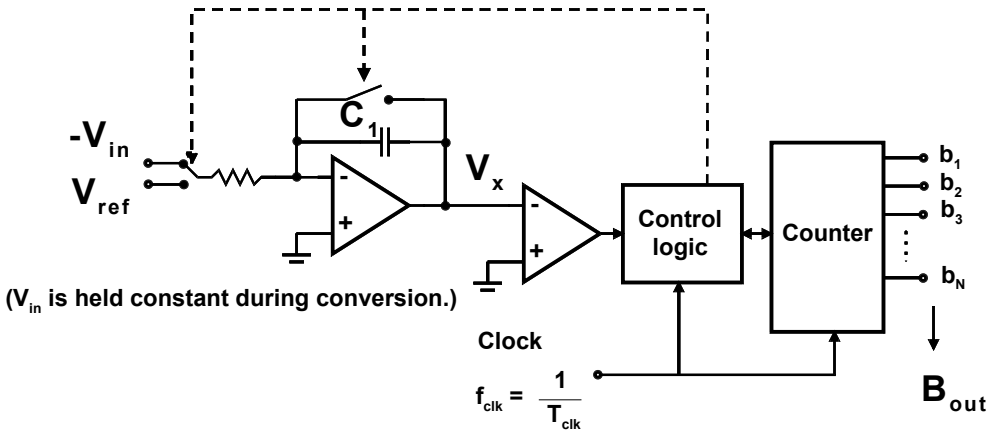
(a) Example of INL and DNL for a 3-bit ADC.

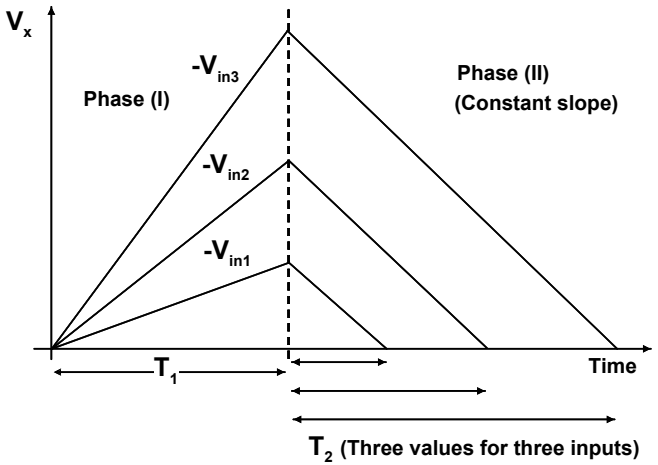
(b) Example of nonmonitonic 3-bit ADC.

Block diagram of a single-slope serial A/D converter



Integrating dual slope A/D converter





Integration:

$$V_X(t) = -\int_0^t \frac{-V_{in}}{R_1 C_1} d\tau = \frac{V_{in}}{R_1 C_1} t$$

T_2 is related to T_1 by:

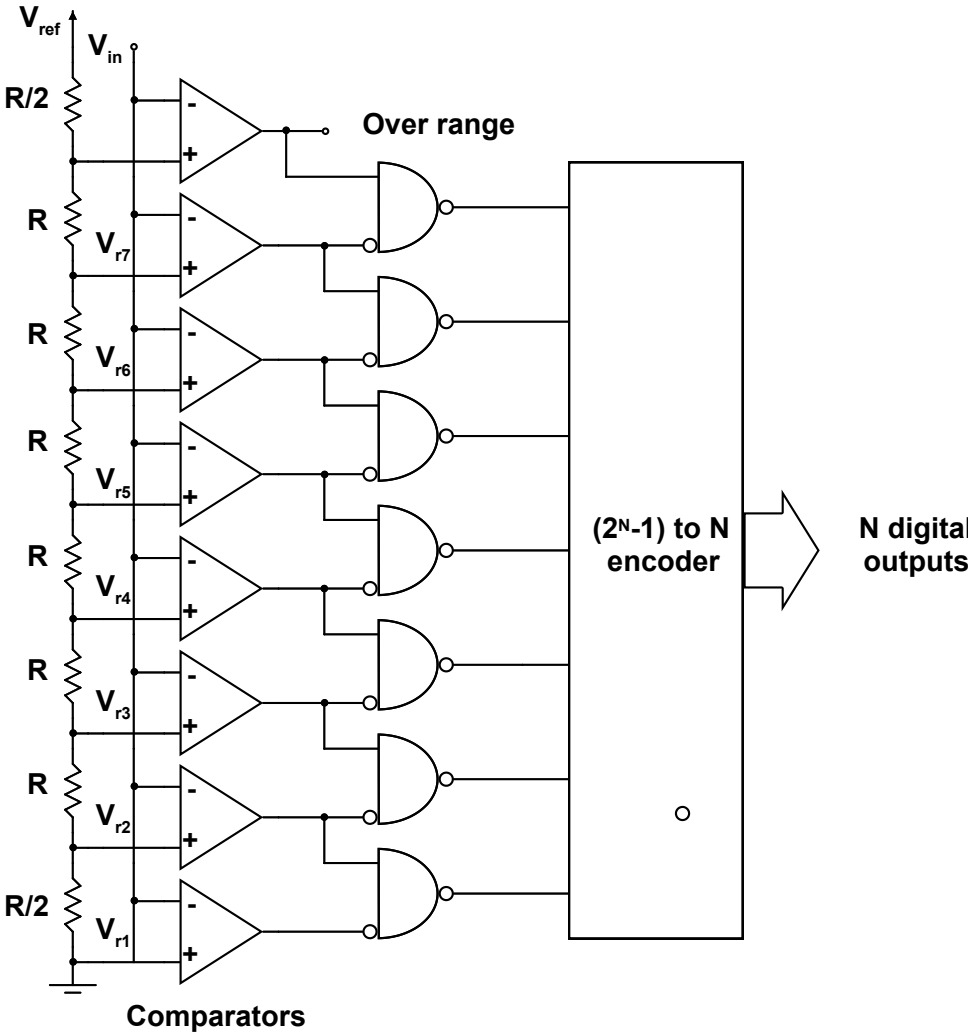
$$T_2 = T_1 \left(\frac{V_{in}}{V_{ref}} \right)$$

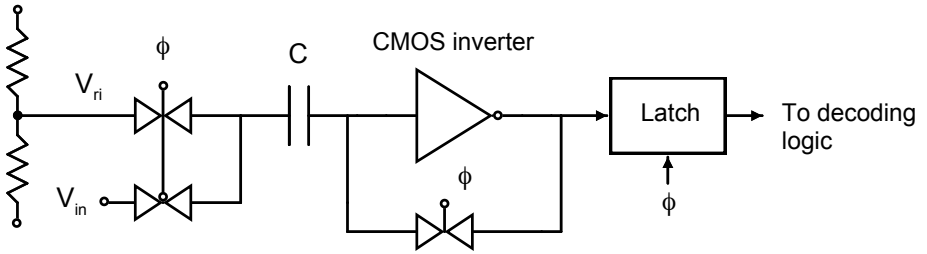
Counter output:

$$B_{out} = b_1 2^{-1} + b_2 2^{-2} + \ldots$$
$$+ b_{N-1} 2^{-(N-1)} + b_N 2^{-N} = \frac{V_{in}}{V_{ref}}$$

- Max. conversion time 2^N, very slow
- Simple architecture, easy to reach hihgh accuracy
- Applications with 18-20bits or better accuracy

A 3-bit flash A/D converter

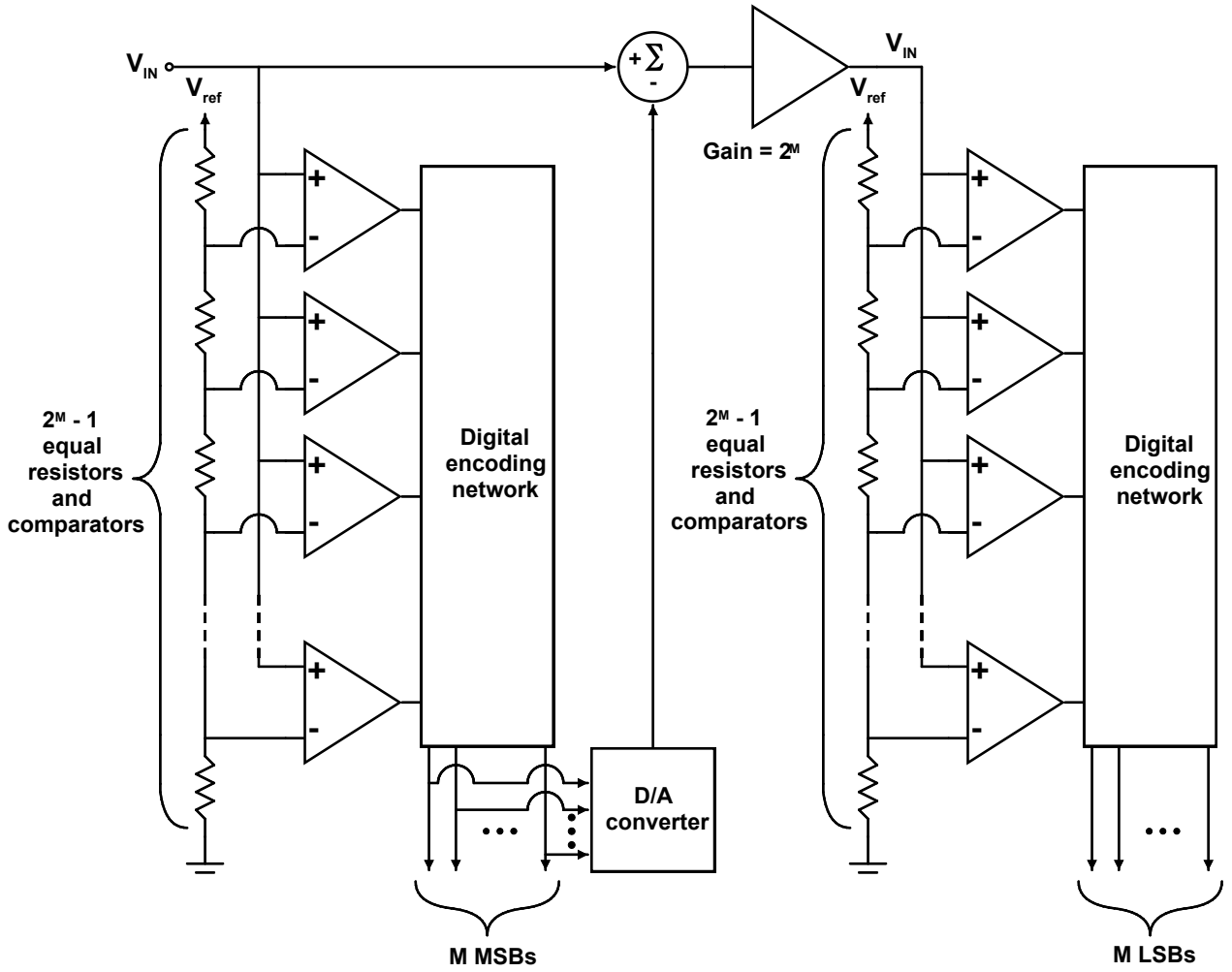




A clocked CMOS comparator

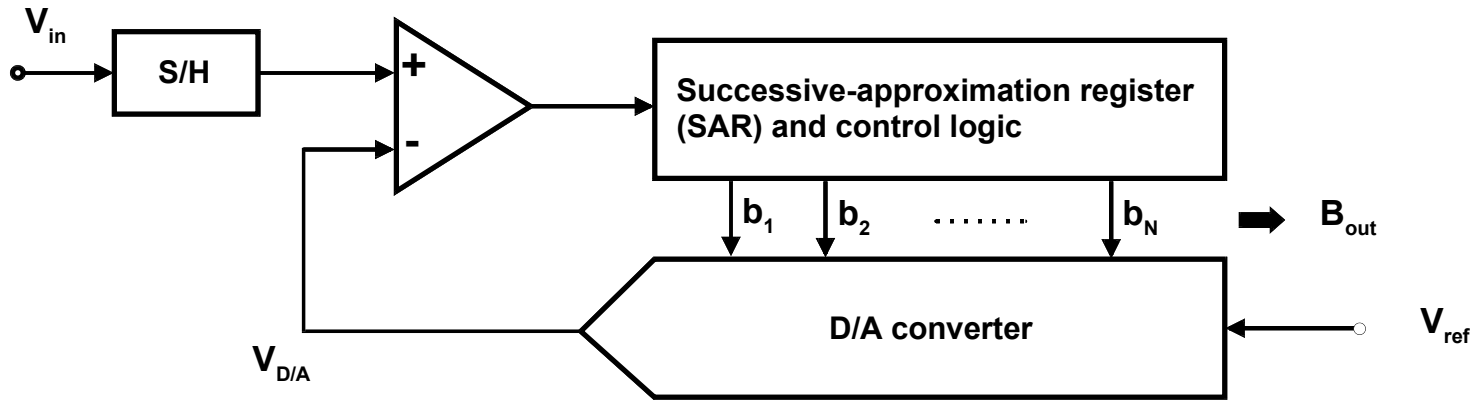
- 2^N comparators needed, high power consumption
- 2^N resistors needed, difficult to use common centroid geometry
- Monotonic
- Conversion in single clock cycle, fastest converter
- Used with resolutions 6 bits and less

A 2M-bit parallel-series A/D converter configuration

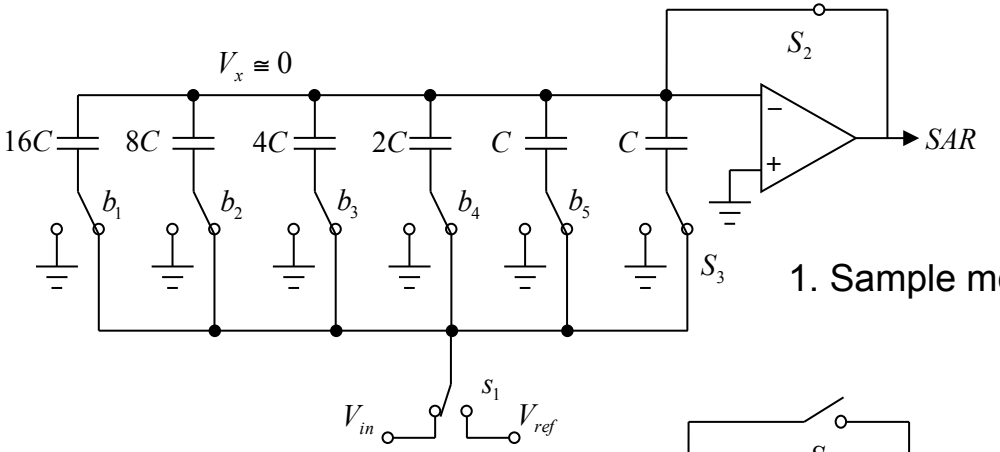


- Number of comparators reduced to $2^{N/2}$
- Gain of $2^{N/2}$ amplifier needed, limits speed and accuracy
- Conversions every clock-cycle, latency 2 clock cycles

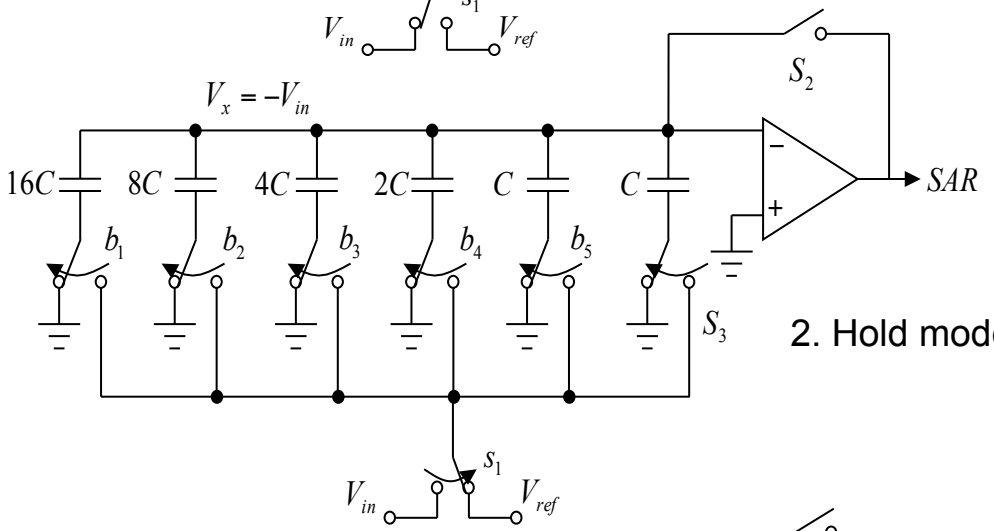
D/A converter-based successive-approximation converter



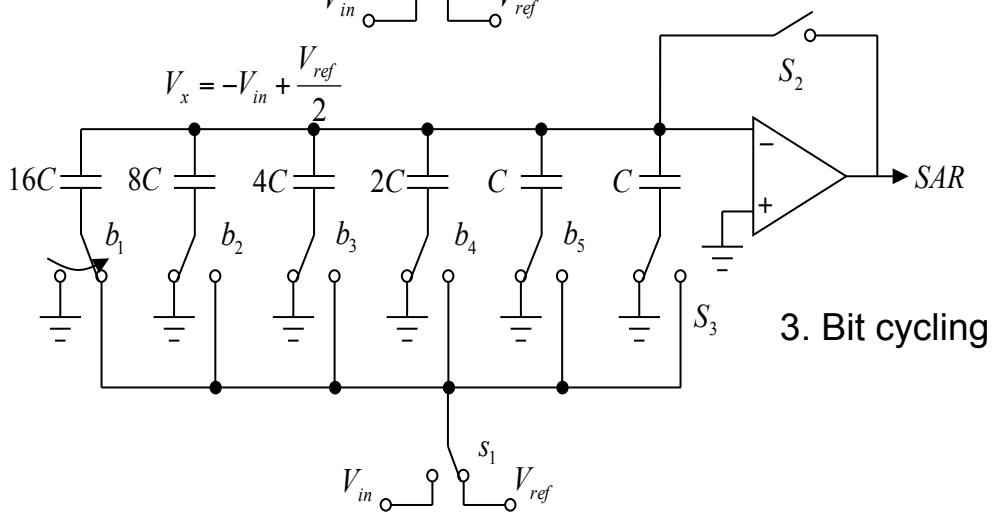
- Medium accuracy 10 bits
- Medium speed, n clock-cycles per conversion
- No amplifiers, only comparator needed
- Any D/A-converter , or hybrid can be used



1. Sample mode

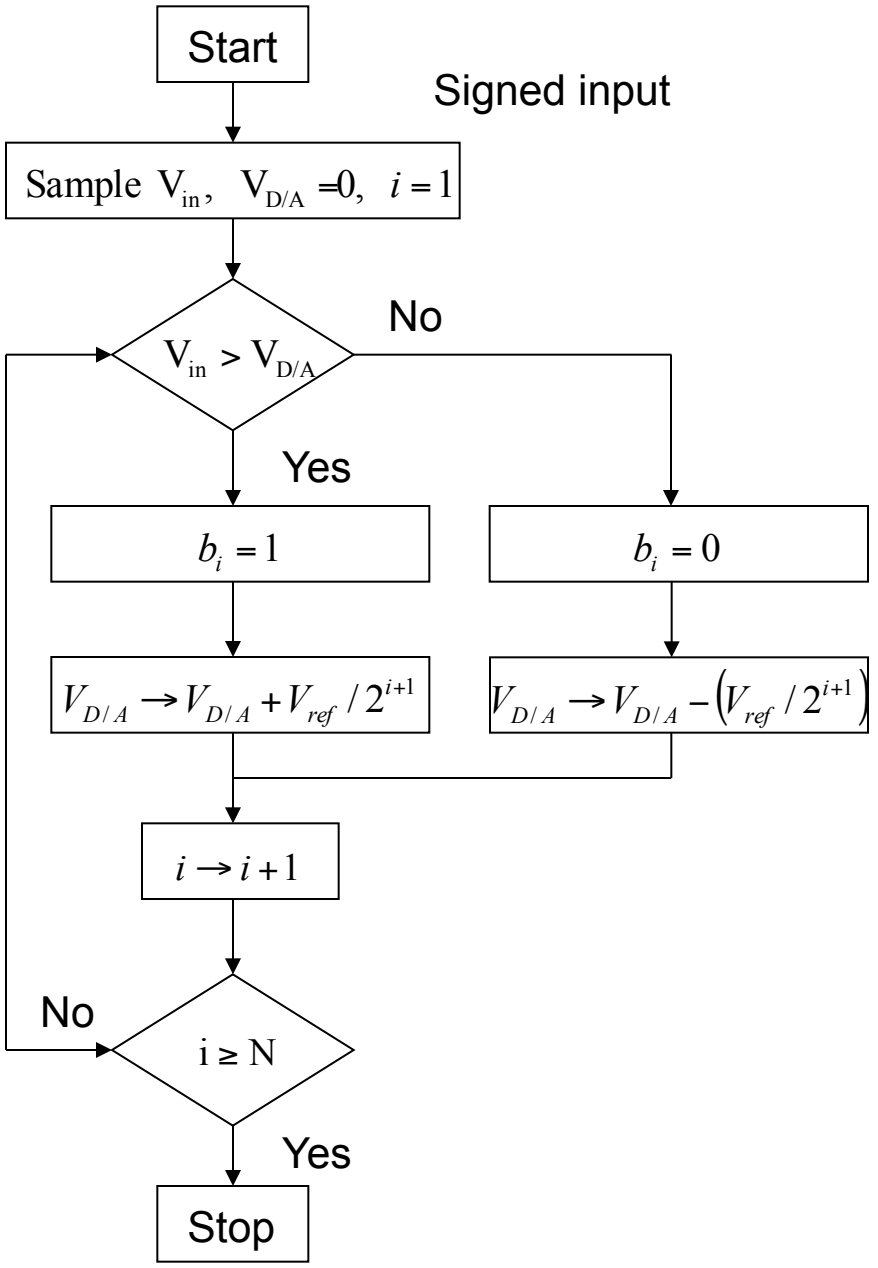


2. Hold mode

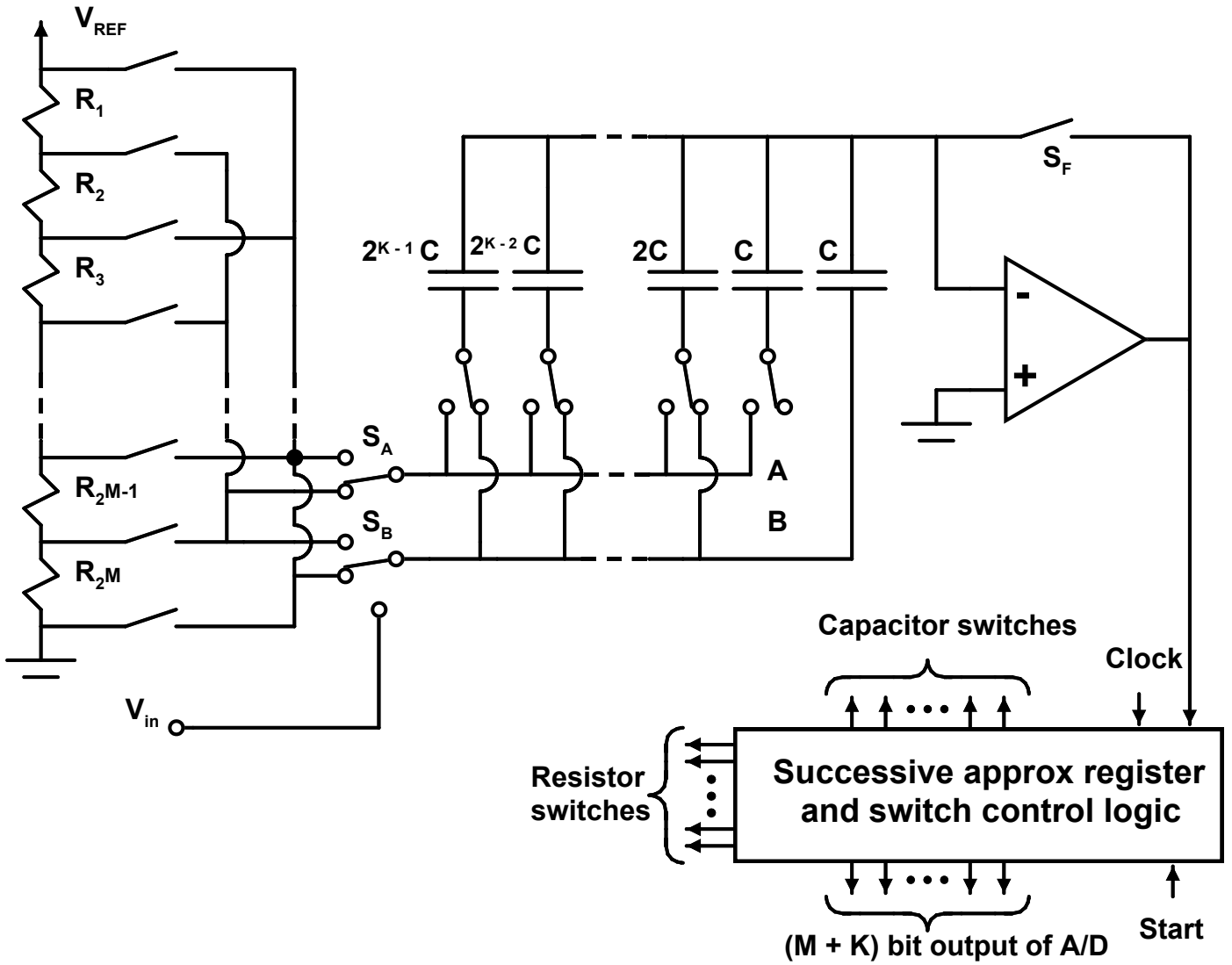


3. Bit cycling

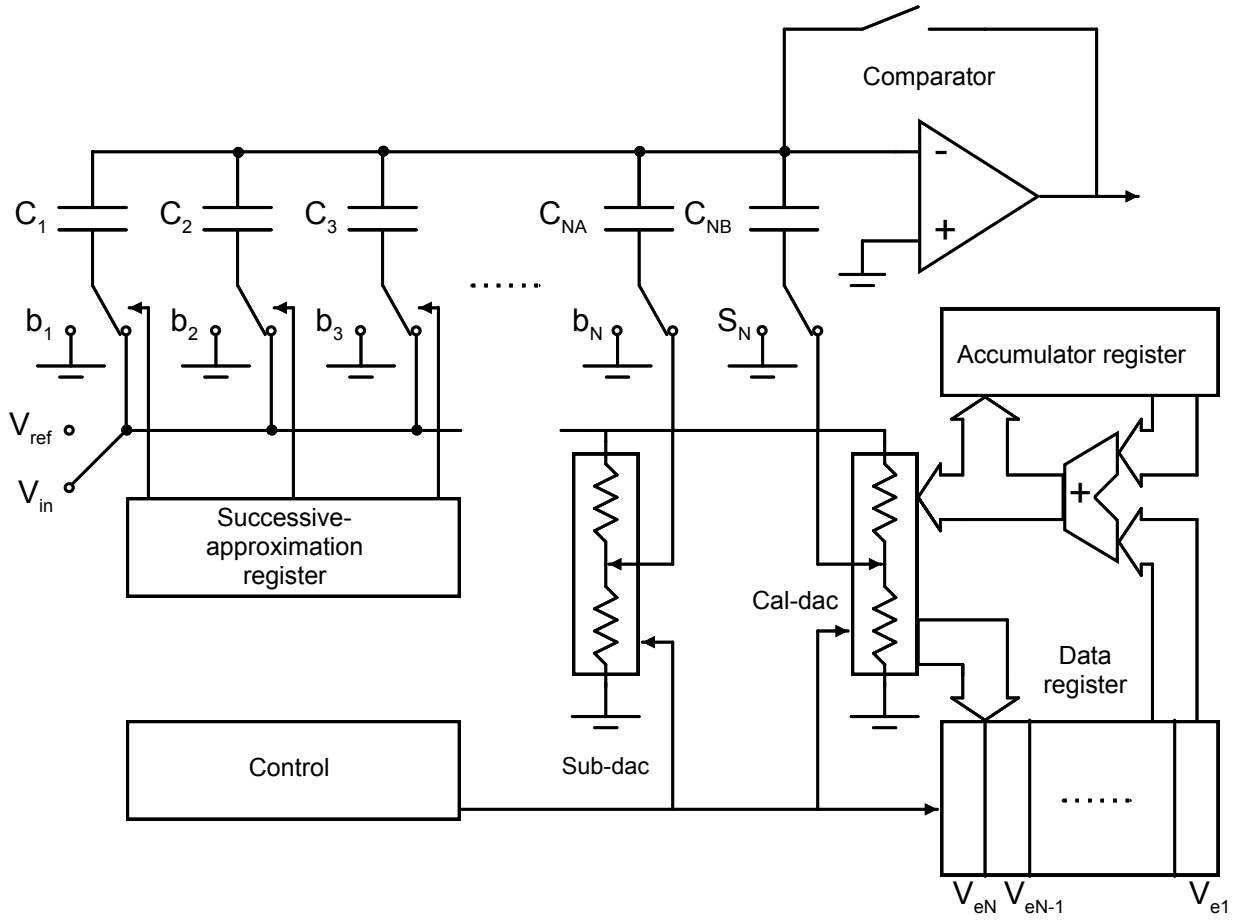
Flow graph for the successive-approximation approach



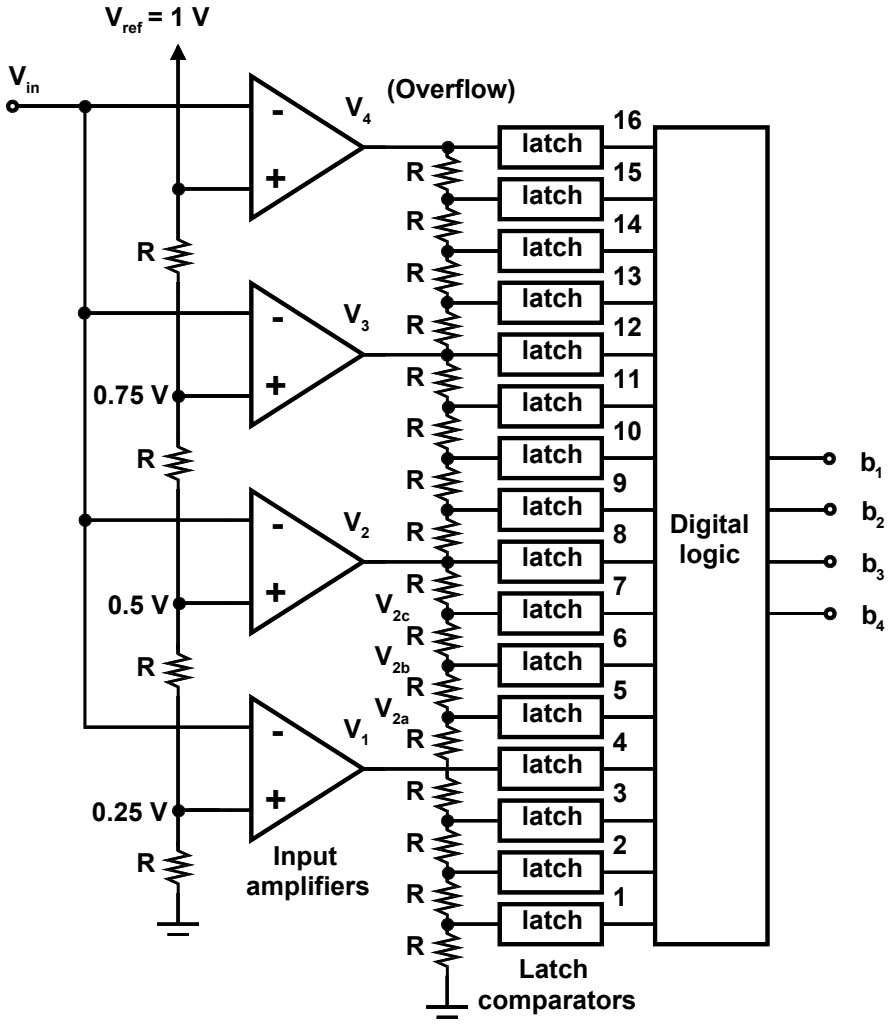
A voltage-scaling, charge-scaling, successive-approximation A/D converter

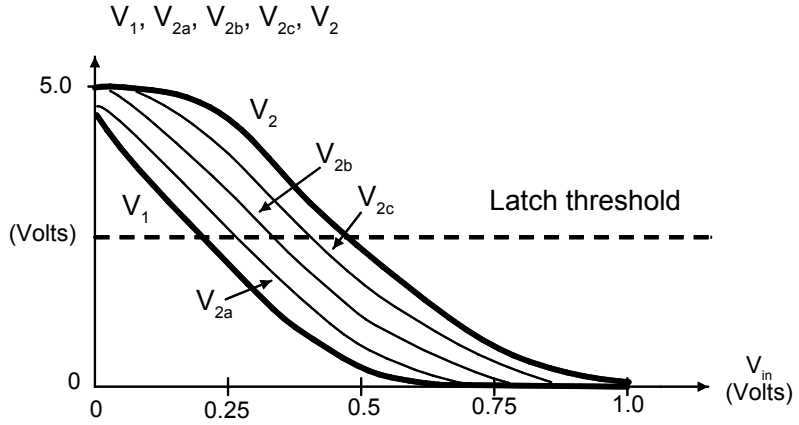


A charge-redistribution A/D converter with error correction



A 4-bit interpolating A/D converter (interpolating factor of 4)

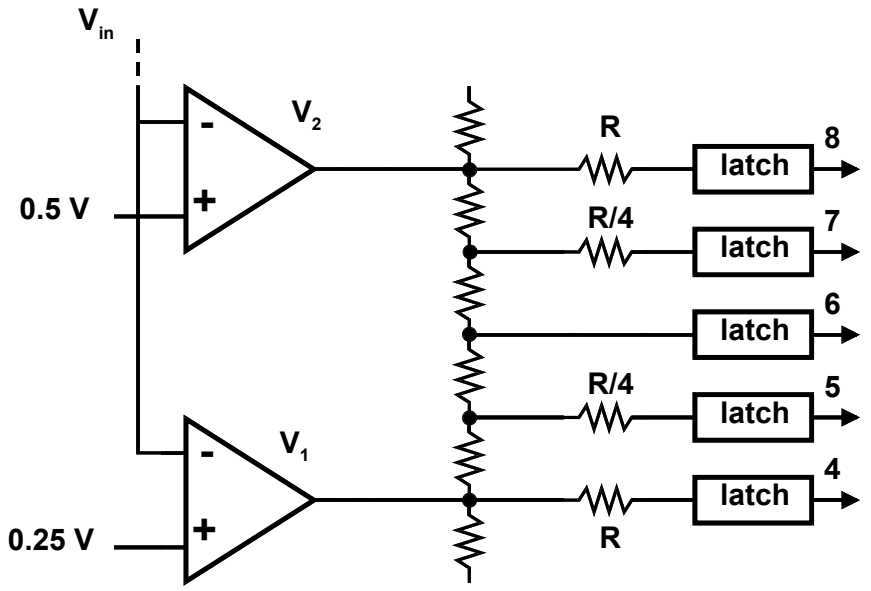




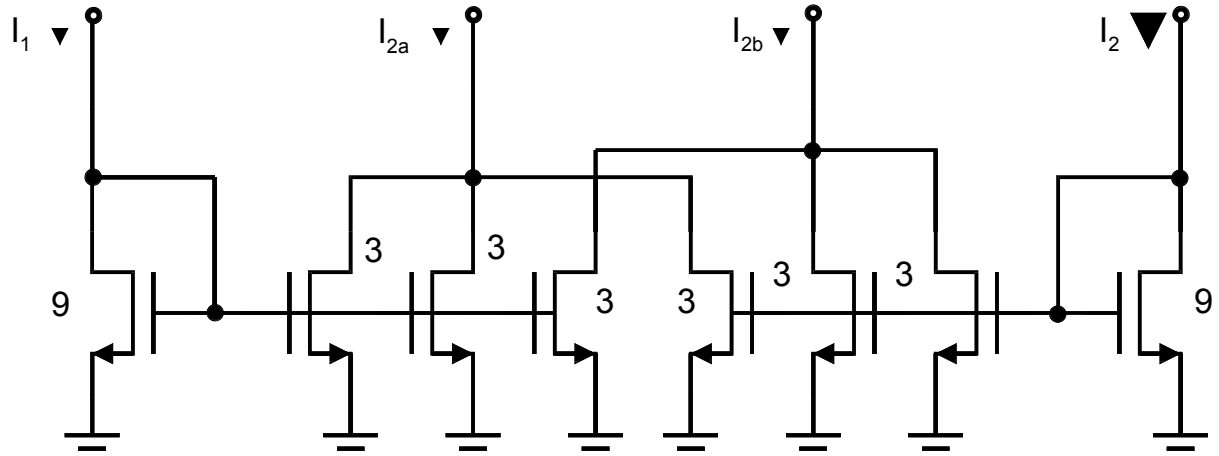
The transfer responses of V_1 and V_2, and their interpolated signals.

Number of comparators rediced with interpolation
Comparators replaced with differential single stage amplifiers

Adding series resistors to equalize delay times to the latch comparators



Interpolating by three between two current ouputs

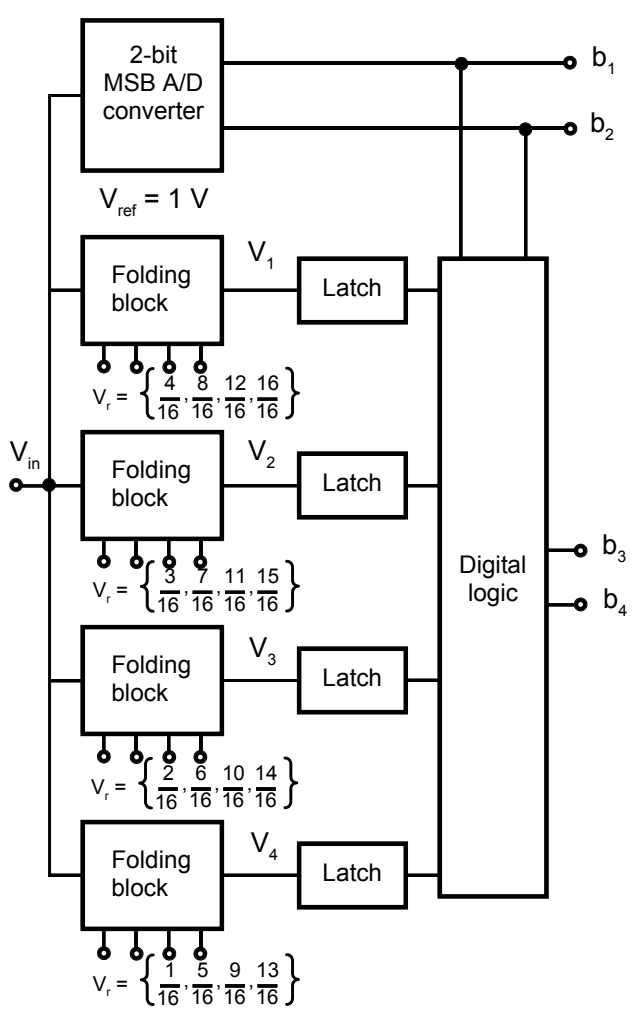


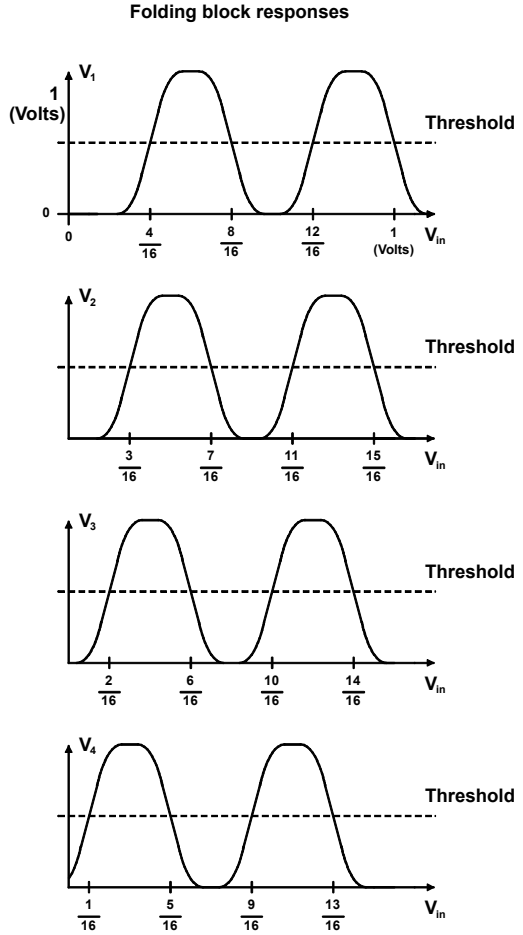
(Relative width sizing shown)
(All lengths same)

$$I_{2a} = \frac{3}{2} I_1 + \frac{1}{3} I_2$$

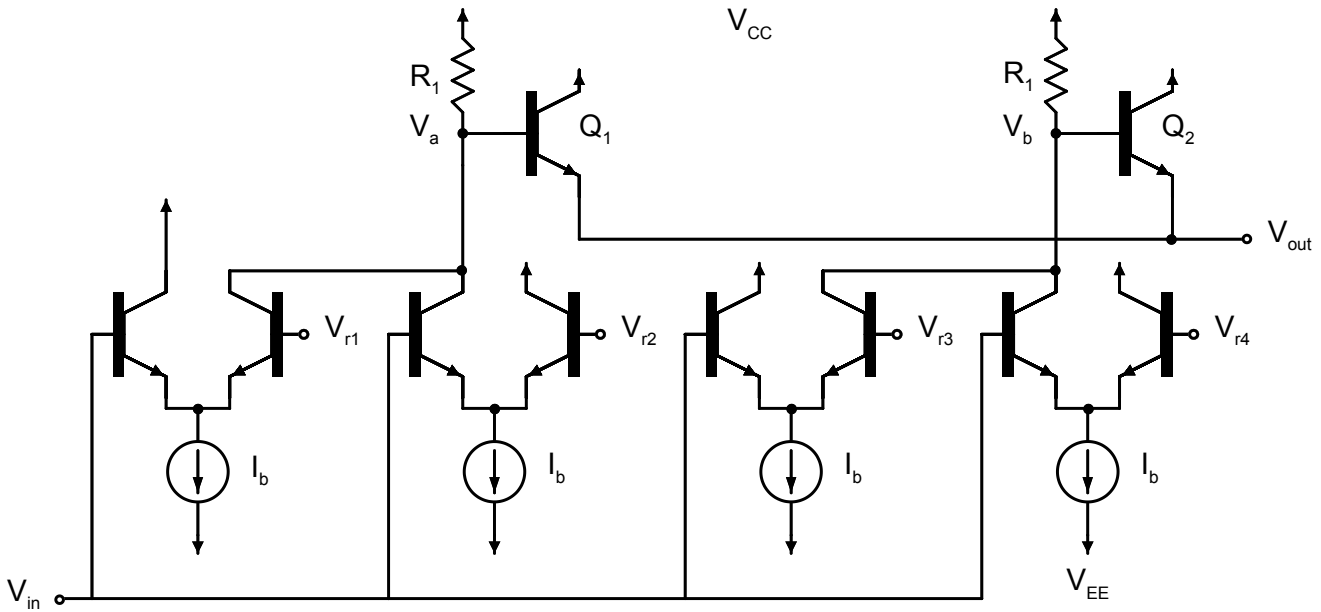
$$I_{2b} = \frac{1}{3} I_1 + \frac{2}{3} I_2$$

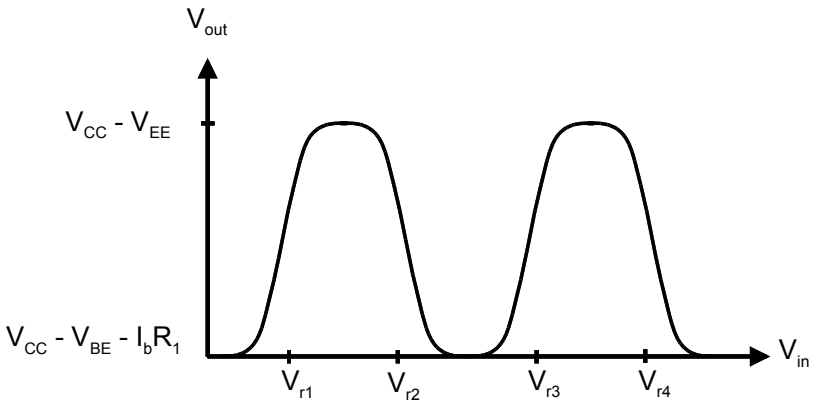
A 4-bit folding A/D converter wih a folding-rate of four



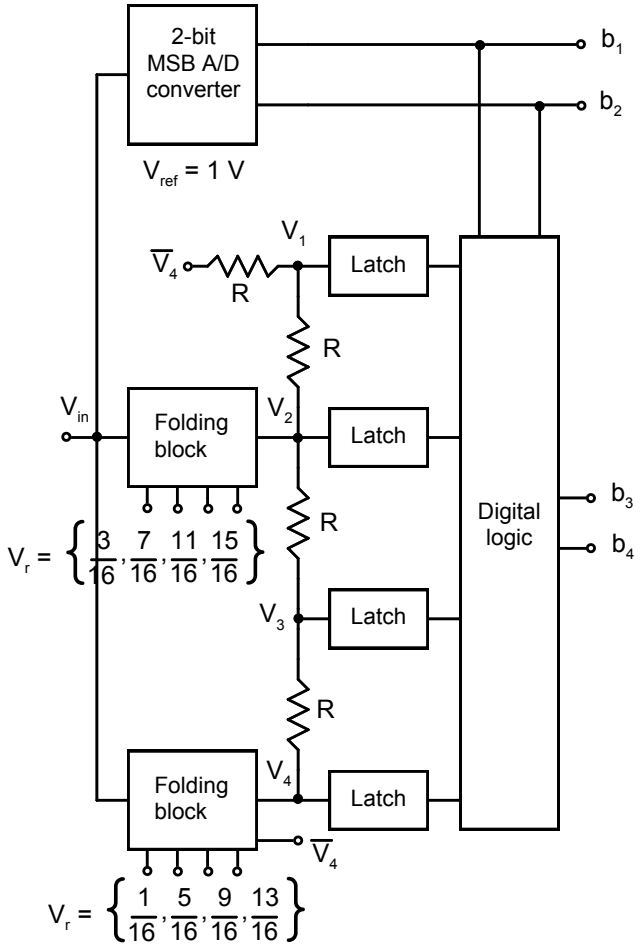


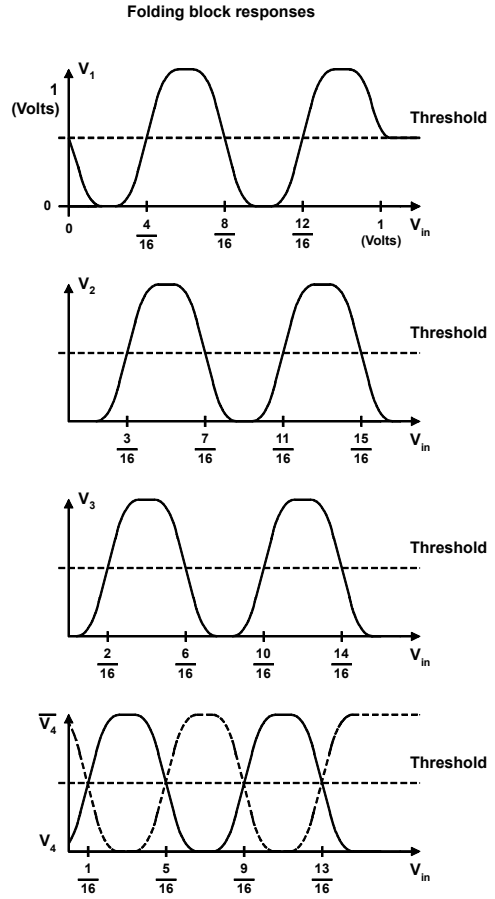
A folding block with a folding-rate of four





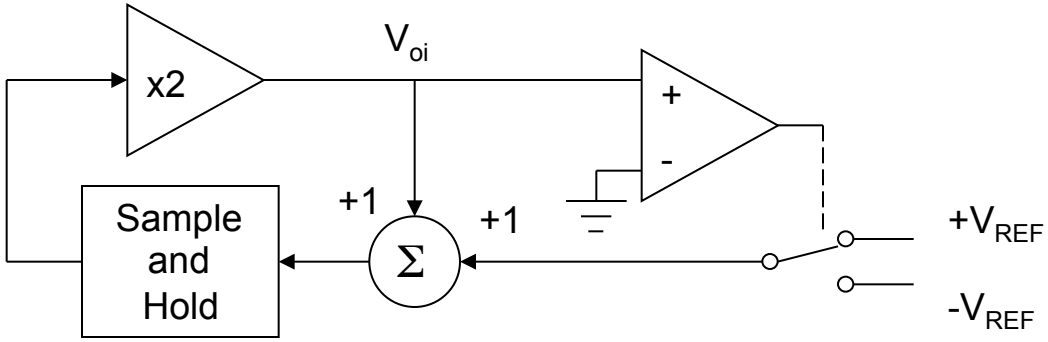
A 4-bit folding A/D converter with a folding rate of four and an interpolate-by-two

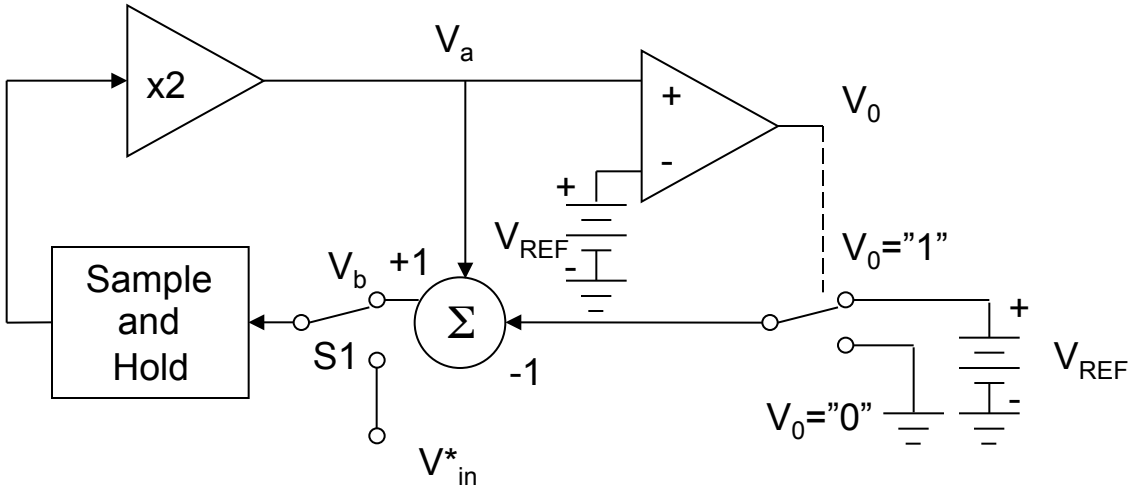




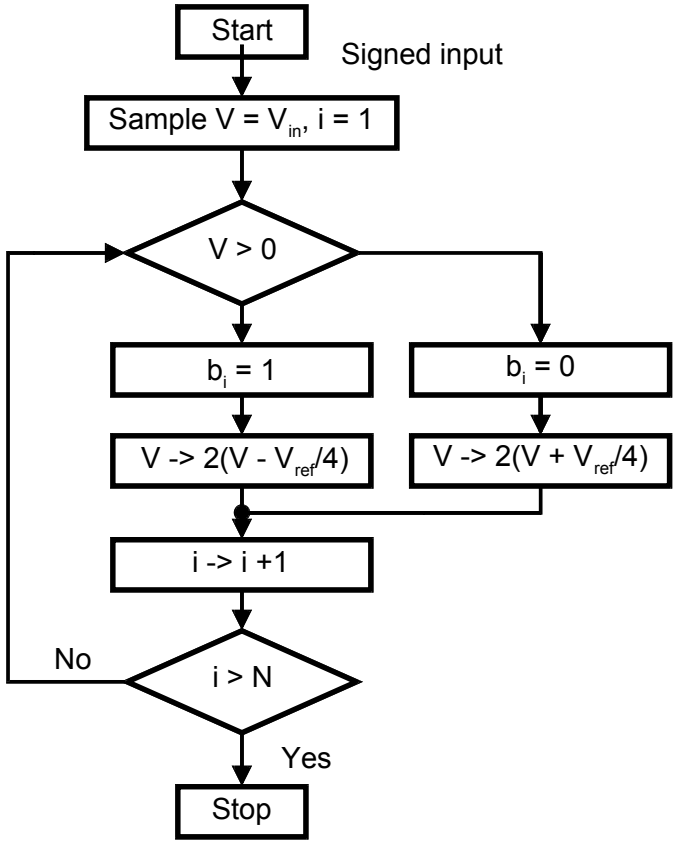
Iterative algorithmic ADC

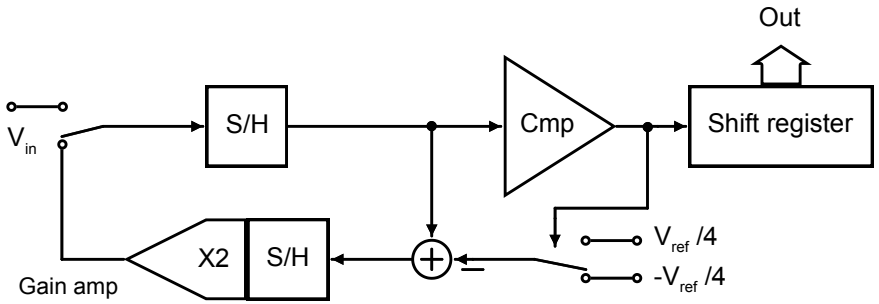
$$V_{oi} = \left[2V_{o,i-1} - b_i V_{REF}\right] z^{-1} \qquad b_i = \begin{cases} +1 & \text{if } V_i > 0 \\ -1 & \text{if } V_i < 0 \end{cases}$$



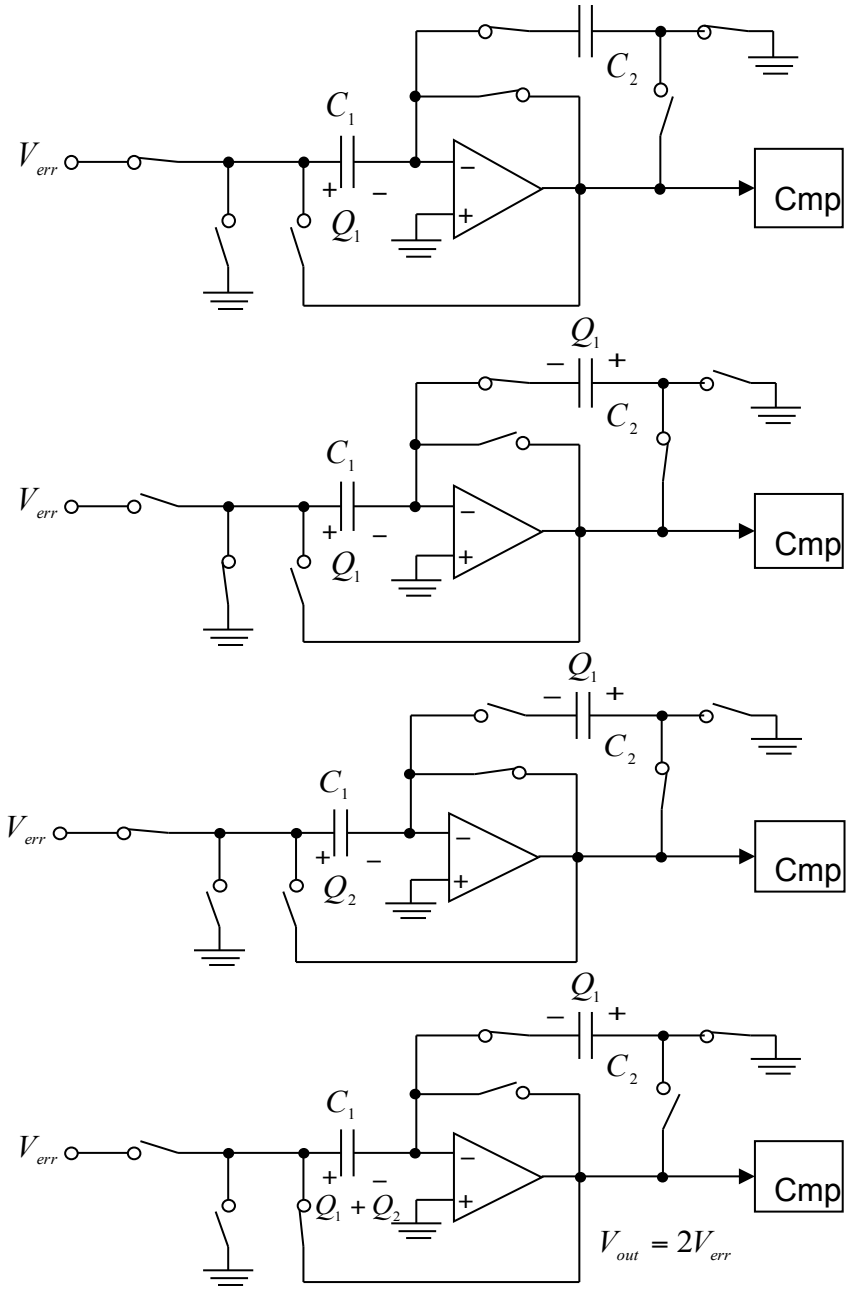


Flow graph for the algorithmic approach





Alogorithmic converter



1. Sample remainder and cancel input-offset voltage.

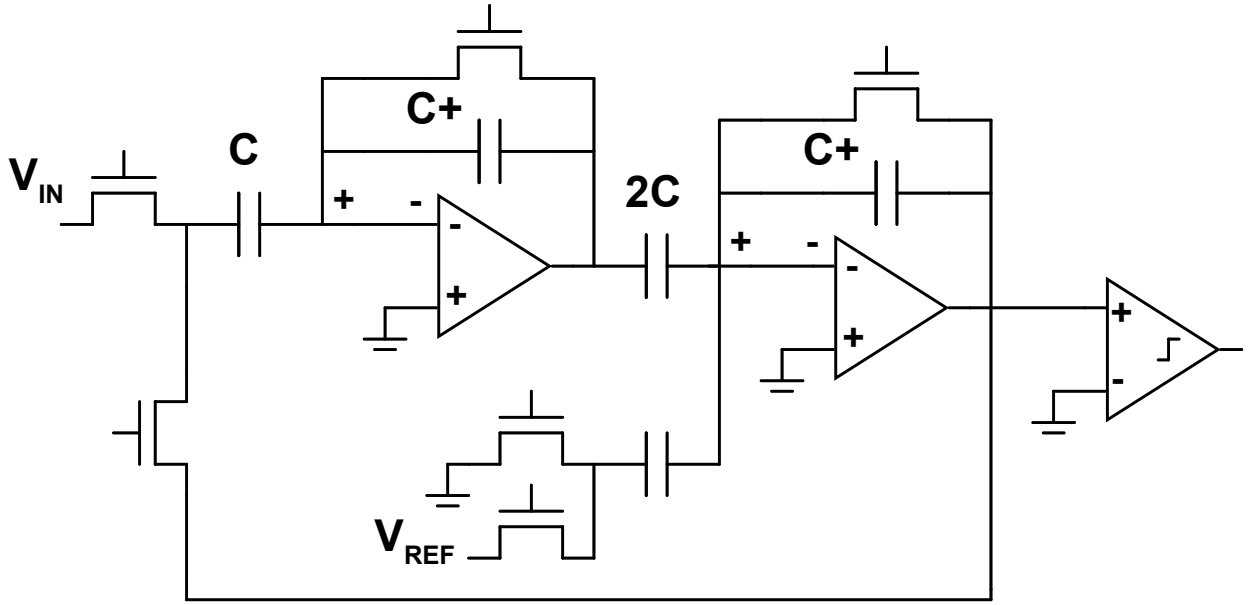
2. Transfer charge Q_1 from C_1 to C_2.

3. Sample input signal with C_1 again, after storing charge Q_1 on C_2.

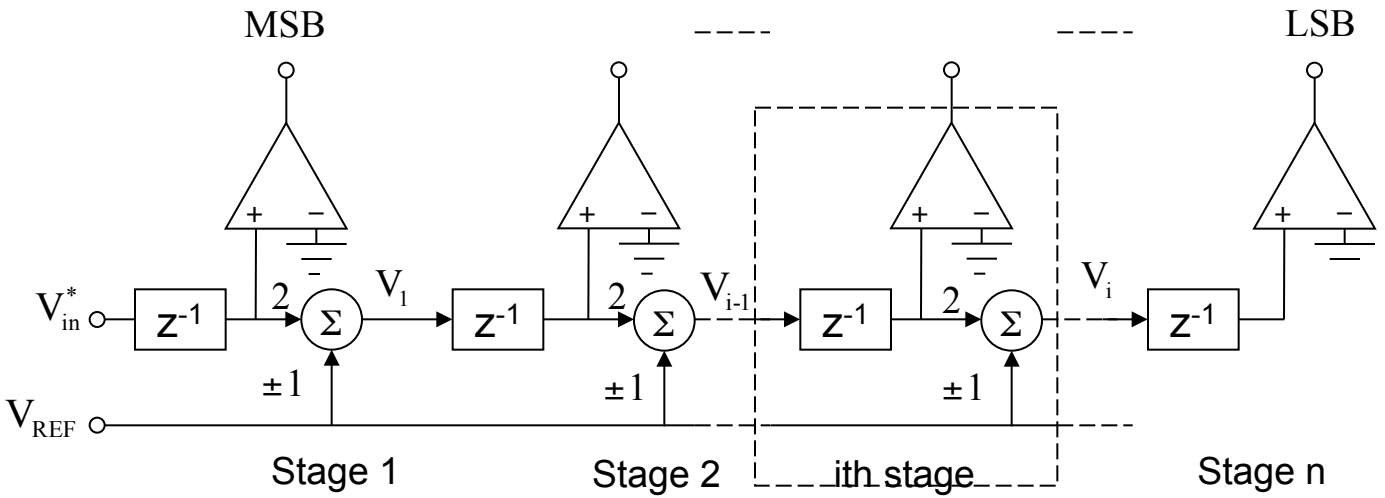
4. Combine Q_1 and Q_2 on C_1, and connect C_1 to output.

Multiply-by-two gain circuitry for an algorithmic converter that does not depend on capacitor matching.

Typical Circuit Implementation of an Algorithmic Converter



Pipeline implementation of the algorithmic ADC



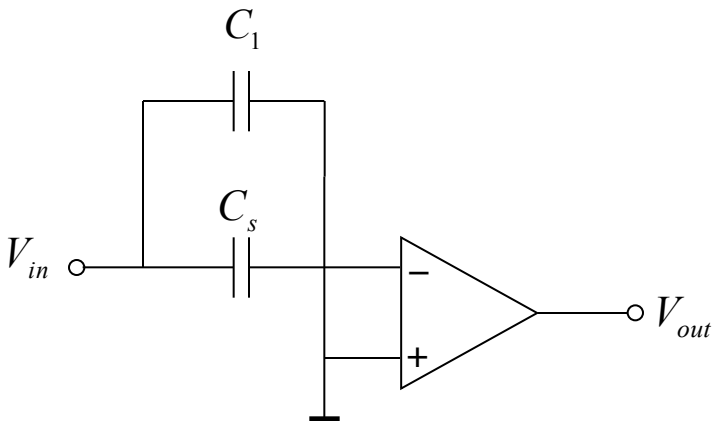
$$V_i = 2V_{i-1} - b_{i-1}V_{REF}$$

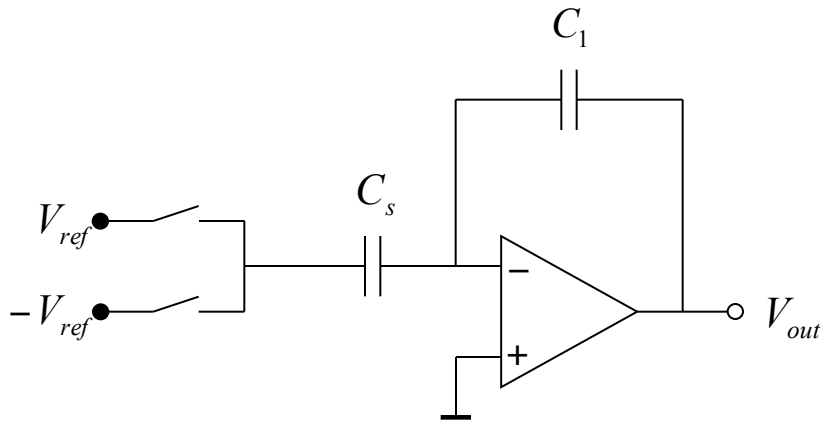
where b_{i-1} is given as

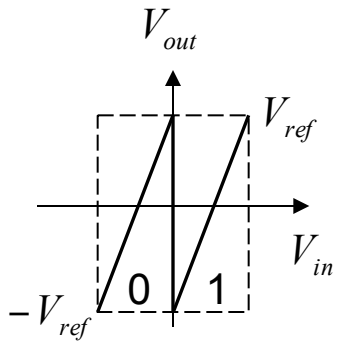
$$b_{i-1} = \begin{cases} +1 & \text{if } V_{i-1} > 0 \\ -1 & \text{if } V_{i-1} < 0 \end{cases}$$

1-bit MDAC

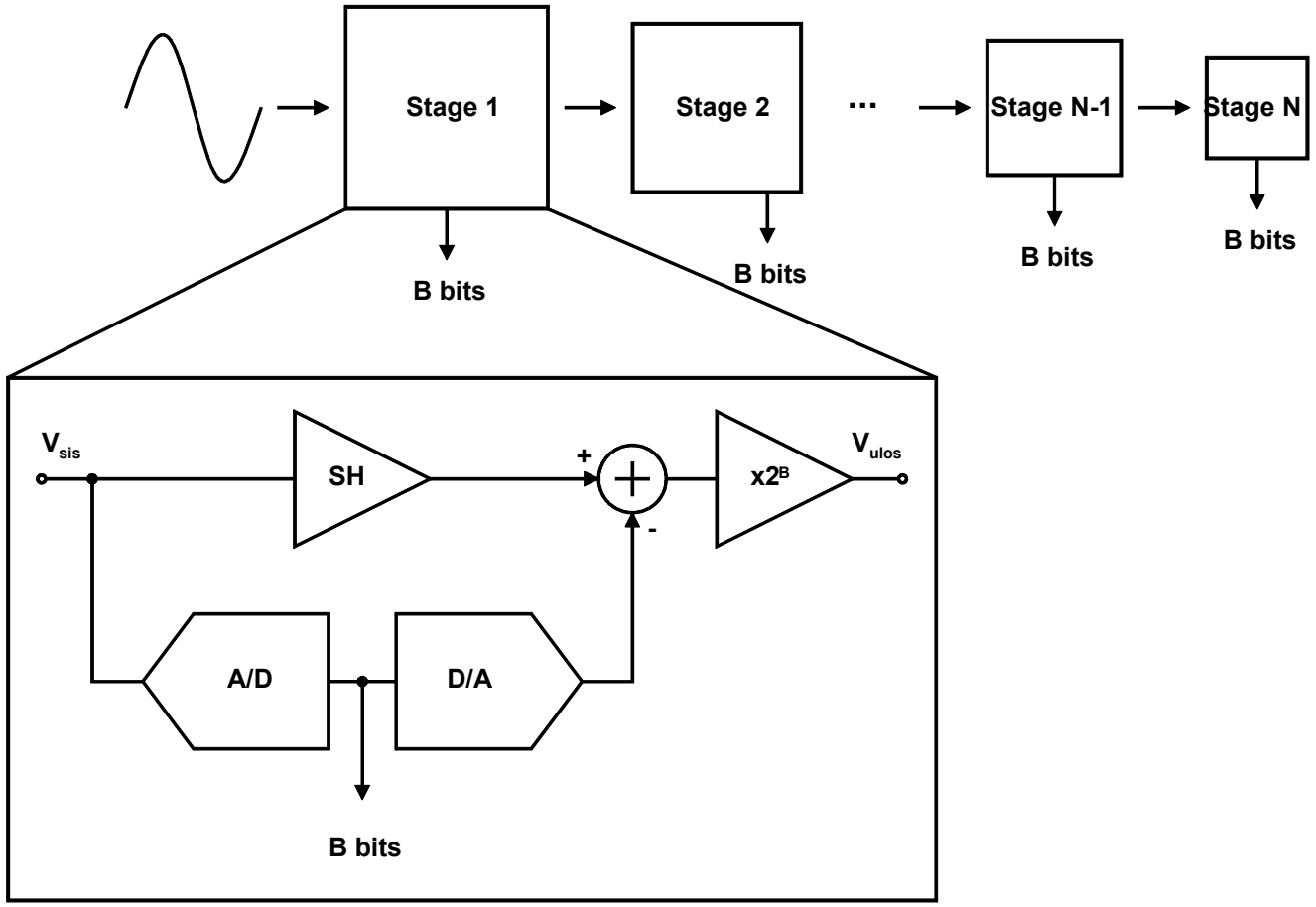
$$V_{out} = 2V_{in} \pm V_{ref}$$



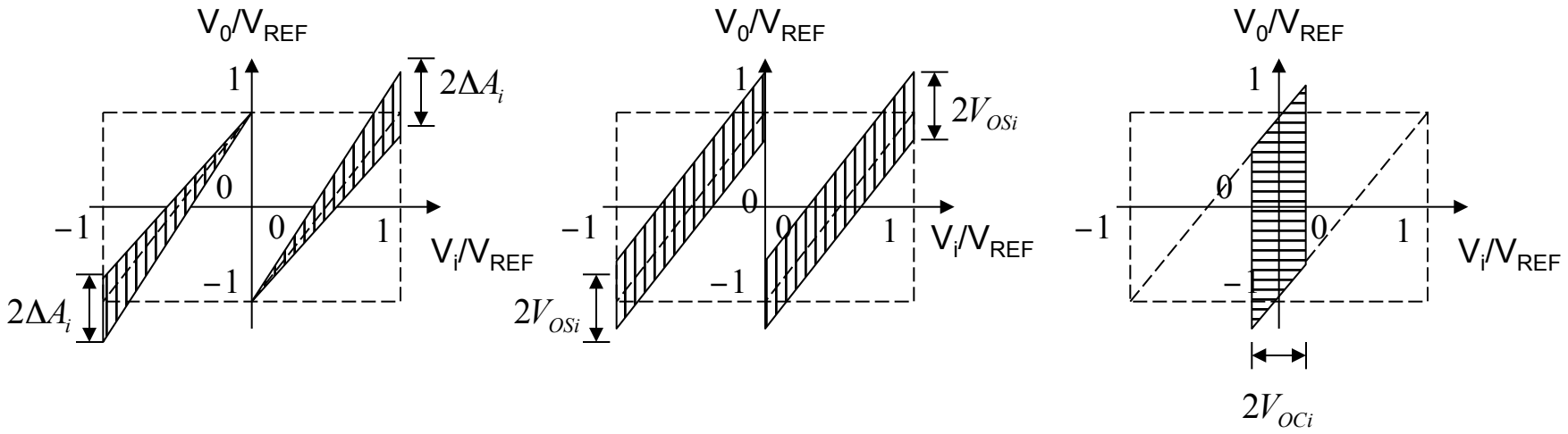




Scaled pipeline AD converter



Errors in pipeline A/D converter



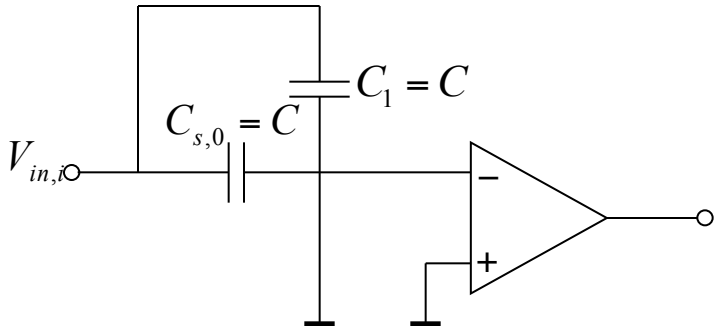
a) Gain error, A_i b) System offset error, V_{OSi} c) Comparator offset error, V_{OCi}

$$V_i = A_i V_{i-1} + V_{OSi} - b_i A_{si} V_{REF}$$

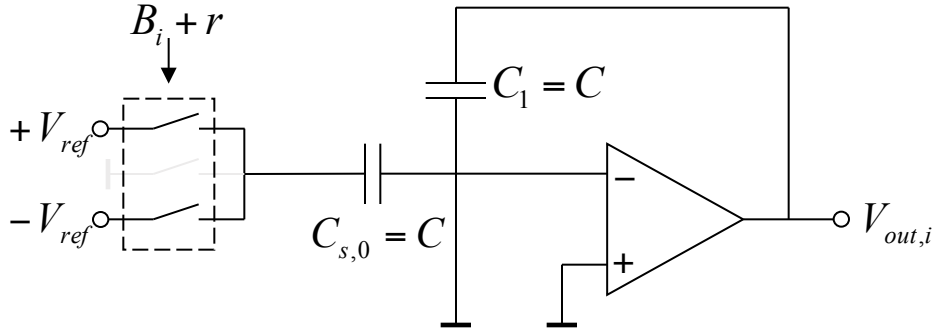
and

$$b_i = \begin{cases} +1 & \text{if } V_{i\text{-}1} > V_{OCi} \\ -1 & \text{if } V_{i\text{-}1} < V_{OCi} \end{cases}$$

Operation of 1.5-bit unit capacitor MDAC



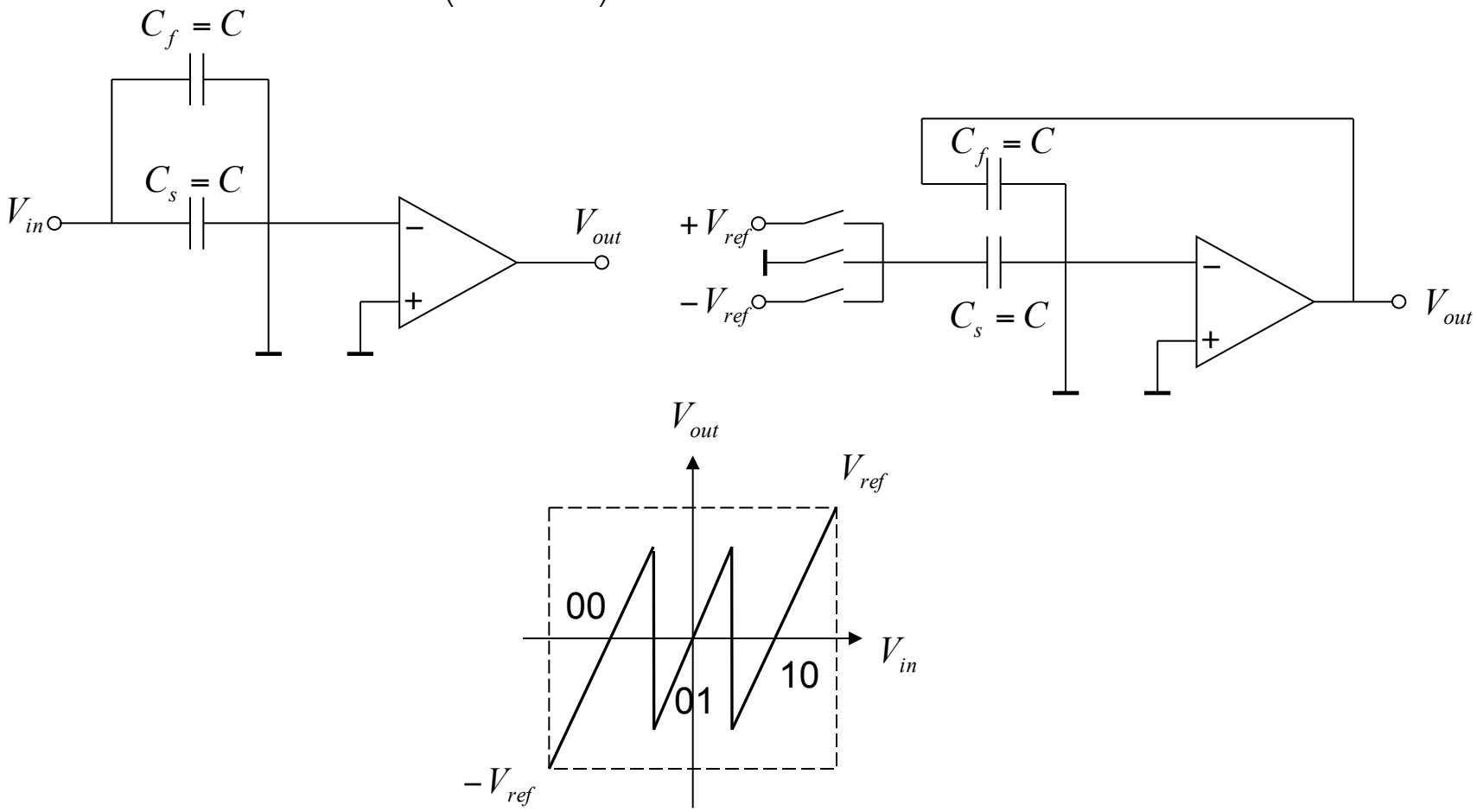
sample-mode



hold-mode

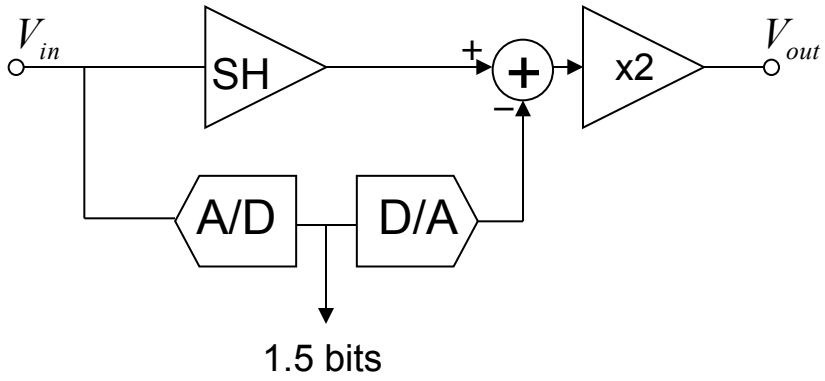
1.5-bit MDAC

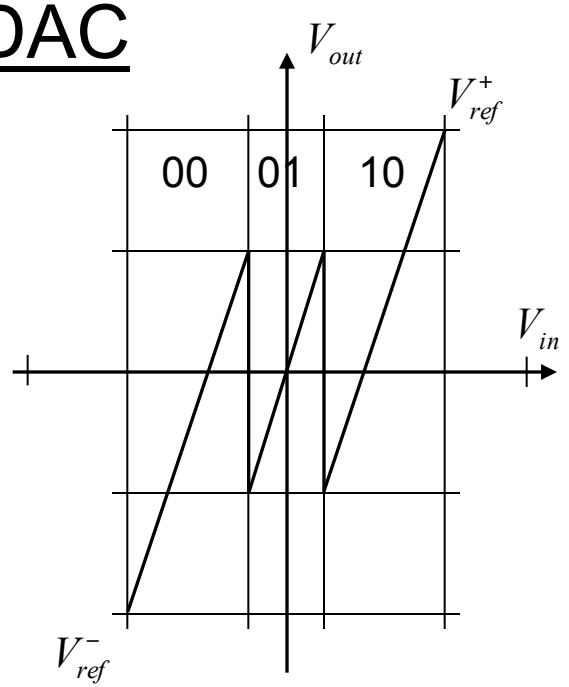
$$V_{out} = \left(\frac{C_f + C_s}{C_f} \right) V_{in} - Q \cdot \frac{C_s}{C_f} \cdot V_{ref} = 2V_{in} - Q \cdot V_{ref}$$

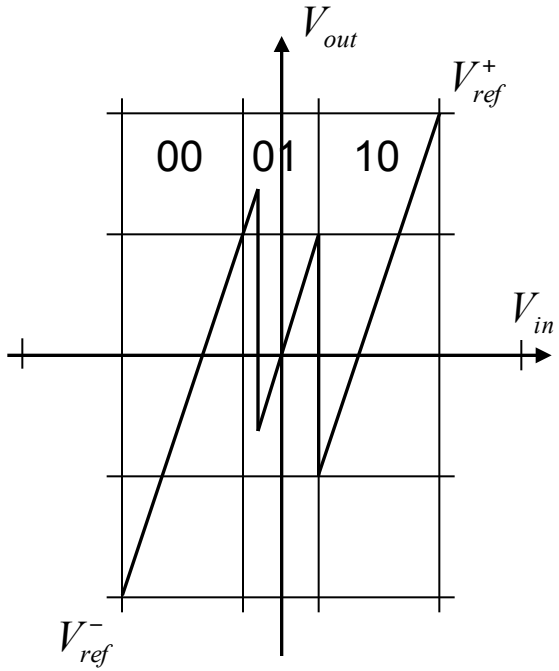


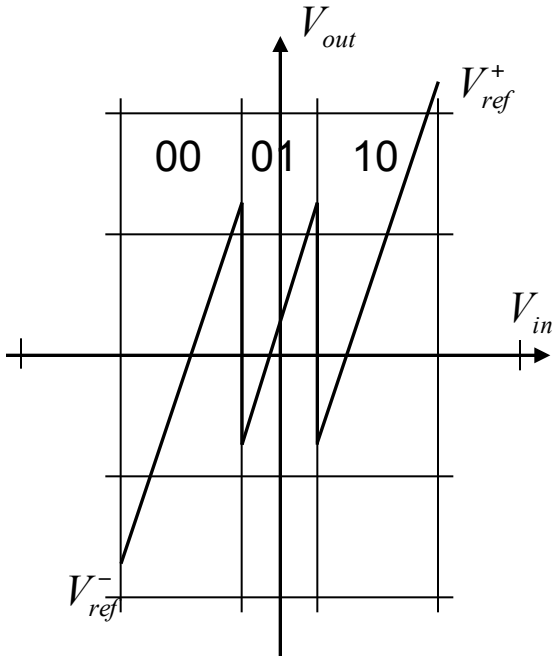
transfer function of 1,5-bit MDAC.

1.5-bit MDAC

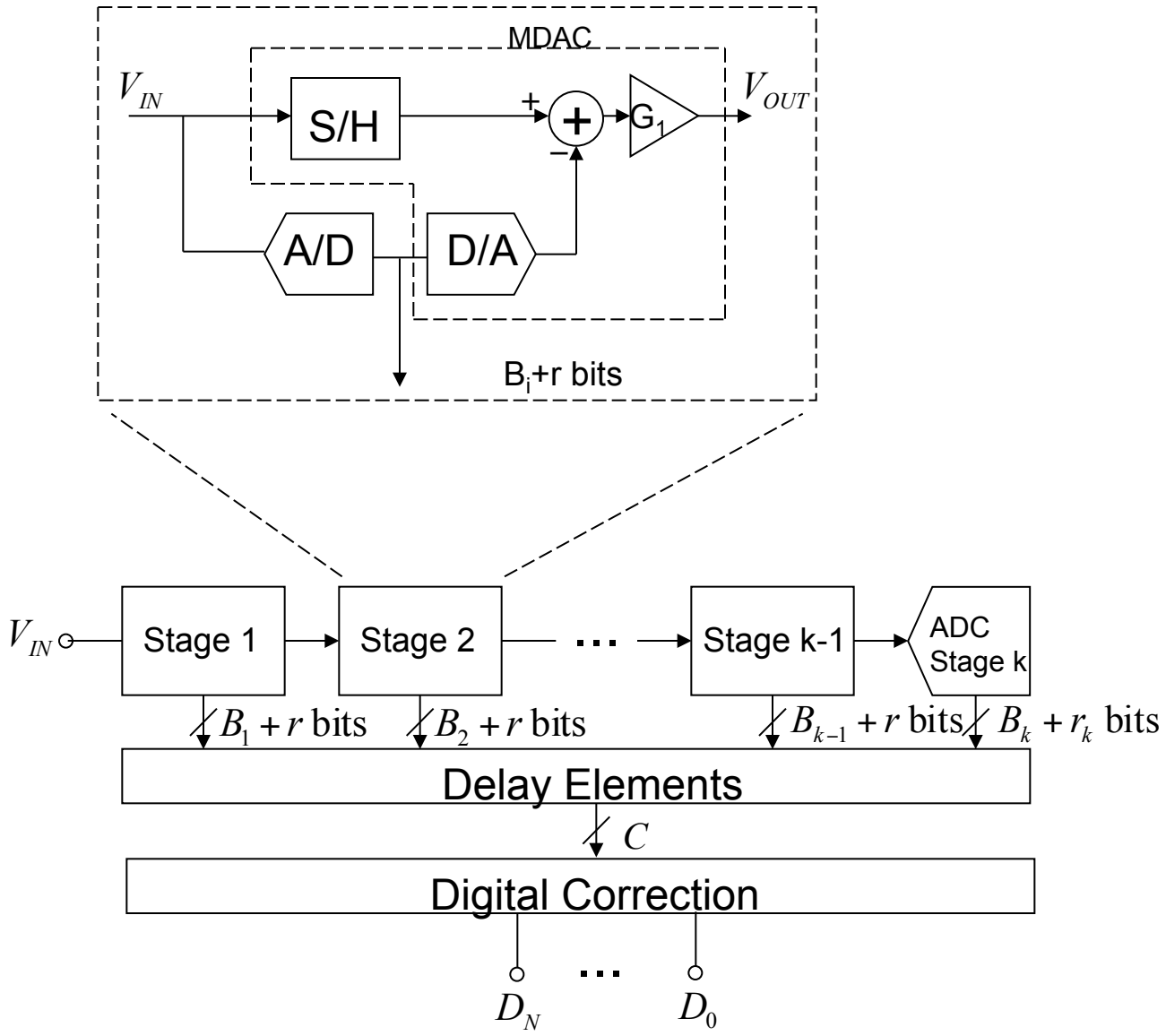

V_{in}
SH
+
+
−
x2
V_{out}
A/D
D/A
1.5 bits


V_{out}
V_{ref}^{+}
00
01
10
V_{in}
V_{ref}^{-}

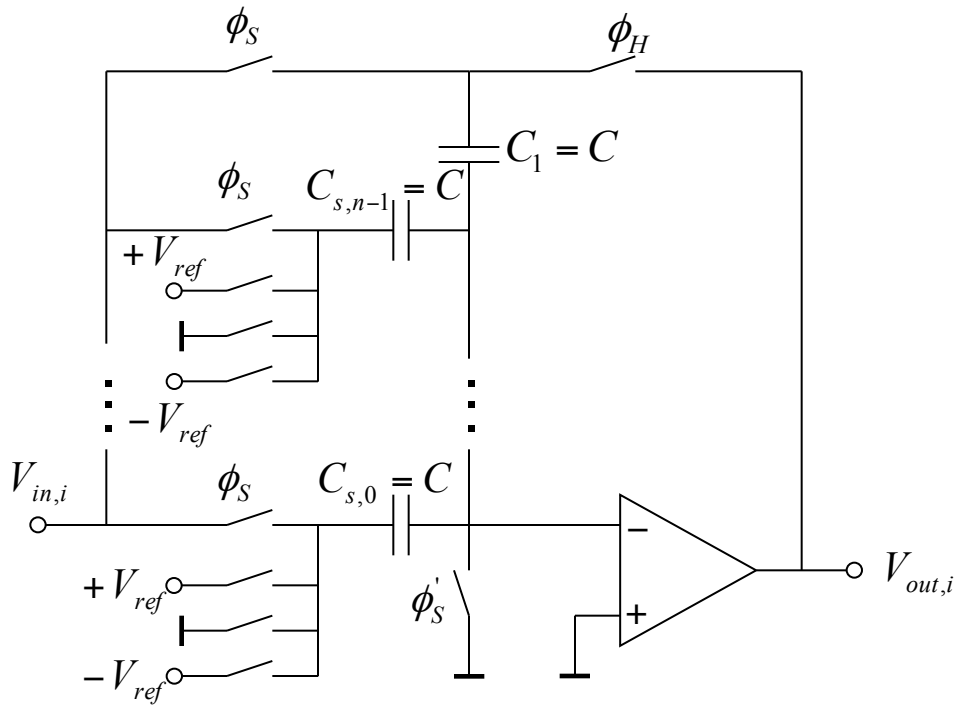

V_{out}
V_{ref}^{+}
00
01
10
V_{in}
V_{ref}^{-}


V_{out}
V_{ref}^{+}
00
01
10
V_{in}
V_{ref}^{-}

Pipeline A/D converter



Unit capacitor switched capacitor MDAC



Binary weighted SC MDAC