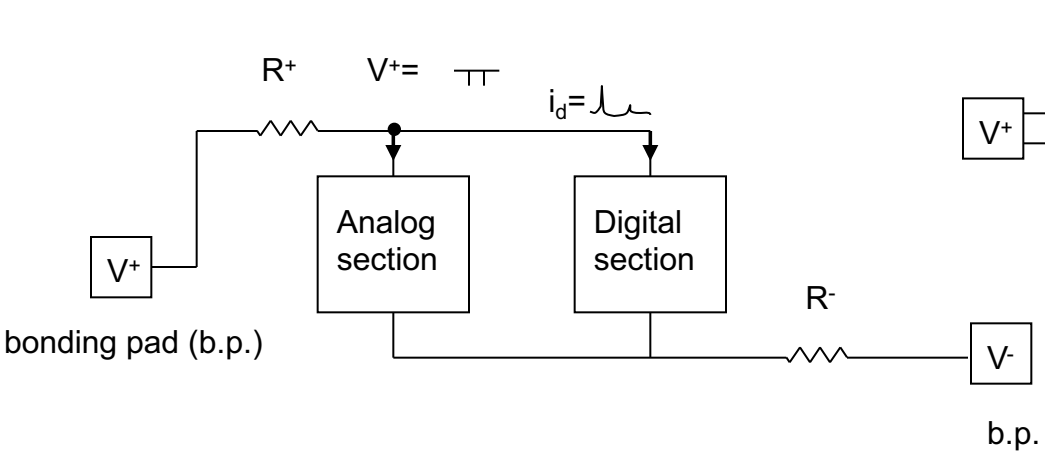
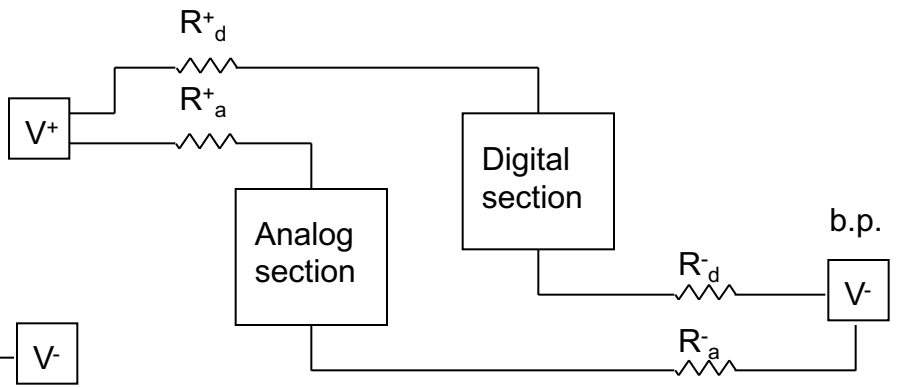
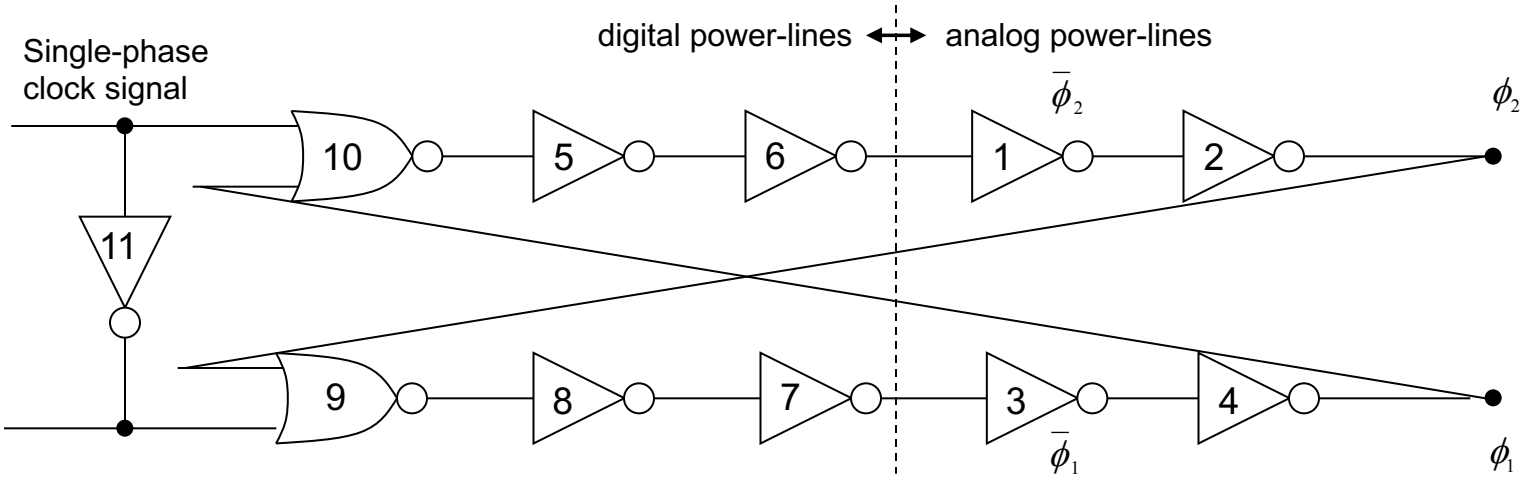
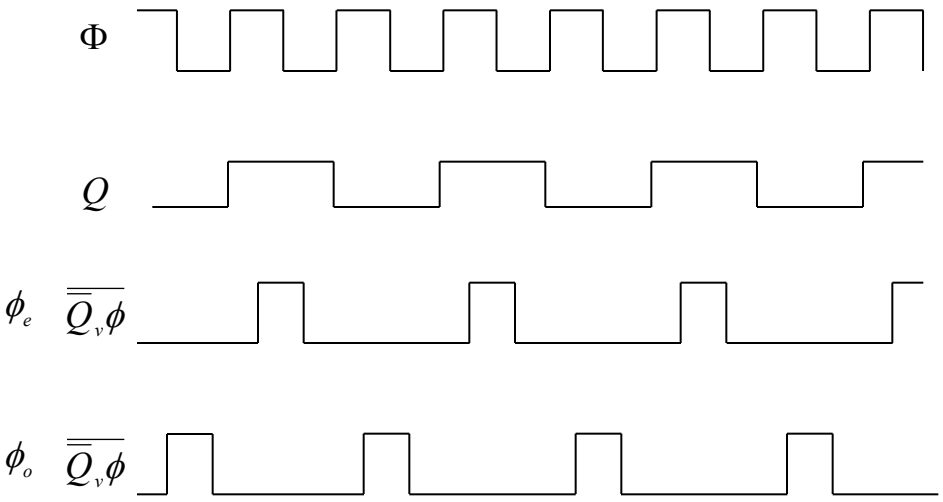
The series resistance in power lines

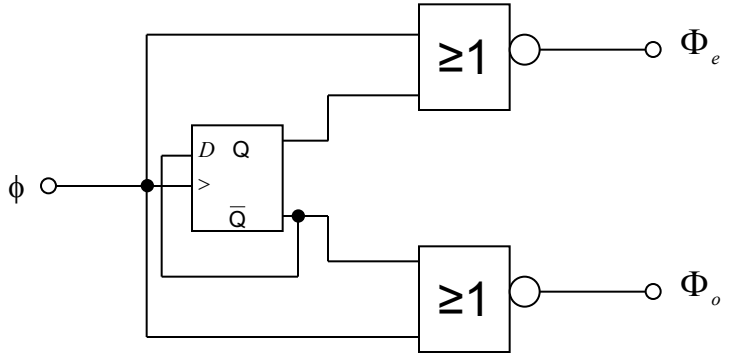




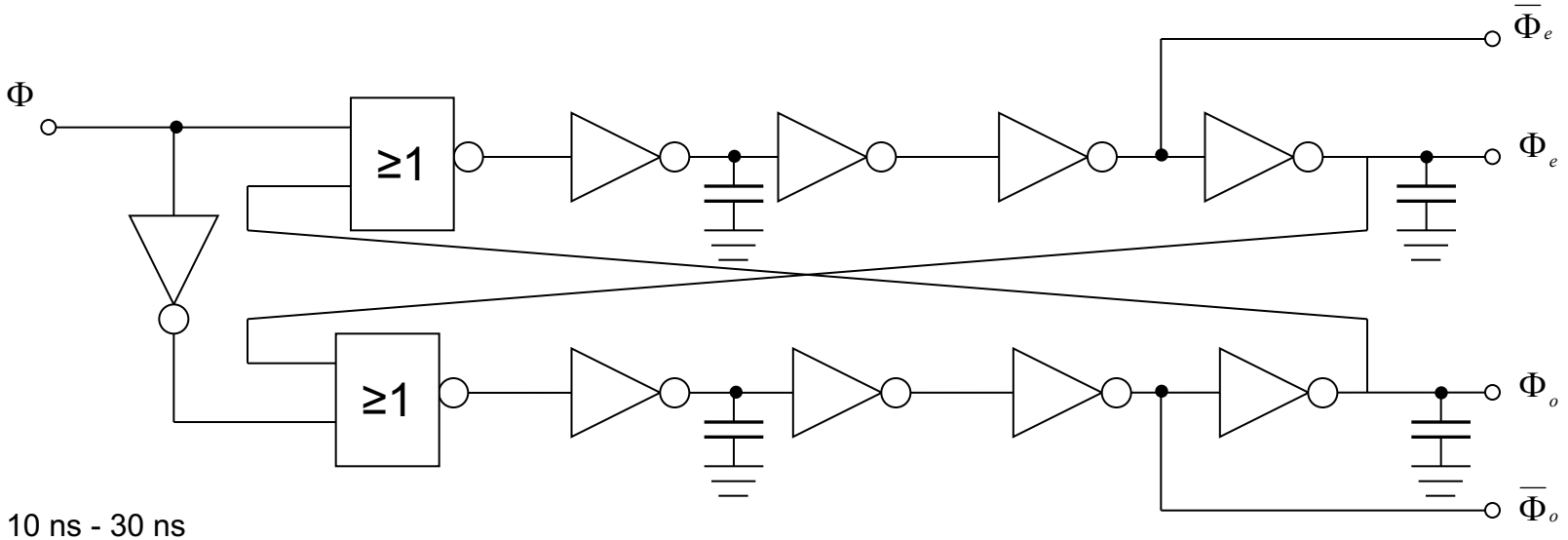


The power routing of the clock-generator

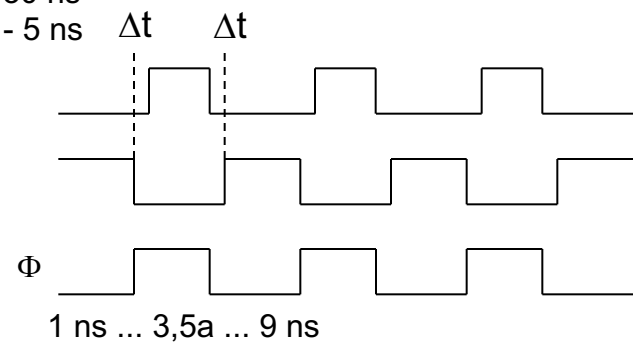


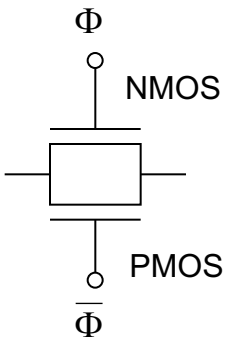


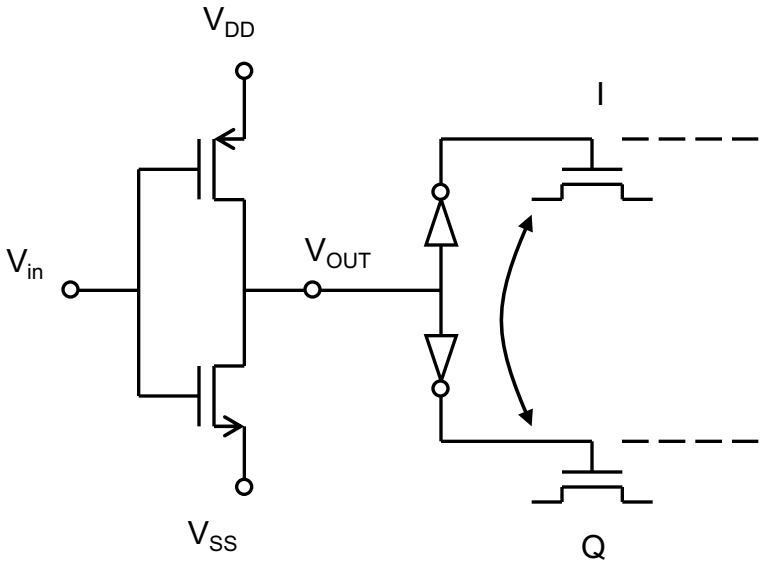
Non-overlapping clock generation for SC-circuits.



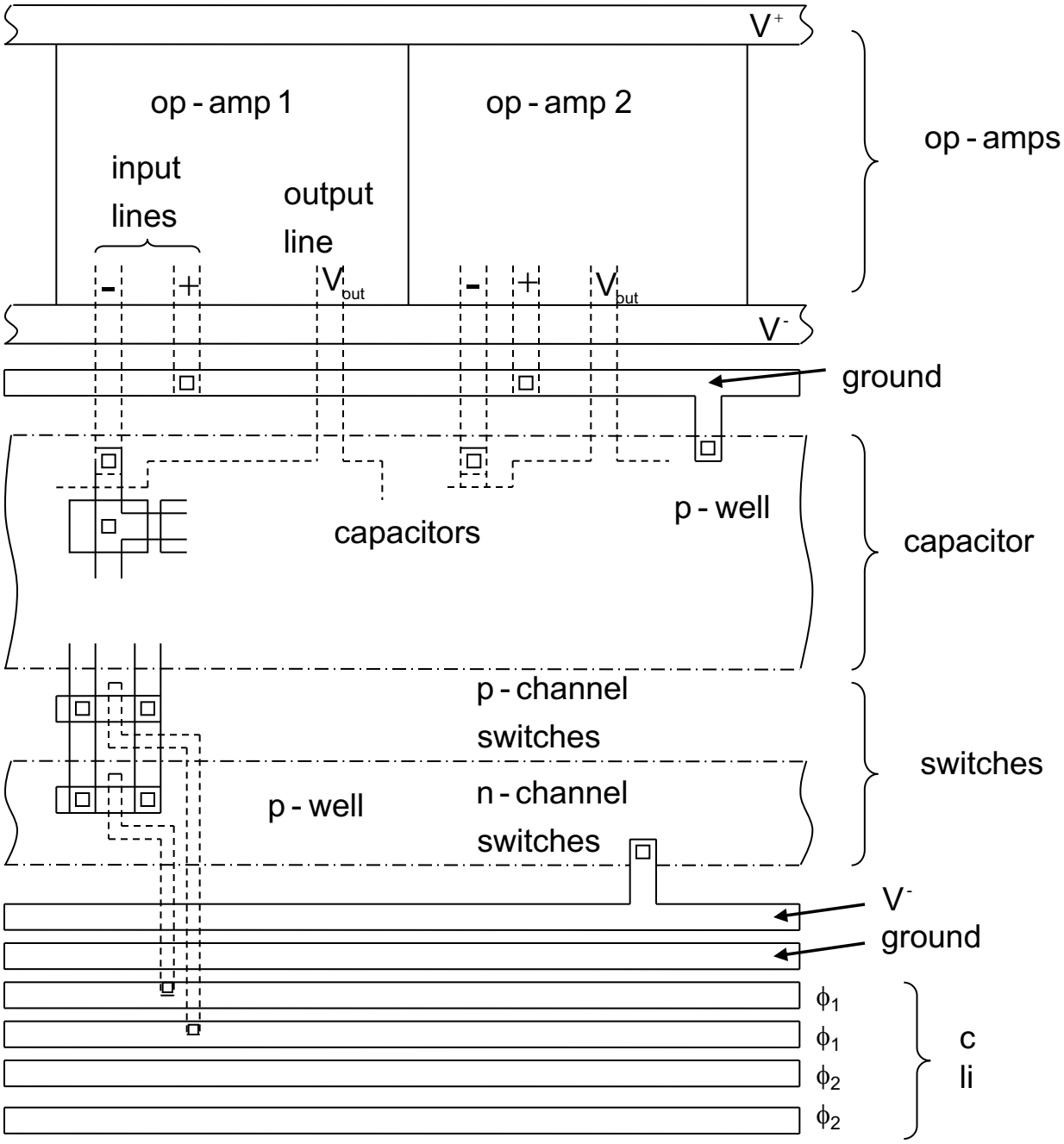
10 ns - 30 ns
Δt 1 ns - 5 ns



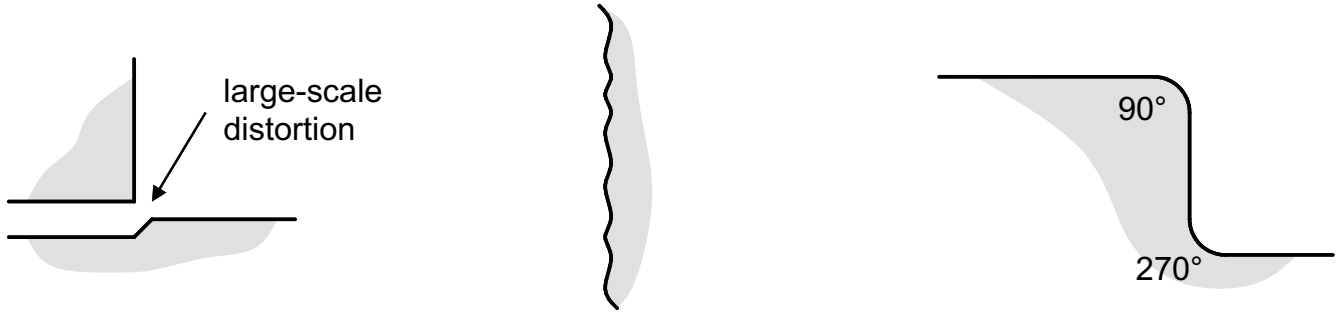



V_{DD}
I
V_{in}
V_{OUT}
V_{SS}
Q

Typical floorplan of an SC-circuit

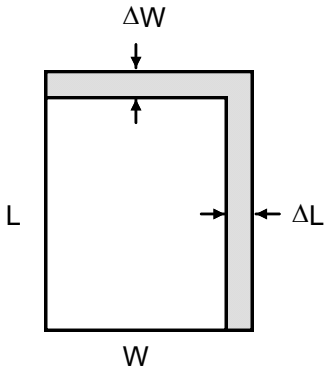


Nonideal effects in switched-capacitor circuits



(a) large-scale distortion (b) random edge location (c) corner rounding

Different forms of nonuniform undercut.



$$z_L = z_w \Rightarrow \varepsilon = \frac{z_C}{C} = z_L\sqrt{w^{-2} + L^{-2}}$$

$$\text{ol. } L = w \Rightarrow \varepsilon = \frac{\sqrt{2}z_L}{L} \approx \frac{\sqrt{2}z_L}{C^{\frac{1}{2}}}$$

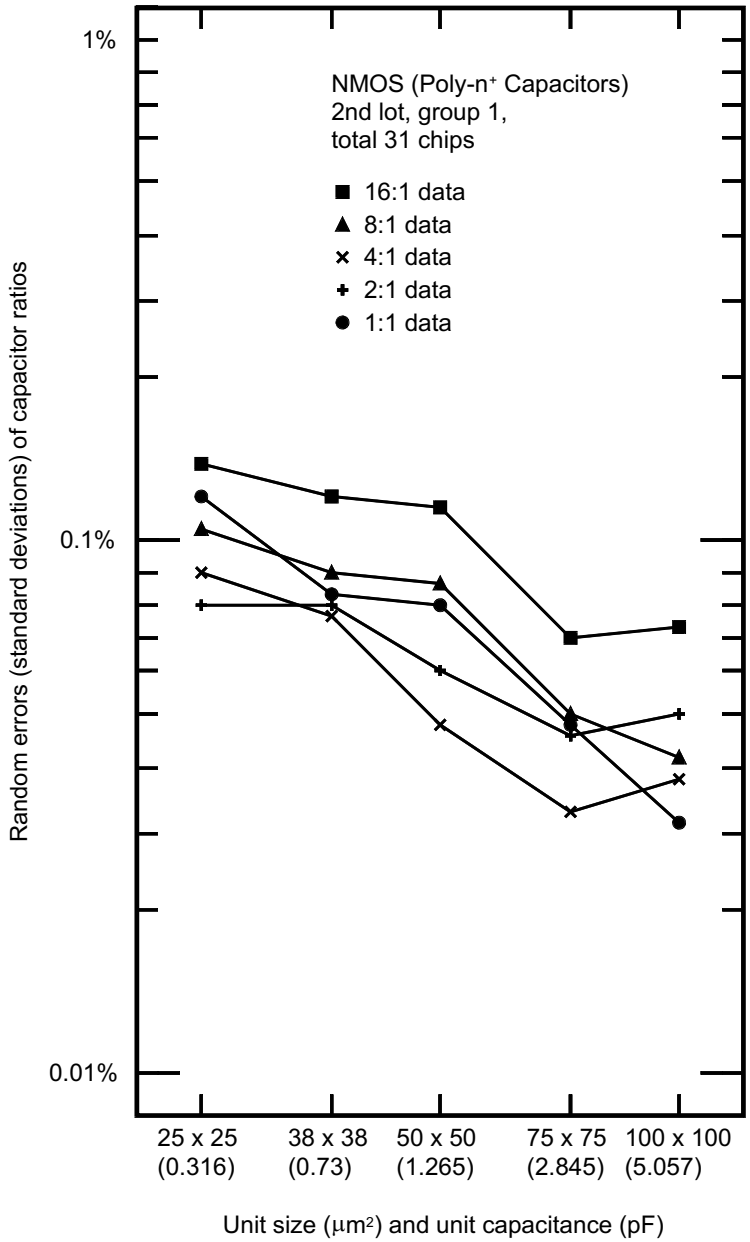
capacitance ratio:

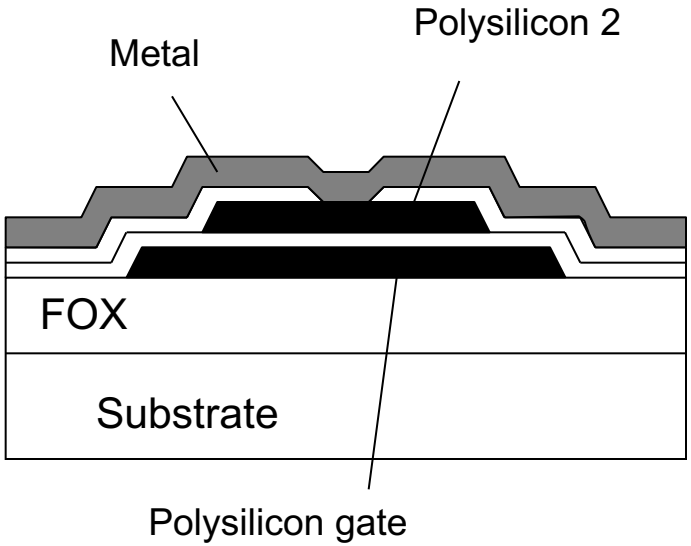
$$\alpha = \frac{C_L}{C_Z}$$

$$\varepsilon = \frac{z_\alpha}{\alpha} = z_L\sqrt{L_1^{-2} + w_1^{-2} + L_2^{-2} + w_2^{-2}}$$

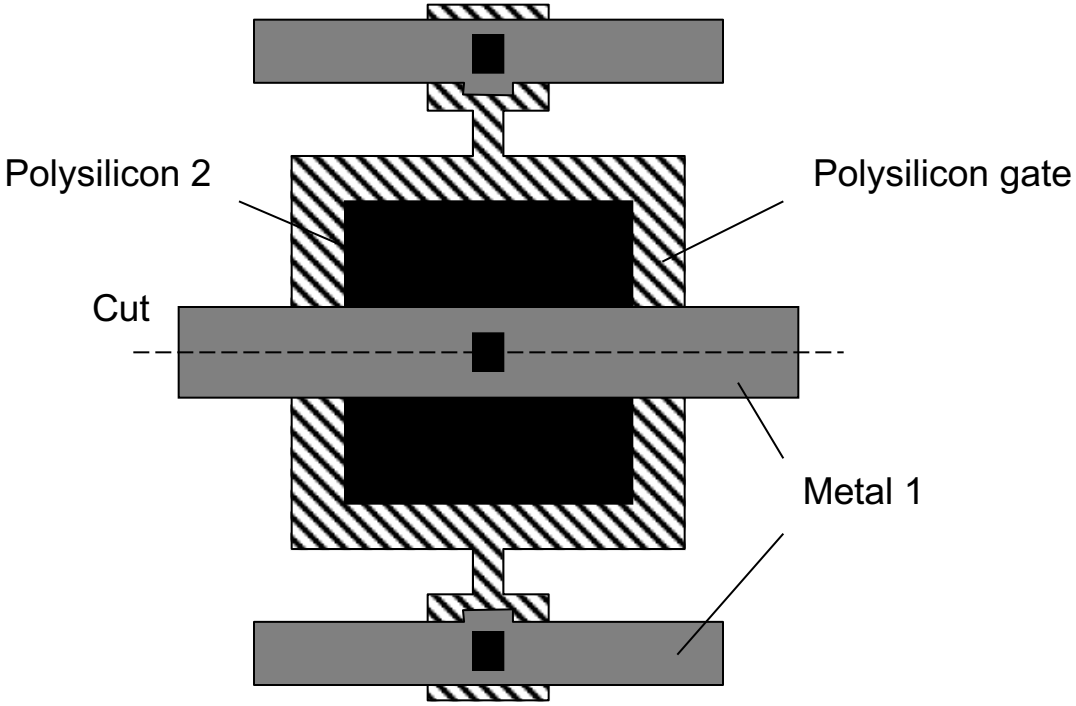
$$\text{ol. } L_1 = w_1 = L_2\sqrt{\alpha} = w_2\sqrt{\alpha}$$

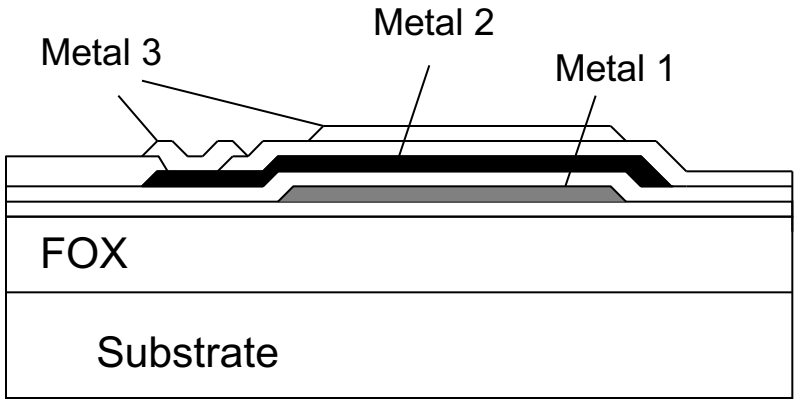
$$\varepsilon = \frac{z_L}{L_2}\sqrt{2(1+\alpha)}$$

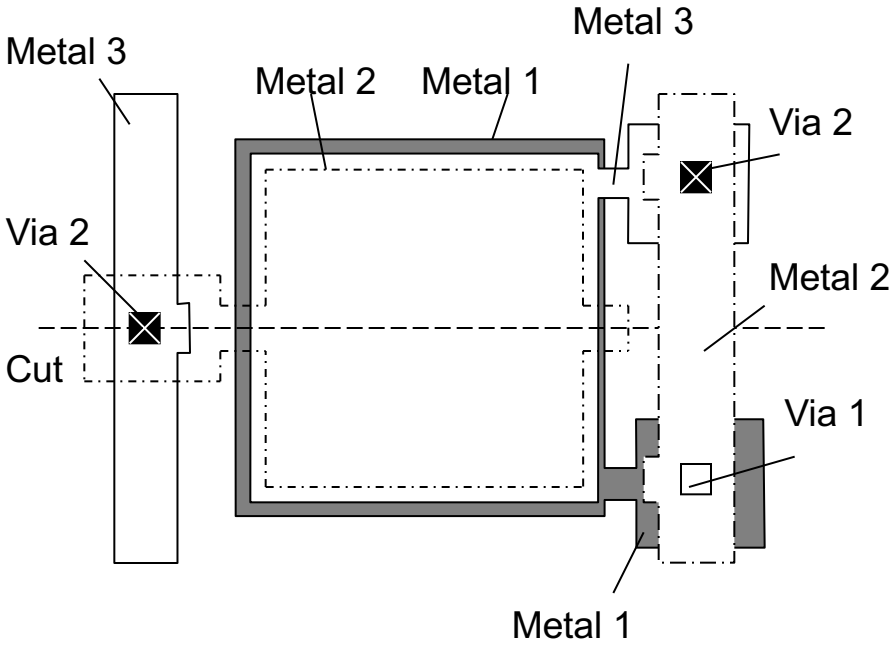




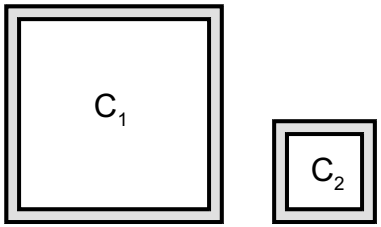
Double-polysilicon capacitor







Triple-level metal capacitor

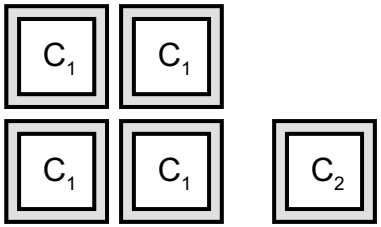


$$\frac{C_1}{C_2} = 4$$

$$\frac{C_1'}{C_2'} = \frac{C_1 + C_{p1}}{C_2 + C_{p2}} \neq 4$$

$$\frac{C_1}{C_2} = 4{,}333$$

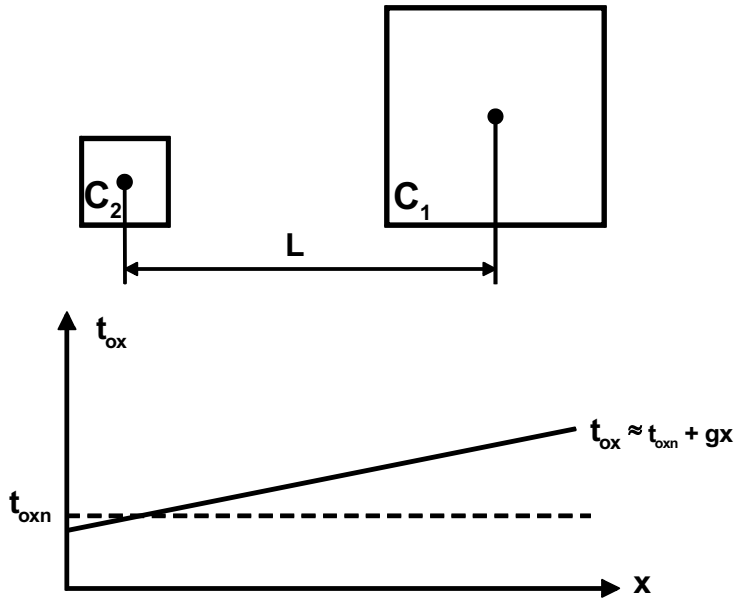
$$3 \cdot C_{unit} + 1{,}333 \cdot C_{unit}$$



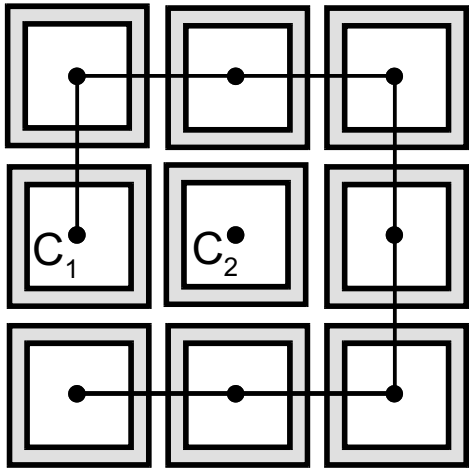
$$C_1 = 4C_2$$

$$C_1' = 4C_2' = 4\left(C_2 + C_{p2}\right)$$

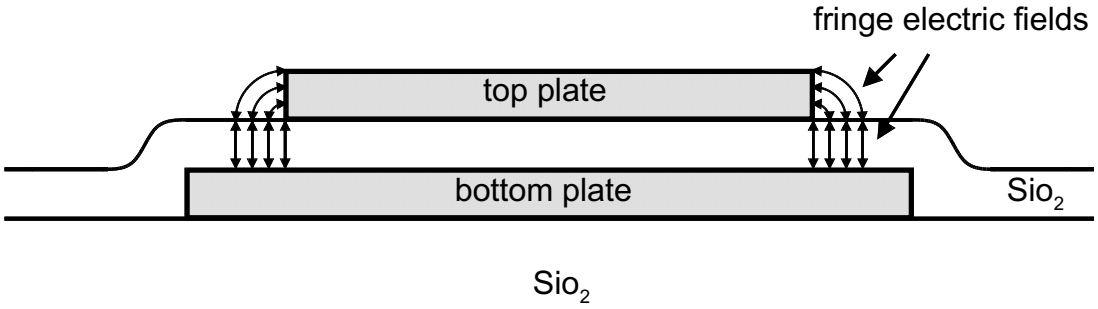
Capacitor lay-out with and without unit capacitors



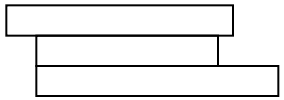
Capacitor ratio error due to thin-oxide gradient.



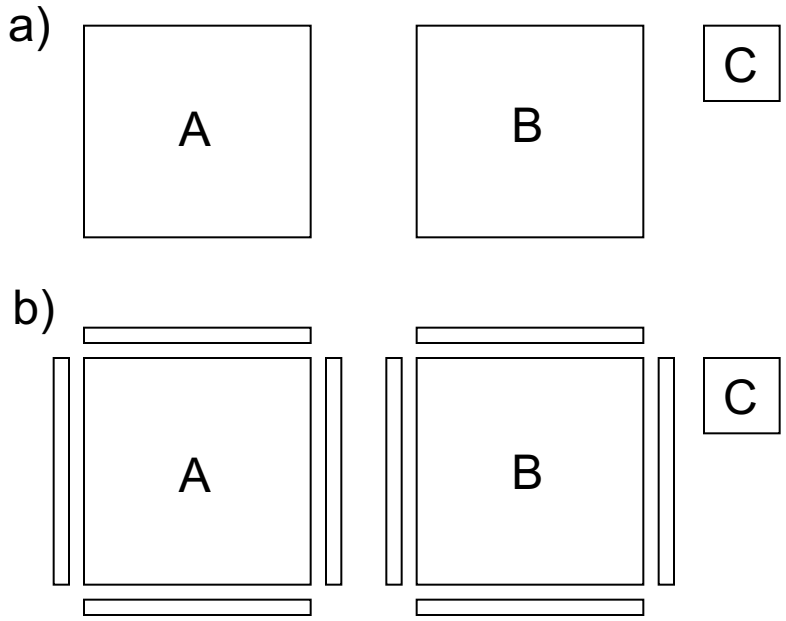
Common centrode geometry of capacitors



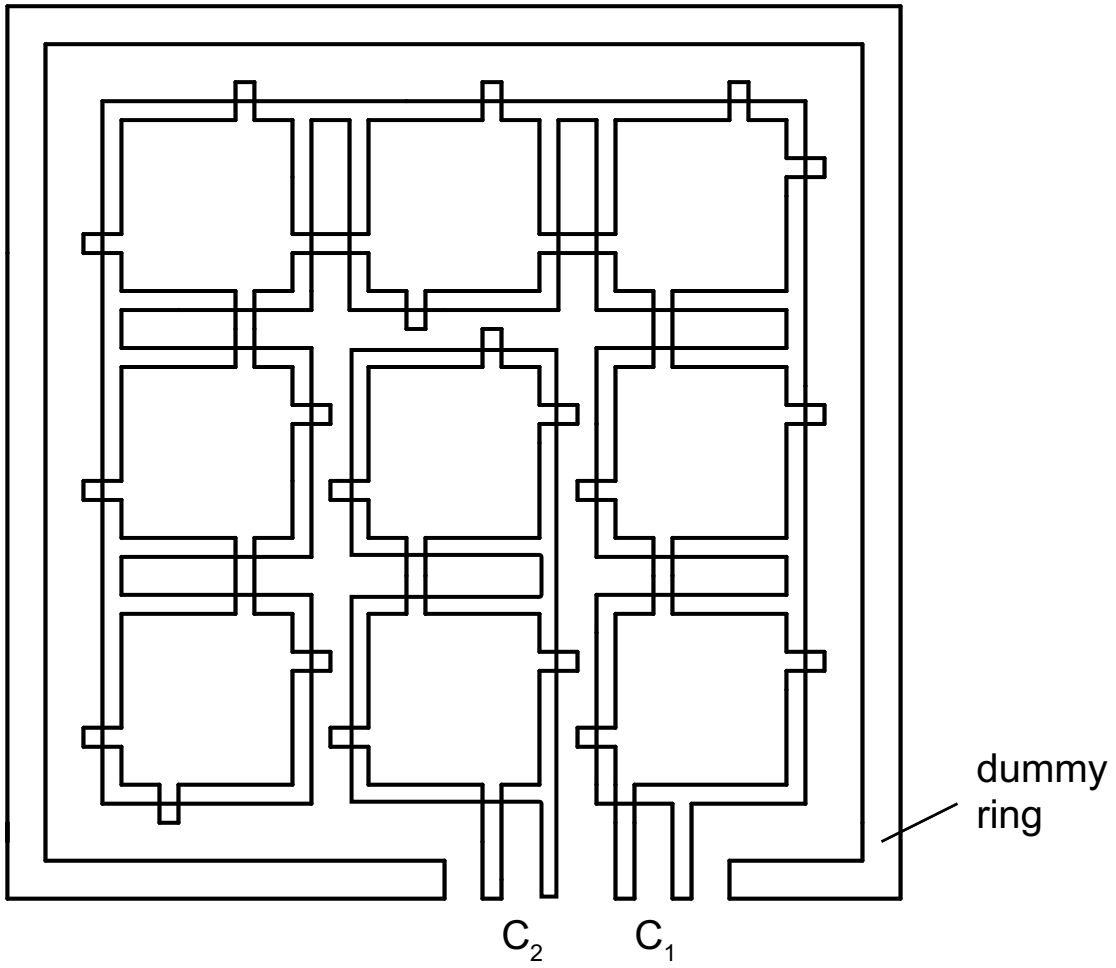
The fringing field of planar capacitors



$$C_1 = C_{ox} \cdot A_1 + C_p' P_1$$
$$C_2 = C_{ox} \cdot A_2 + C_p' P_2$$
$$\Rightarrow \frac{A_1}{A_2} = \frac{P_1}{P_2}$$



a) Illustration of how matching of A and B is disturbed by the presence of C.
b) Improved matching achieved by matching surroundings of A and B.



Example of matched C ratio of 3.5.

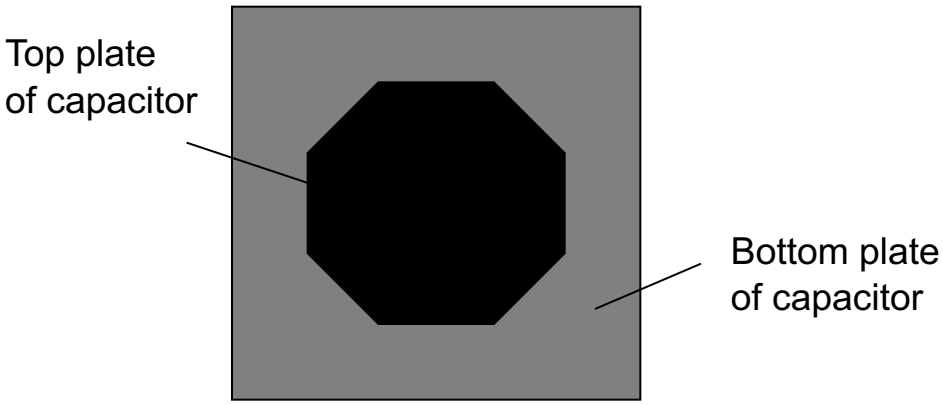
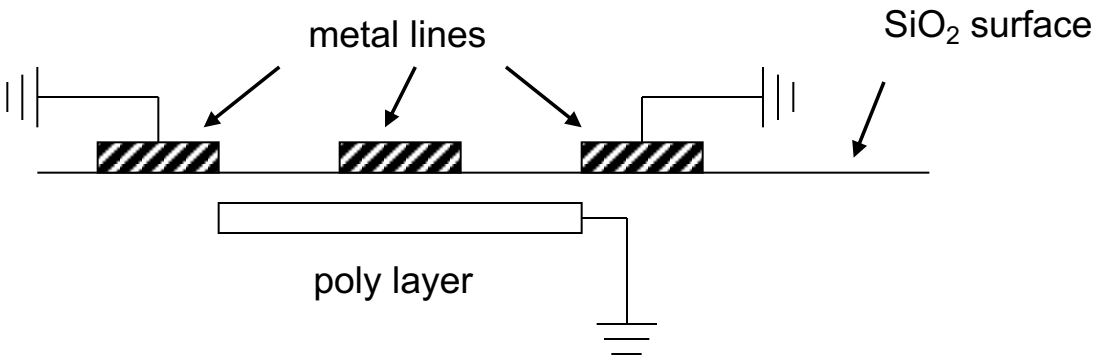
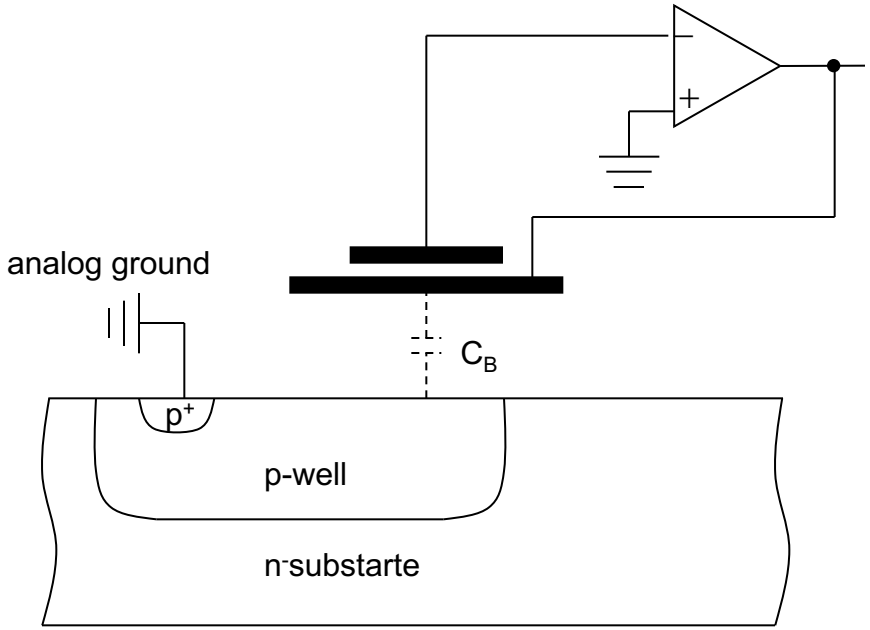


Illustration of a capacitor using an octagon to approximate a circle to minimize the ratio of perimeter to area.



The shielding of sensitive signal lines.



The shielding of the bottom plate capacitor.