CMOS technology

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Chapter 26

Previous material

- All process steps
- Integration
- MEMS

CMOS steps

- Main process steps:
  - High temperature processing
    - Oxidation
    - Diffusion
    - Fusion bonding
  - Film deposition
  - Lithography
  - Etching
  - CMP

  - Silicide formation

Doping doses and units

- Volume concentration, at/cm^3, ion/cm^3
  - Real doping
  - Si atom concetration 4.5×10^{22} Si/cm^3
  - Semiconductor doping is always < 1 at%, i.e., < 4×10^{20} P/cm^3.
  - Highest doping takes place in poly-SI, 1×10^{20} at/cm^3

- Surface concetnration, ion/cm^2
  - Technological approach, used in implantation
  - Surface concentration = (volume concentration)$^{2/3}$
  - Si atom surface concentration $(4.5\times10^{22})^{2/3} = 1.3\times10^{14}$ Si/cm^2
  - Implantation dose 10^{12}-10^{16} P^+/cm^2, energy 20-200 keV

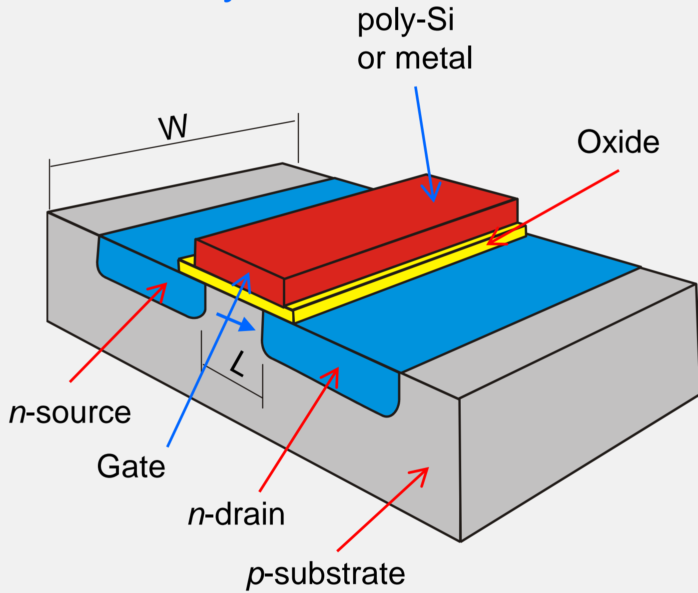
Content

- MOS (MOSFET) transistor
- Self-alignment concept
- 5 µm polysilicon gate CMOS transistors
- LDD, silicide and STI
- New oxide materials

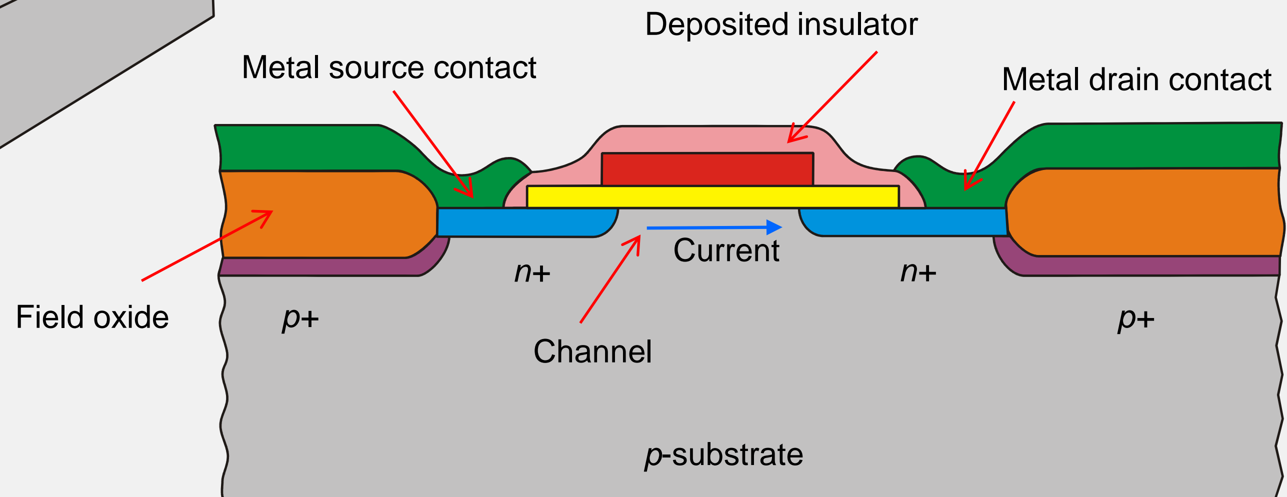
n-channel MOSFET transistor

Theory

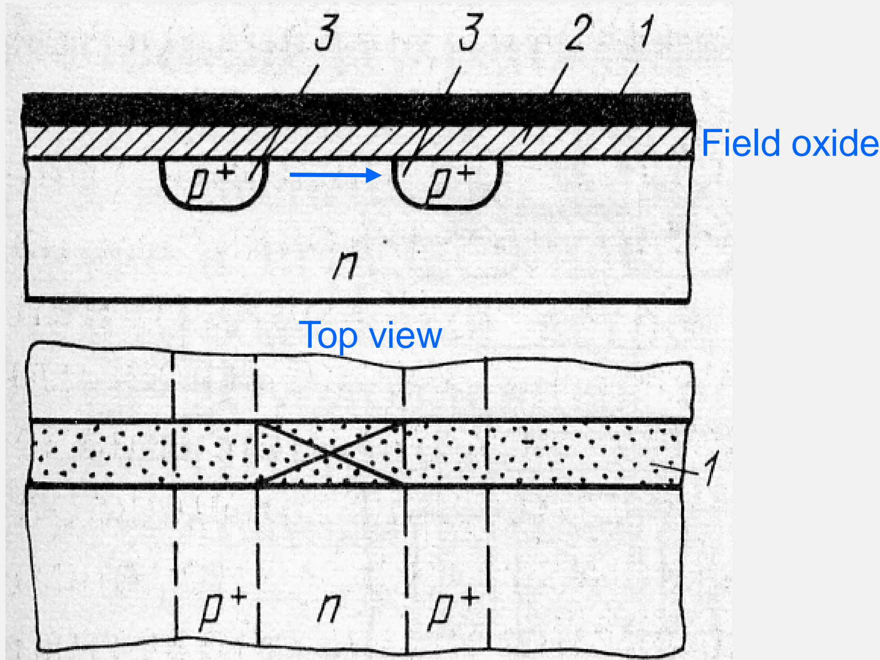
MOS – Metal Oxide Semiconductor



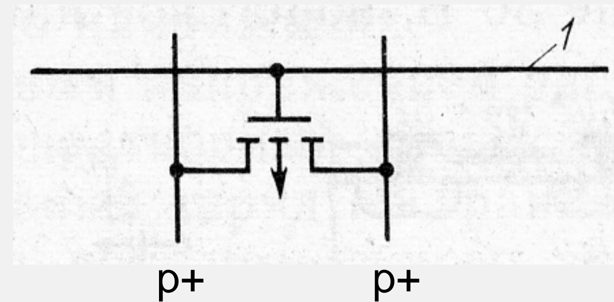
Real life



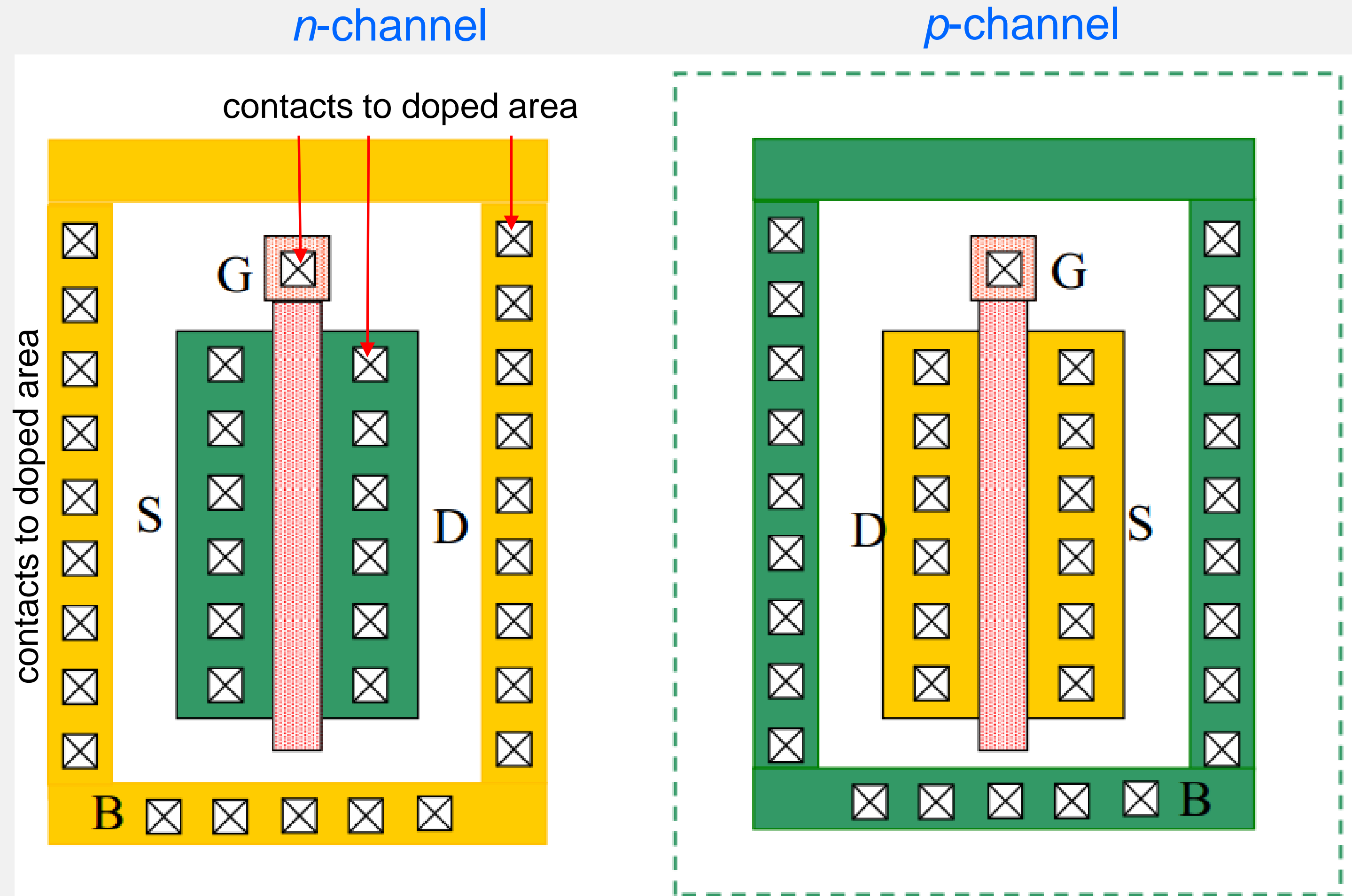
Parasitic *p*-channel MOS transistor



1 – Al
2 – SiO_2
3 – diffused area



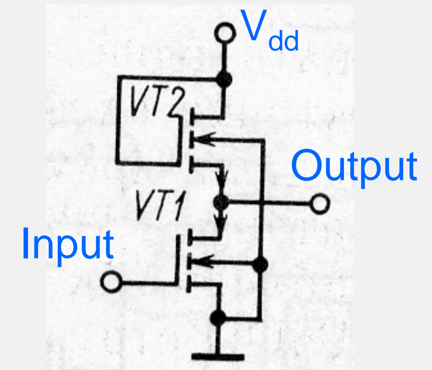
Transistor isolation by guard rings (top view)



n-channel MOS inverter

Input
G1
VT2
A
A
D1
VT1
S1D2
S2G2
Ground
Output
V_{dd}

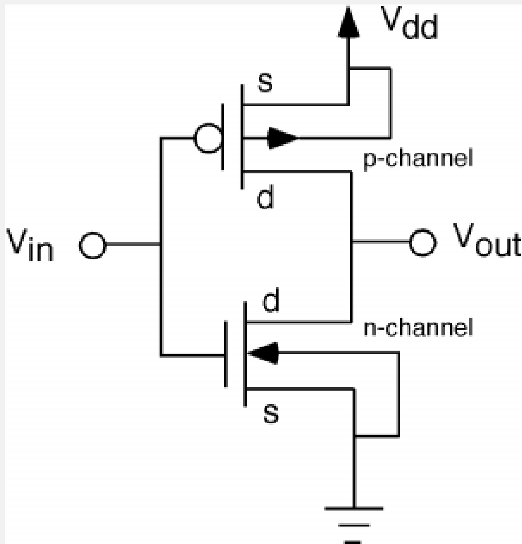
A-A
SiO_2
Al
n^+
VT1
n^+
VT2
n^+
p

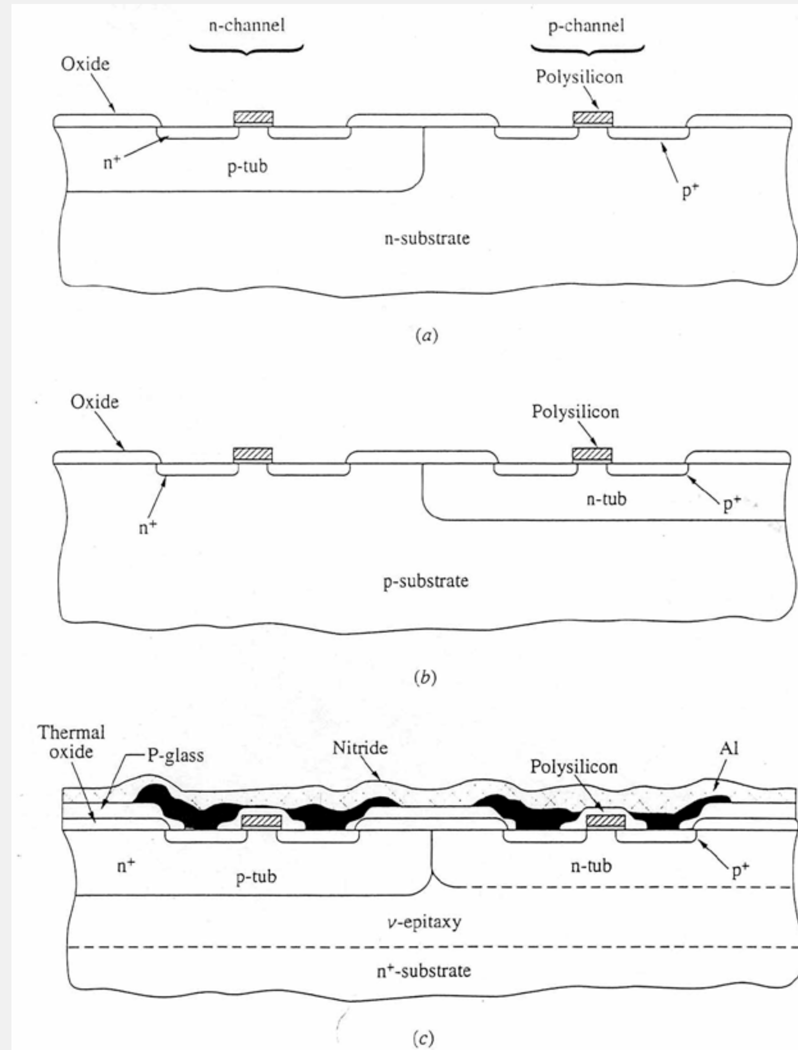


Only Al gate, not poly-Si!

CMOS inverter

CMOS – complementary metal–oxide–semiconductor





p-well

n-well

twin-well

Old - Al gate
New - poly-Si gate

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- 5 µm polysilicon gate CMOS transistors
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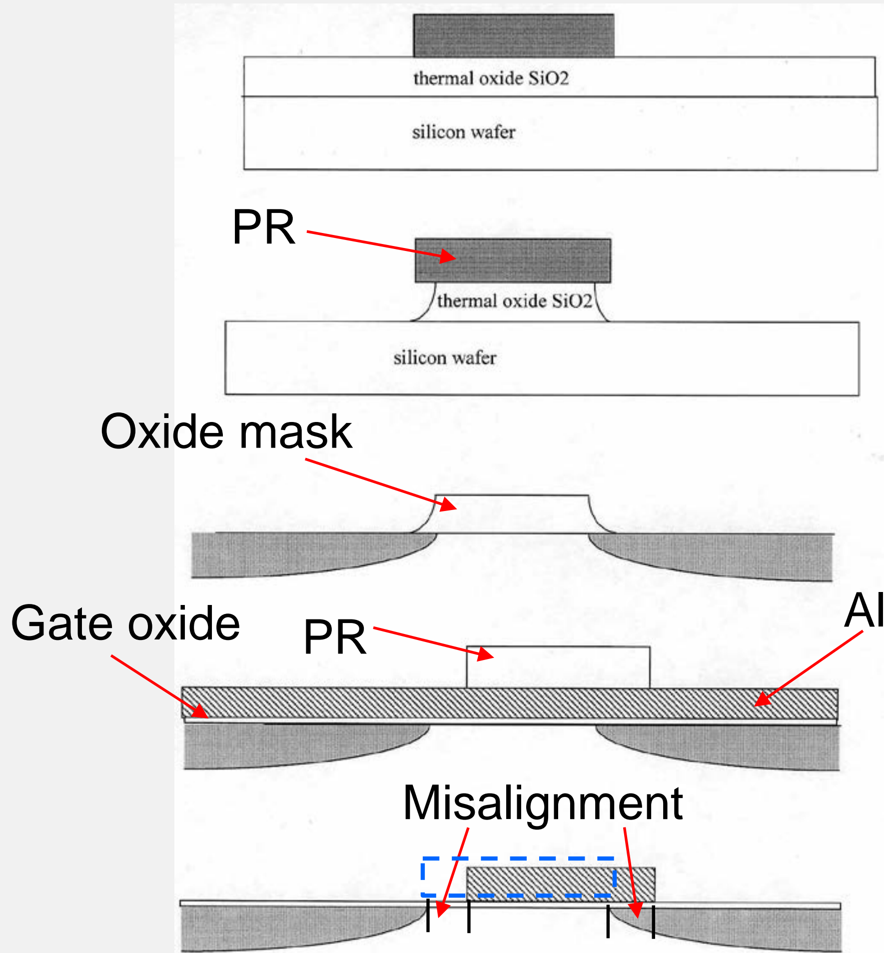
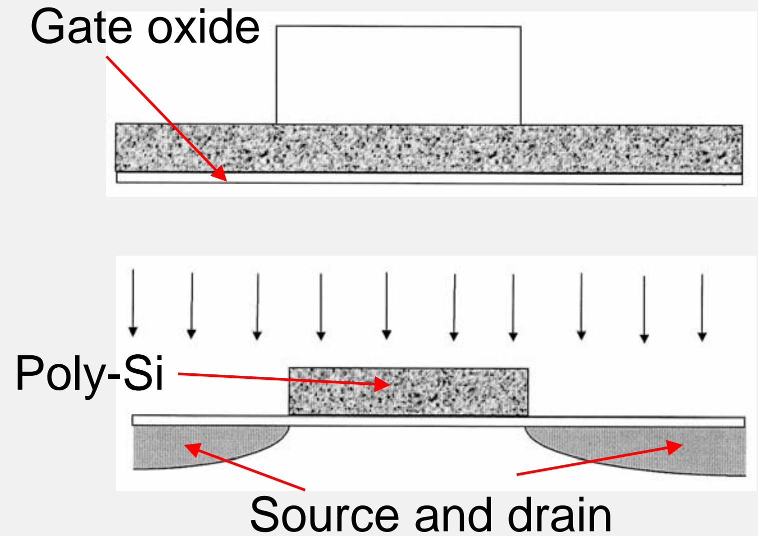
MOSFET gate alignment

Lithographic alignment. Diffusion

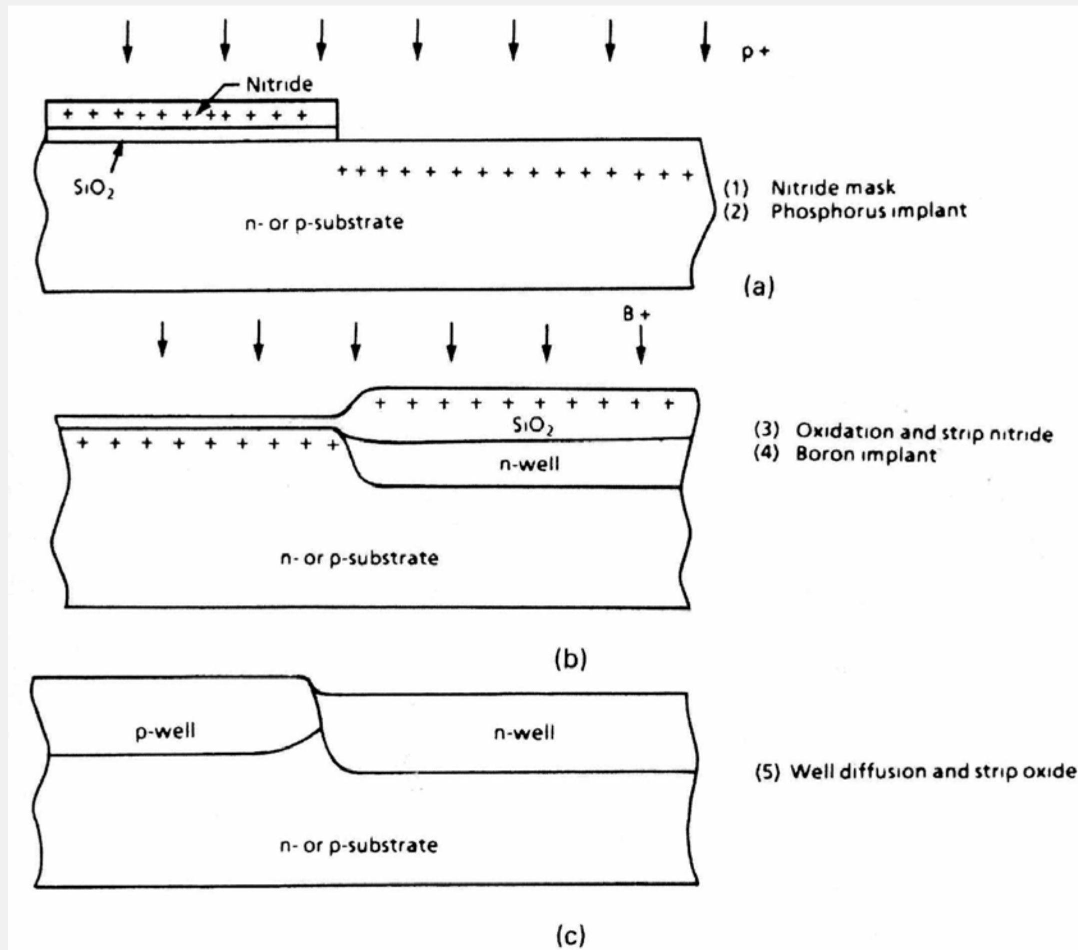


Self-alignment. Implantation



Theoretical misalignment is zero!

Self-aligned wells



Content

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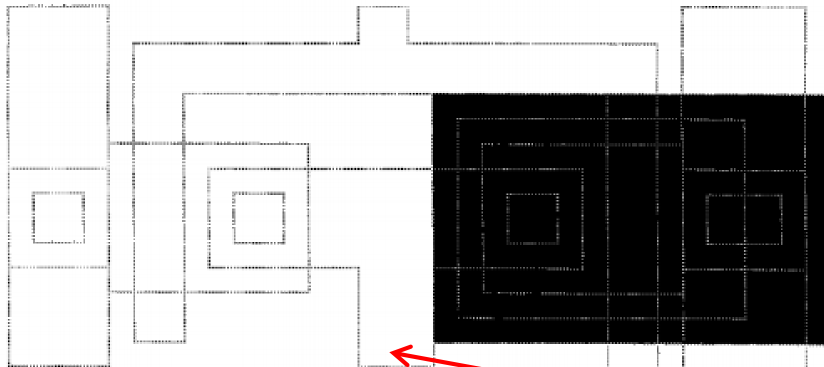
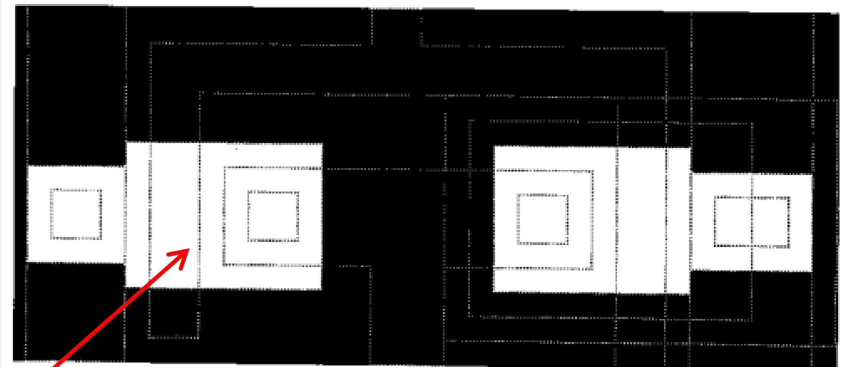
Polysilicon gate CMOS inverter I

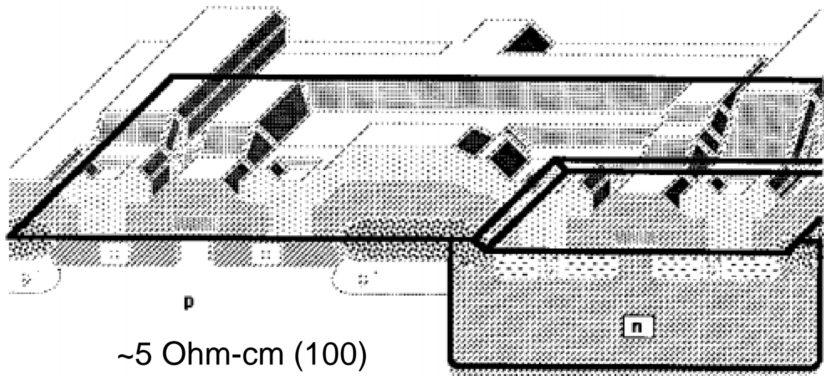
n-well implant (P, 50 keV, 10^{13} cm^{-2}) and drive-in (1150 °C, 8 h)

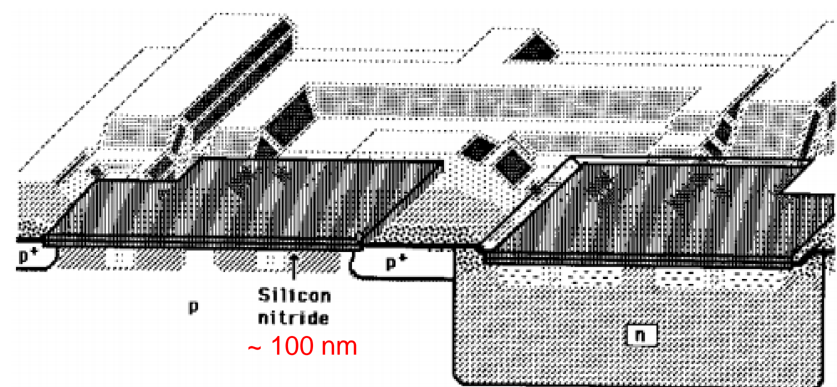
Channel-stop implant (B, 30 keV, 10^{12} cm^{-2}) Si_3N_4/SiO_2 mask





PR protected areas





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Polysilicon gate CMOS inverter II

Field oxide growth (LOCOS, 1050 C, 6 h)
PMOS threshold implantation
(B, 50 keV, 10^{12} cm^{-2})

~ 1.2 µm

SiO_2

p^+

p

n

~ 4 µm

Gate oxide growth (blank)
1050 °C, 65 min

SiO_2

Gate oxide ~ 80 nm

p^+

p

n

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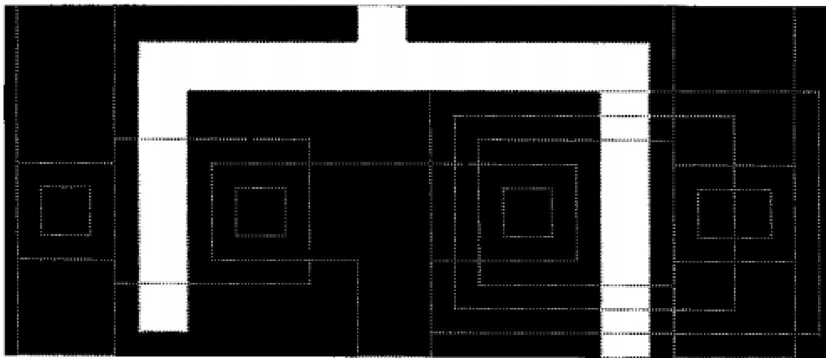
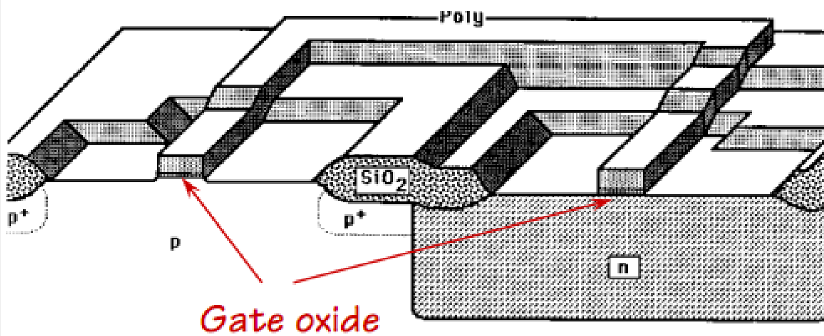
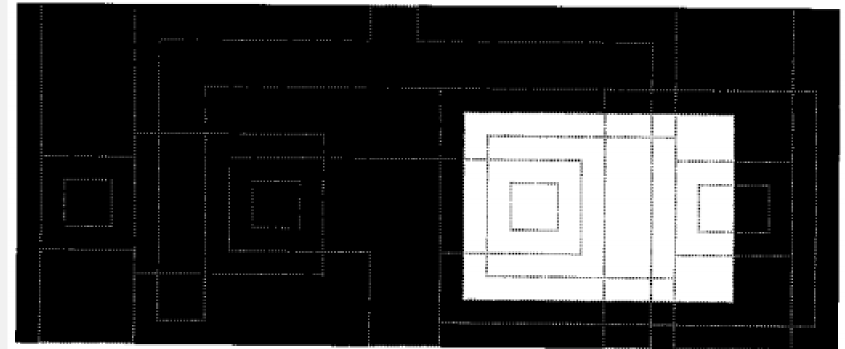
Polysilicon gate CMOS inverter III

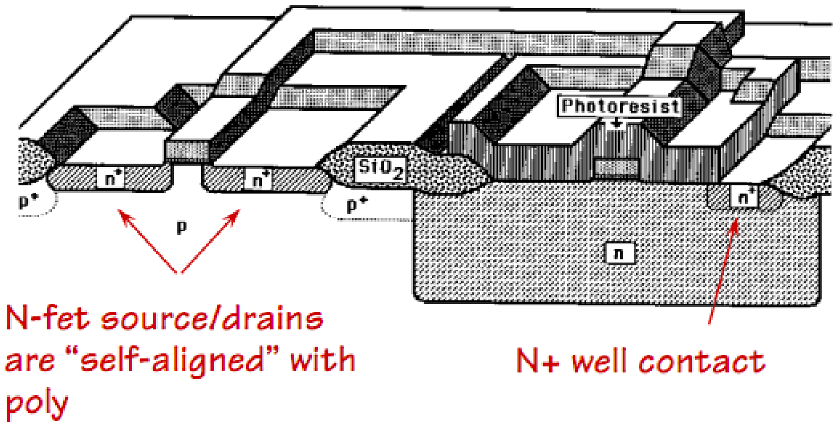
n+-poly (30 Ω/sq, 5×10^{19} cm^{-3}) deposition (500 nm) and dry etching





n^+ source/drain implant (50 keV, 10^{15} cm^{-2})





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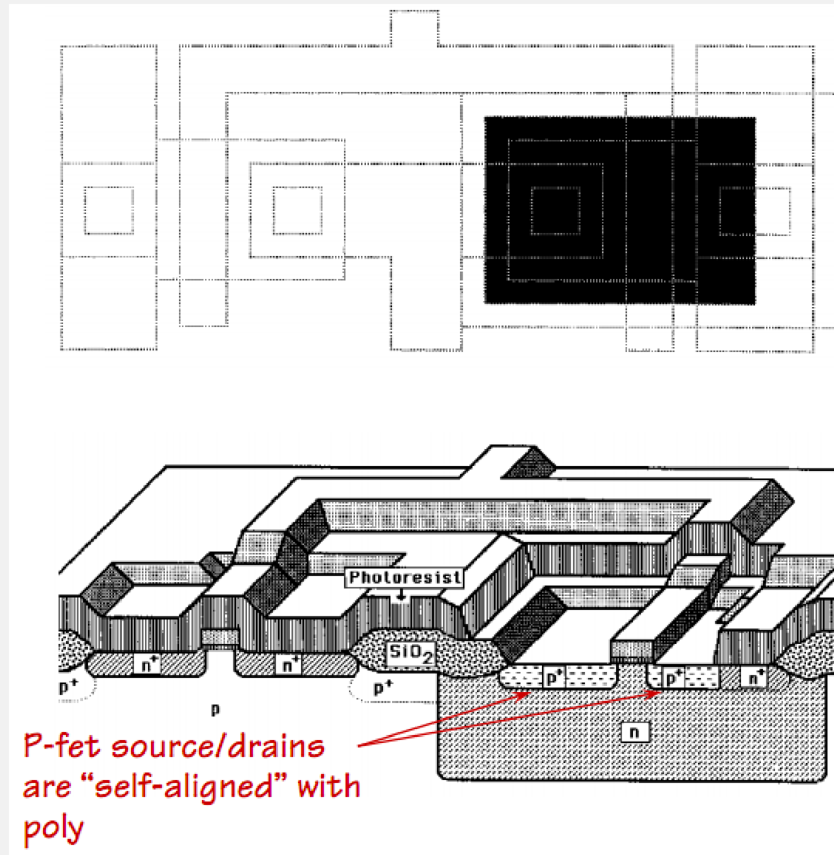
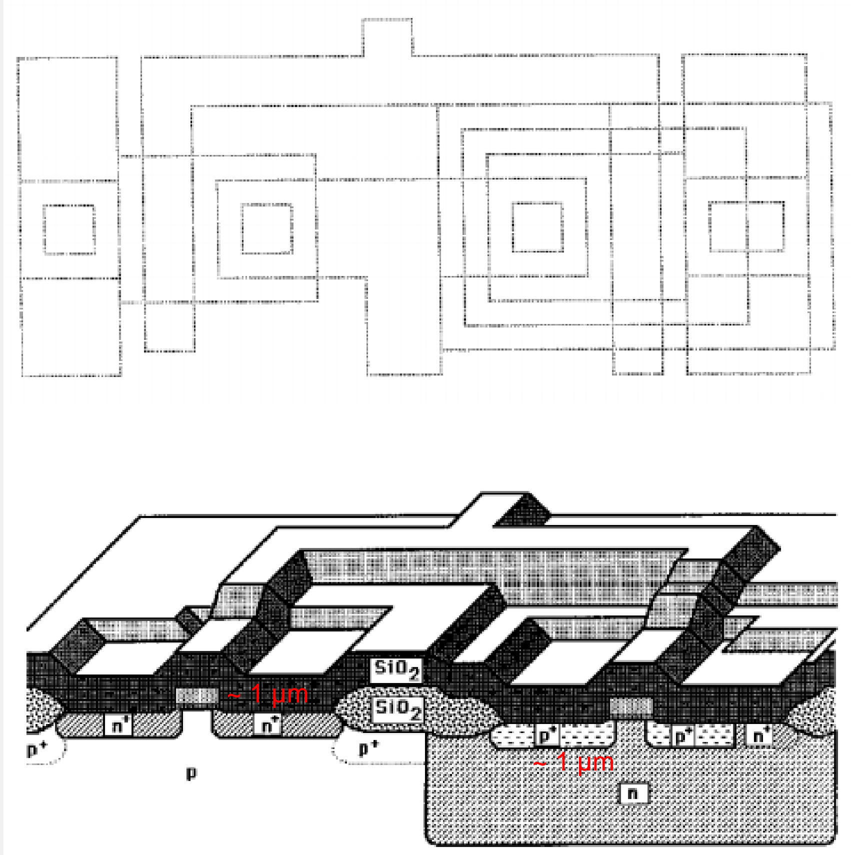
Polysilicon gate CMOS inverter IV

p^+ source/drain implant (40 keV, 10^{15} cm^{-2})



Interlayer CVD oxide (PSG)



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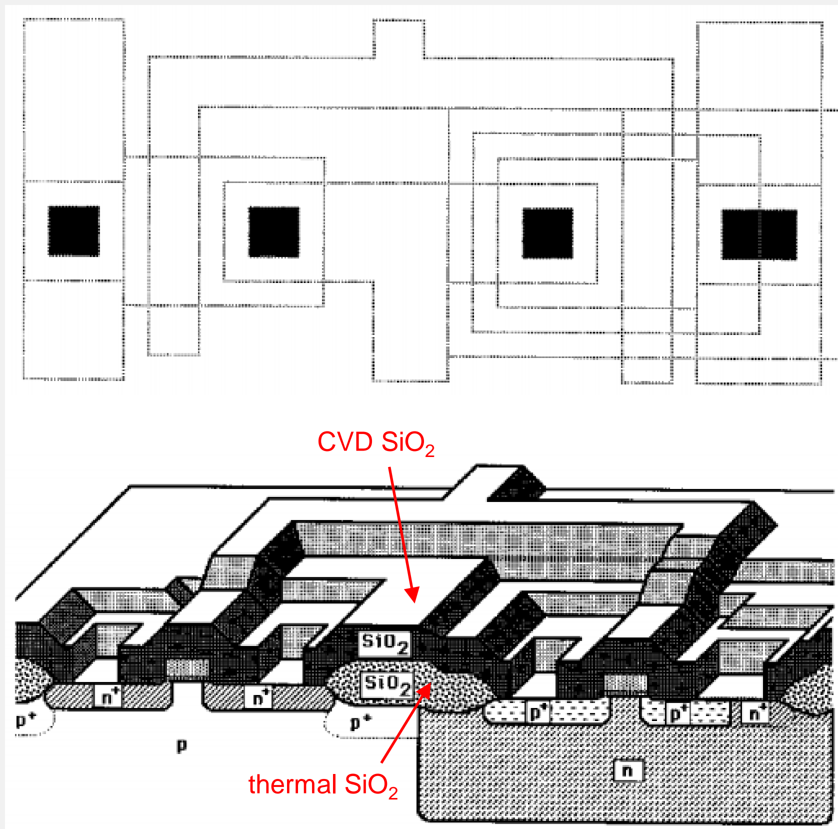
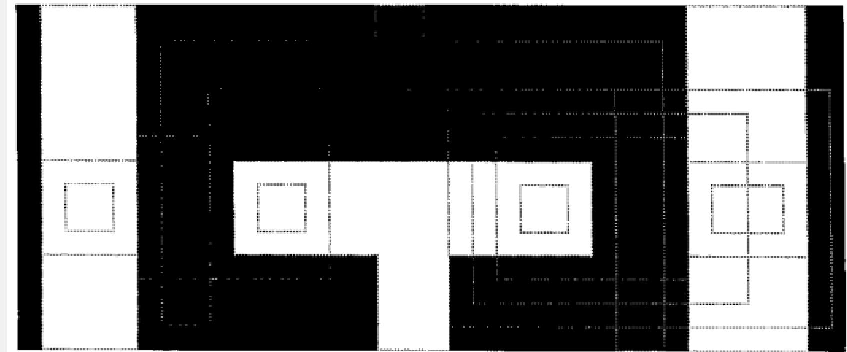
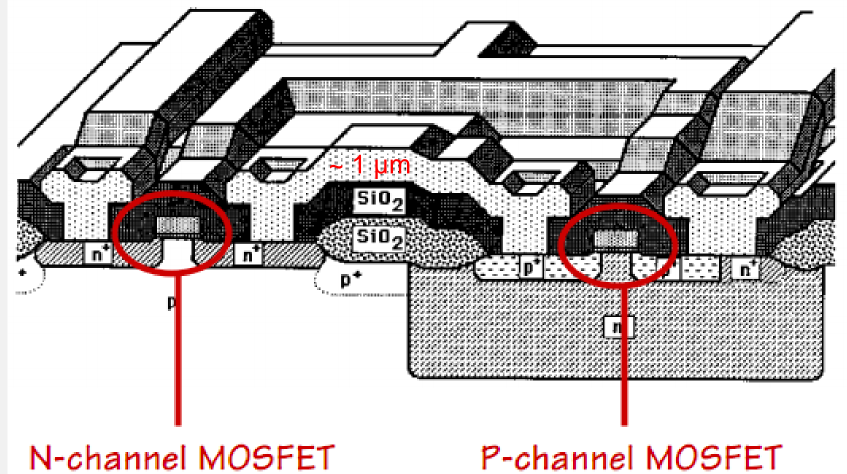
Polysilicon gate CMOS inverter V

Vias opening (wet)



Metal deposit and wet etching





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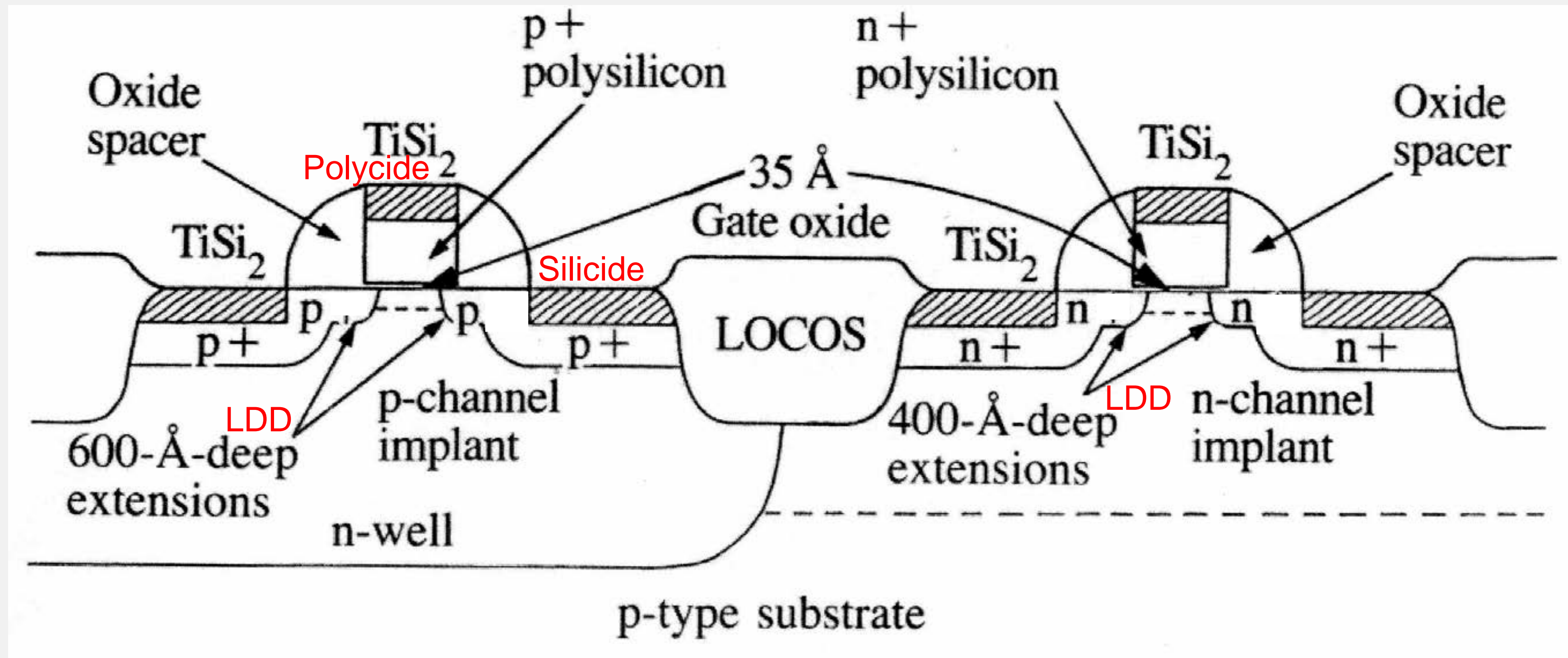
Content

- MOS transistor
- Self-alignment concept
- 5 um polysilicon gate CMOS transistors (8 masks)
- LDD, silicide and STI

0.5 µm CMOS with LDD

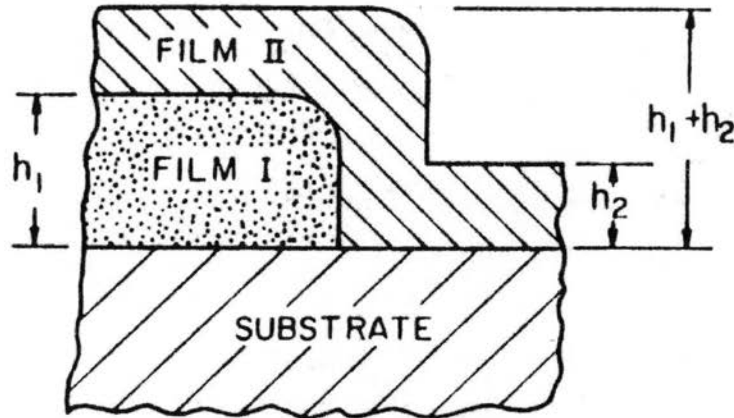


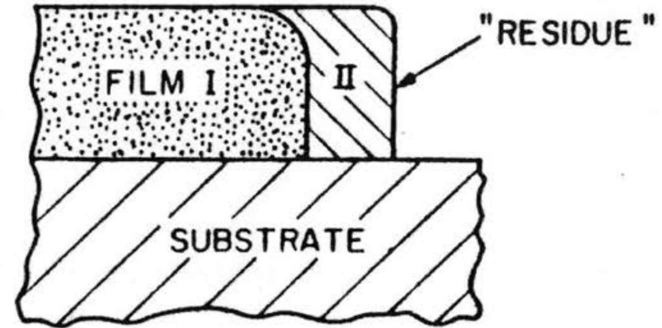
RTA for defect annealing

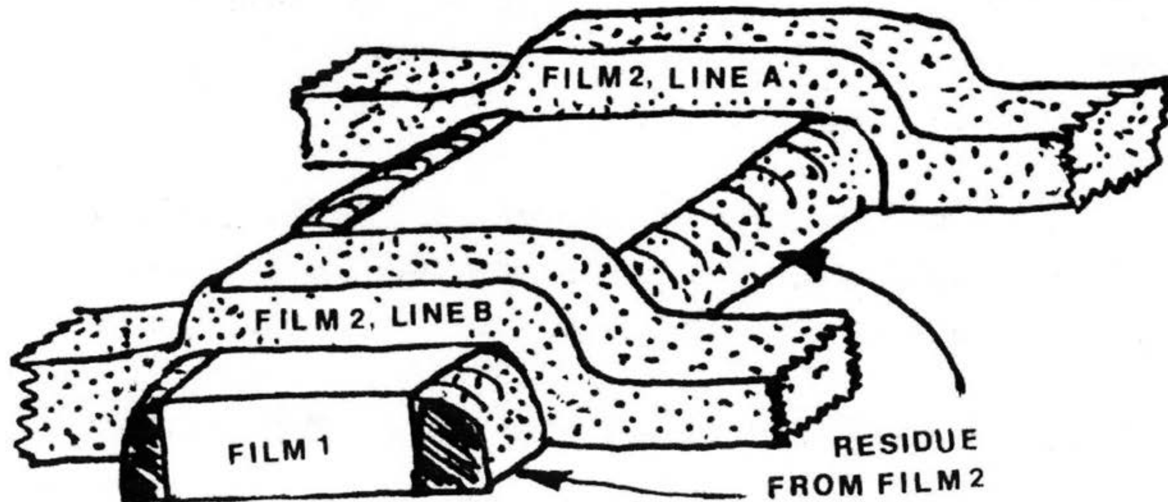
LDD size is less than photolithography resolution!

Spacers

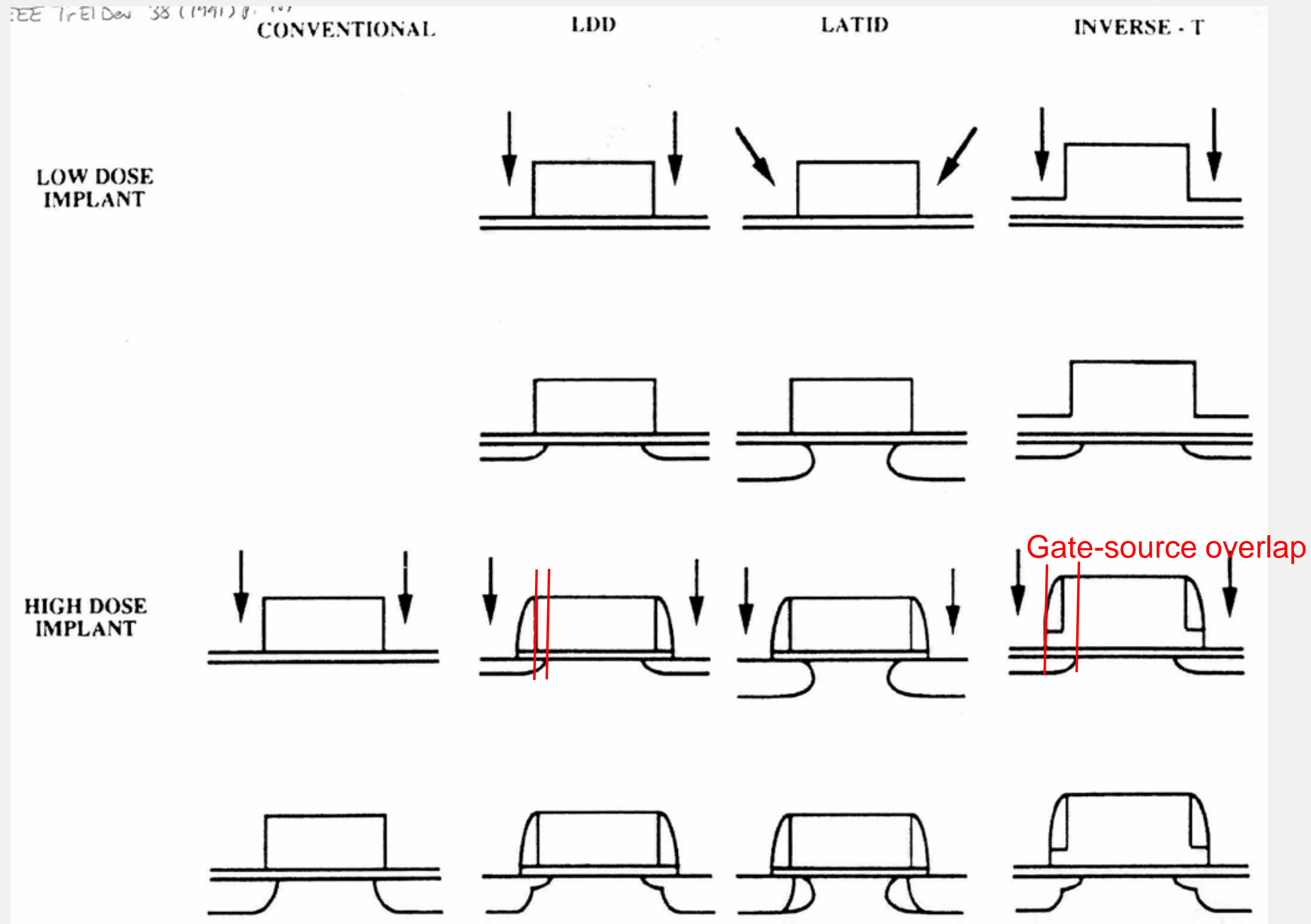
CONFORMAL DEPOSITION



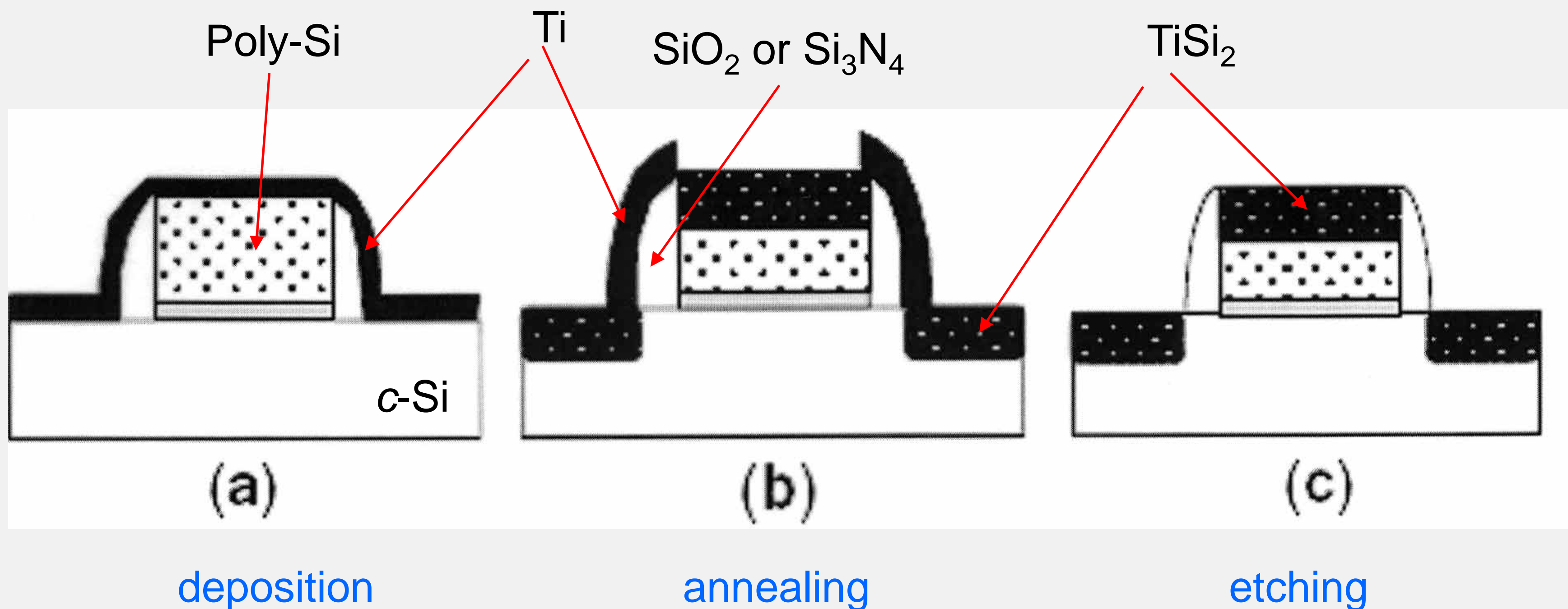




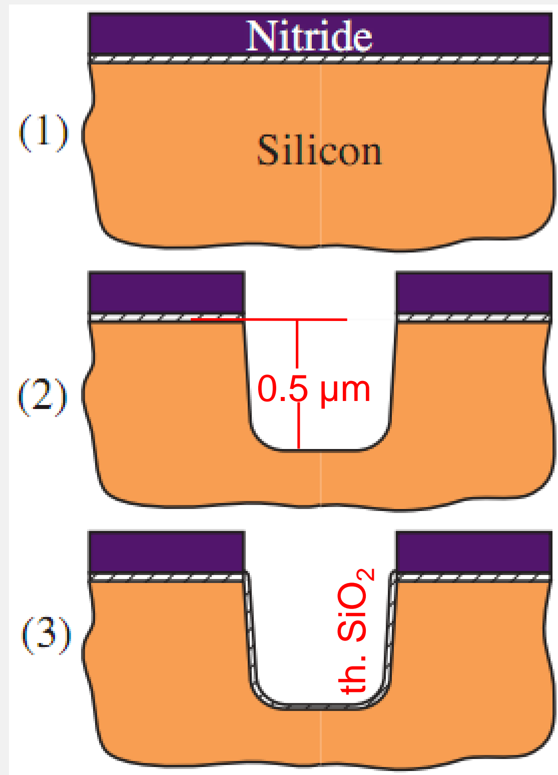
LDD variations

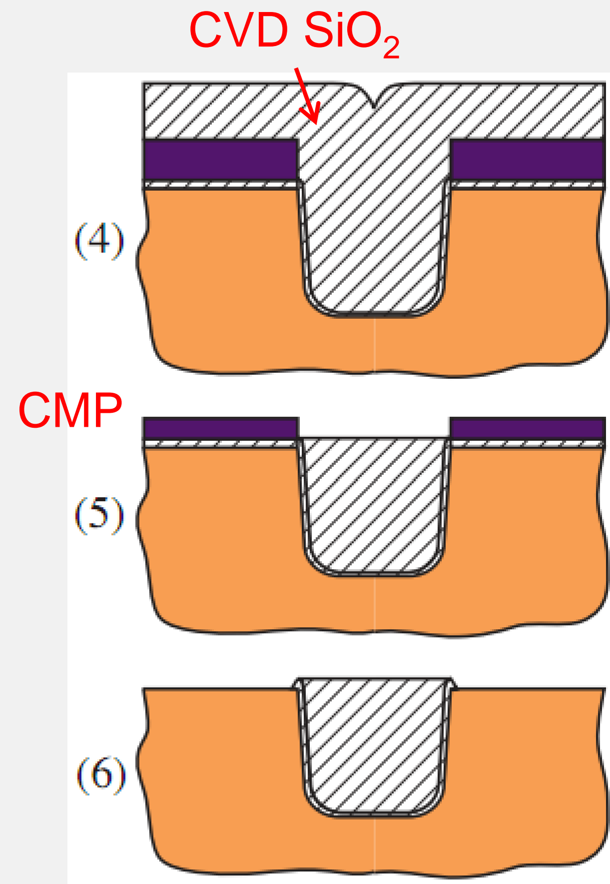


Self-aligned silicide (salicide)



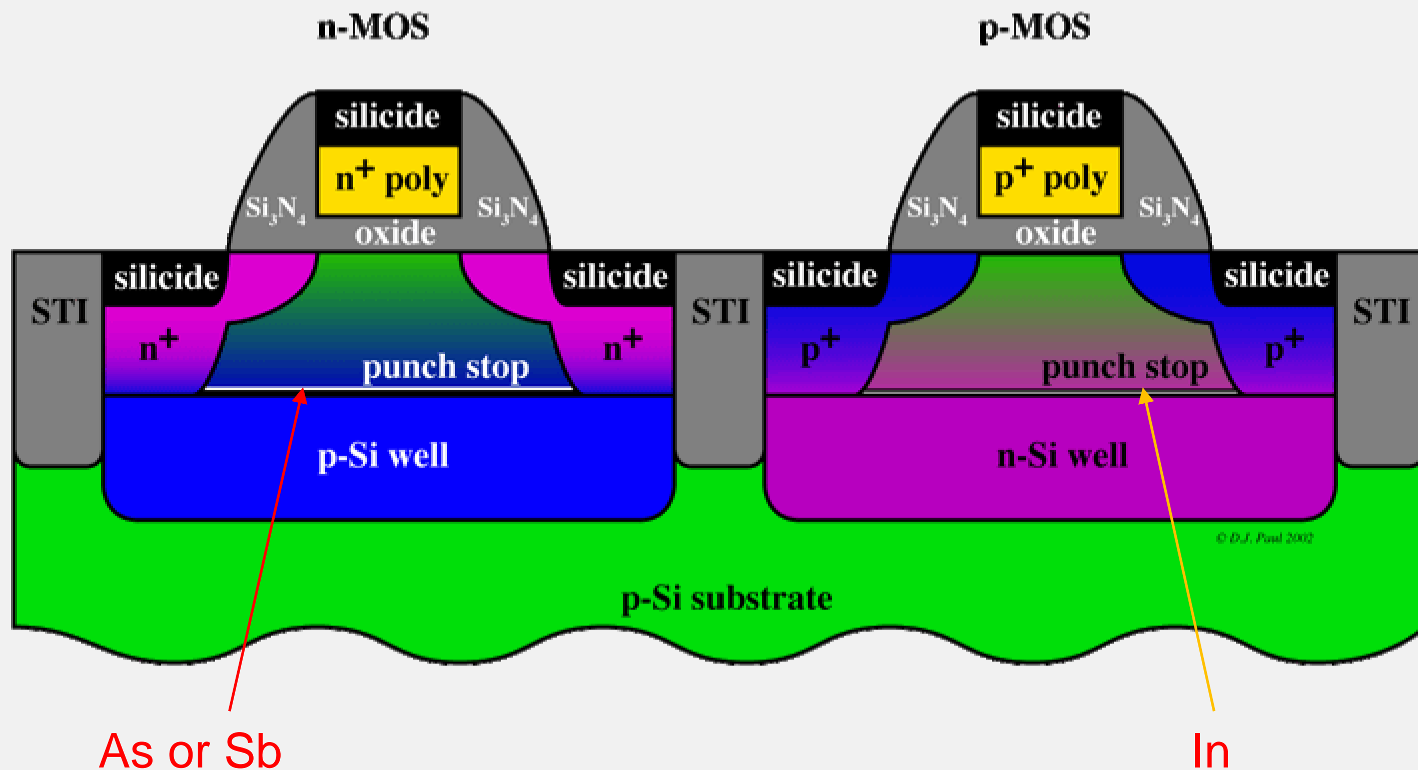
Shallow trench isolation STI



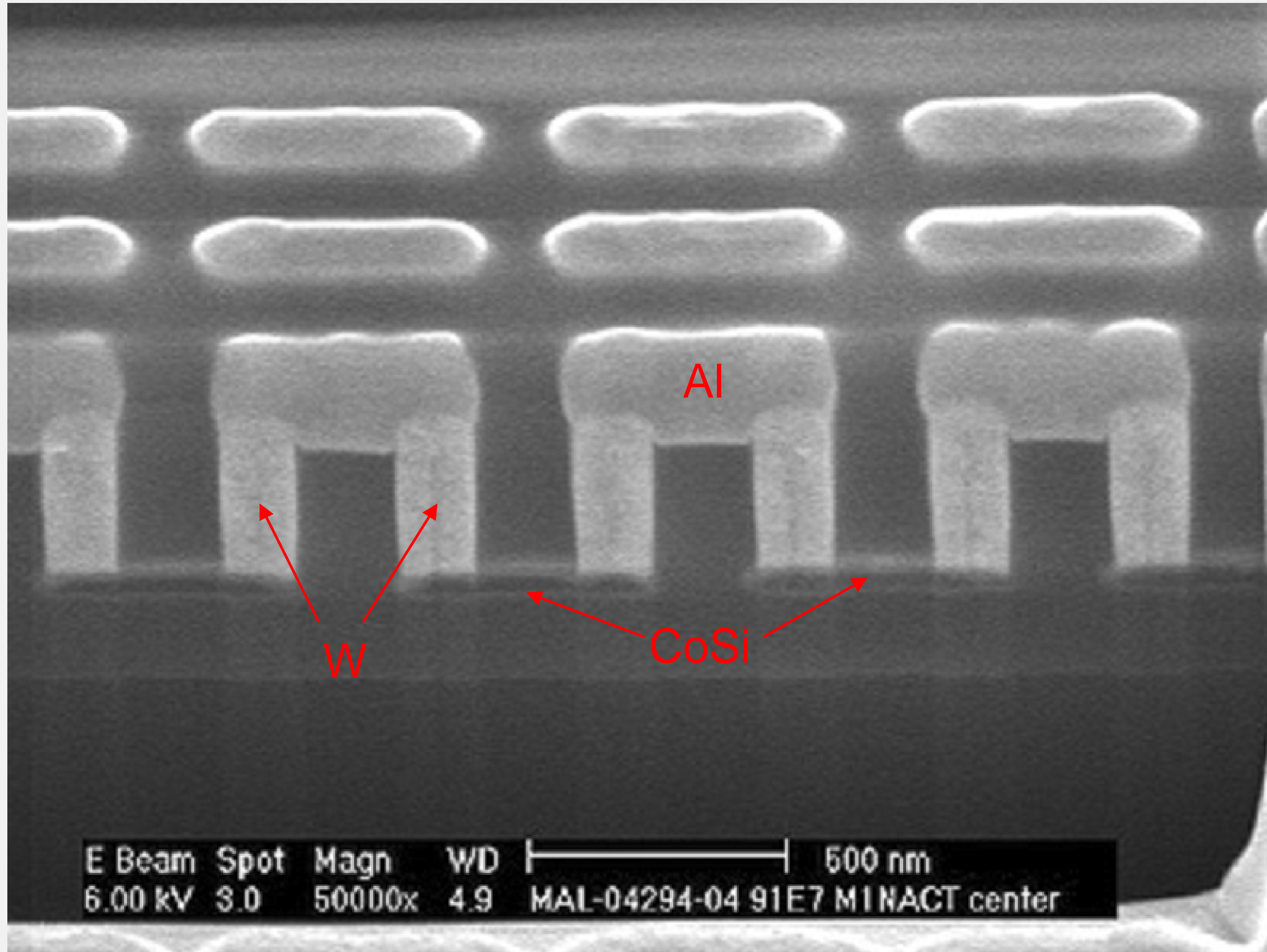


Modern CMOS

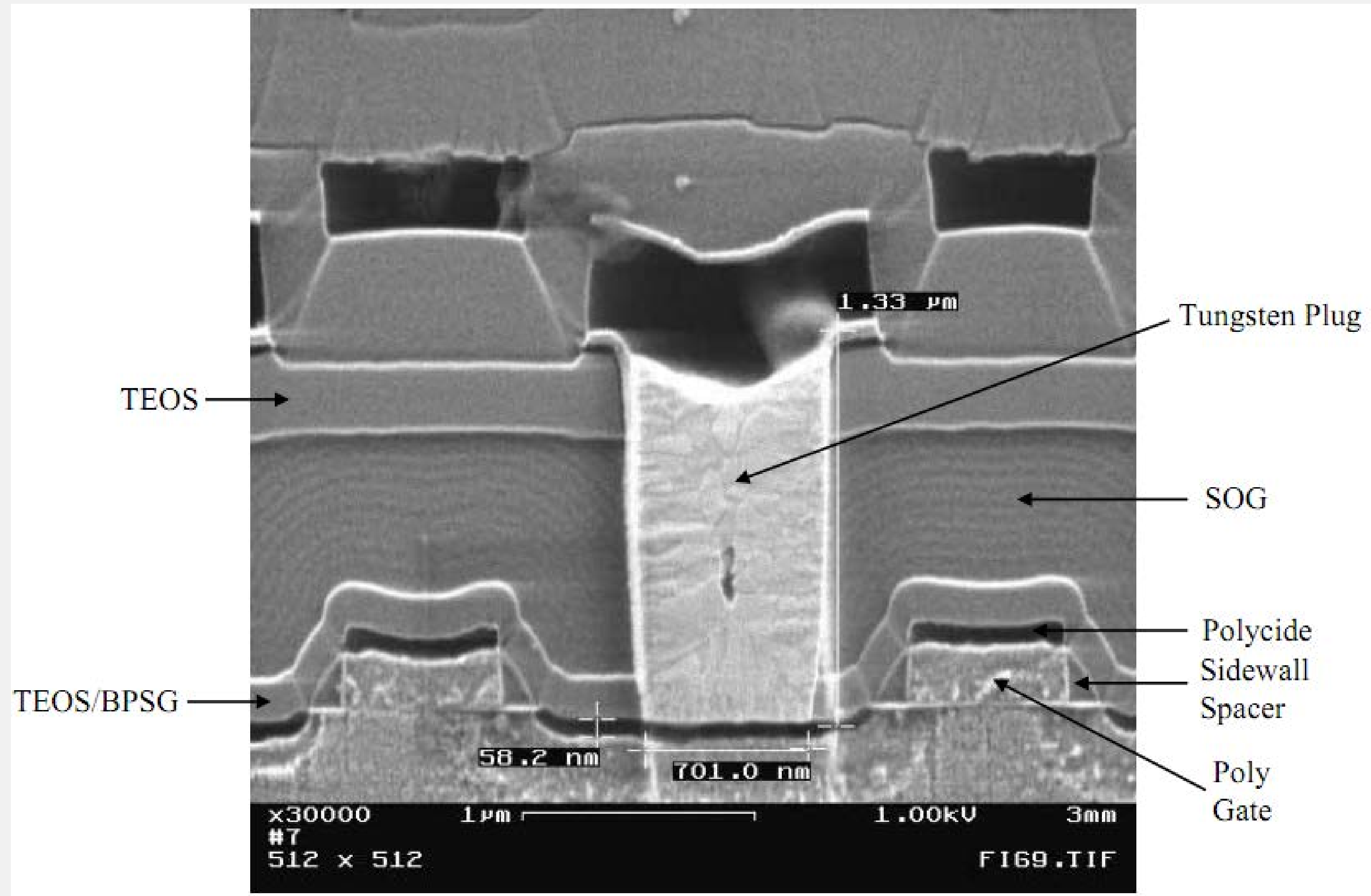
Punch-through-stop layer is done by implantation immediately after doping of wells and STI



CVD-W plugs



0.5 µm MOSFET cross-section



Gate oxide materials

• SiO_2	Thermal oxide, ε=4
• NO, ONO	Nitrided oxide, oxidized nitrided oxide, ε=6
• Al_2O_3, HfO_2 ZrO_2, Ta_2O_5	Amorphous and polycrysralline deposited oxides, ε=10 – 30
• <Y_2O_3> <$La_2Hf_2O_7$>	Single crystalline deposited oxides, ε=10 – 30
• $Ba_xSr_{1-x}TiO_3$	Very high dielectric constant materials, ε=200

Equivalent oxide thickness EOT

$$EOT = (\varepsilon_{SiO_2}/\varepsilon_{high}) \times t_{high-\varepsilon} + t_{SiO_2}$$

EOT (6 nm ZrO_2) with zero SiO_2 interfacial layer:

EOT = (4/23) * 6 nm =1.04 nm

EOT (6 nm ZrO_2) with 1 nm SiO_2 interfacial layer:

EOT = (4/23) * 6 nm + 1 nm = 2.04

Conclusions

- Al gate MOSFET is a start point of the CMOS process
- Further modifications of the CMOS were introduced: self-alignment, STI, LDD...
- Advanced CMOS is a mile stone of the modern microfabrication