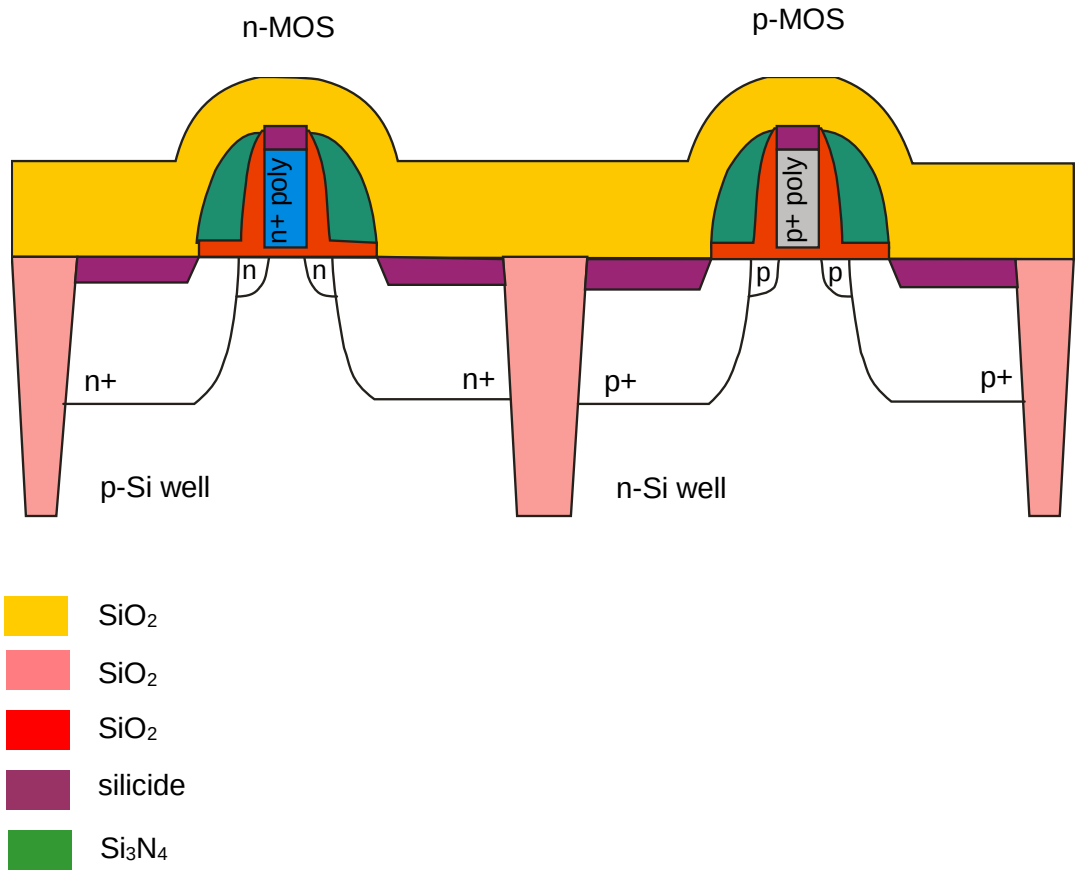
Microfabrication, Exercise 5: CMOS
(return by 14.04. 2019, 10 pm)

Session will be on April 16th, 9:15 o'clock.

1. A 45-nm dual-*k* gate CMOS inverter is shown below. Mark all functional areas of the structure, i.e. gate, S/D etc. Estimate layer thicknesses (depths). Where is critical dimension of the structure? There are three SiO_2 materials. Why? Propose process flow for one of the transistors (n-MOS or p-MOS). (2p)



2. Design fabrication process for a thin film MOS transistor given below. Choose materials and thicknesses for all layers. Propose deposition and doping methods. Maximum allowable process temperature is 300 ºC. Give top view of the transistor. How small is it (length and width)? (2p)

   Note. i-Si means intrinsic Si, i.e. undoped Si.