Aalto University

Reconfigurable switched-capacitor power converters

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ELEC-L3520 - Postgraduate Course in Electronic Circuit Design II

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Outline

- Introduction
- Topologies and optimization strategies
- Power loss in multi-gain SC converter
- SFG modeling and approach
- Case study
  - Reconfigurable SC Power Converter for Low-Voltage, Low Power TEG Applications
    - SQSC vs. SPSC power stage
    - power loss minimization techniques
- Conclusion
- References

Introduction

- SC power converters
  - Enables robust operation at ultra-low power levels
  - enhances the operation lifetime
  - achieve monolithic implementation
  - reduced size, cost and PCB footprint of overall system
- Efficiency of a SC power converter:

  [All the power losses are neglected]

$$\eta = \frac{V_{out}}{CG.V_{in}}$$

  - V_{in} and V_{out}: input and output voltage
  - CG: conversion gain

Introduction

- Energy harvesting mechanism: output voltage fluctuates
- Even for a fixed V_{out} the efficiency changes : V_{in} (from EH) changes
- To effectively utilize the limited harvested energy
  - power management techniques: DVFS (Dynamic Voltage and Frequency Scaling)
  - adaptive variation of V_{out} w.r.t. workload
- ENTERS : reconfigurable SC power converter
  - supplies variable output for variable input voltages

Topologies and Optimization Strategies

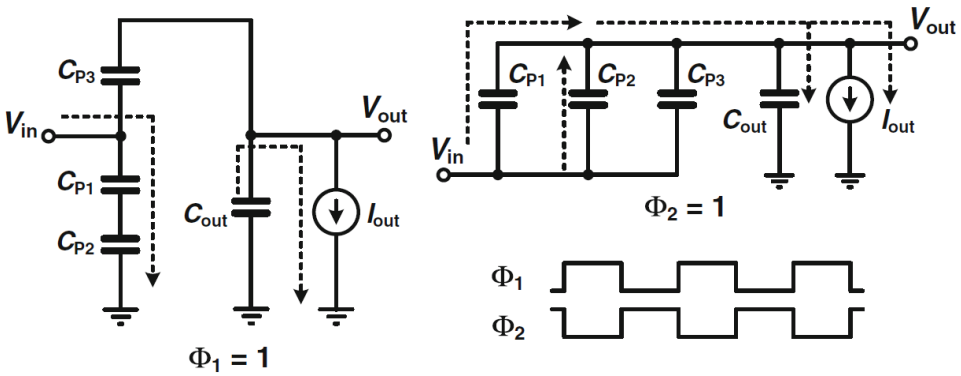


Fig.1: Power regulation scheme to provide a CG of 3/2 [Rao et. al.]

Drawbacks:

- separate charge and discharge path
- leads to large current and voltage ripples
- C_{P3} remains idle

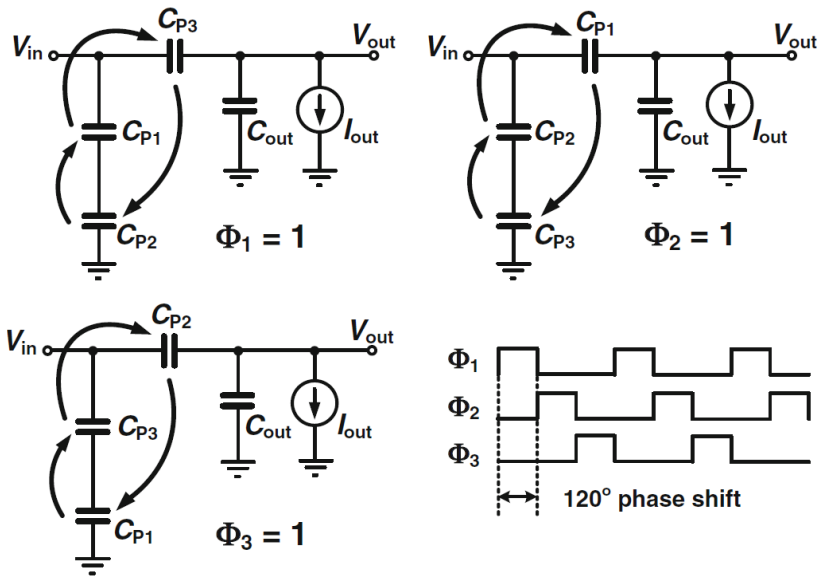


Fig.2: Interleaving regulation scheme for the multi-gain SC power converter.

Dynamic reconfiguration of charge pumping capacitors

Topologies and Optimization Strategies

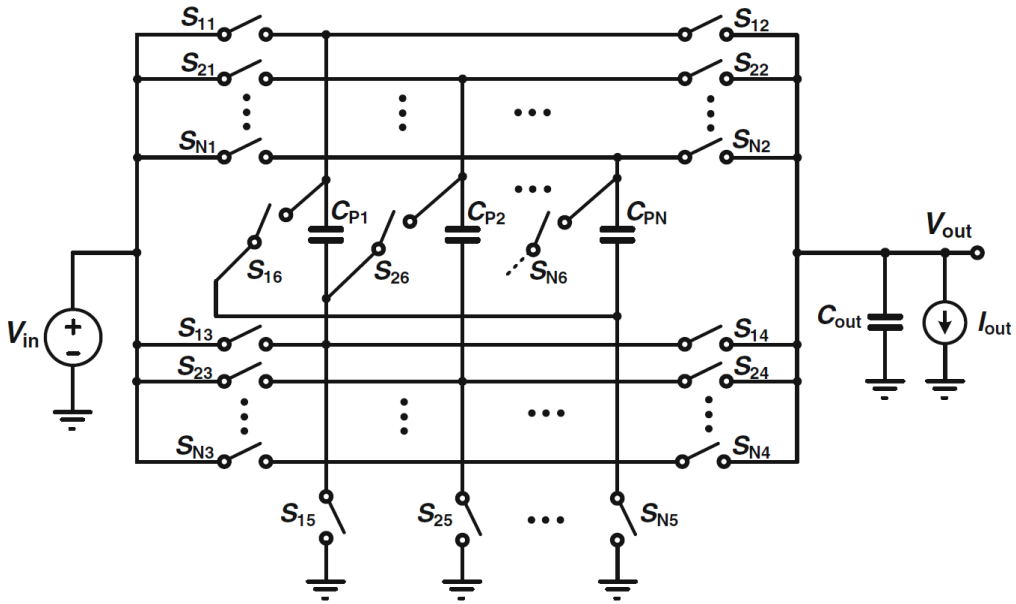


Fig.3: Generic architecture of the multi-gain reconfigurable SC power converter

- N pumping capacitors and 6N switches
- 4N-5 different CGs
- 1 to N interleaving phases

Topologies and Optimization Strategies

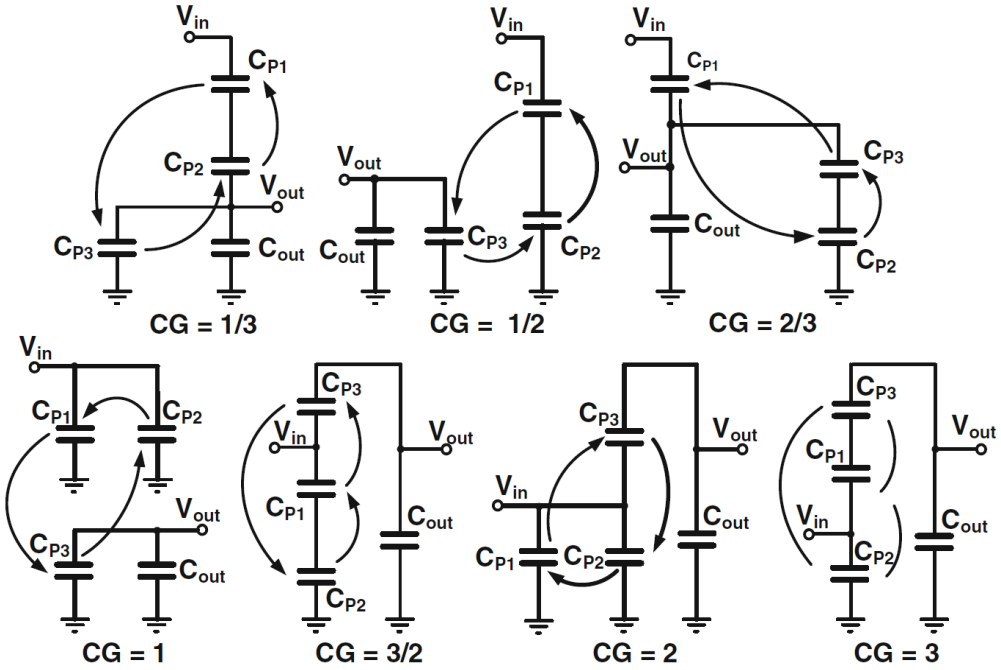


Fig.4: Different CG configuration of the reconfigurable SC power converter

- N = 3 pumping capacitors
- CGs : 4 x 3 – 5 = 7
- 7 CGs: 1/3, 1/2, 2/3, 1, 3/2, 2 and 3

Topologies and Optimization Strategies

CG	1/3	1/2	2/3	1	3/2	2	3
α	2/3	1/2	1/3	1	1	1	1
β	1	1	½	1	1	1	1/2
γ	0	0	0	0	1	1	1
ζ	1	1	1	0	0	0	0
δ	1/2	1	1	1	1/2	1	1
D	2/3	2/3	1/3	2/3	2/3	2/3	1/3

Table 1: CG configuration parameter for N = 3

- Output voltage of the converter is given as:

$$V_{\text{out}} = \frac{\beta\gamma + \delta}{\beta + \delta\zeta} V_{\text{in}} - \frac{\alpha I_{\text{out}} t_{\text{d}}}{(\beta + \delta\zeta) C_{\text{P}}} \left(\frac{1}{1 - e^{-t_{\text{d}}/\tau_{\text{d}}}} + \frac{1}{1 - e^{-t_{\text{c}}/\tau_{\text{c}}}} - 1 \right)$$

- α, β, γ, ζ, δ are circuit related coefficient that are determined by CG configuration
- D is duty ratio

Power loss in a multi-gain SC converter

- Redistribution power loss:

$$P_{\mathrm{D}} = \frac{\alpha I_{\mathrm{out}}^2 t_{\mathrm{d}}}{(\beta + \delta\zeta) C_{\mathrm{P}}} \left(\frac{1}{1 - e^{-t_{\mathrm{d}}/\tau_{\mathrm{d}}}} + \frac{1}{1 - e^{-t_{\mathrm{c}}/\tau_{\mathrm{c}}}} - 1 \right)$$

- Switching loss:

$$P_{\mathrm{sw}} = \sigma f_{\mathrm{S}} C_{\mathrm{ox}} \sum_{\mathrm{j}=1}^{6N} L_{\mathrm{j}} W_{\mathrm{j}} V_{\mathrm{GS(j)}}^2$$

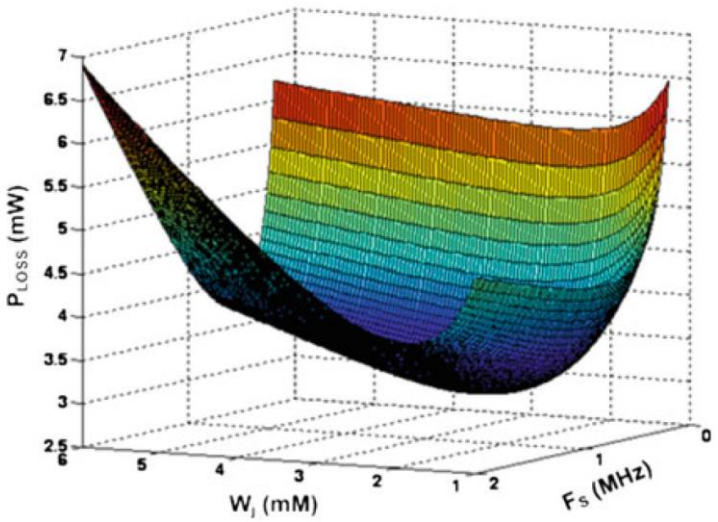


Fig.5: Plot of power loss P_{loss} versus W_j and f_S for CG = 3/2

- Total loss in power stage:

$$P_{\mathrm{loss}} = \frac{\alpha I_{\mathrm{out}}^2 t_{\mathrm{d}}}{(\beta + \delta\zeta) C_{\mathrm{P}}} \left(\frac{1}{1 - e^{-t_{\mathrm{d}}/\tau_{\mathrm{d}}}} + \frac{1}{1 - e^{-t_{\mathrm{c}}/\tau_{\mathrm{c}}}} - 1 \right) + \sigma f_{\mathrm{s}} C_{\mathrm{ox}} L_{\mathrm{min}} \sum_{\mathrm{j}=1}^{6N} W_{\mathrm{j}} V_{\mathrm{GS(j)}}^2$$

SFG Modeling and Design Approach

- Highly reconfigurable power stage : increased number of power components
  - pumping capacitors and power switches
  - complexity of controller
- Using SFG:
  - reconfiguration algorithm can be optimized to achieve multiple desired voltage CGs
  - highly efficient energy delivery
  - minimised number of power components
  - small-signal analysis to be conducted at different reconfiguration scenarios

SFG Modeling and Design Approach

- Following assumptions are made for SFG modelling:
  - all power switches are assumed to be ideal
  - passives components are assumed to be linear and time-invariant
  - equivalent series resistance (ESR) is neglected
- In order to achieve 2N+1 number of CGs
  - N pumping capacitor
  - Nodes = 2N +4

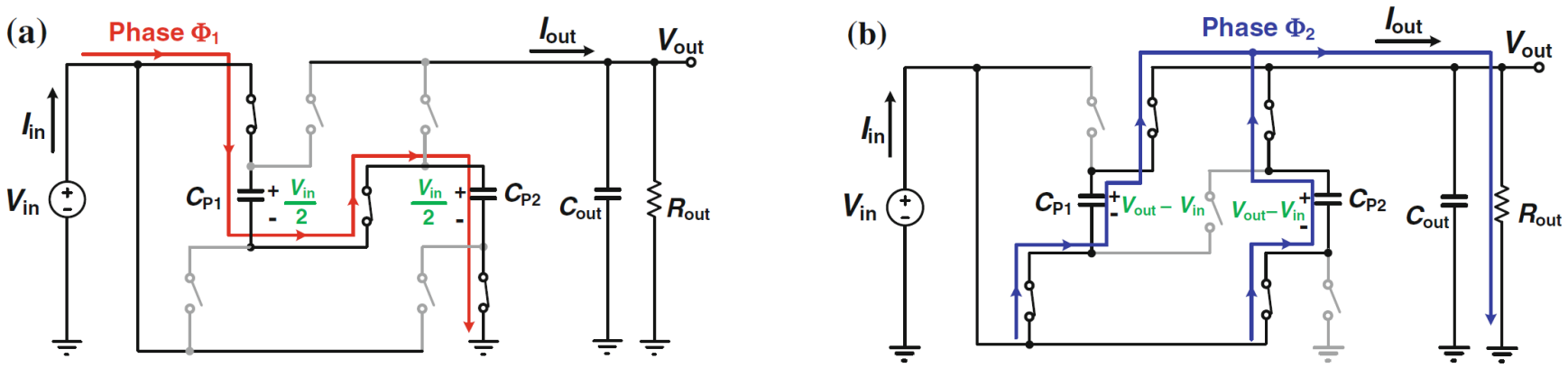
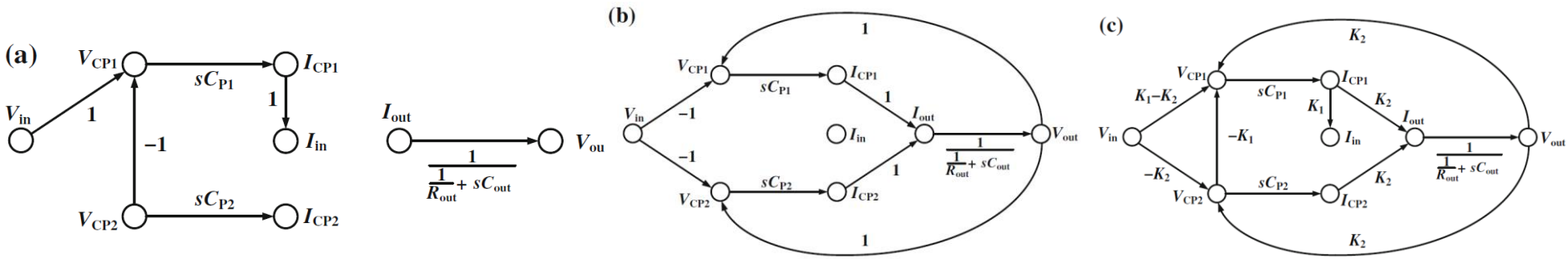


Fig.6: Power stage configuration in both phases for CG = 3/2

$$V_{in} = V_{CP1} + V_{CP2} \qquad I_{CP1} = s \cdot C_{CP1} \cdot V_{CP1} \qquad V_{out} = V_{CP1} + V_{in}$$

$$I_{in} = I_{CP1} = I_{CP2} \qquad I_{CP2} = s \cdot C_{CP2} \cdot V_{CP2} \qquad V_{out} = V_{CP2} + V_{in}$$

$$I_{out} = (1/R_{out} + s.\, C_{out}) \cdot V_{out} \qquad I_{out} = I_{CP1} + I_{CP2}$$



SFG Modeling and Design Approach

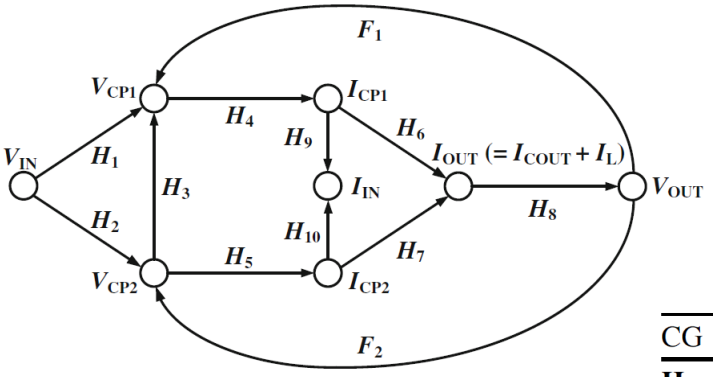


Fig.7: SFG of the SC power convertor with five CGs

CG	1/2	2/3	1	3/2	2
$\mathbf{H}_1$	K_1	K_1	K_1	$K_1 - K_2$	$K_1 - K_2$
$\mathbf{H}_2$	K_1	K_1	K_1	$-K_2$	$K_1 - K_2$
$\mathbf{H}_3$	0	$-K_2$	0	$-K_1$	0
$\mathbf{H}_4$	sC_{P1}	sC_{P1}	sC_{P1}	sC_{P1}	sC_{P1}
$\mathbf{H}_5$	sC_{P2}	sC_{P2}	sC_{P2}	sC_{P2}	sC_{P2}
$\mathbf{H}_6$	1	1	K_2	K_2	K_2
$\mathbf{H}_7$	1	1	K_2	K_2	K_2
$\mathbf{H}_8$	$R_{out}/(1+sR_{out}C_{out})$	$R_{out}/(1+sR_{out}C_{out})$	$R_{out}/(1+sR_{out}C_{out})$	$R_{out}/(1+sR_{out}C_{out})$	$R_{out}/(1+sR_{out}C_{out})$
$\mathbf{H}_9$	K_1	K_1	K_1	K_1	K_1
$\mathbf{H}_{10}$	K_1	K_1	K_1	0	K_1
$\mathbf{F}_1$	$-K_1 + K_2$	$-K_1 + K_2$	K_2	K_2	K_2
$\mathbf{F}_2$	$-K_1 + K_2$	$-K_1$	K_2	K_2	K_2

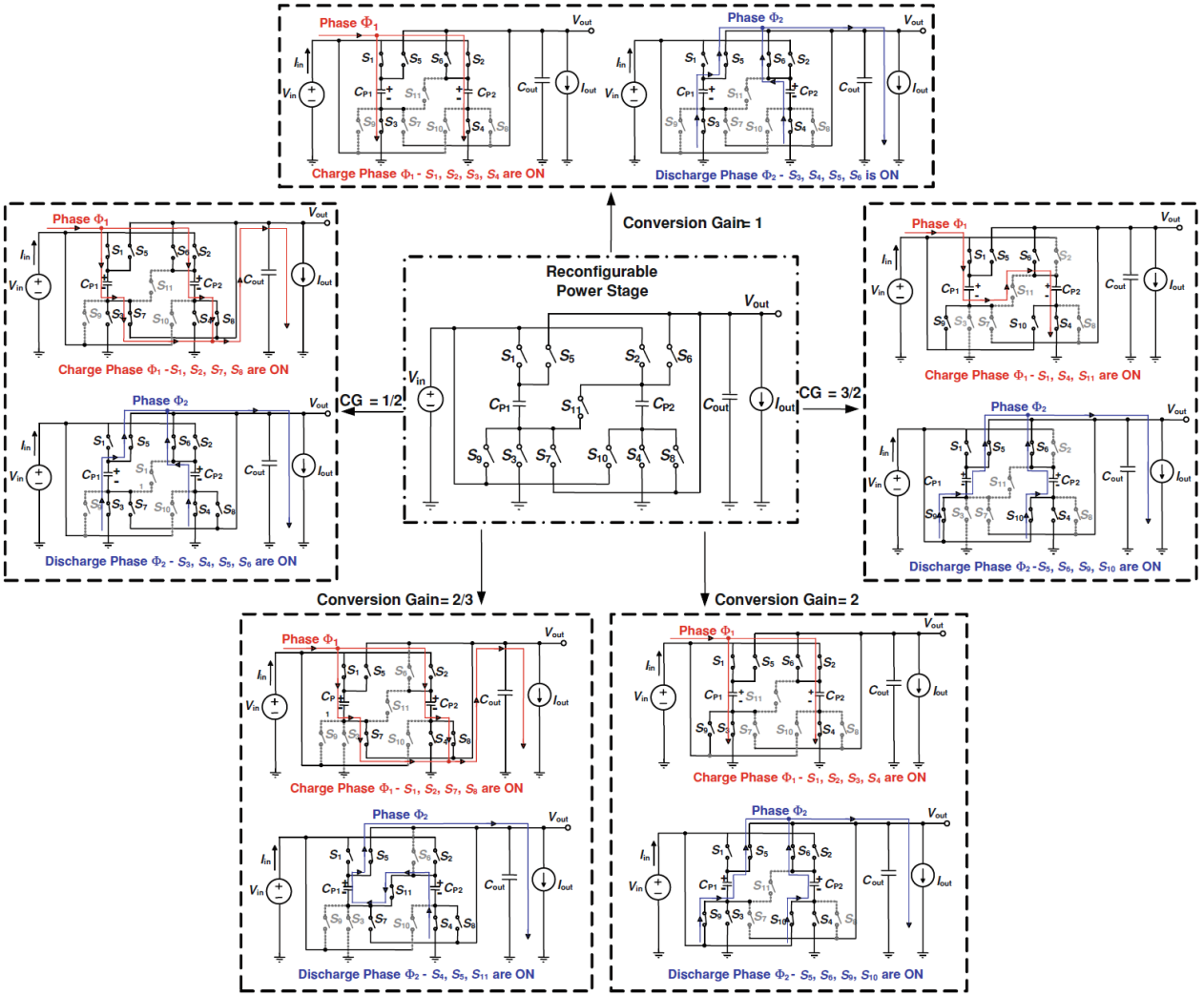


Fig.8: Illustration of step-up/step-down reconfigurable SC power converter with five CGs

Case Study:

Reconfigurable SC Power Converter for Low-Voltage, Low Power TEG Applications

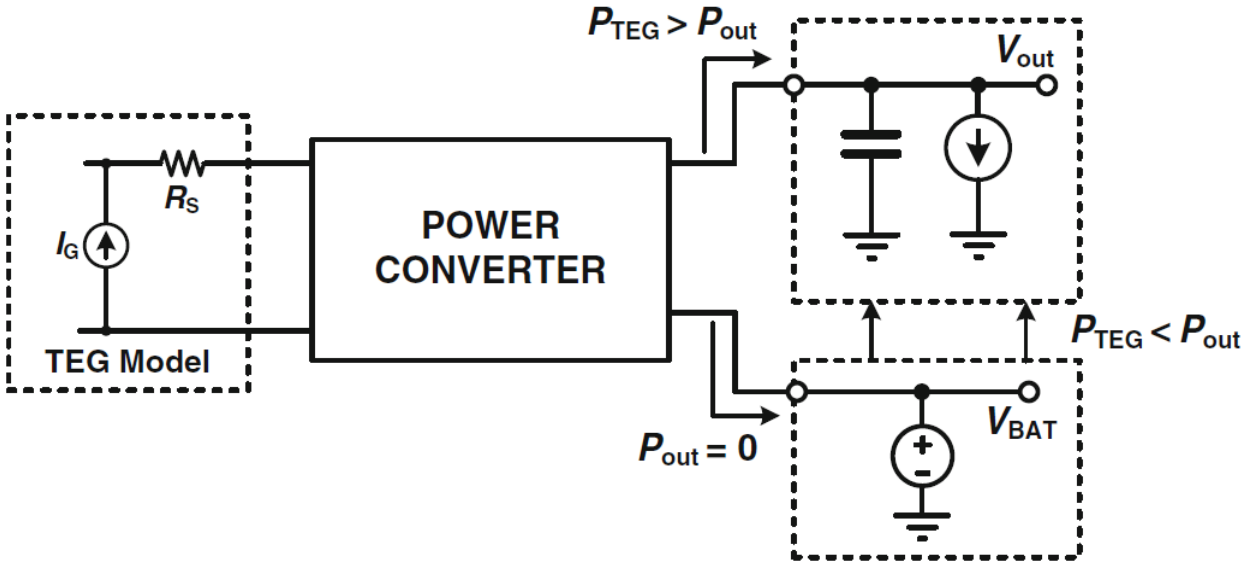


Fig.8: Power management system with TEG as the power source

Case Study:
SQSC vs SPSC power stage

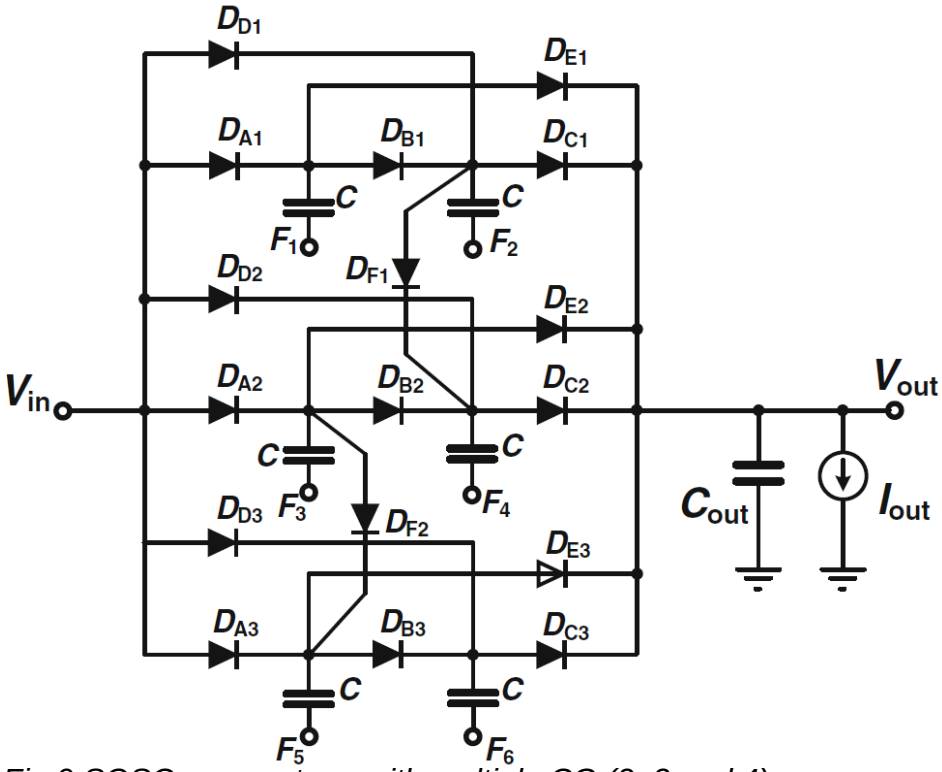


Fig.9:SQSC power stage with multiple CG (2, 3 and 4) implementation

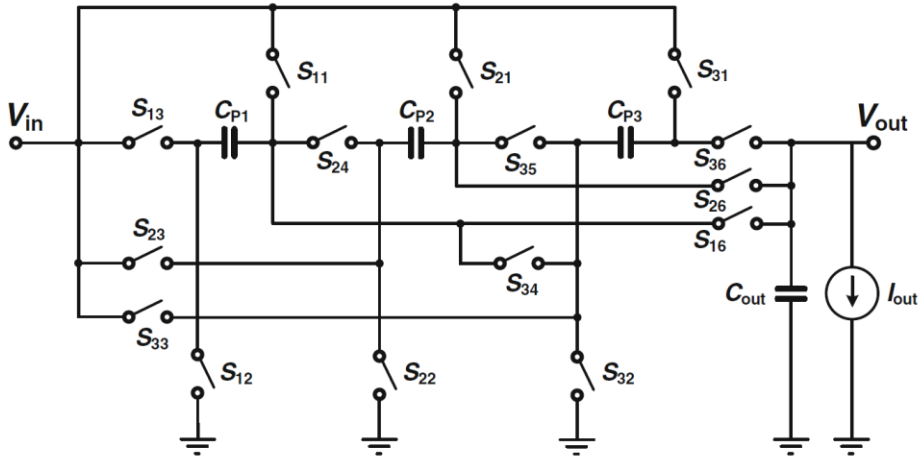


Fig.10:SPSC power stage with multiple CG (3/2, 2, 5/2, 3 and 4) implementation

Case Study: SQSC vs SPSC power stage

- SQSC: preferred power stage for power converter
- Advantage of SQSC: bottom plate parasitic capacitance experience and voltage swing of just V_{in}
  - In SPSC bottom plate parasitic capacitance for first stage is charge to V_{in} and for the last stage is $(N+1).V_{in}$.
- Drawback of SQSC: it provides step-up voltage from a fixed input source
  - provides only integer CG: not efficient for low-power applications
- Advantage of SPSC: can provide fractional CGs

Case Study:
SPSC power stage

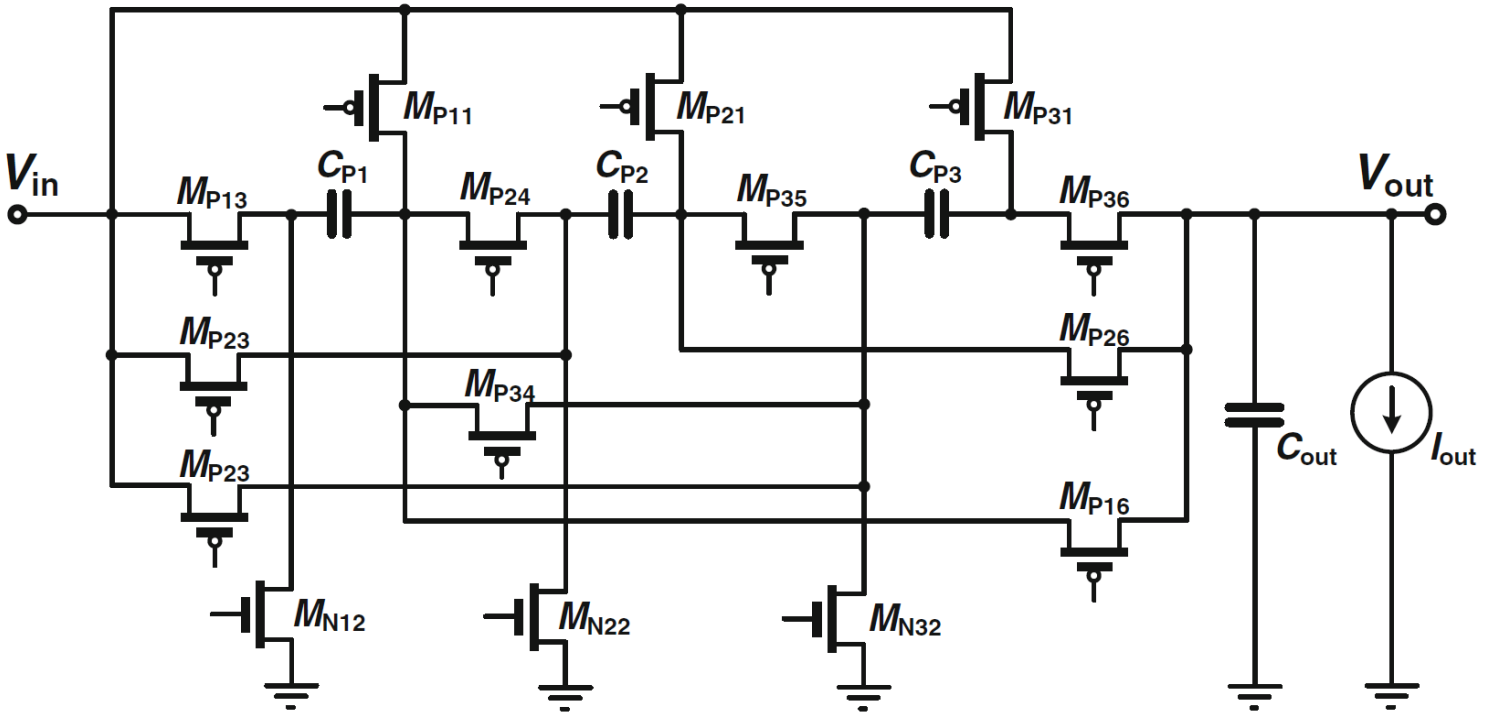


Fig.11:Transistor level power stage implementation of the SPSC convertor

Case Study:
SPSC power stage

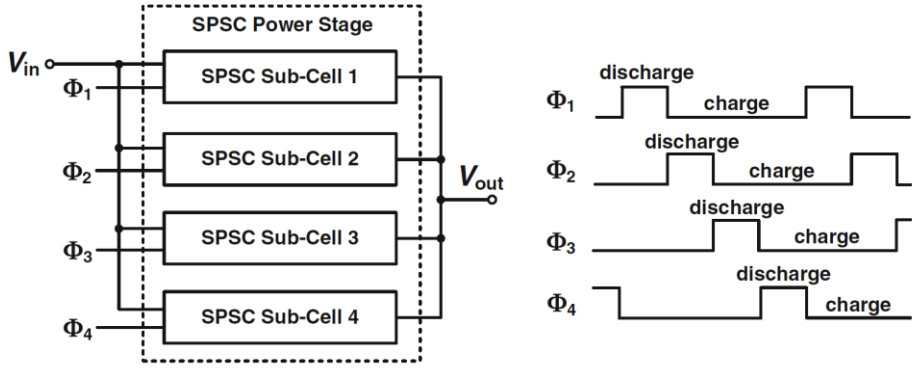


Fig.12:Four cell interleaving SPSC power stage with 4-phase clock

- Interleaving technique: to reduce overall switching noise in system efficiently
- divide power stage into 4 cells and operate them with four clock phases
- each cell is discharged to the output in one phase and charged during rest three phases

Case Study:
Switching power loss in SPSC

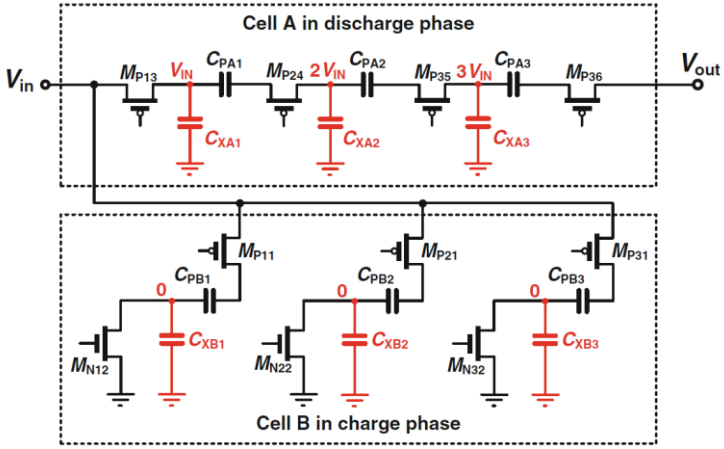


Fig.13:Two cell SPSC power stage charge and discharge operation

- During first phase
  - Parasitic capacitors of cell-A [charging] : Bottom plates of pumps are V_{in}, $2V_{in}$ and $3V_{in}$
  - Parasitic capacitors of cell-B [discharging] : Bottom plate is grounded and discharged.
- During next phase:
  - voltage across parasitic caps would interchange
  - additional charge has to be supplied from Vin
  - Meanwhile, pumping capacitors compensates its charge: degrades efficiency

Case Study:
Power loss minimization technique

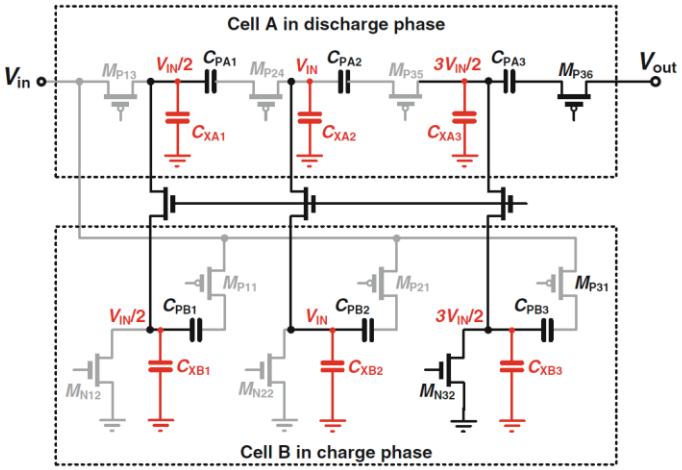


Fig.14:Charge recycling during the transistor phase

- this mechanism takes place during the transition of cell from discharge phase to charge phase
- before configuration of pumping cap is altered
  - all the connection broken off by turning off power switches
  - the parasitic capacitor's plates are connected together respectively
  - charge of parasitic caps from discharging phase is shared with those in charging phase
  - only half of the charge is required from V_{in} in this case: charge re-utilized

Case Study:
Power loss minimization technique

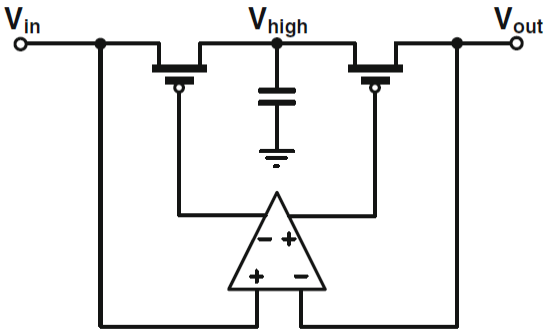


Fig.15:Conventional gate drive circuit used in step-up SC power convertors.

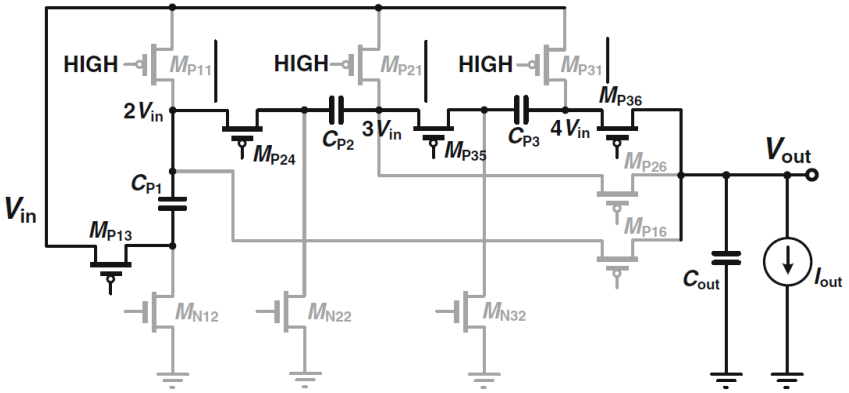


Fig.16:Reversion loss at start-up with high voltage gate drive

- fig. 15 shows that the drive circuit is operated from the higher of V_{in} and V_{out} voltage
- this voltage powers gate driver of the power transistors in charge pump: this architecture suffers from significant reversion loss during start-up process

Case Study:
Power loss minimization technique

- modified version of classic level shifter
- controlled by differential gate signals applied at the NMOS transistor pair M_{N1A} and M_{N1B}
- fig. 18 depicts the state change of power transistor between ON and OFF

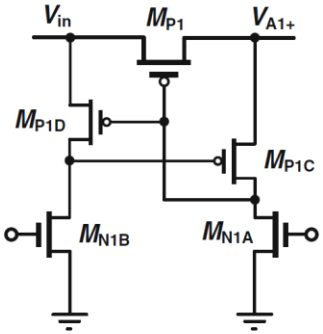


Fig.17:Local gate drive circuit

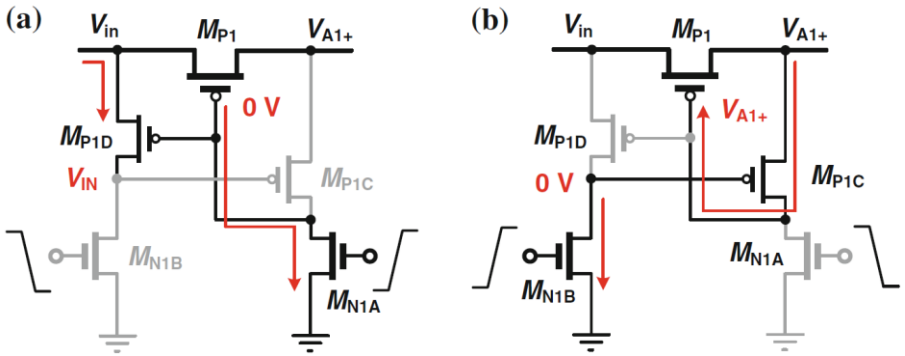
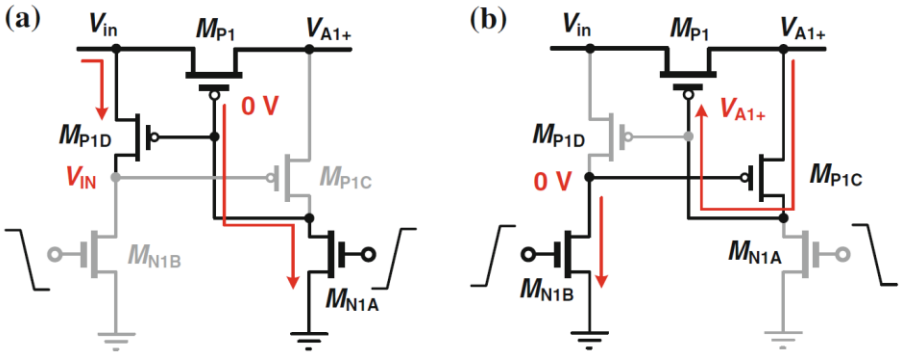


Fig.18:Operation of the local gate drive circuit

Case Study:
Power loss minimization technique



- the gate control signal of M_{N1B} goes low, thereby turning it off,
- while the gate control signal of M_{N1A} goes high, turning it on.
- As a result, M_{N1A} pulls the gate voltage of M_{P1} and M_{P1D} to zero, turning on those transistors.
- works well : the difference between the NMOS pair control signal voltage and the terminal voltage at the PMOS power transistor is **moderate**.

Case Study:
Power loss minimization technique

- If the difference becomes **too large**, the NMOS pair cannot discharge the gate potential of the PMOS power transistor to zero quickly.
- This results in a large shoot-through current
- To prevent this, an additional PMOS transistor is added to the shoot-through current paths as shown.
- This transistor prevents a shoot-through current, even when a large voltage difference exists

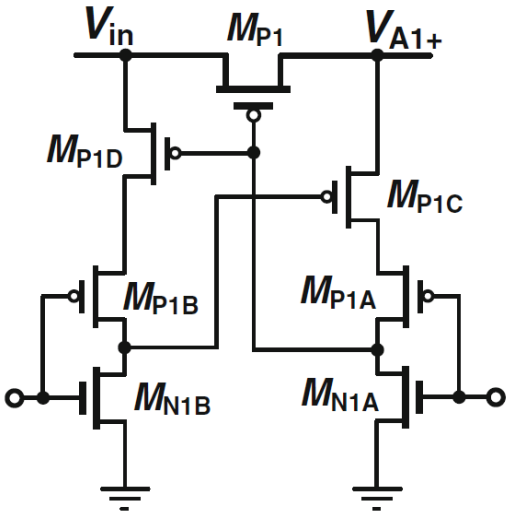


Fig.19:Gate drive circuit used for large voltage shifting

Case Study:
Power loss minimization technique

- If the substrate of these transistors is connected to a voltage lower than any of its other terminal voltages, a reverse current can occur
- connecting the substrate of these devices to the highest voltage in the system is not a good
  - leads to a large threshold voltage
- to obtain optimal performance, control the body bias in an adaptive manner

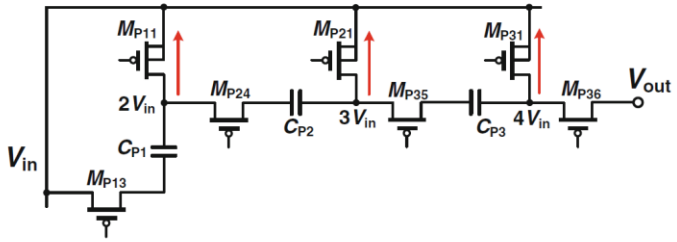


Fig.20:Improper body biasing of the PMOS power transistor

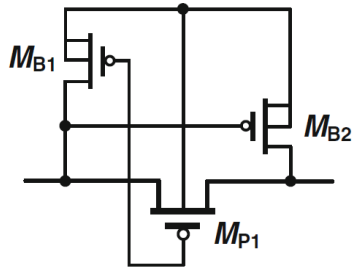


Fig.21:Adaptive body biasing circuit

Case Study:
Power loss minimization technique

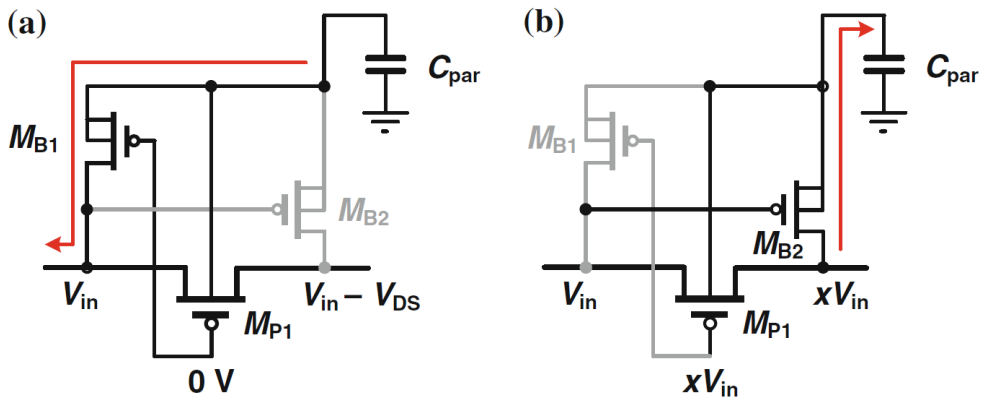


Fig.22:Operation of body biasing technique during charge and discharge phase

- when the circuit is charging, the voltage at the gate terminal of M_{P1} is 0 V
  - this turns on M_{B1} and turns off M_{B2}
  - parasitic capacitance at the body of M_{P1} is discharged to Vin
  - cancels any threshold modulation
- similarly, the parasitic capacitance is charged to voltage $x.V_{in}$
  - preventing any possible reverse current

Conclusion

- General topologies and control schemes for dynamic reconfiguration in SC power convertors are discussed
- Introduced to interleaving regulation scheme with multi-phase CG reconfiguration
- Generic reconfigurable charge pump topology was discussed
- Challenges during the optimization of SC power converters due to increased number of power component was discussed
- A step-up SC power converter designed specifically for TEG based energy harvesting application is discussed.

References

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Home-Work

- Explain briefly the charge recycling technique used in SPSC converters.
- Explain briefly the technique to prevent reversion loss in SPSC converters.