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Engineering

Postgraduate Course in Electronic Circuit Design II V

Interleaving regulation in switched-capacitor power converters
24.04.2019

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Leo Nyman

LECTURE OVERVIEW

1. Switched-capacitor power converter
2. Interleaving regulation
3. On-chip implementation
4. Circuit examples
5. Conclusions
6. Homework

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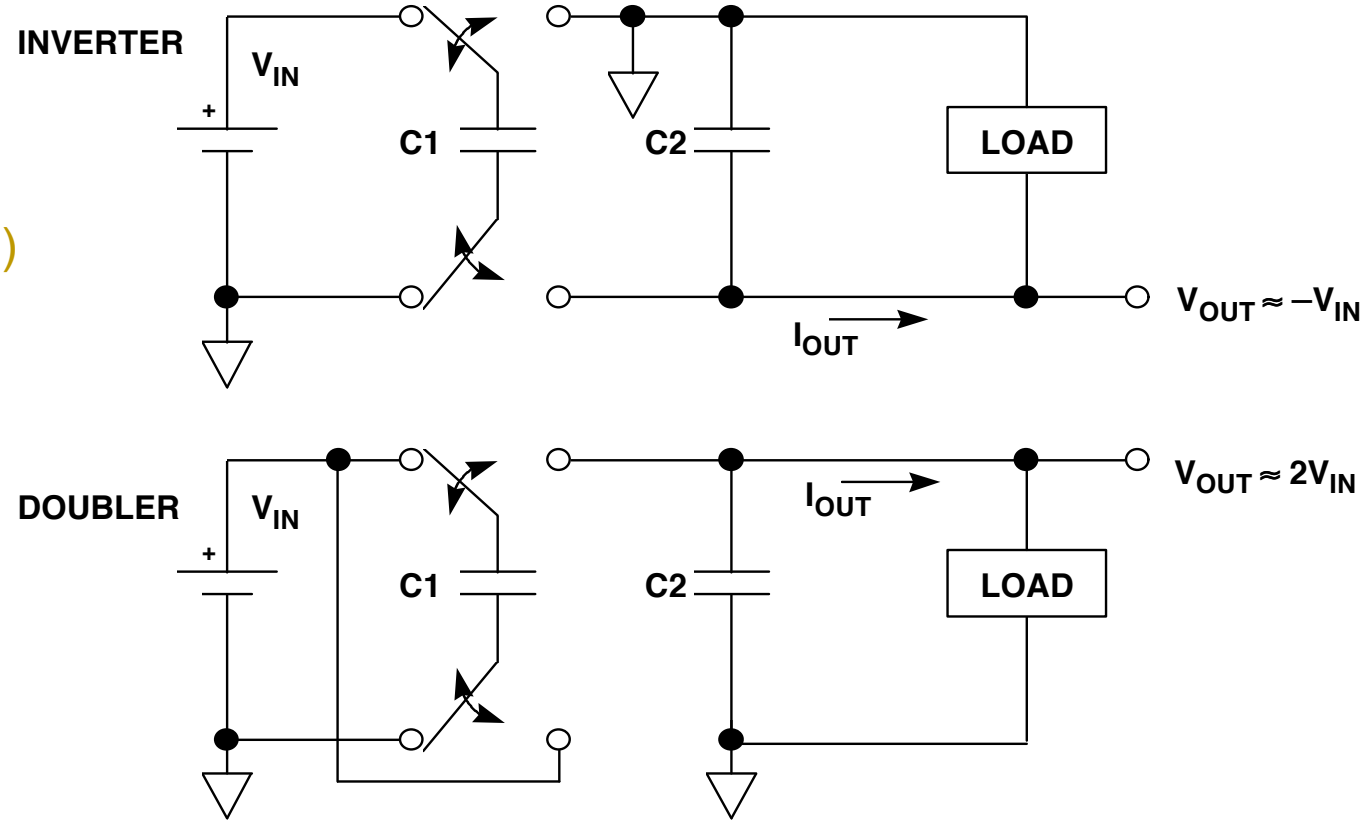
SWITCHED–CAPACITOR POWER CONVERTER (SCC)

Common use cases:

Typically *switching frequency* = 25..400 kHz

Charge Pump (CP)



Hundreds of other designs exists..

Credit: Kester, W., Erisman, B. and Thandi, G., 1998. Switched capacitor voltage converters. In Power and Thermal Management Design Techniques Seminars, Section IV, Analog Device Design Center.

SWITCHED–CAPACITOR POWER CONVERTER

pros

- Inductor and its associated magnetic design issues can be eliminated. Capacitors–only design enables monolithic integration and miniaturization. Can be implemented using plain **CMOS** technology.[1]
- Lower input current peaks, less output voltage ripples
- Simple circuits, low component count, small space requirements
- Good efficiency (~85..95 %) over a wide load range
- Able to operate with < 1 V input voltage

1. *Ma, D., & Bondade, R. (2010). Enabling power-efficient DVFS operations on silicon. IEEE Circuits and Systems Magazine, 10(1), 14-30.*

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SWITCHED–CAPACITOR POWER CONVERTER

cons

- Switching emits RFI. The circuit design needs careful bypassing, shielding and filtering of both input and output blocks.[1]
- Efficiency goes down, if output voltage deviates from the ideal conversion ratio of the circuit. This has slowed the acceptance of this converter type for a number of applications.[2]

1. *The ARRL Handbook for Radio Communications 2016. American Radio Relay League.*
2. *Le, H. P. (2013). Design techniques for fully integrated switched-capacitor voltage regulators (Doctoral dissertation, UC Berkeley)*

SWITCHED–CAPACITOR POWER CONVERTER

design

- Higher switching frequency enables smaller components
- Minimum switching frequency is considered to be 25 kHz, to remain above human audible range
- Fast switch transition between ON and OFF states is crucial.[1] Longer transitions reduce efficiency factor.
- Clocking management.[2]
    - For example, for low power operation, switching frequency can be reduced, and results in better efficiency.[3]
- Adding an extra capacitor to smoothen input current peaks reduces noise, but requires extra space.[3]

1. *Maniktala, Sanjaya. Switching Power Supplies A-Z. Elsevier, 2012.*
2. *Ma, D., Su, L., & Somasundaram, M. (2010). Integrated interleaving SC power converters with analog and digital control schemes for energy-efficient microsystems. Analog Integrated Circuits and Signal Processing, 62(3), 361-372.*
3. *Allard B. (2016). Design of Power Systems-On-Chip. Wiley. Chapter 7.*

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SWITCHED–CAPACITOR POWER CONVERTER

other

- Nanosecond control response and wide-range voltage conversion has been demonstrated.[1]

1. *Allard B. (2016). Design of Power Systems-On-Chip. Wiley. Chapter 7.*

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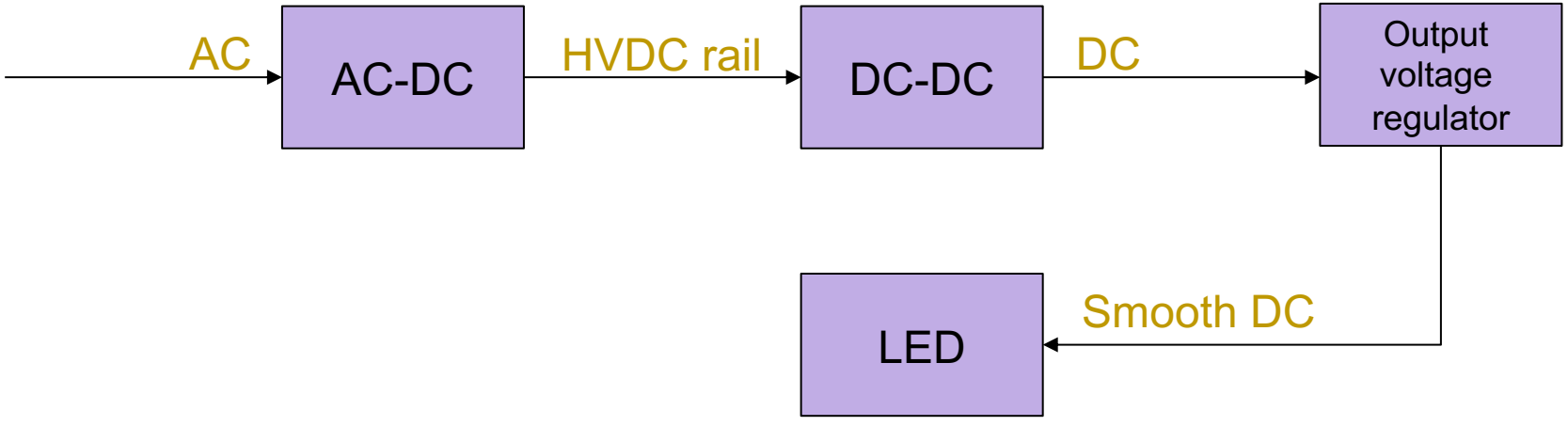
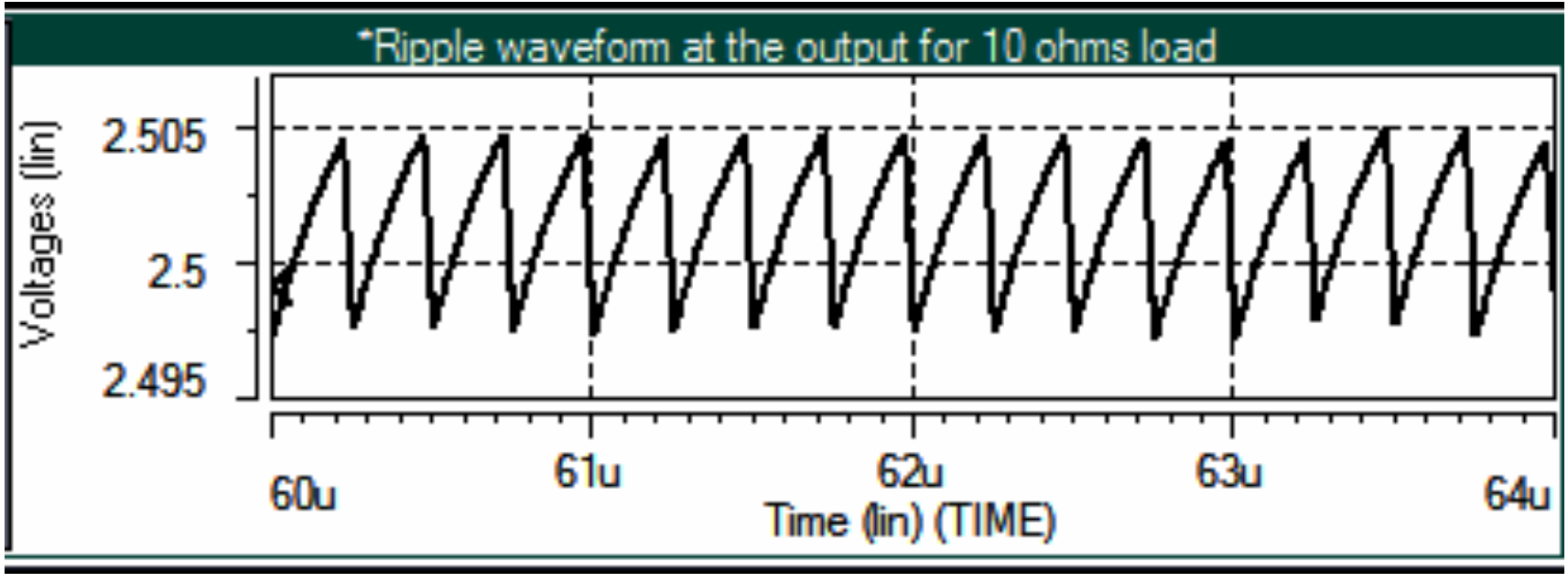
SWITCHED CAPACITOR POWER CONVERTER

Example – LED light powered by AC mains:



OUTPUT VOLTAGE RIPPLE



INTERLEAVING REGULATION

Basic idea known already in 1970s:
Split the power converter into N smaller units, operating with the same frequency but equally shifted N-phases between them.

1. Reduces output ripple
2. Load transient response is improved
3. Smoothens input current peak demand[1]
4. Less filtering required for the device
5. Better power conversion density[2]

1. *Allard B. (2016). Design of Power Systems-On-Chip. Wiley. Chapter 7.*
2. *Miwa, B. A., Otten, D. M., & Schlecht, M. E. (1992, February). High efficiency power factor correction using interleaving techniques. In [Proceedings] APEC'92 Seventh Annual Applied Power Electronics Conference and Exposition (pp. 557-568). IEEE.*

INTERLEAVING REGULATION TERMINOLOGY

Several names used in the literature[1]

- **Interleaving** regulation
- Multi-phase conversion
- Staggered phase conversion
- Interdigitating
- Polyphase chopping
- Staggered clock timing
- Ripple current cancellation
- Phase-shifted parallel
- Phase-synchronous

1. *Miwa, B. A., Otten, D. M., & Schlecht, M. E. (1992, February). High efficiency power factor correction using interleaving techniques. In [Proceedings] APEC'92 Seventh Annual Applied Power Electronics Conference and Exposition (pp. 557-568). IEEE.*

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INTERLEAVING POWER CONVERTER

Features:

- Multiple sub-cells in the power stage[1]
- Regulation achieved with interleaving power flow control[1]

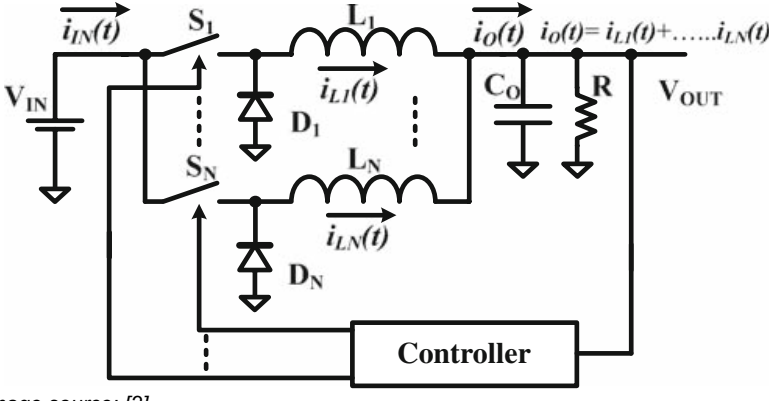
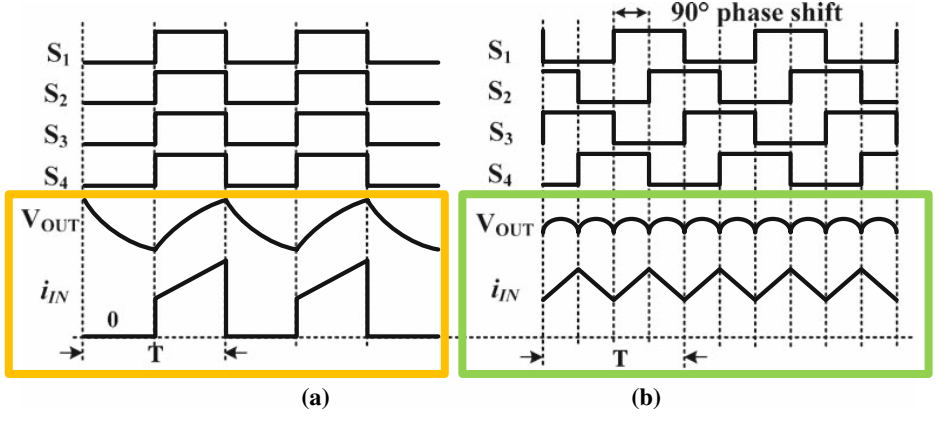


Image source: [2]

Multiple CPs

The controller enables control of V_{OUT}



a) All clocks in sync
b) Interleaving applied

1. *Ma, D., Su, L., & Somasundaram, M. (2010). Integrated interleaving SC power converters with analog and digital control schemes for energy-efficient microsystems. Analog Integrated Circuits and Signal Processing, 62(3), 361-372.*
2. *Perreault, D. J., & Kassakian, J. G. (1997). Distributed interleaving of paralled power converters. IEEE Transaction on Circuits and Systems-I, 44(8), 728–734.*

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INTERLEAVING REGULATION

Regulation:

- Controller enables “smart” control schemes to be implemented.
- For example, reducing switching frequency increases efficiency and vice versa.

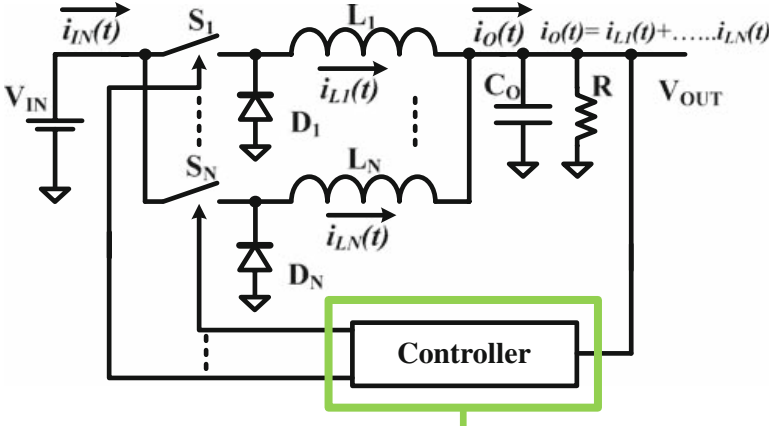
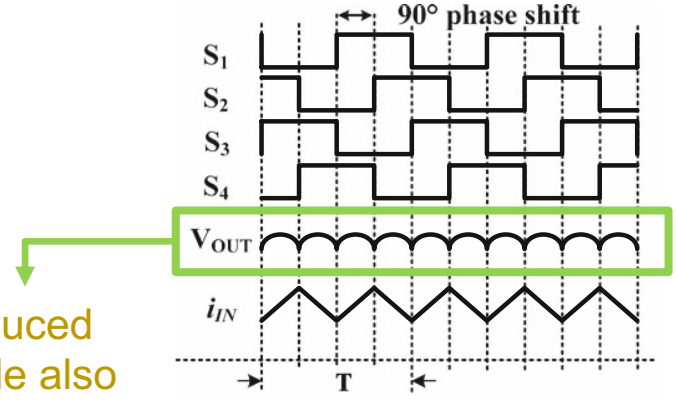


Image source: [2]

Closed loop control aids in achieving the regulation at any precision voltage.[2]



Reduced ripple also increases efficiency.[1]

1. *Allard B. (2016). Design of Power Systems-On-Chip. Wiley. Chapter 7.*
2. *Somasundaram, Mohankumar N., and Dongsheng Ma. "Integrated low-ripple-voltage fast-response switched-capacitor power converter with interleaving regulation scheme." 2006 IEEE International Symposium on Circuits and Systems. IEEE, 2006.*

INTERLEAVING REGULATION ON-CHIP

Benefits:

- On-chip SCC and power regulation reduces motherboard footprint, since external components are not needed.

When implemented *on a **single die***:

- Flying capacitors can be replaced with multiple smaller capacitors, without affecting die size. This enables better interleaving regulation topology.
- Power density (W/mm^2) and efficiency is still not good, compared to ***in-package*** or ***off-chip*** methods.

When implemented in-package:

- Allows different technologies to be used

1. *Allard B. (2016). Design of Power Systems-On-Chip. Wiley. Chapter 7.*

TOO MANY N IS NOT ENOUGH?

Adding more sub-cells reduces the ripple.

".. Because the maximum reduction from the interleaving function occurs over the duty ratio range when the ripple is largest, the worst-case interleaved ripple amplitude is reduced from the worst-case non-interleaved ripple amplitude by a further factor of N, for a total of N^2 reduction in worst-case ripple amplitude." [1]

1. *Miwa, B. A., Otten, D. M., & Schlecht, M. E. (1992, February). High efficiency power factor correction using interleaving techniques. In [Proceedings] APEC'92 Seventh Annual Applied Power Electronics Conference and Exposition (pp. 557-568). IEEE.*

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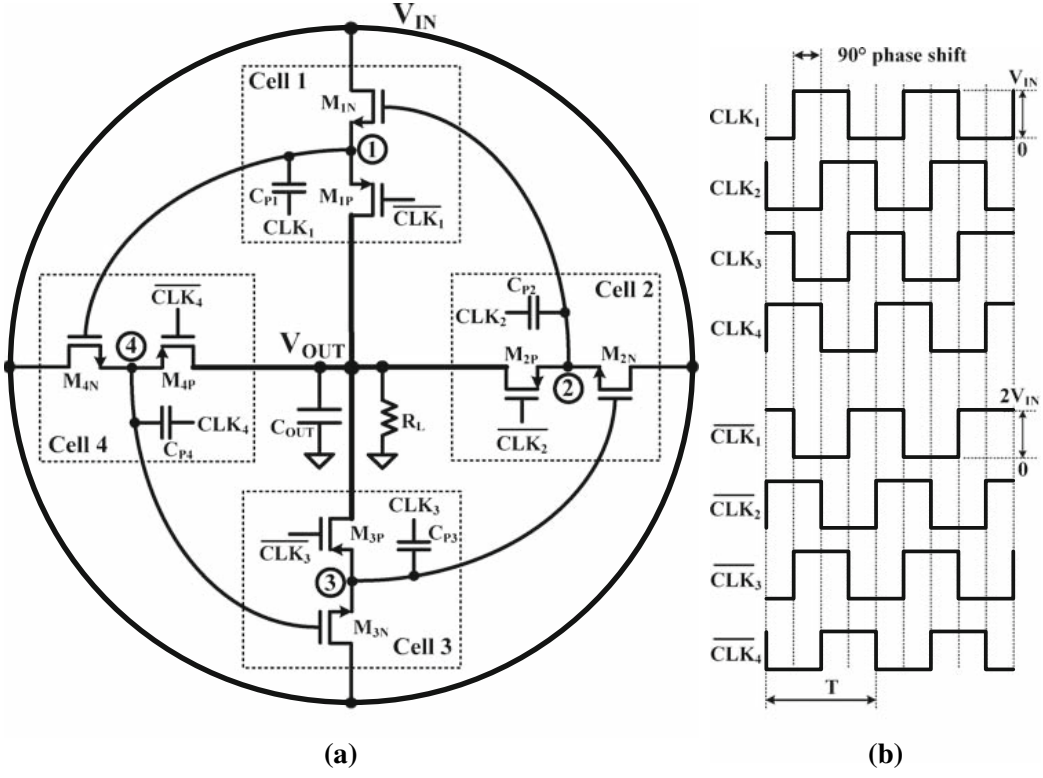
PROPOSED 4-CELL TYPE BY MA ET AL.



Requires:

- Two clock inputs
- V_{in} and $2V_{in}$

Load transient response is not optimal

Open-loop (no controller)

Image source: [1]

1. *Ma, D., Su, L., & Somasundaram, M. (2010). Integrated interleaving SC power converters with analog and digital control schemes for energy-efficient microsystems. Analog Integrated Circuits and Signal Processing, 62(3), 361-372.*

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PROPOSED 2-CELL CROSS-COUPLED TYPE BY MA ET AL.

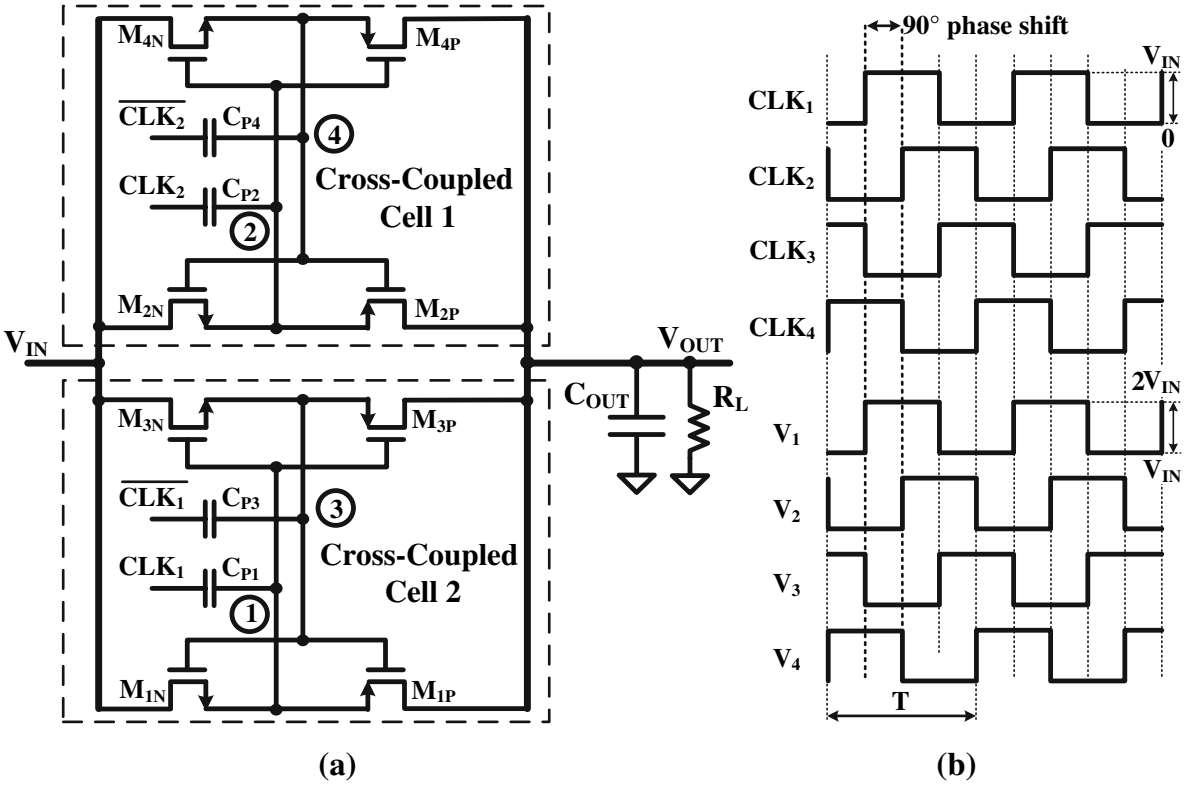

Image source: [1]

Requires:

- One clock input
- V_{in}

$V_{out} = 2V_{in}$

Pumping capacitors are always pre-charged to V_{in} which speeds up transient response

Fault-tolerant

Open-loop (no controller)

1. *Ma, D., Su, L., & Somasundaram, M. (2010). Integrated interleaving SC power converters with analog and digital control schemes for energy-efficient microsystems. Analog Integrated Circuits and Signal Processing, 62(3), 361-372.*

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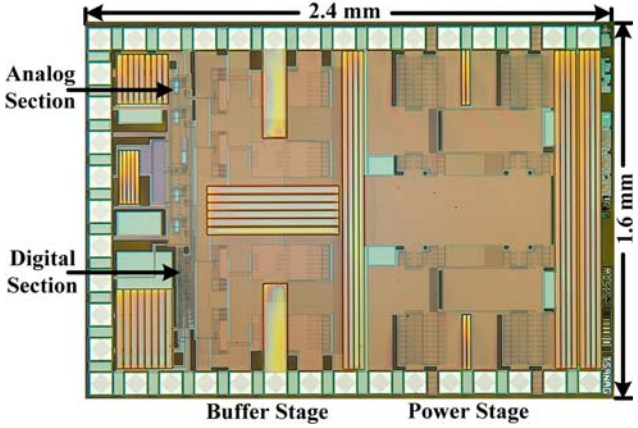
PROPOSED 2-CELL CROSS-COUPLED TYPE BY MA ET AL.



350 nm CMOS process

Measured output ripple

Actual clock signals

Image source: [1]

1. *Ma, D., Su, L., & Somasundaram, M. (2010). Integrated interleaving SC power converters with analog and digital control schemes for energy-efficient microsystems. Analog Integrated Circuits and Signal Processing, 62(3), 361-372.*

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PROPOSED CLOSED-LOOP TYPE BY SOMASUNDARAM AND MA

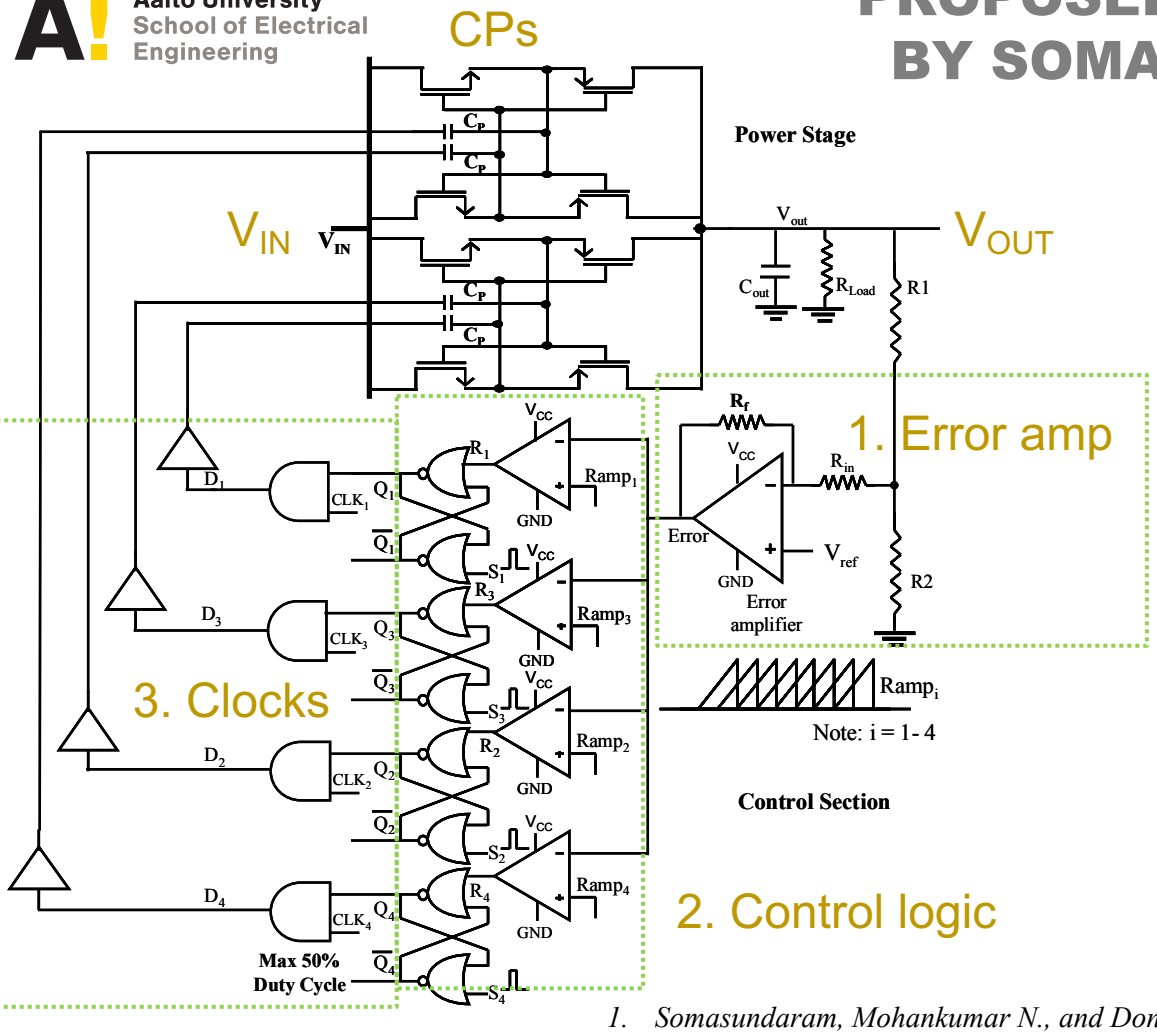


Image source: [1]

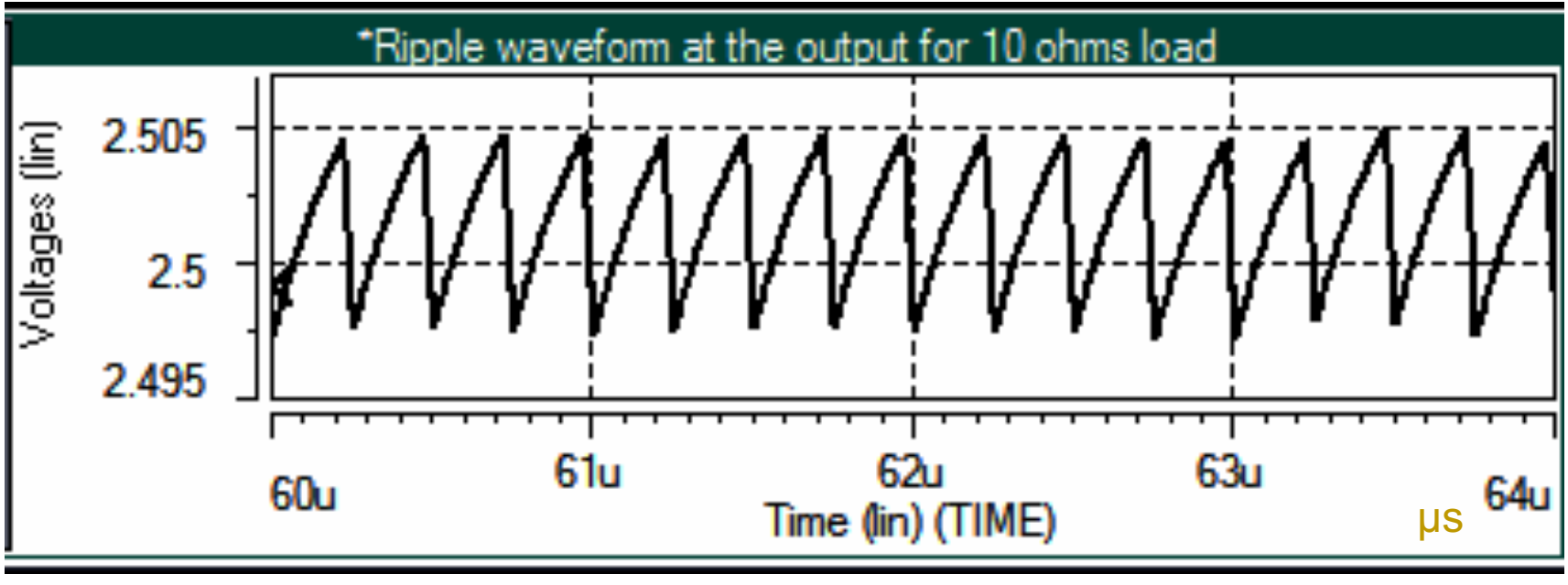
Regulation achieved at any precision voltage, with the help of closed-loop controller.

4 clocks with 90° phase difference

1. *Somasundaram, Mohankumar N., and Dongsheng Ma. "Integrated low-ripple-voltage fast-response switched-capacitor power converter with interleaving regulation scheme." 2006 IEEE International Symposium on Circuits and Systems. IEEE, 2006*

PROPOSED CLOSED-LOOP TYPE BY SOMASUNDARAM AND MA

Simulated output ripple



Compared to cross-coupled voltage doubler, this design has 50 % lower ripple voltage. Simulated efficiency of the converter is 83.2 %.

Image source: [1]

1. *Somasundaram, Mohankumar N., and Dongsheng Ma. "Integrated low-ripple-voltage fast-response switched-capacitor power converter with interleaving regulation scheme." 2006 IEEE International Symposium on Circuits and Systems. IEEE, 2006*

PROPOSED CLOSED-LOOP TYPE BY SOMASUNDARAM AND MA

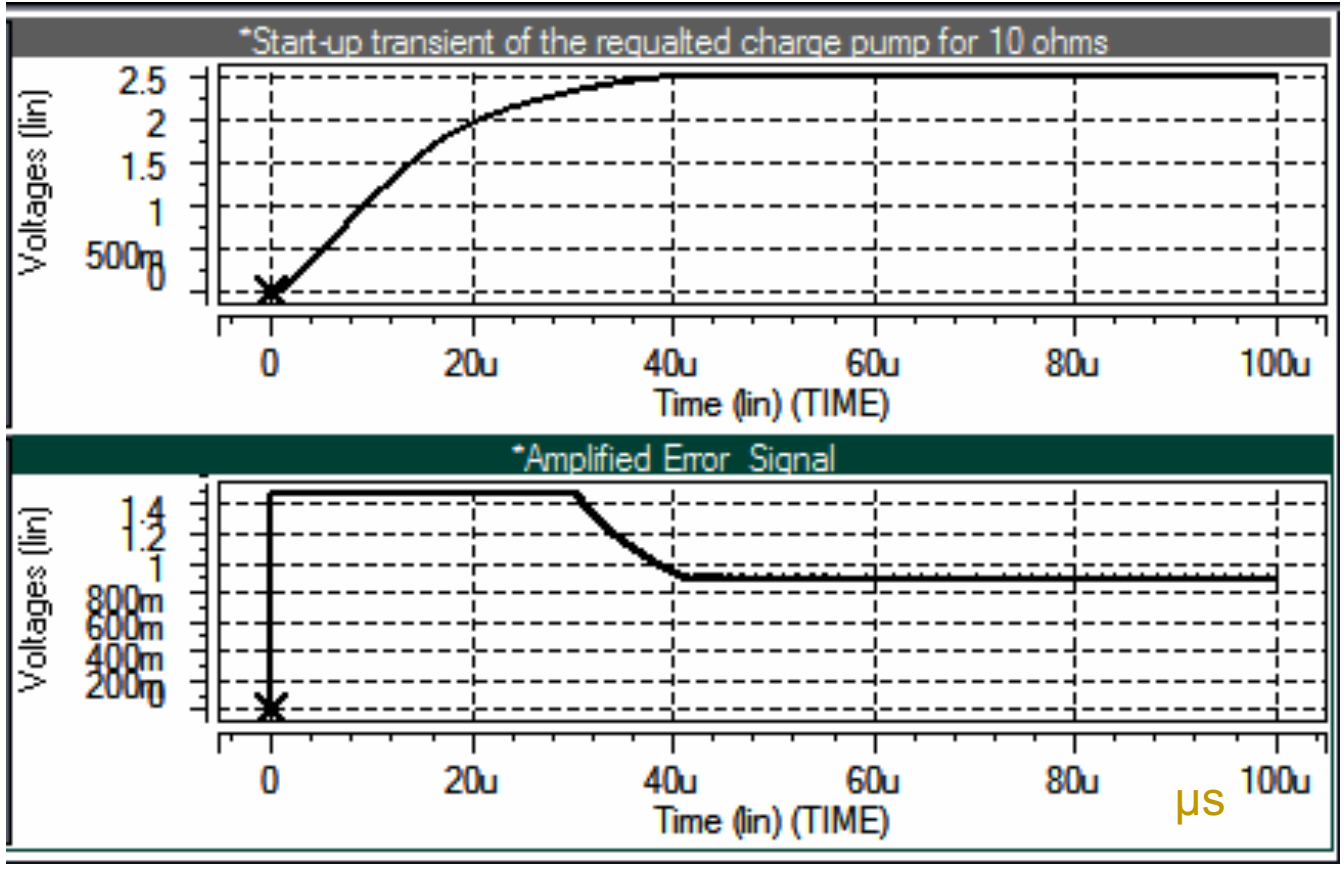


Image source: [1]

1. *Somasundaram, Mohankumar N., and Dongsheng Ma. "Integrated low-ripple-voltage fast-response switched-capacitor power converter with interleaving regulation scheme." 2006 IEEE International Symposium on Circuits and Systems. IEEE, 2006*

PROPOSED CLOSED-LOOP TYPE BY SOMASUNDARAM AND MA

Load current step increase from 165 mA to 250 mA →

Zoom of the output voltage shows voltage settling within 3 µs with a drop of only 22 mV →

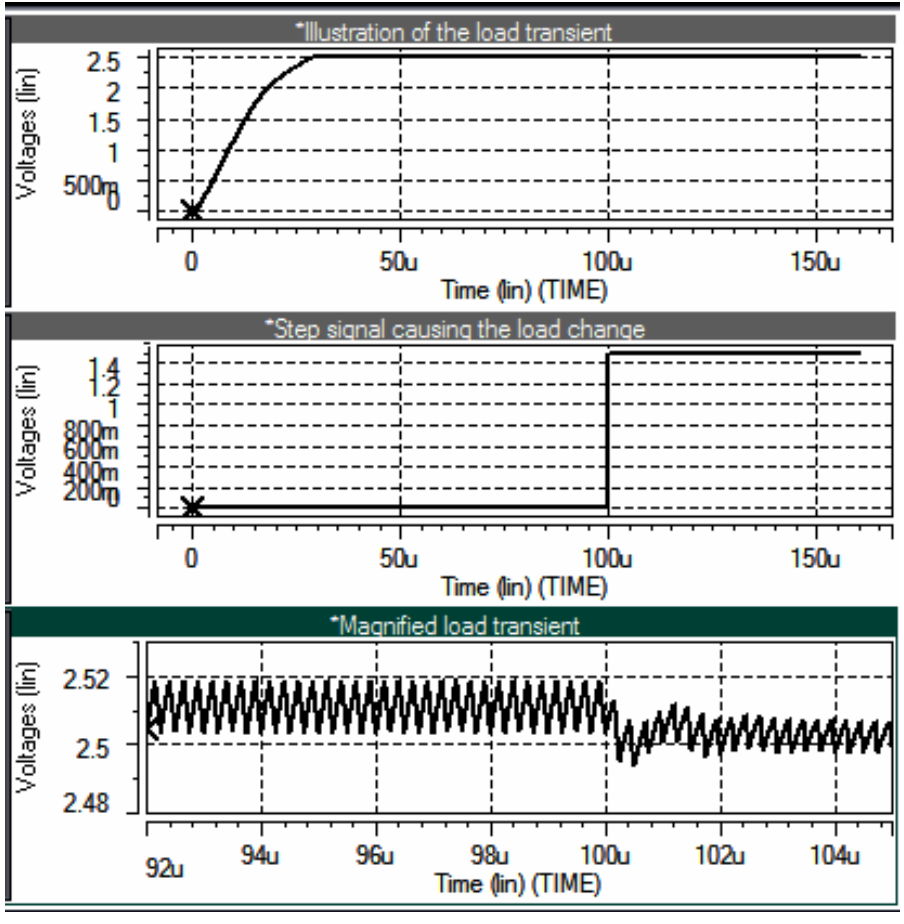


Image source: [1]

1. *Somasundaram, Mohankumar N., and Dongsheng Ma. "Integrated low-ripple-voltage fast-response switched-capacitor power converter with interleaving regulation scheme." 2006 IEEE International Symposium on Circuits and Systems. IEEE, 2006*

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PROPOSED DIGITAL CLOSED-LOOP TYPE BY SOMASUNDARAM AND MA

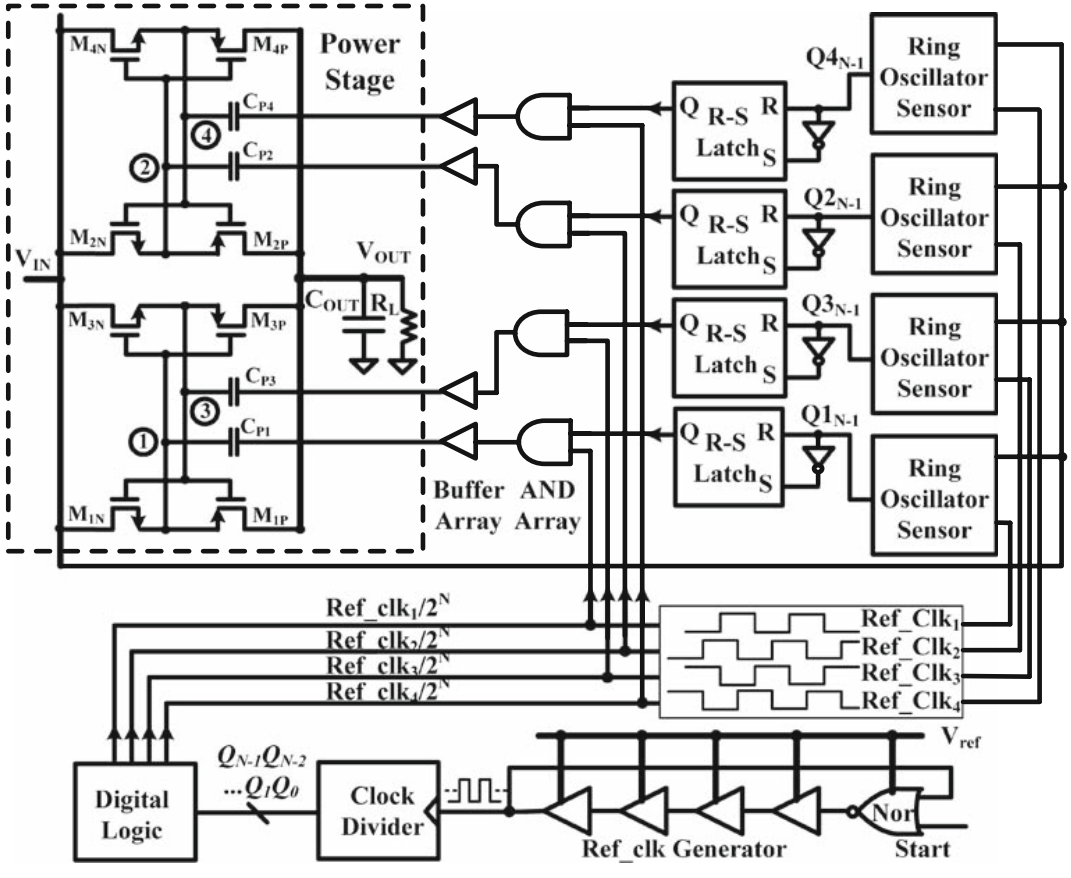

Image source: [1]

V_{OUT} fed into **ring-oscillator A/D converter** → f_{OUT}

f_{OUT} and f_{ref} are used to control duty cycles and therefore keep V_{OUT} at a design set point

1. *Ma, D., Su, L., & Somasundaram, M. (2010). Integrated interleaving SC power converters with analog and digital control schemes for energy-efficient microsystems. Analog Integrated Circuits and Signal Processing, 62(3), 361-372.*

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MULTI-PHASE 1GHZ VOLTAGE DOUBLER CHARGE-PUMP IN 32NM LOGIC PROCESS

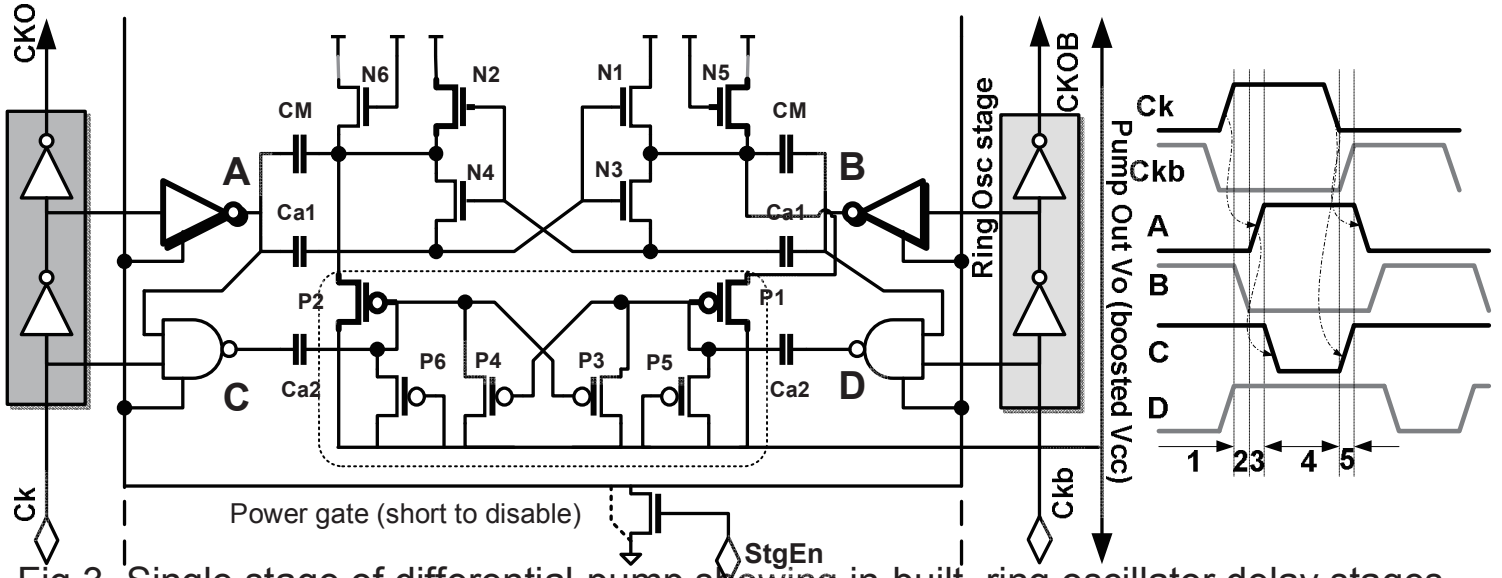

Fig 3. Single stage of differential-pump showing in-built ring oscillator delay stages, main and auxilary drivers, commutation switches, gate drive and fail-safe circuits

Dickson type CPs. Operation in 1-2-3-4-3-2-1 eliminates short-circuit paths which prematurely discharge the capacitor and allow for efficiency to approach ideal efficiency

1. *Somasekhar, D., Srinivasan, B., Pandya, G., Hamzaoglu, F., Khellah, M., Karnik, T., & Zhang, K. (2010). Multi-phase 1 GHz voltage doubler charge pump in 32 nm logic process. IEEE Journal of Solid-State Circuits, 45(4), 751-758.*

Image source: [1]

MULTI-PHASE 1GHZ VOLTAGE DOUBLER CHARGE-PUMP IN 32NM LOGIC PROCESS

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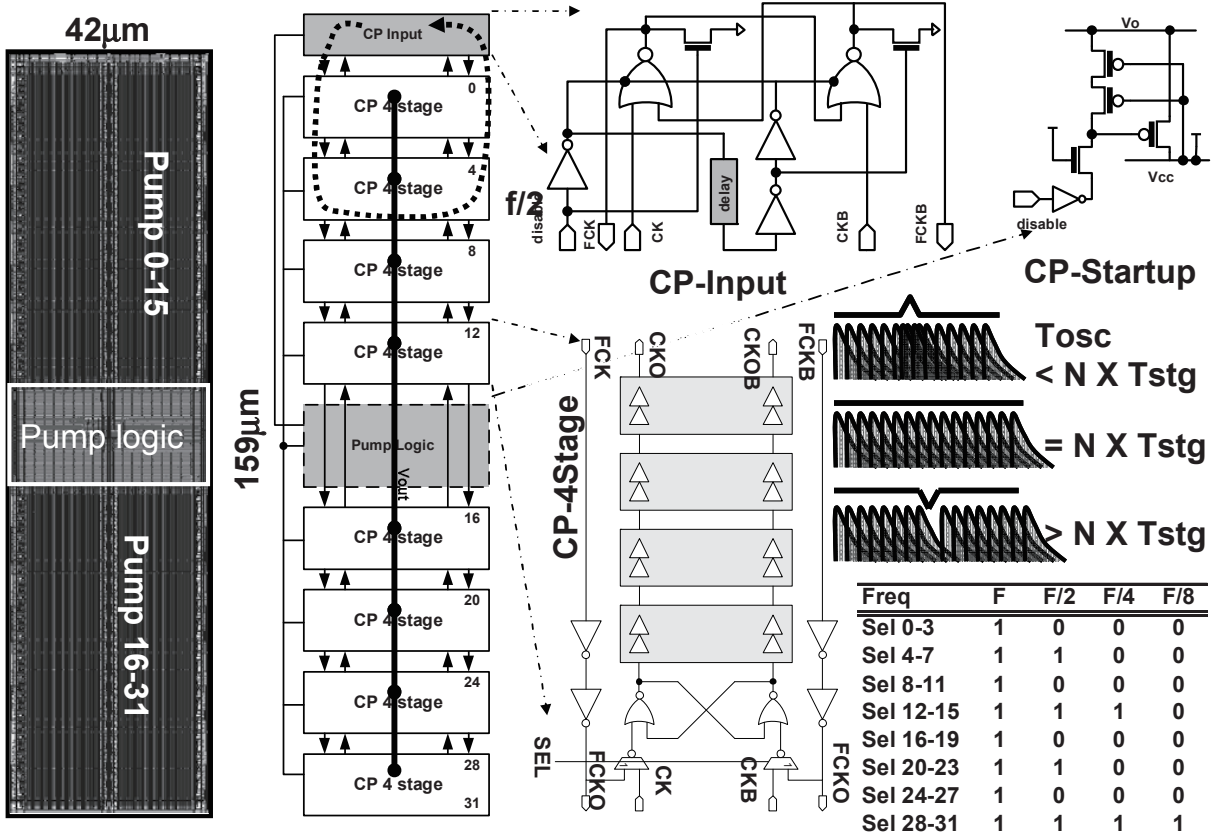
- Implementation on a die
- Self contained clocking
- Interleaving enables fast (5ns) ON/OFF output transition
- Operates as 1V to 2V doubler with >5mA capability
- Frequency and Rout of the pump can be digitally varied for regulation purposes

Image source: [1]



Freq	F	F/2	F/4	F/8
Sel 0-3	1	0	0	0
Sel 4-7	1	1	0	0
Sel 8-11	1	0	0	0
Sel 12-15	1	1	1	0
Sel 16-19	1	0	0	0
Sel 20-23	1	1	0	0
Sel 24-27	1	0	0	0
Sel 28-31	1	1	1	1

Fig 4. Multi-phase pump with in built ring oscillator, frequency control, local overlap generation, and startup circuits

1. *Somasekhar, D., Srinivasan, B., Pandya, G., Hamzaoglu, F., Khellah, M., Karnik, T., & Zhang, K. (2010). Multi-phase 1 GHz voltage doubler charge pump in 32 nm logic process. IEEE Journal of Solid-State Circuits, 45(4), 751-758.*

MULTI-PHASE 1GHZ VOLTAGE DOUBLER CHARGE-PUMP IN 32NM LOGIC PROCESS

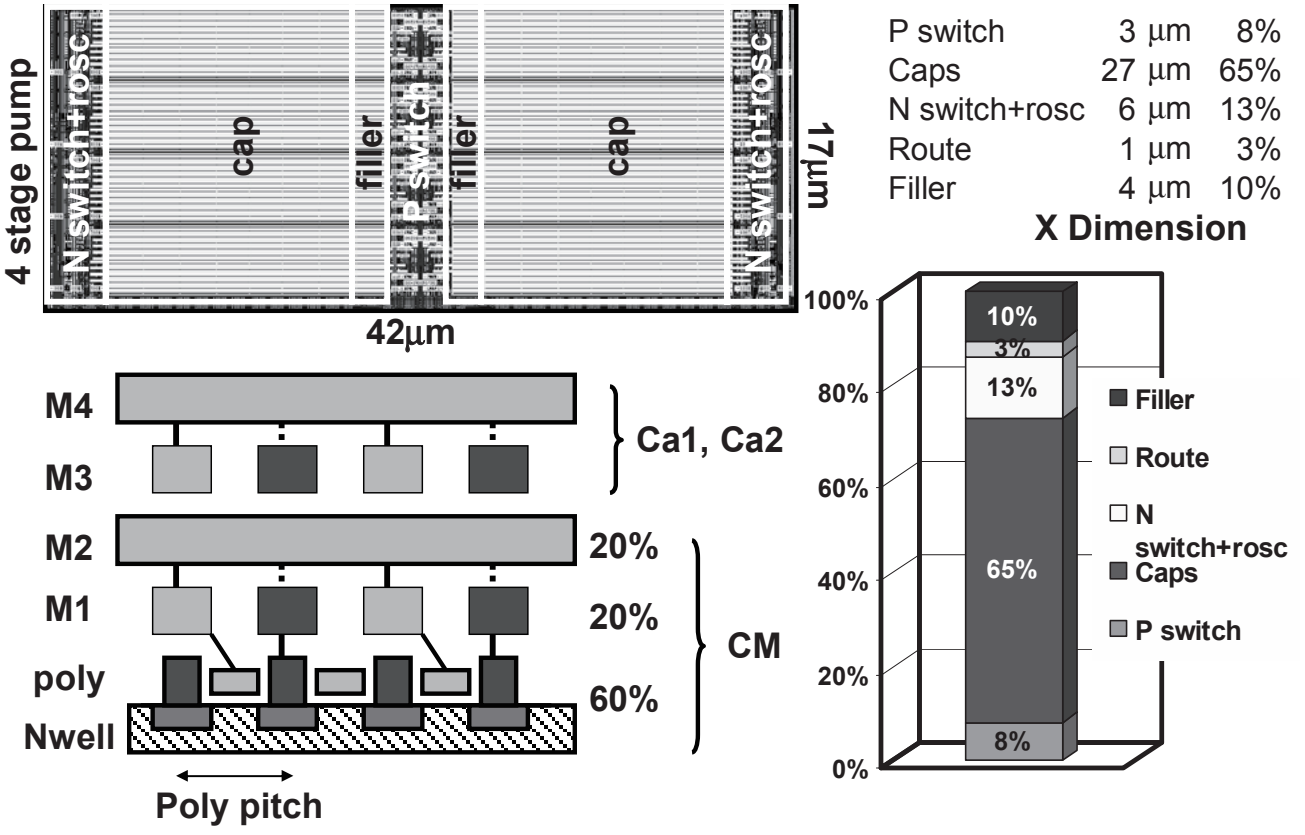


Fig 5. Layered capacitor structure for main and auxilary caps highlighting the use of trench to poly cap. Breakdown of charge pump layout usage and placement of components

Image source: [1]

1. *Somasekhar, D., Srinivasan, B., Pandya, G., Hamzaoglu, F., Khellah, M., Karnik, T., & Zhang, K. (2010). Multi-phase 1 GHz voltage doubler charge pump in 32 nm logic process. IEEE Journal of Solid-State Circuits, 45(4), 751-758.*

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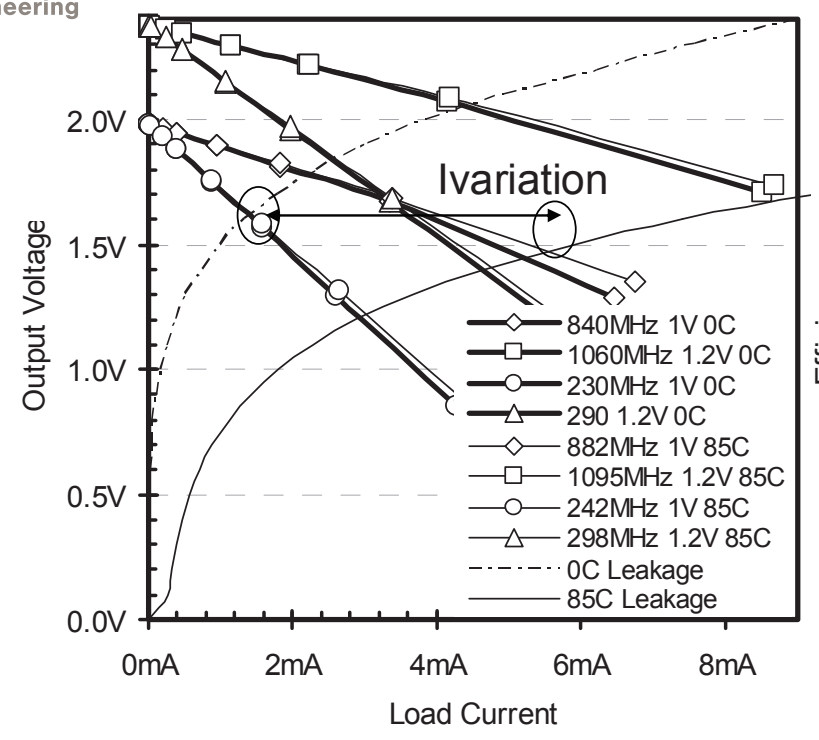

Fig 6: Simulated Load Line at and slow frequency showing range of fmax to tolerate lkg variation with temperature

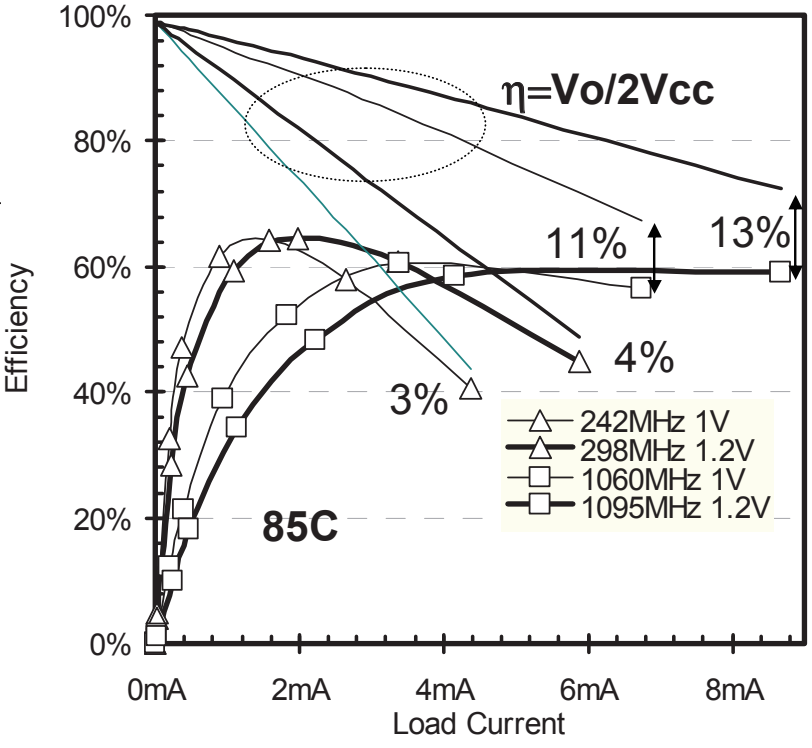

Fig 7. Pump Efficiency plots vs ideal efficiency

Image source: [1]

1. *Somasekhar, D., Srinivasan, B., Pandya, G., Hamzaoglu, F., Khellah, M., Karnik, T., & Zhang, K. (2010). Multi-phase 1 GHz voltage doubler charge pump in 32 nm logic process. IEEE Journal of Solid-State Circuits, 45(4), 751-758.*

MULTI-PHASE 1GHZ VOLTAGE DOUBLER CHARGE-PUMP IN 32NM LOGIC PROCESS

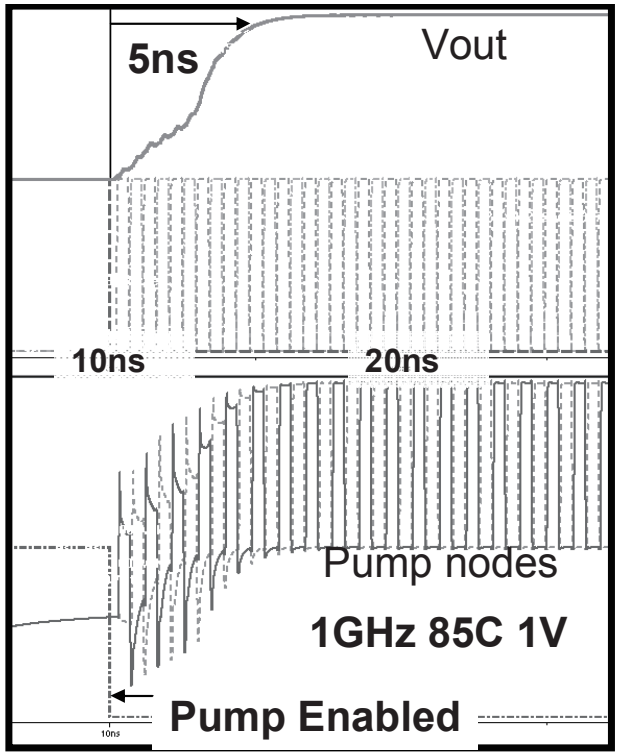

Fig 8: Pump non overlap waverforms, High speed wakeup is shown

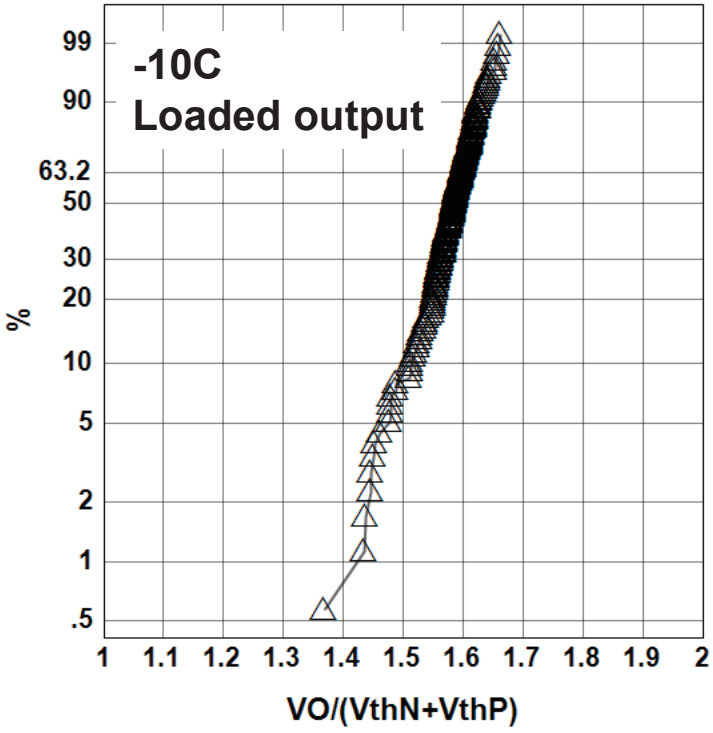

Fig 9: Single wafer measurement proving pump operation at 3Vth point

Image source: [1]

1. *Somasekhar, D., Srinivasan, B., Pandya, G., Hamzaoglu, F., Khellah, M., Karnik, T., & Zhang, K. (2010). Multi-phase 1 GHz voltage doubler charge pump in 32 nm logic process. IEEE Journal of Solid-State Circuits, 45(4), 751-758.*

CONCLUSION

- SCC and interleaving regulation can be designed into off-chip and on-chip circuits
- Enables large scale integration and miniaturization
- Can handle low input voltages
- With large N, very low ripple and fast response circuit designs are possible

Image credit: CBS Television Studios (CTS)

Homework

Exercise 1:

- Propose an alternative scheme to the common 2π / N inter-cell phase angle, and explain what benefits it might have. You can for example check ”Klaassens, J. B., De Chateleux, W. M., & Van Wesenbeeck, M. P. N. (1988). Phase-staggering control of a series-resonant DC-DC converter with paralleled power modules. IEEE transactions on power electronics, 3(2), 164-173”. This paper is available from IEEE Xplore (lib.aalto.fi).

Exercise 2:

- Shortly explain the benefits of increasing the number of sub-cells N in SCC with interleaving regulation

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