Moore’s law

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Chapter 38

You know

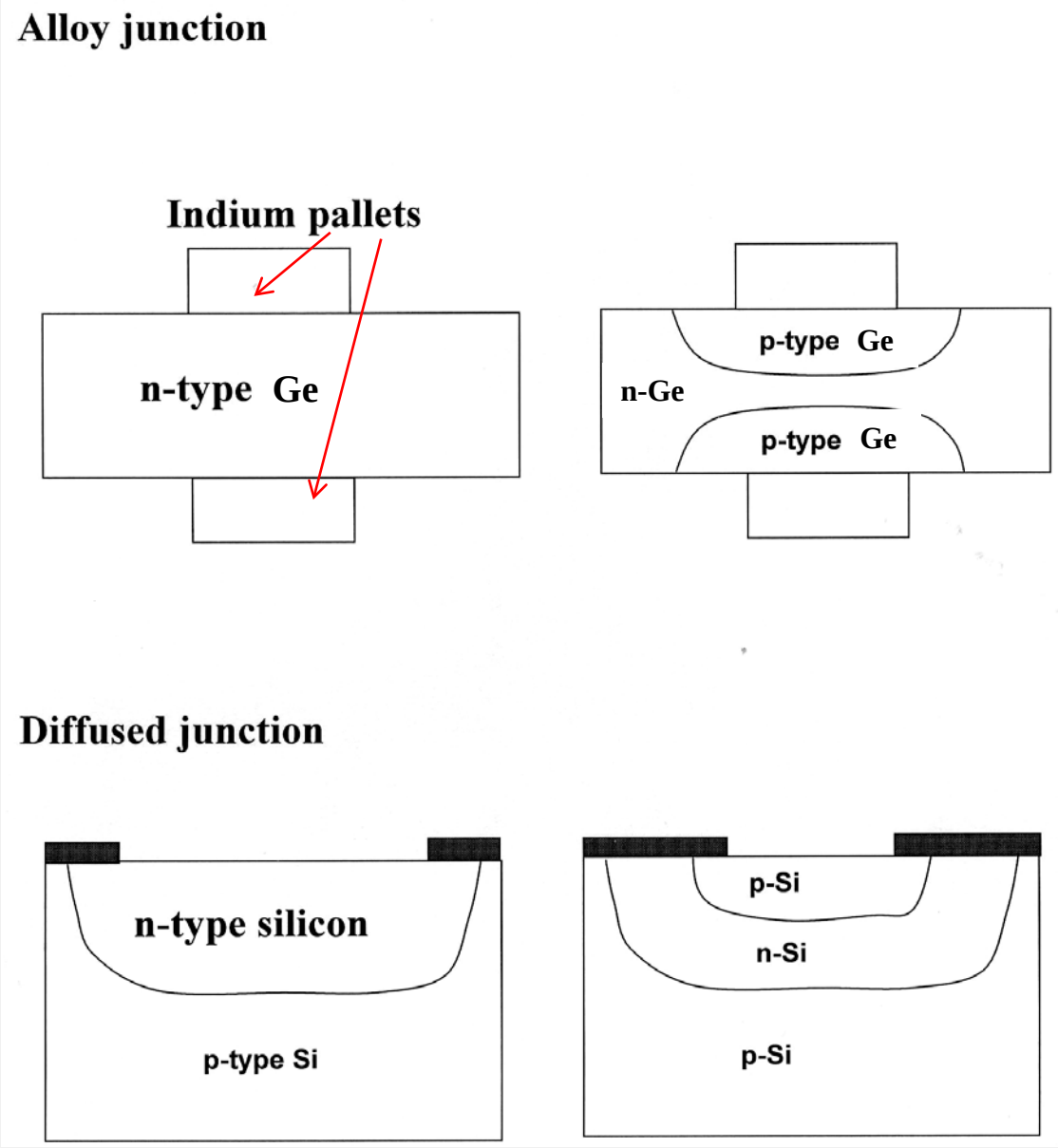
Everything!

Moore’s law

- Moore’s law
- Microlithography trends
- Double patterning
- FinFET

Transistor fabrication, 1950's

One chip – one transistor
Chip size 3 x 3 mm^2



Semiconductor technology nodes

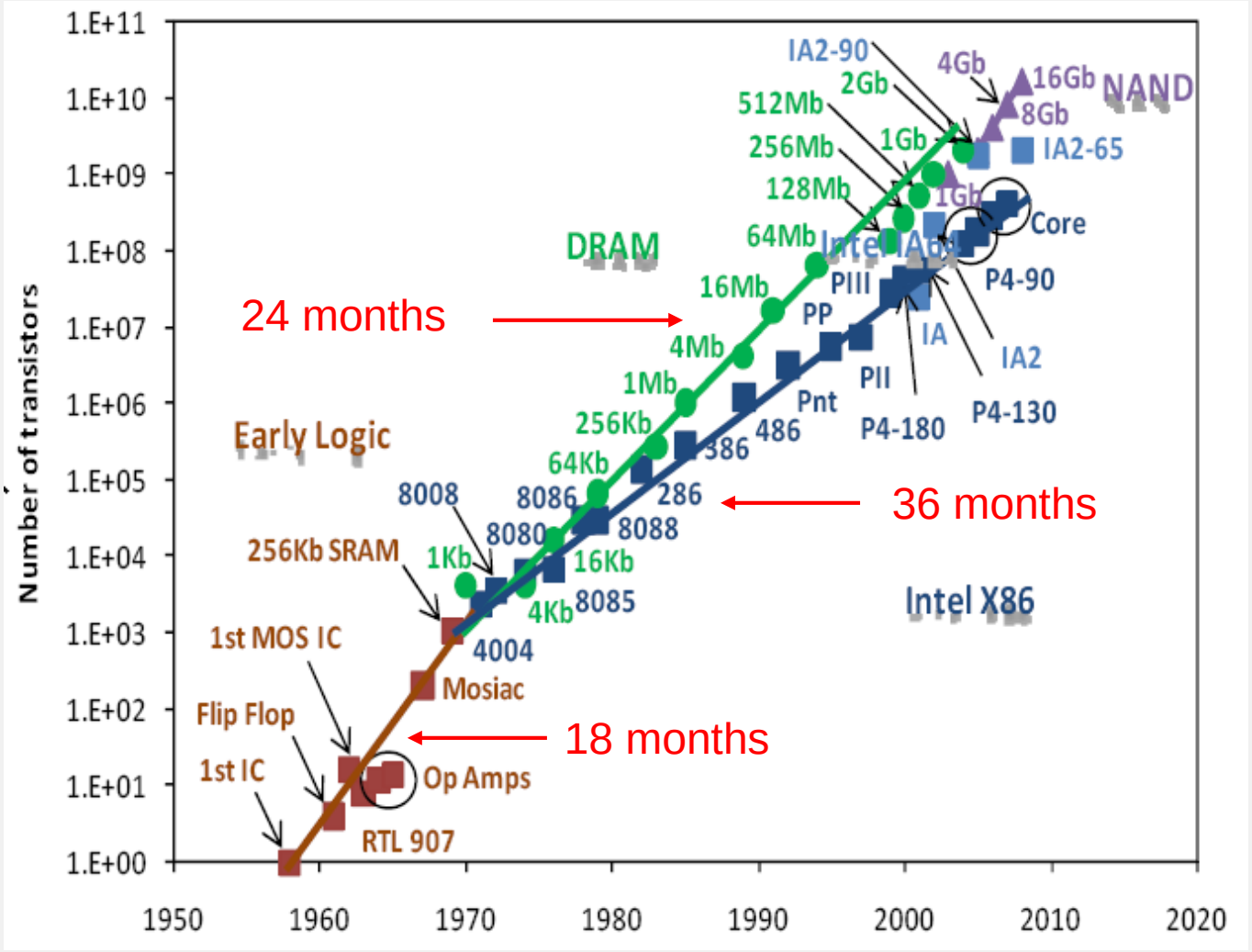
Scaling factor $\sqrt{2}$

- 10 µm – 1971
- 3 µm – 1975
- 1.5 µm – 1982
- 1 µm – 1985
- 0.8 µm – 1989
- 0.6 µm – 1994
- 0.35 µm – 1995
- 0.25 µm – 1998
- 0.18 µm – 1999
- 0.13 µm – 2000
- 90 nm – 2002
- 65 nm – 2006
- 45 nm – 2008
- 32 nm – 2010
- 22 nm – 2012
- 14 nm – 2014
- 10 nm – 2017
- 7 nm – 2018

Moore’s law I

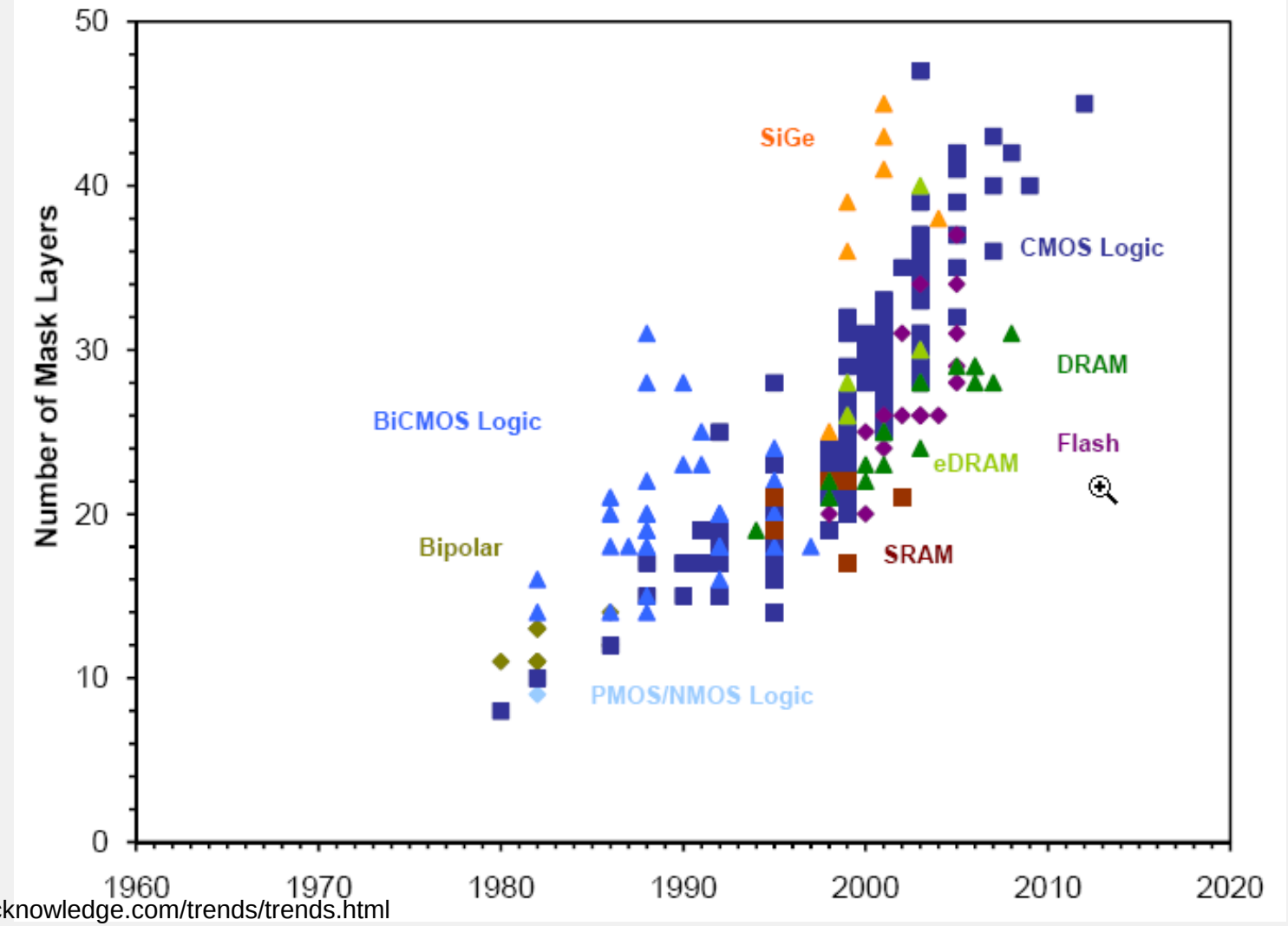
- The number of components per IC doubles every 18 -24 months.
- Introduced in 1965
- Does not depend on technology
- Reflects development of mankind, i.e., technology in general sense

Moore's law II



http://www.icknowledge.com/trends/trends.html

The price of shrinking linewidths I



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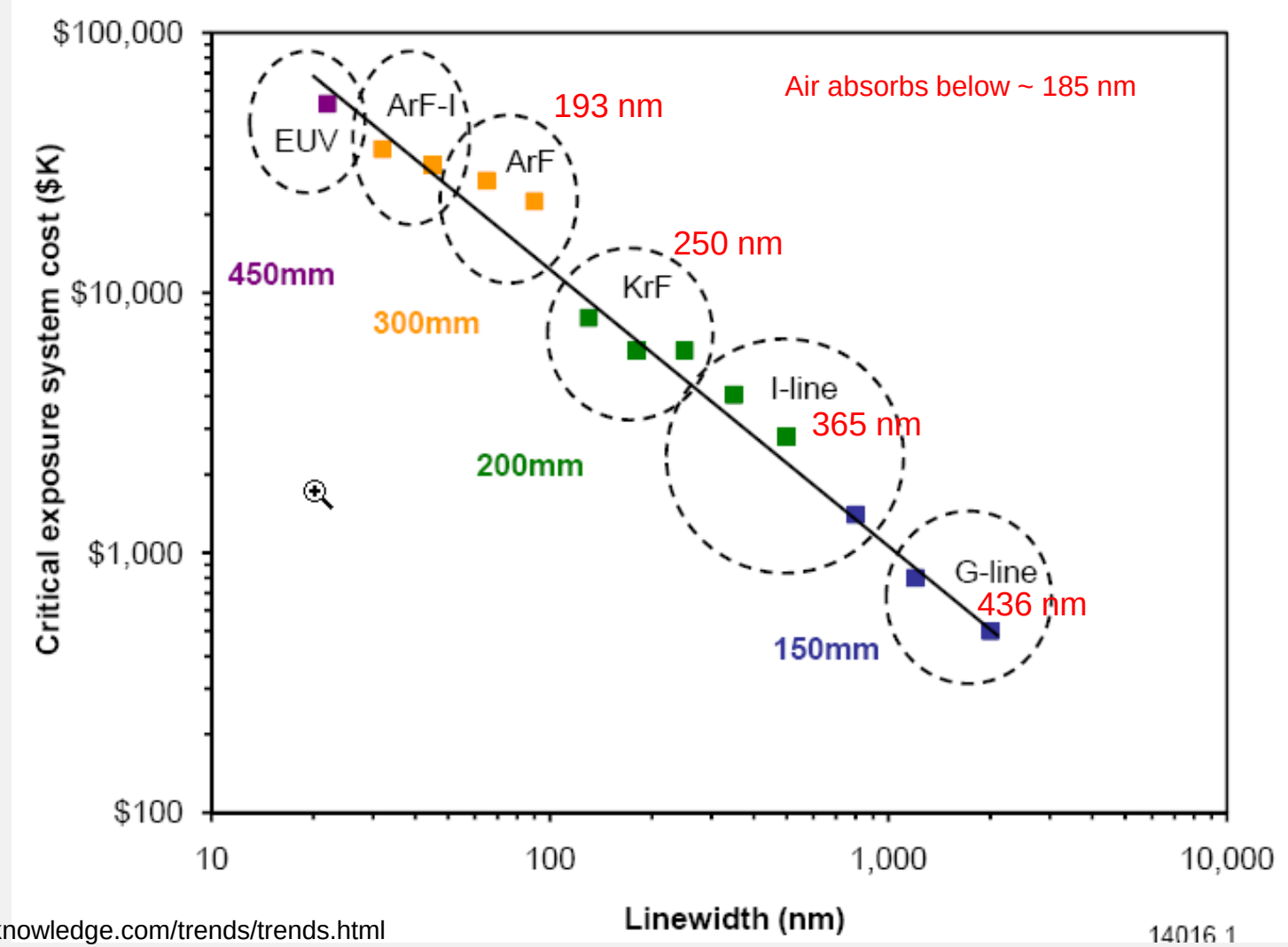
The price of shrinking linewidths II



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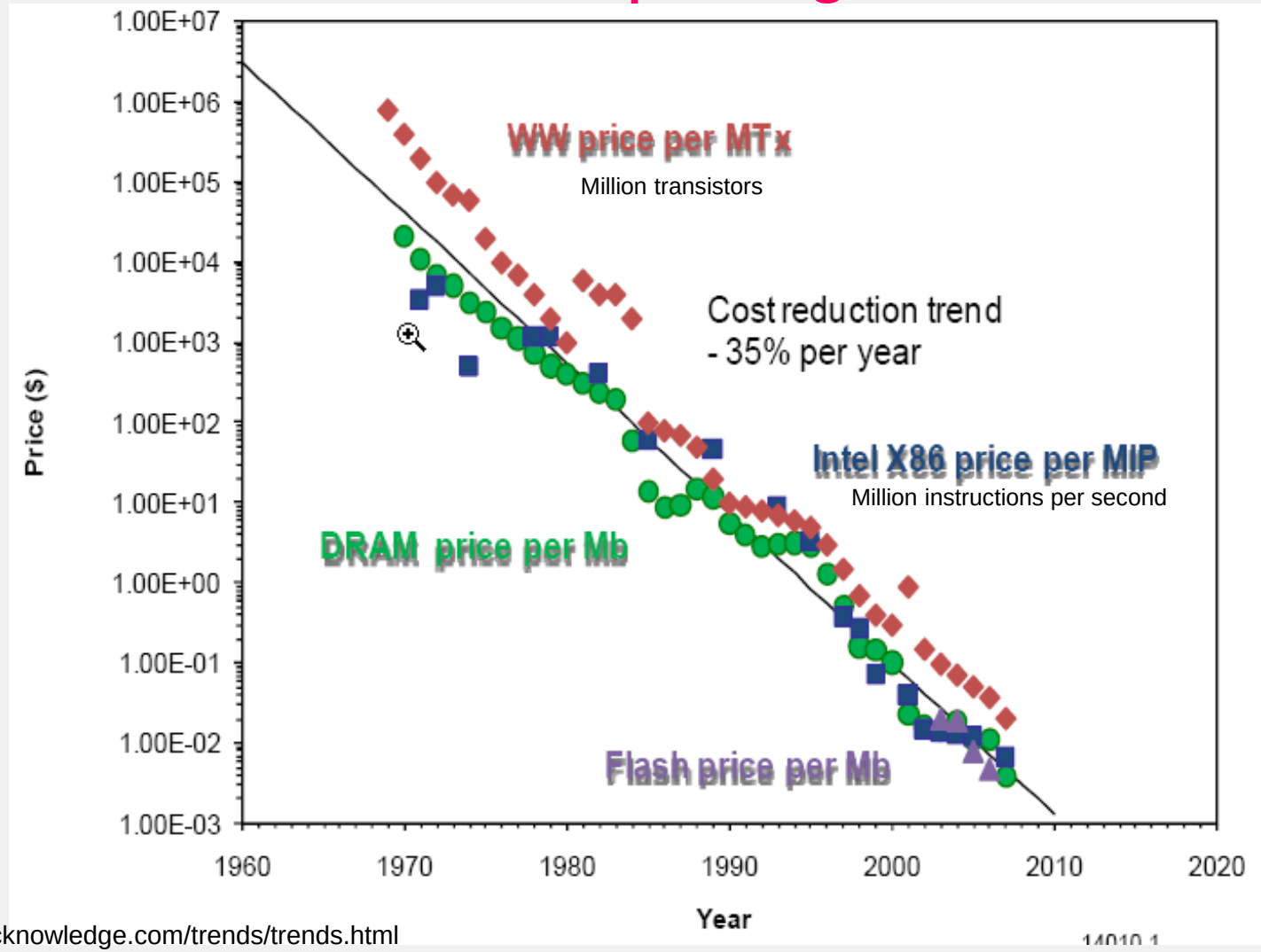
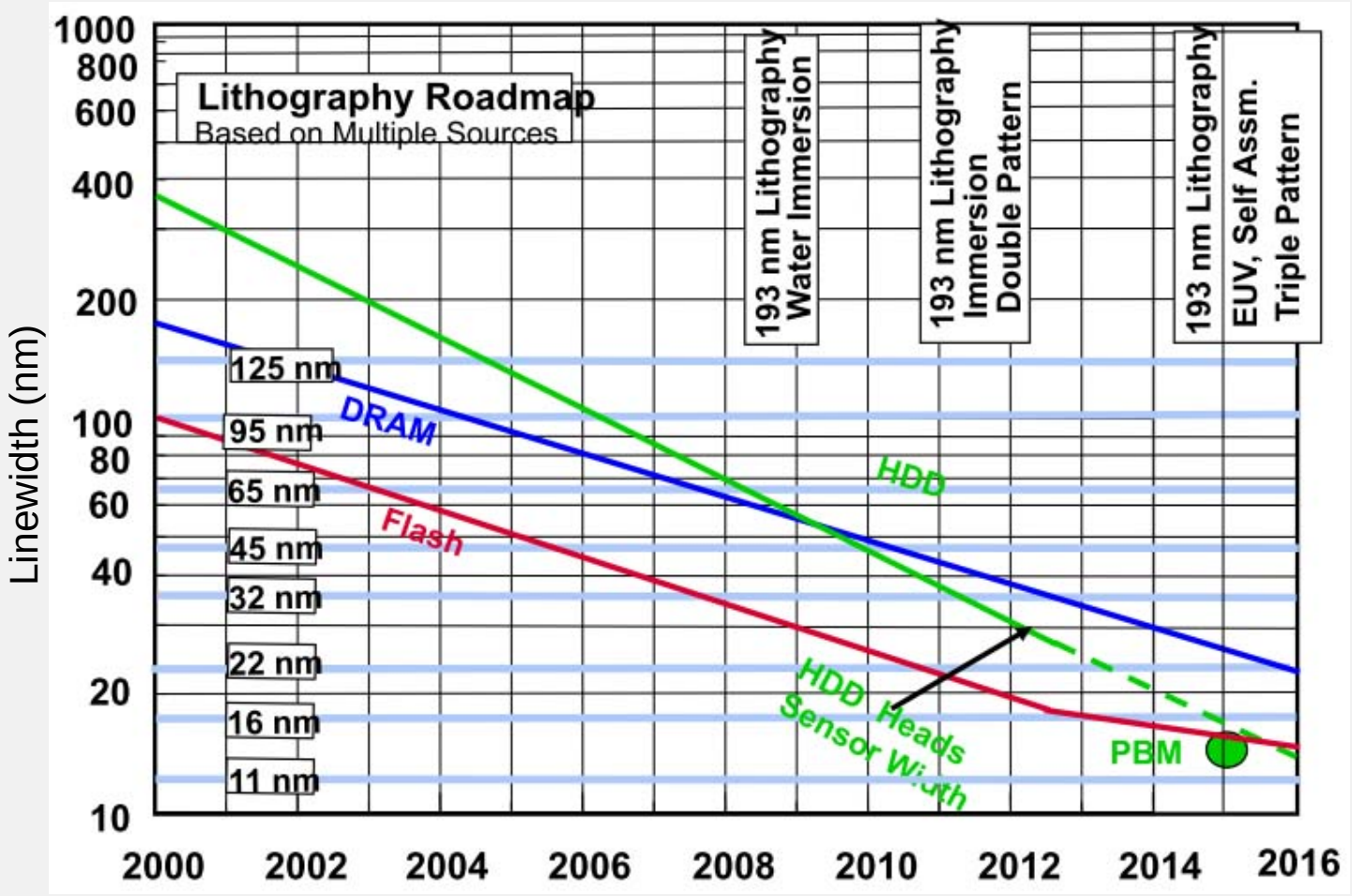
Product pricing



http://www.icknowledge.com/trends/trends.html

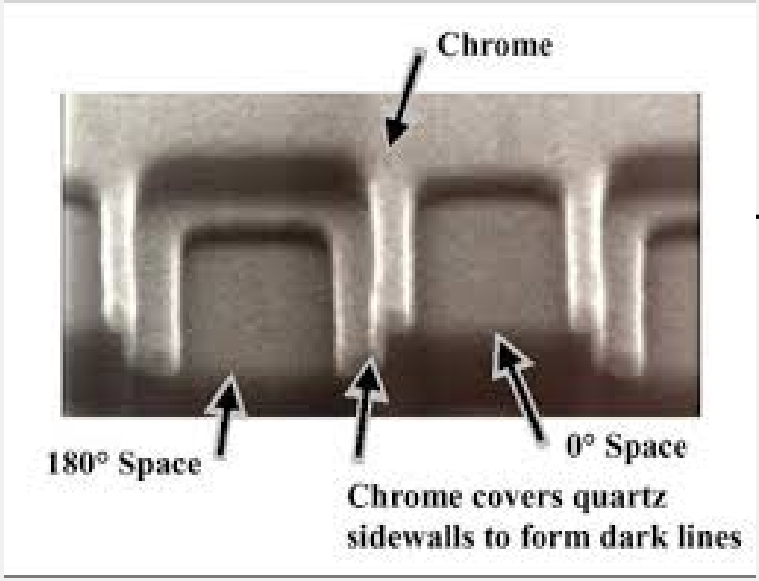
Microlithography trends

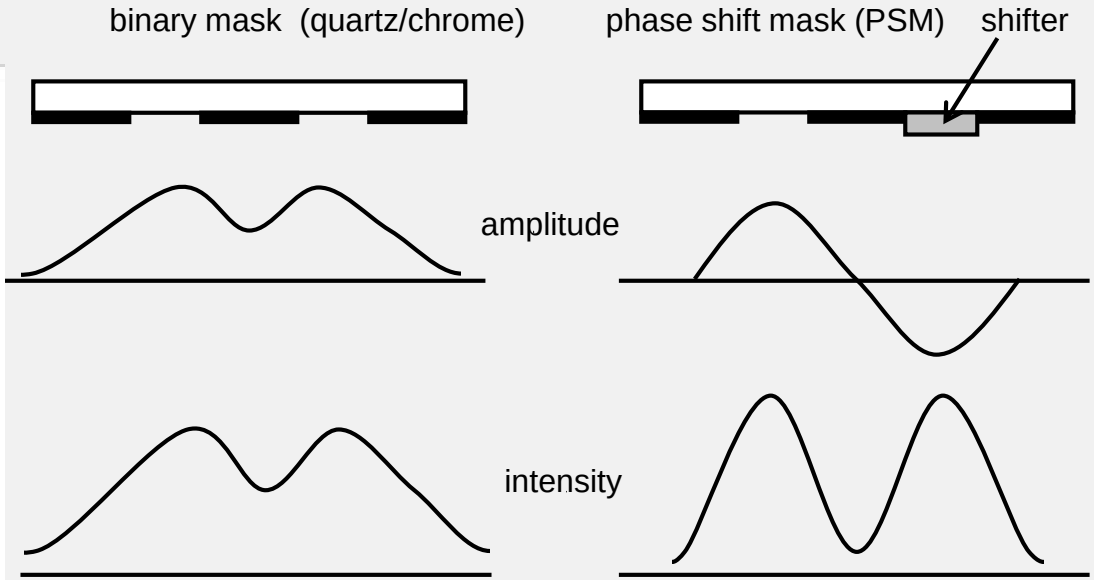


ITRS Roadmap 2012

Phase shift mask (PSM)

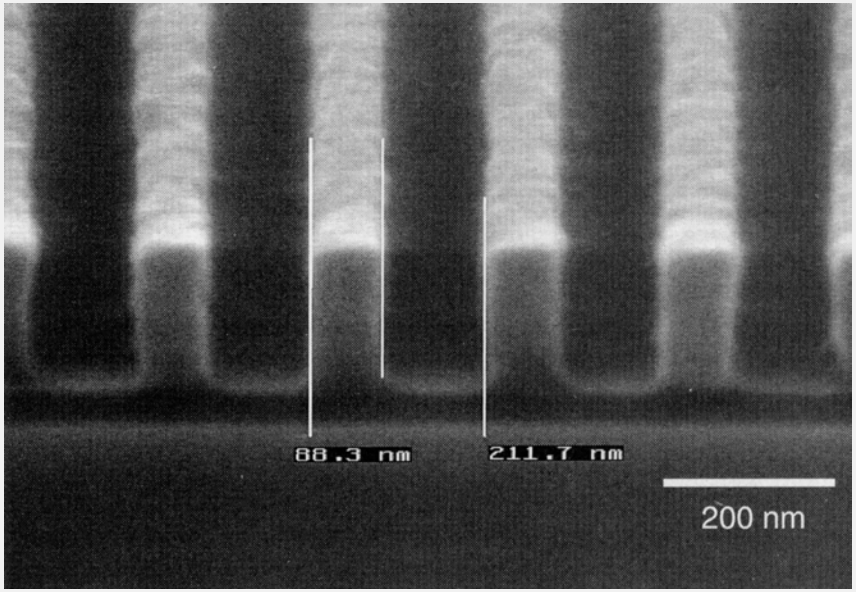
- Phase shift for light traveling:
  - in the air for a distance L is
    $\Phi = 2\pi L/\lambda$,
  - in the phase shifter material with index of refraction "n",
    $\Phi = 2\pi nL/\lambda$.
- For 180 degree phase shift, $\Delta\Phi = 180^{o}$, the condition for shifter thickness is given by
  $L\,(n\text{-}1) = \lambda/2$



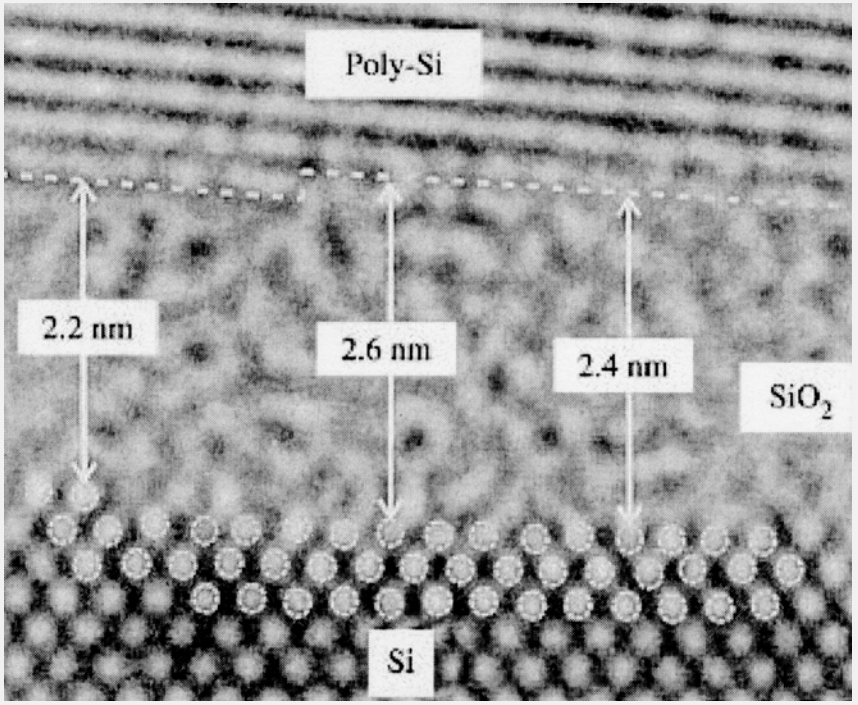


PSM and quantized SiO_2

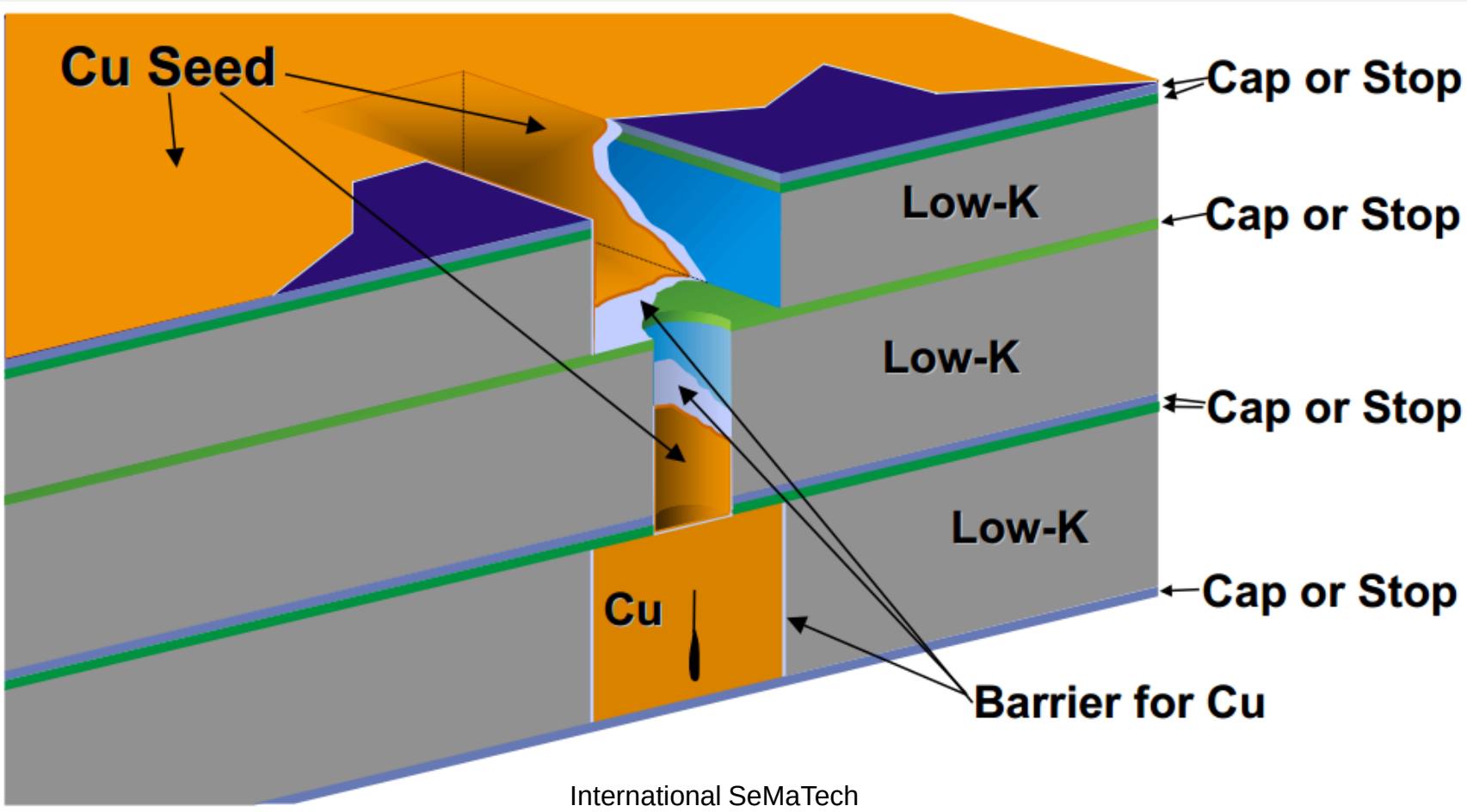
Resolution λ/2, λ=193nm



Quantized gate oxide thickness

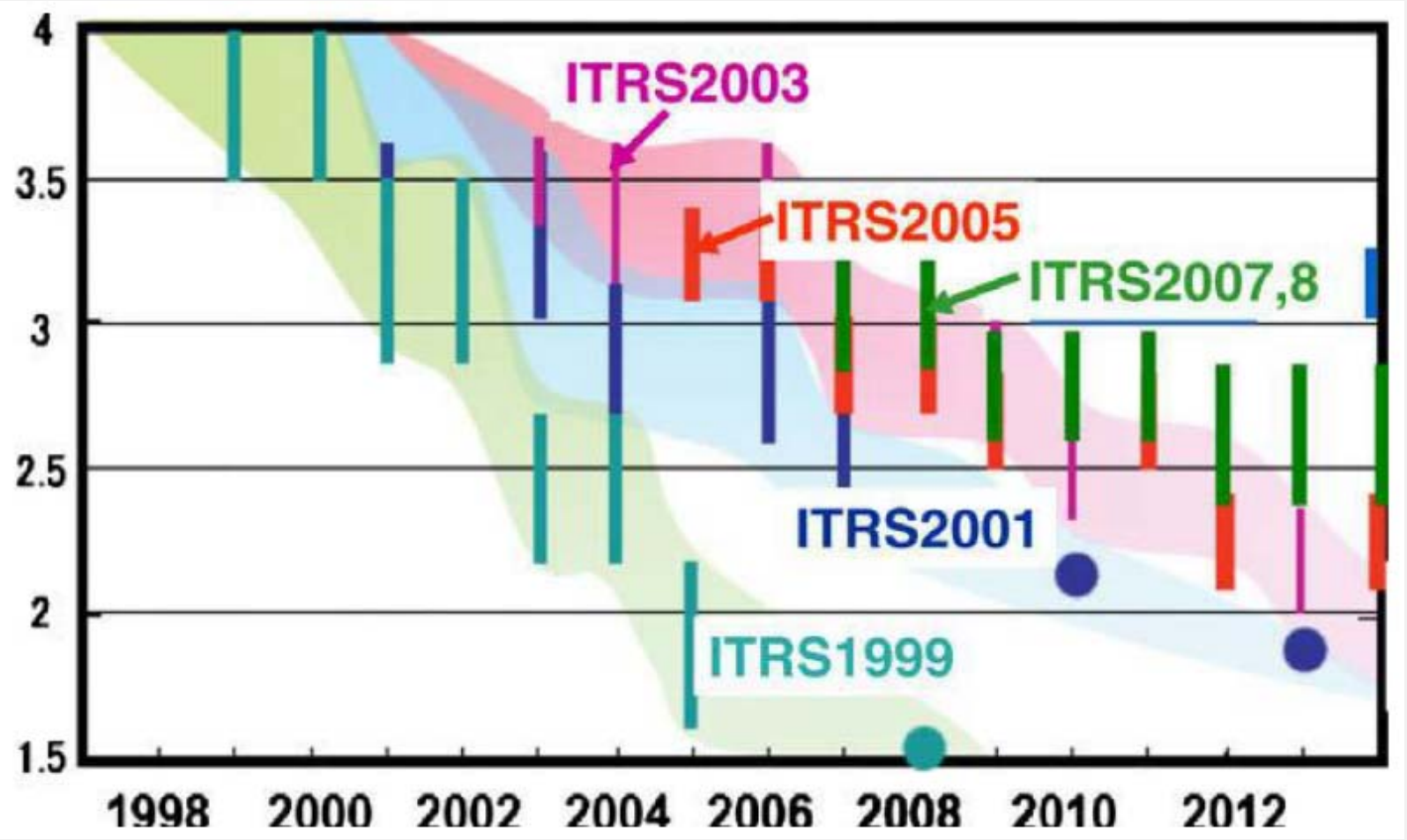


Dual damascene unit structure

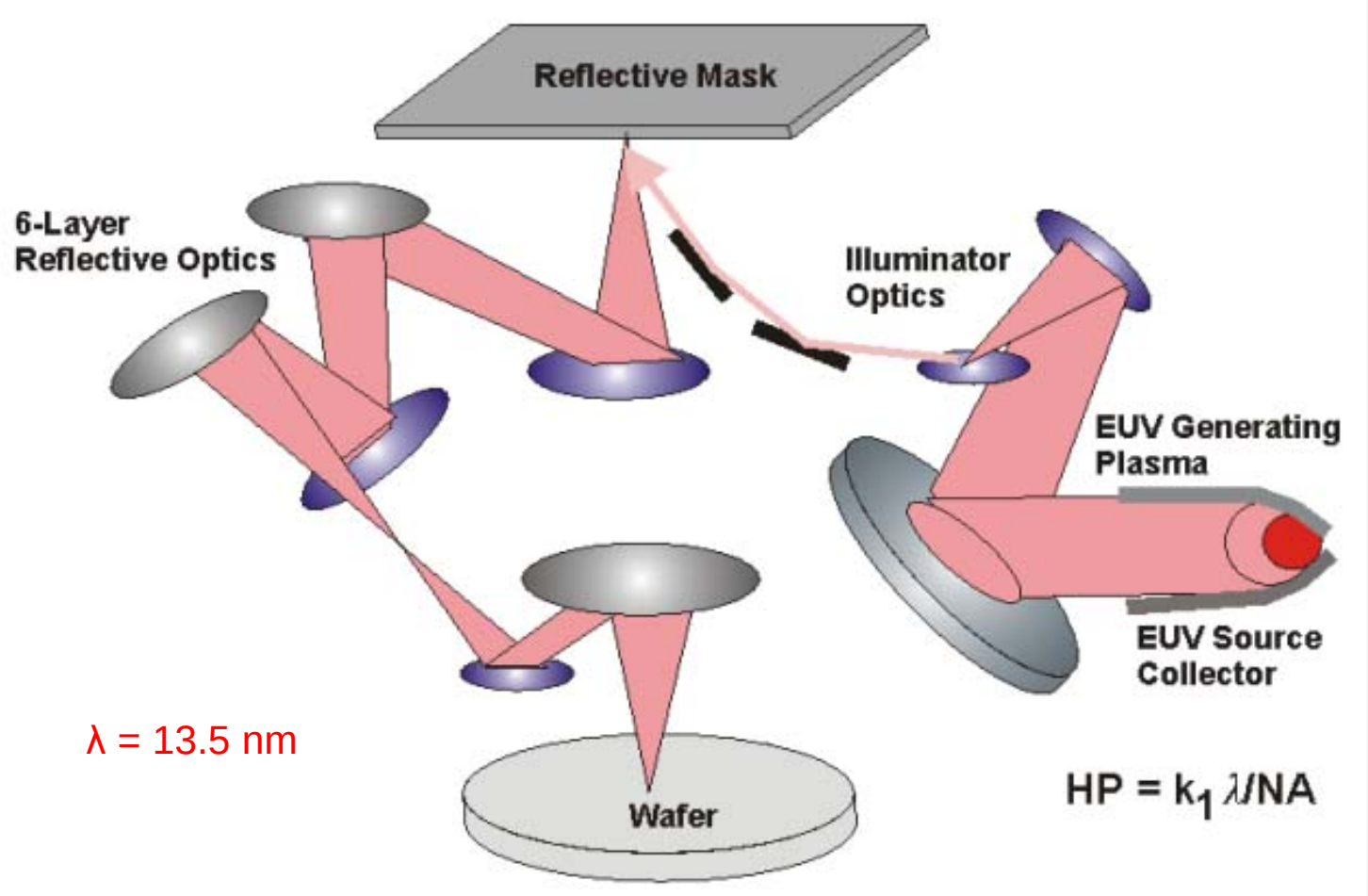


International SeMaTech

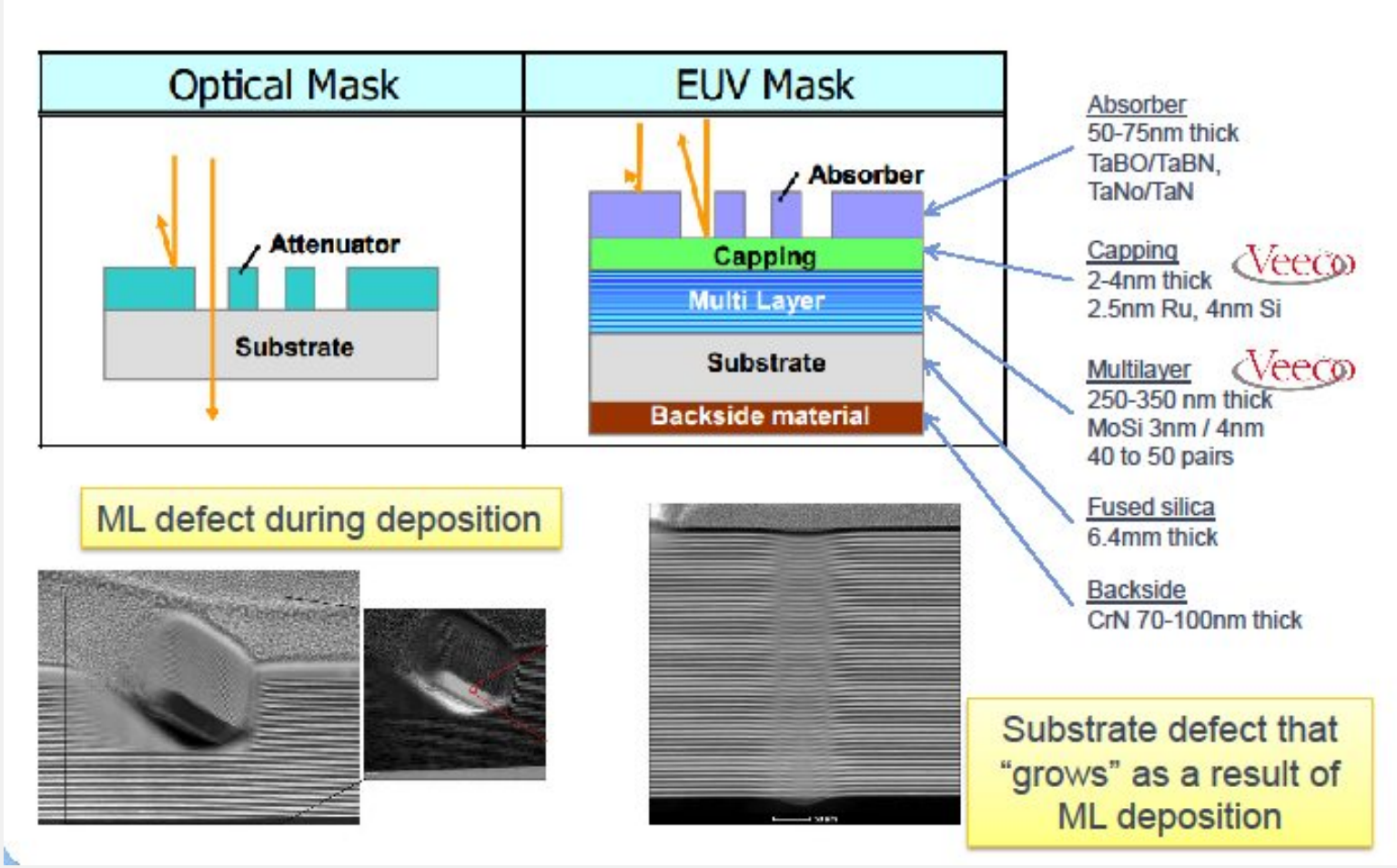
Low-K is hard…


4
3.5
3
2.5
2
1.5
1998
2000
2002
2004
2006
2008
2010
2012
ITRS2003
ITRS2005
ITRS2007,8
ITRS2001
ITRS1999

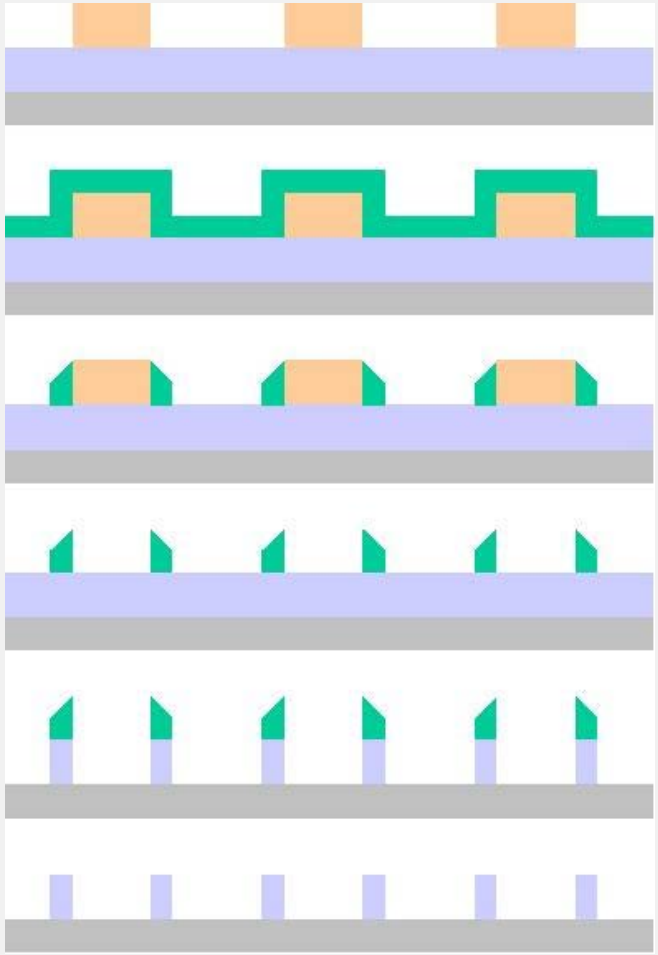
EUV


Reflective Mask
6-Layer
Reflective Optics
Illuminator
Optics
EUV Generating
Plasma
EUV Source
Collector
λ = 13.5 nm
Wafer
HP = k1 λ/NA

EUV mask


Optical Mask
EUV Mask
Attenuator
Substrate
Absorber
Capping
Multi Layer
Substrate
Backside material
Absorber
50-75nm thick
TaBO/TaBN,
TaNo/TaN
Capping
2-4nm thick
2.5nm Ru, 4nm Si
Multilayer
250-350 nm thick
MoSi 3nm / 4nm
40 to 50 pairs
Fused silica
6.4mm thick
Backside
CrN 70-100nm thick
ML defect during deposition
Substrate defect that "grows" as a result of ML deposition

Double patterning



first pattern – PR mask

CVD or ALD deposition

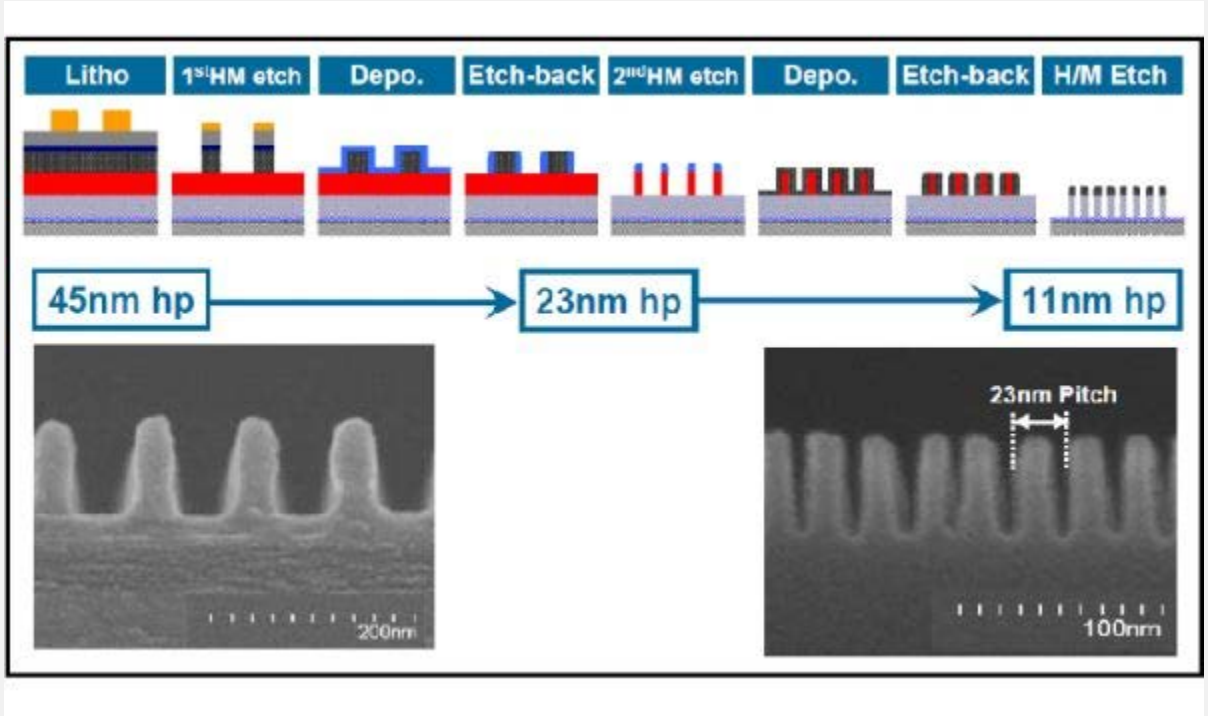
spacer formation by RIE

first pattern (PR) removal

etching with spacer mask

spacer residues removing

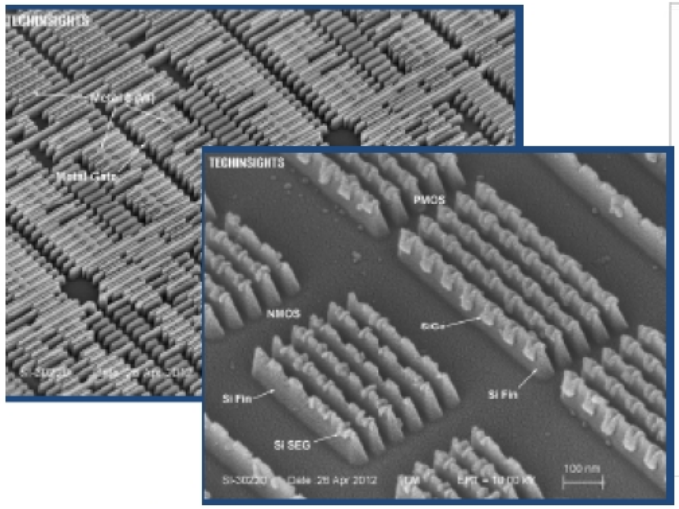
Multiple patterning I



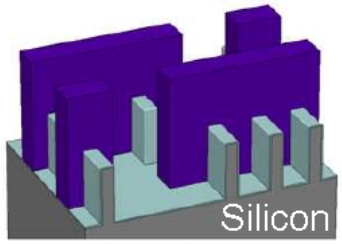
HM – hard mask

Multiple patterining II

FinFET Formation – Scalable to 10nm w/o EUV

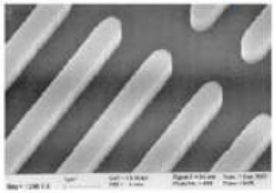


Self Aligned Double Patterning
With Cut Mask for Fin and Gate

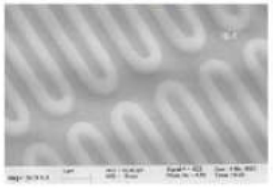


*TechInsights, Intel Ivybridge

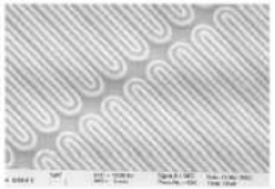
Photo-lithographically defined sacrificial structures



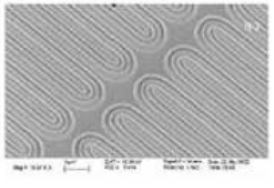
1st Spacers



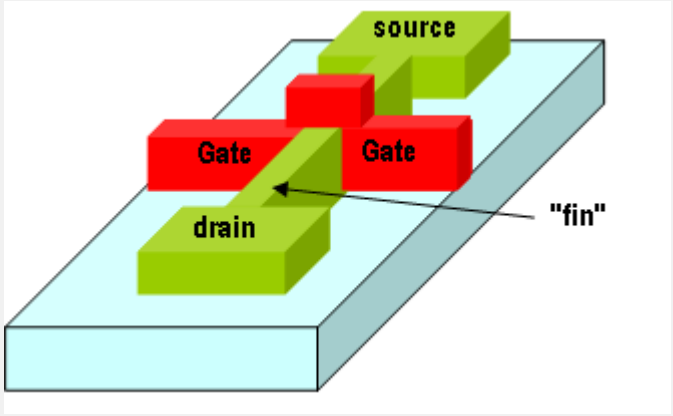
2nd Spacers



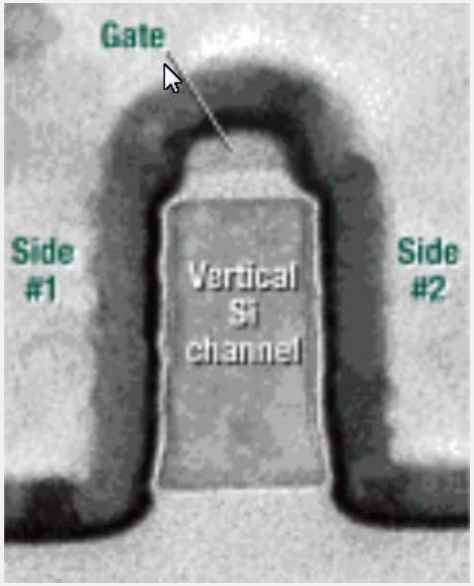
3rd Spacers

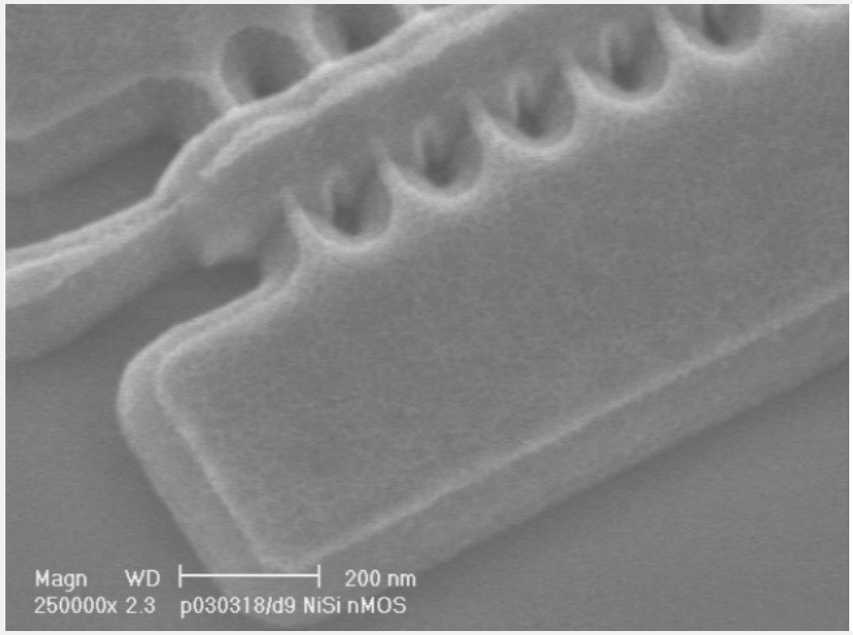


FinFET

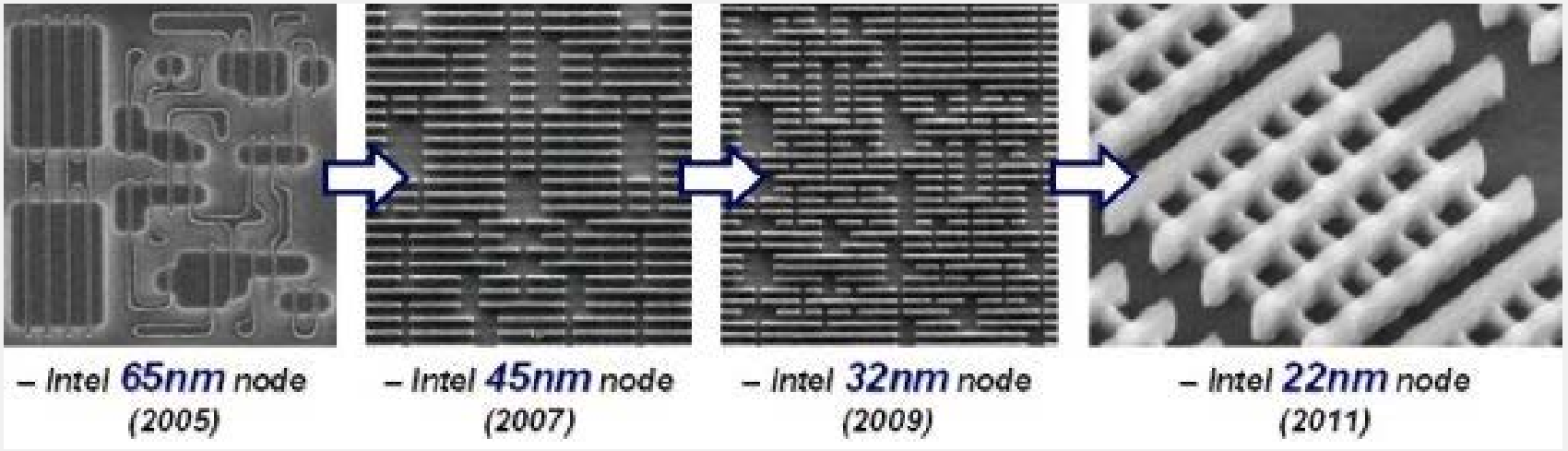


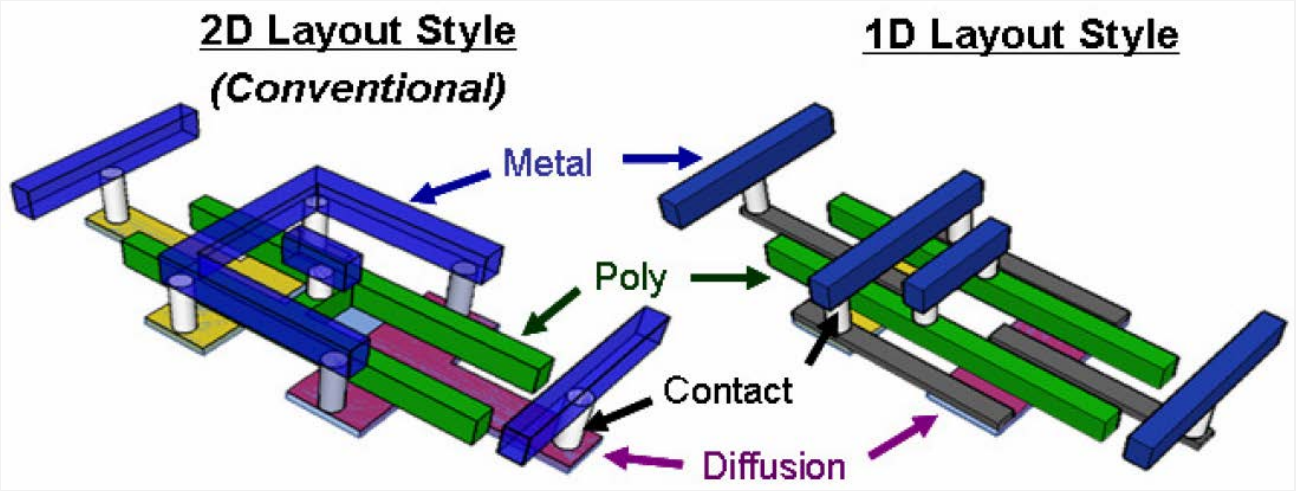
14 nm FinFET: Two levels of air-gap-insulated interconnects at 80 and 160nm minimum pitches. Eight layers of 52nm pitch interconnects embedded in low-k dielectrics. 15 levels of Cu interconnect





1-D gridded layout



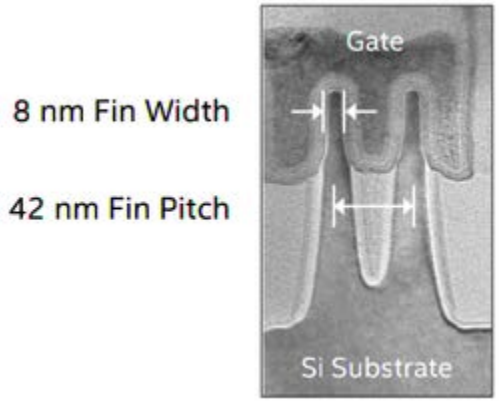


The vertical fins (9nm) of Intel's tri-gate transistors passing through the gates

David K. Lam et al., Multibeam Corporation and Tela Innovations

Modern patterning, 14 nm node

- 193 nm, ArF laser, immersion lithography, 300 mm wafer
- FinFET, TiN pMOS / TiAlN nMOS gate
- Self-Aligned Double Patterning
- Intel, processor Skylake, porous low-*k* 1st pre-metal dielectric



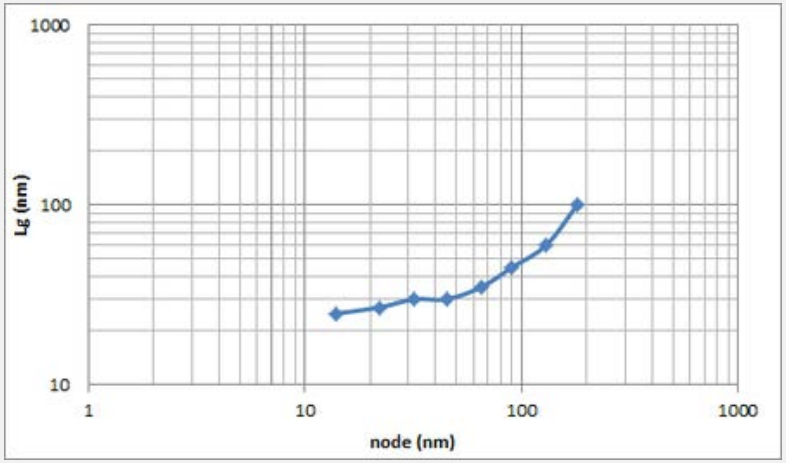
How long can this scaling continue ?

- If all goes as predicted by Moore's law, in 2059, the 100th birthday of the integrated circuit, we will have:
- 2.5 Å minimum linewidth
- 0.04 Å gate oxide thickness
- 2 mV operating voltage
- 64 exabit DRAMs (exa = 10^{18})

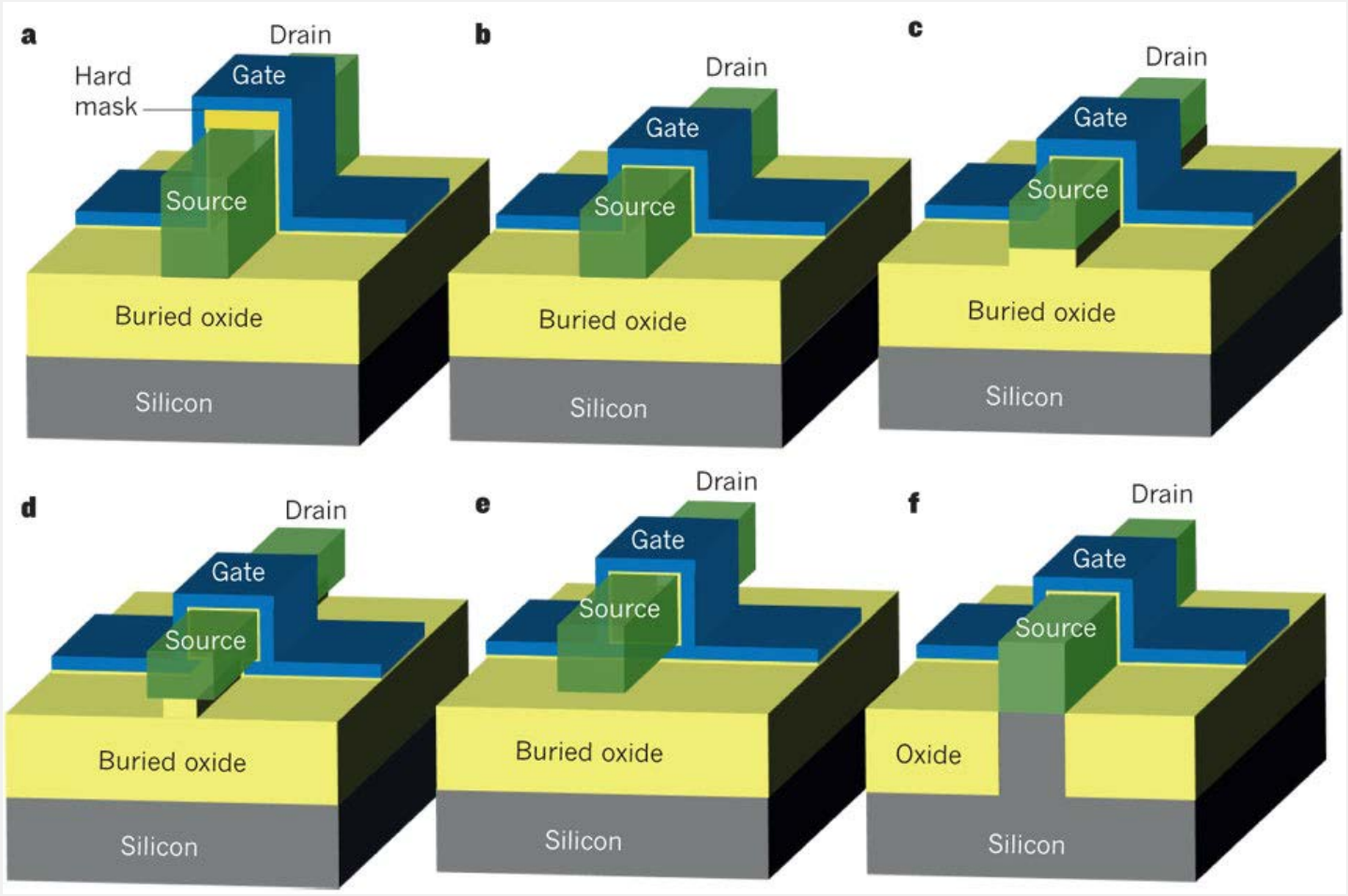
Strategies for device scaling

- multiple gate field effect transistor(MuGFET)
- channel strain engineering
- silicon-on-insulator-based technologies
- high-*k*/metal gate materials

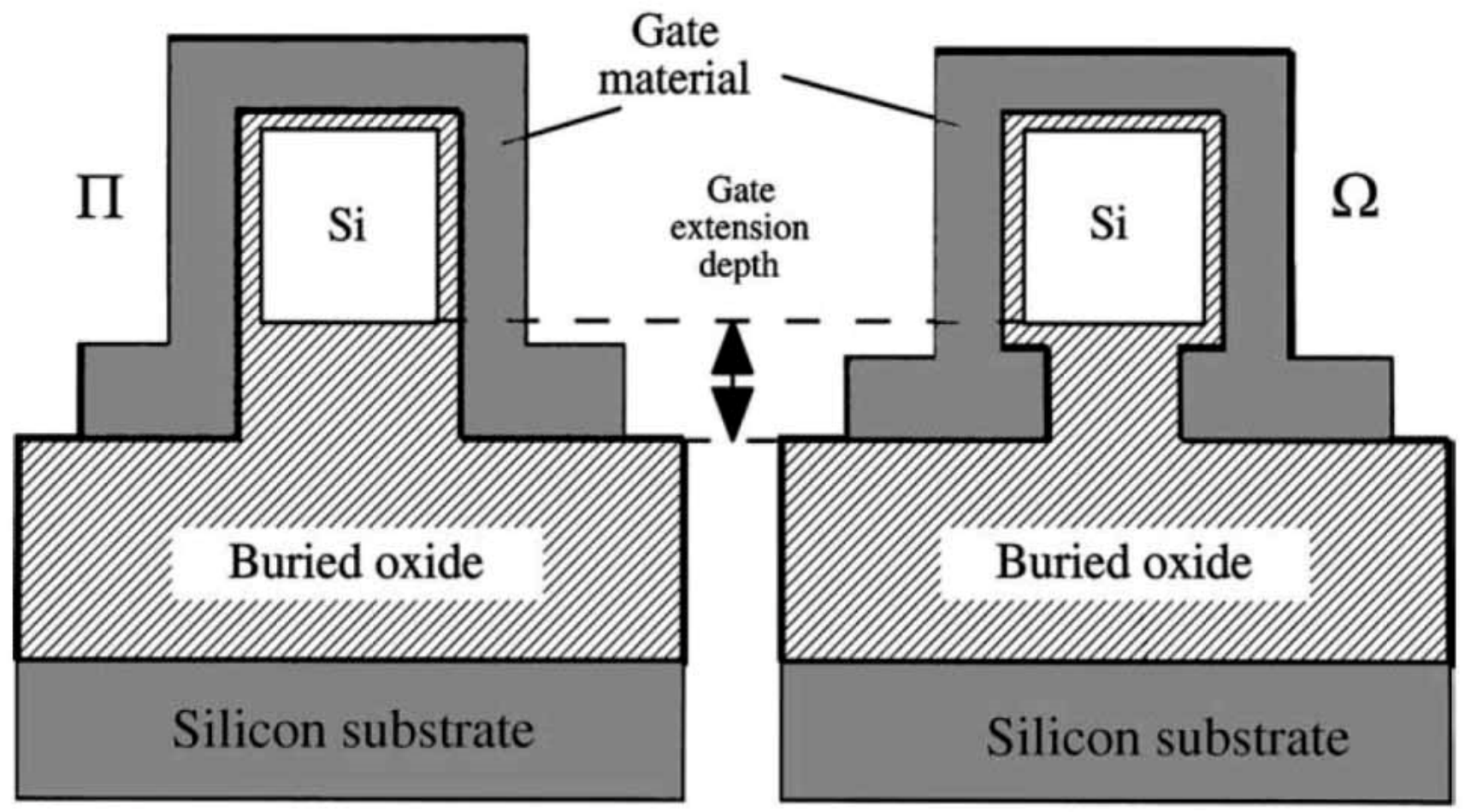
Intel transistor gate length trend



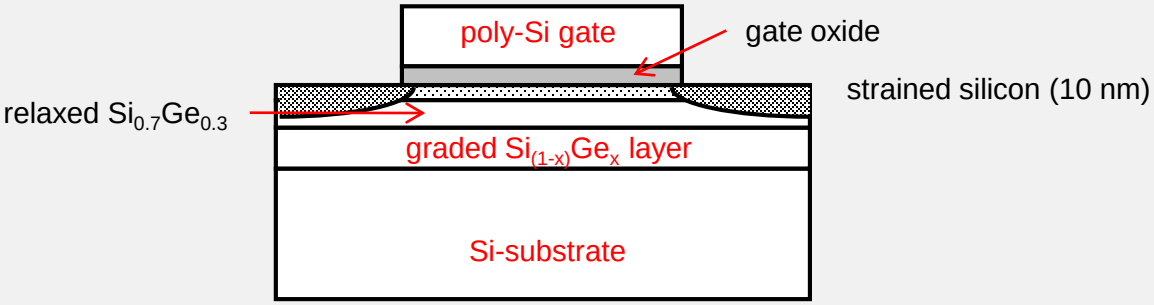
Types of multigate MOSFET



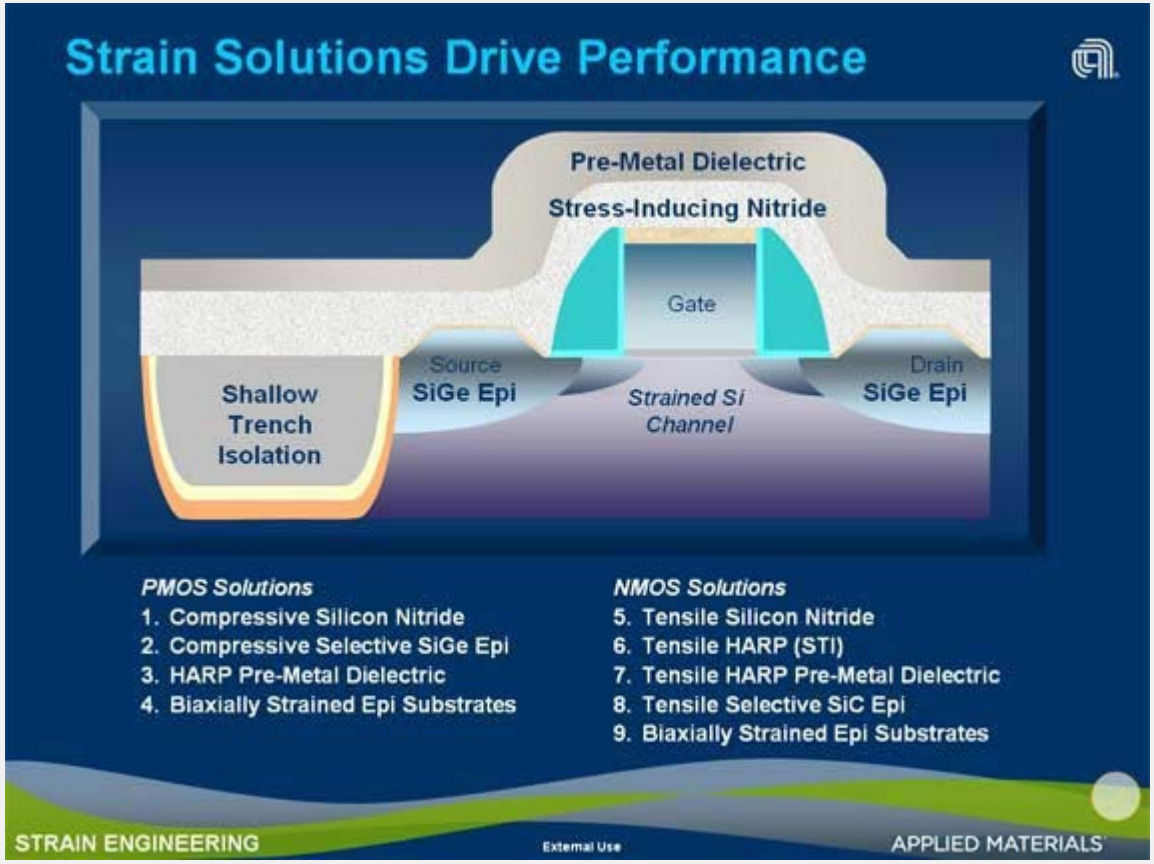
Pi- and Omega-gate FinFETs



Strained Si n-MOSFET



Strained Si CMOS



HARP – high aspect ratio process