Aalto University
School of Electrical
Engineering

Flying capacitor multi-level converters

ELEC-L3520 Postgraduate Course in Electronic Circuit Design II V

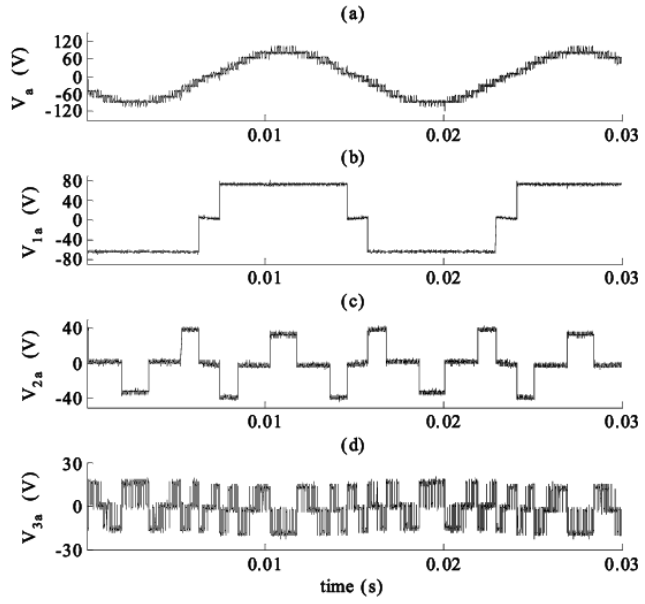
Ilia Kempi

Department of Electronics and Nanoengineering
Aalto University, School of Electrical Engineering

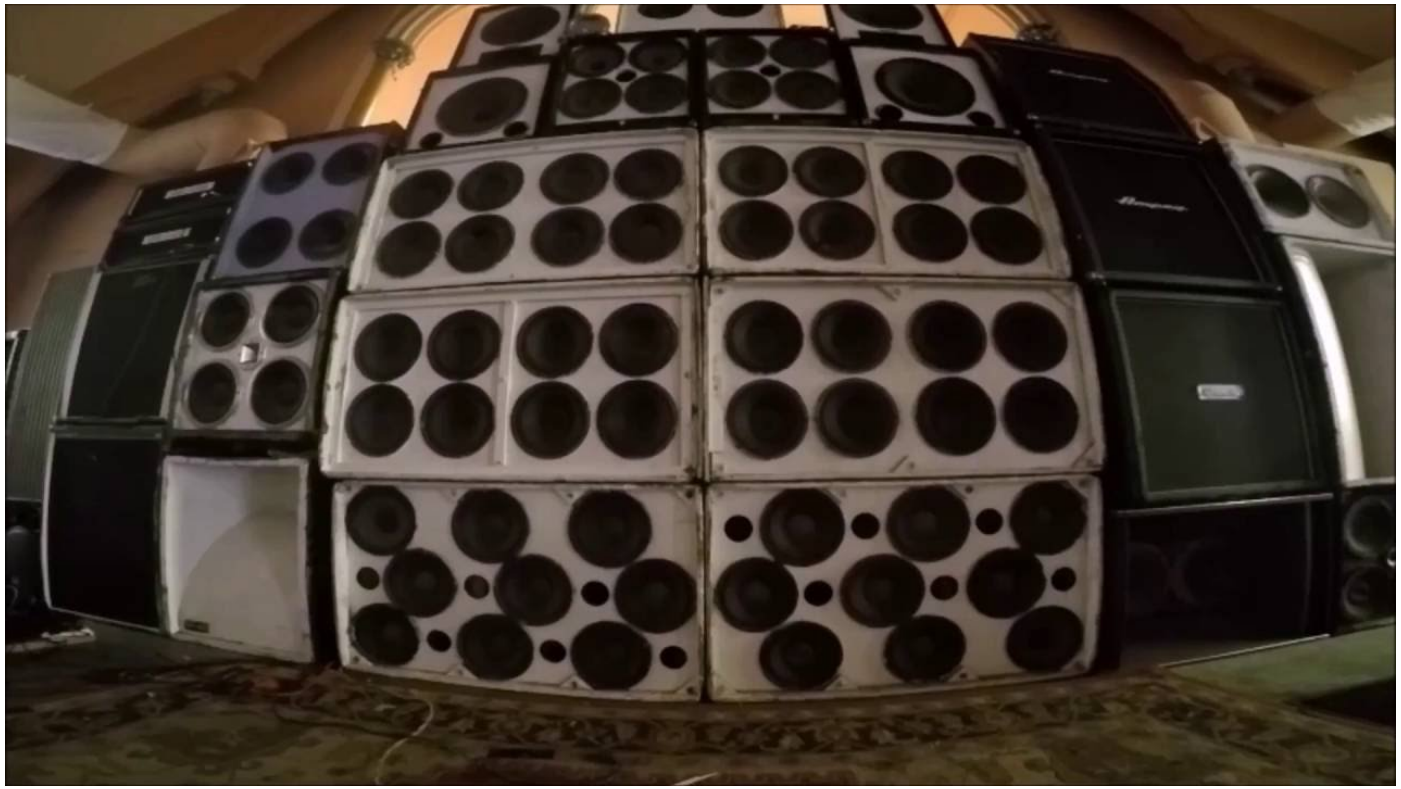
22.5.2019

Flying capacitor multi-level (FCML) converter

- A device to produce waveforms
- Can be seen as a form of DAC
- .. or a complex PWM
- Also used for supply regulation



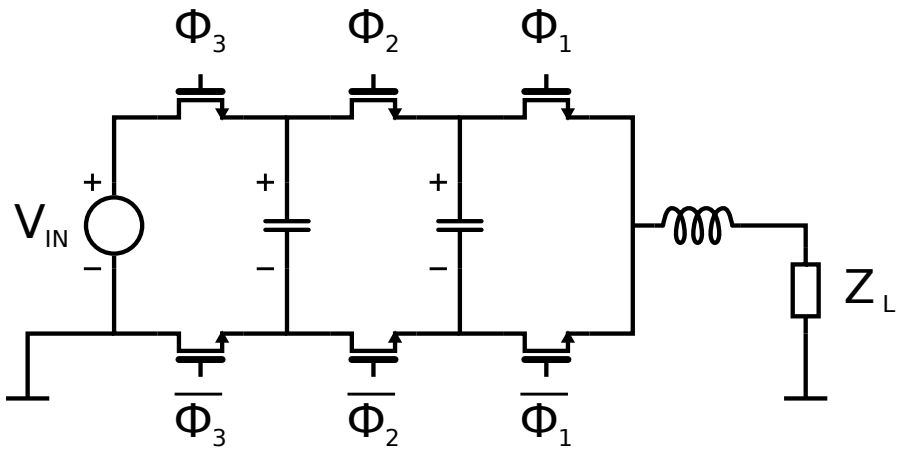
An application

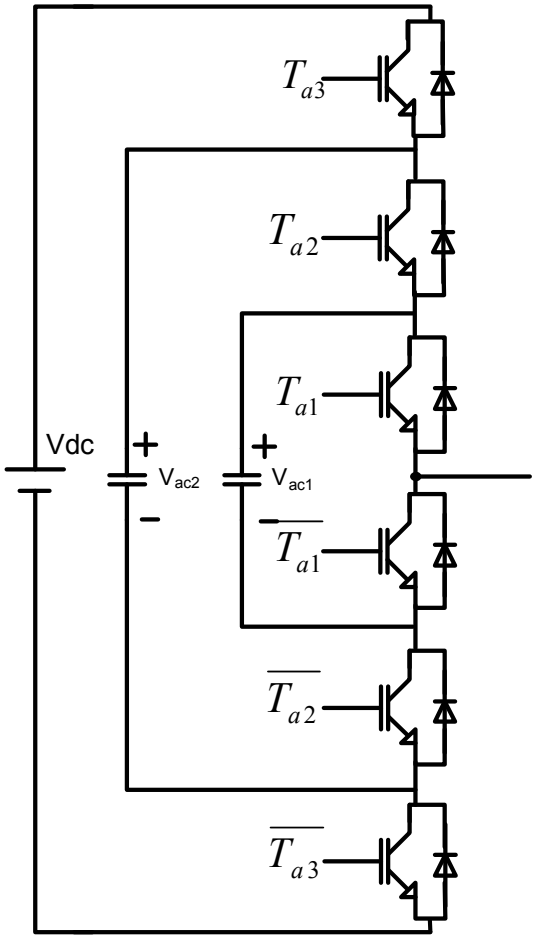


Outline

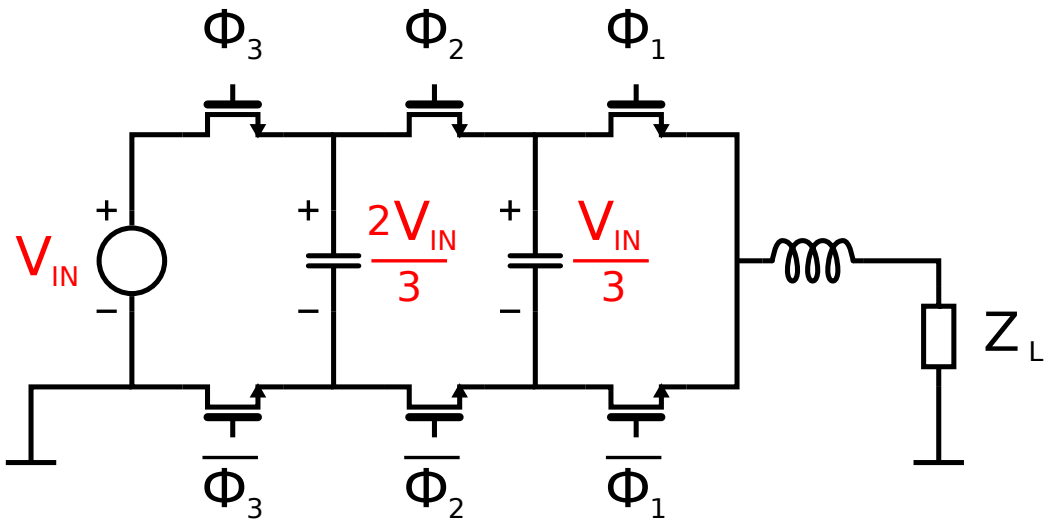
Topology

Both structures are equivalent





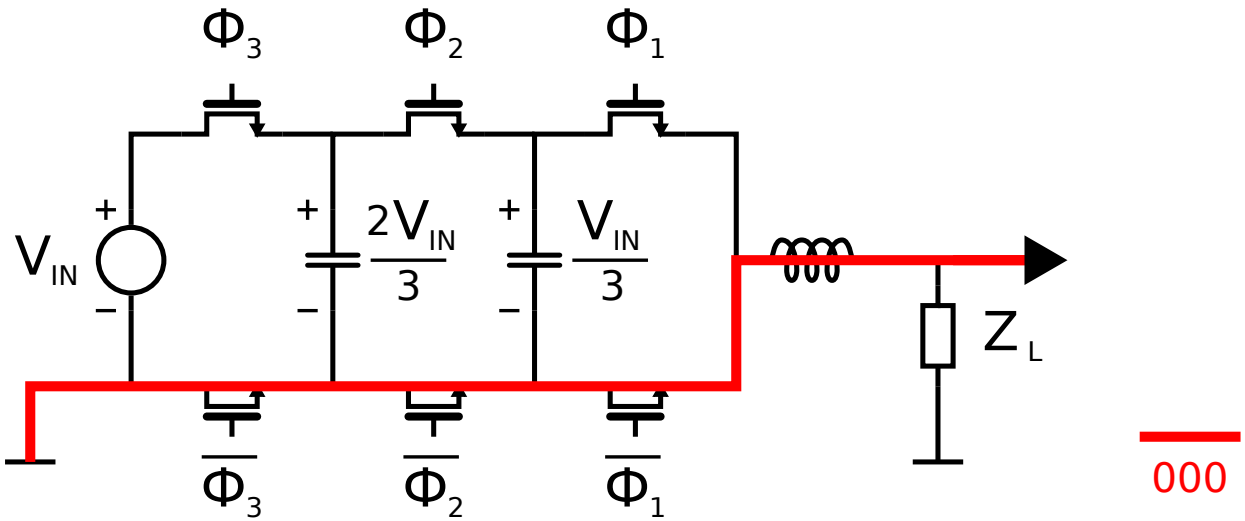
Voltage levels



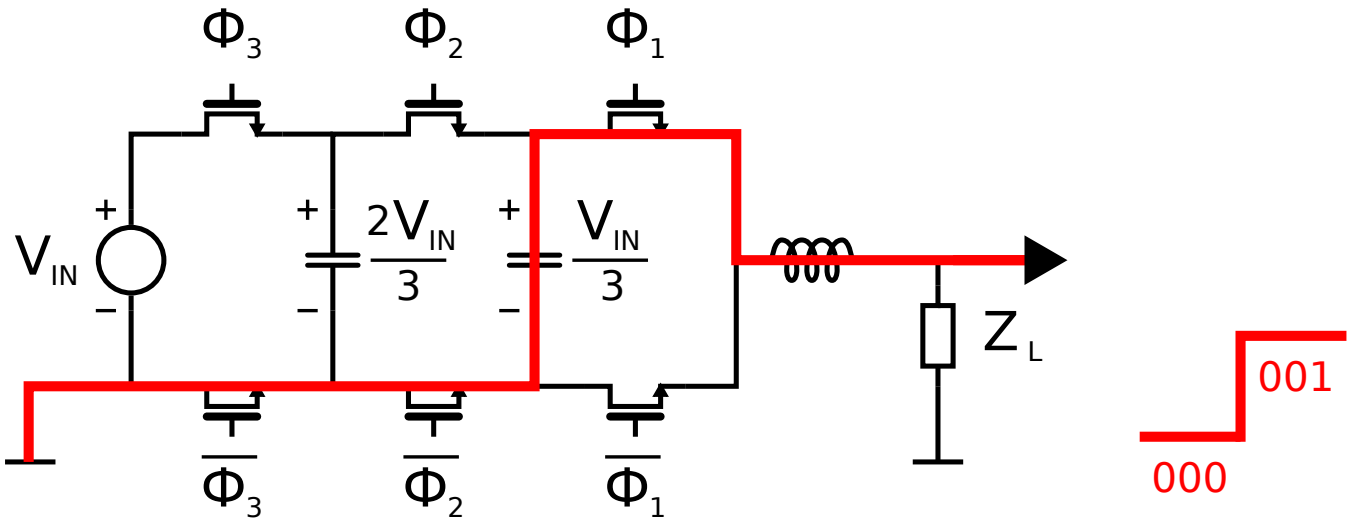
FCML operating conditions

- V_{IN} is divided to N levels (N = stages)
- Each flying capacitor stores fractional voltage level

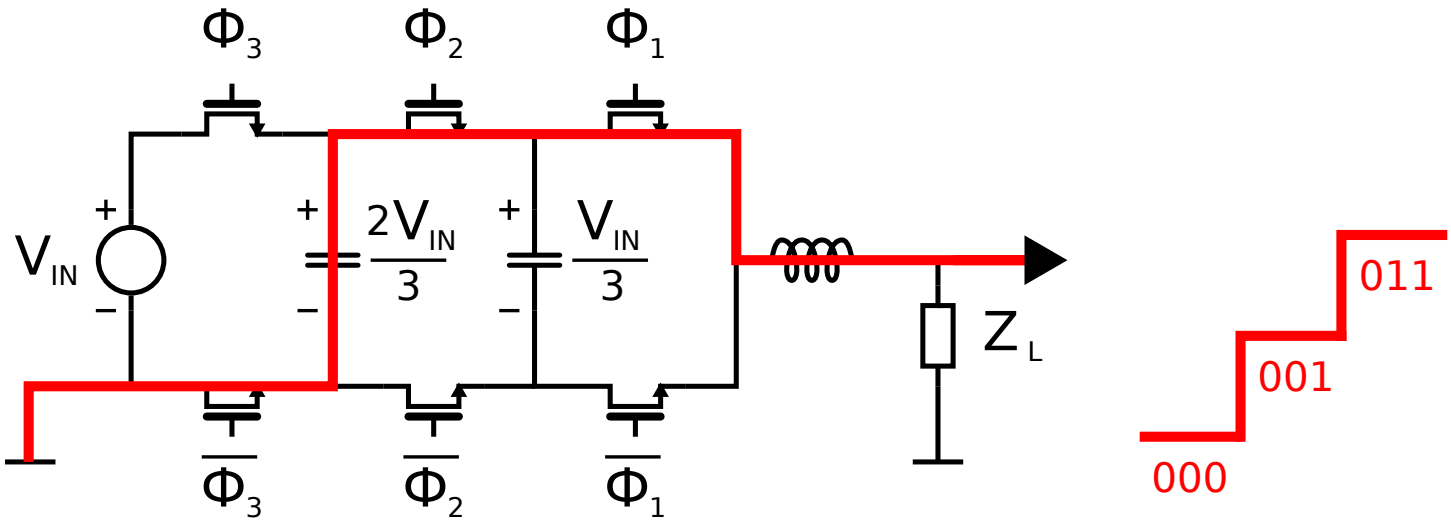
Waveform generation 1



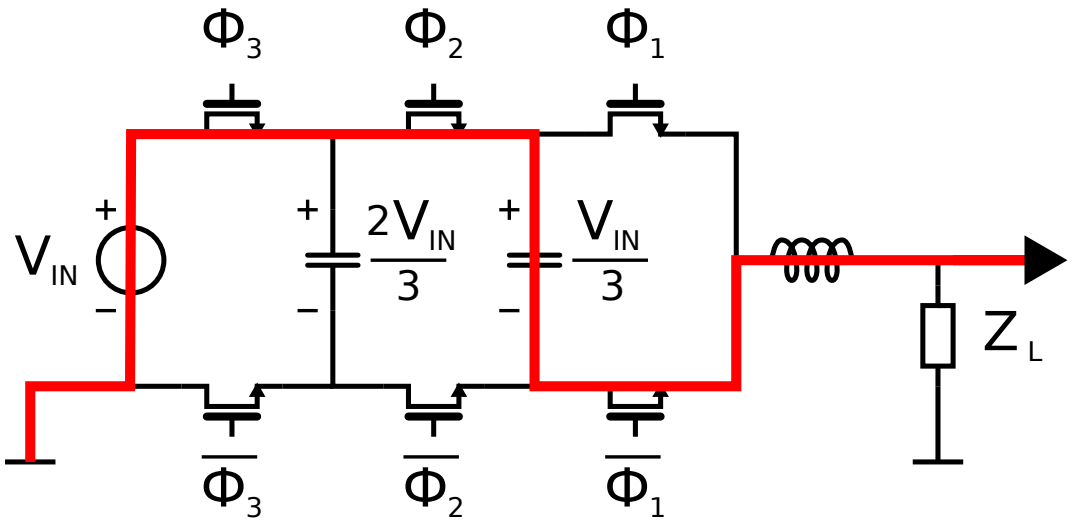
Waveform generation 2

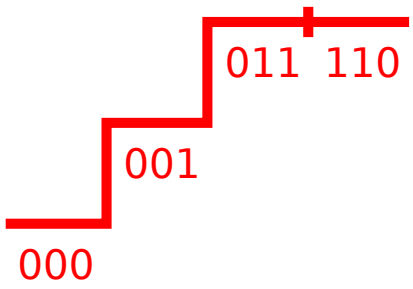


Waveform generation 3

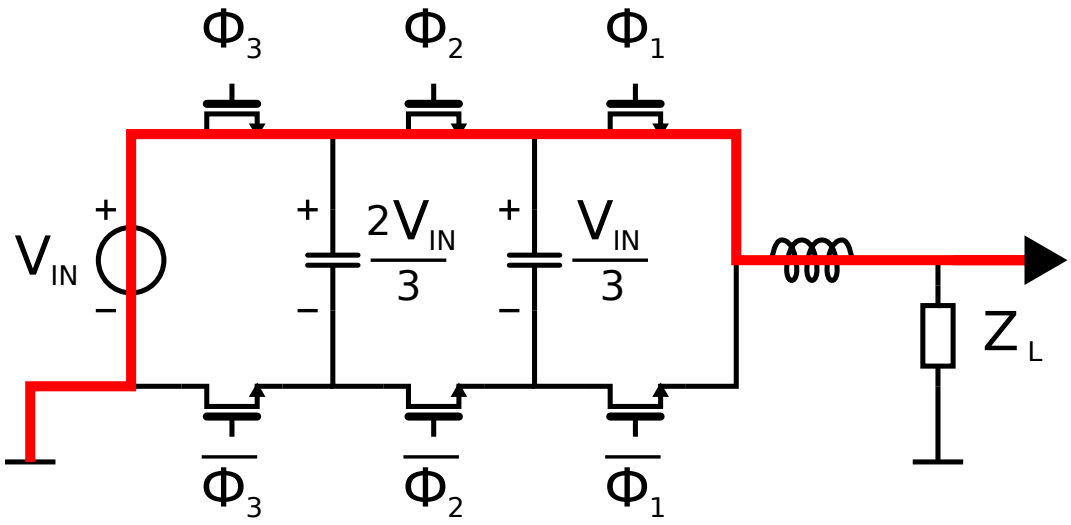


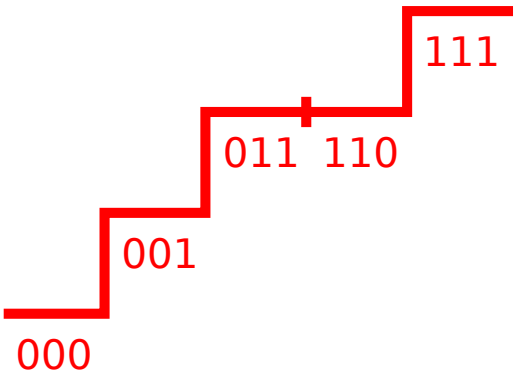
Waveform generation 4



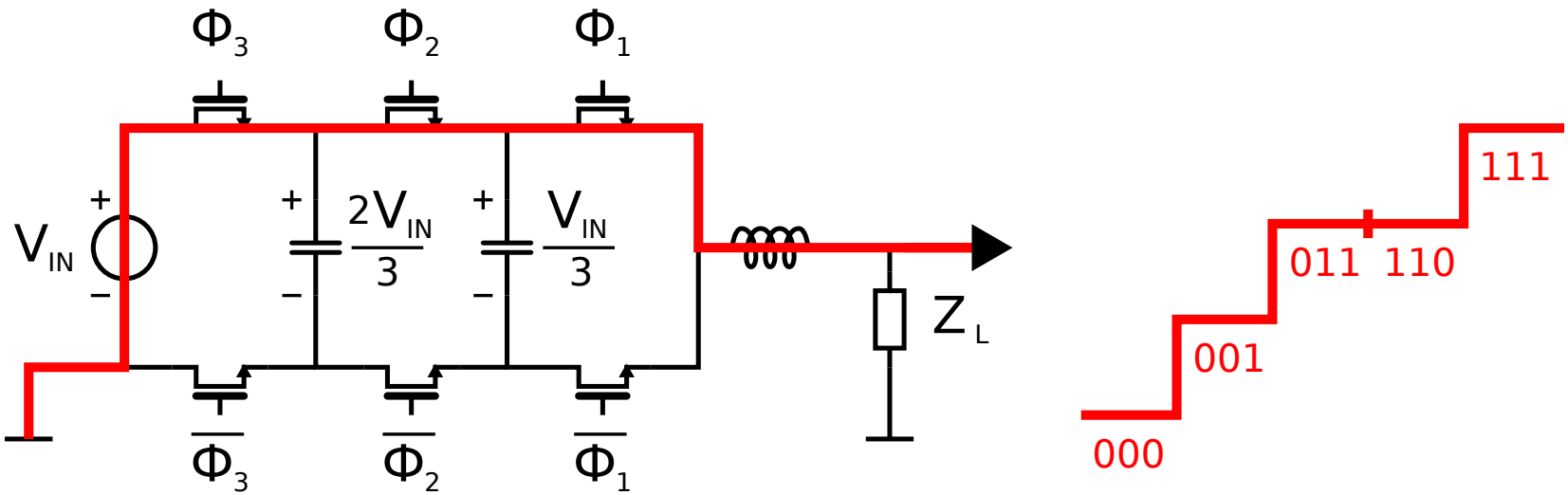


Waveform generation 5





Waveform generation 5 – observations

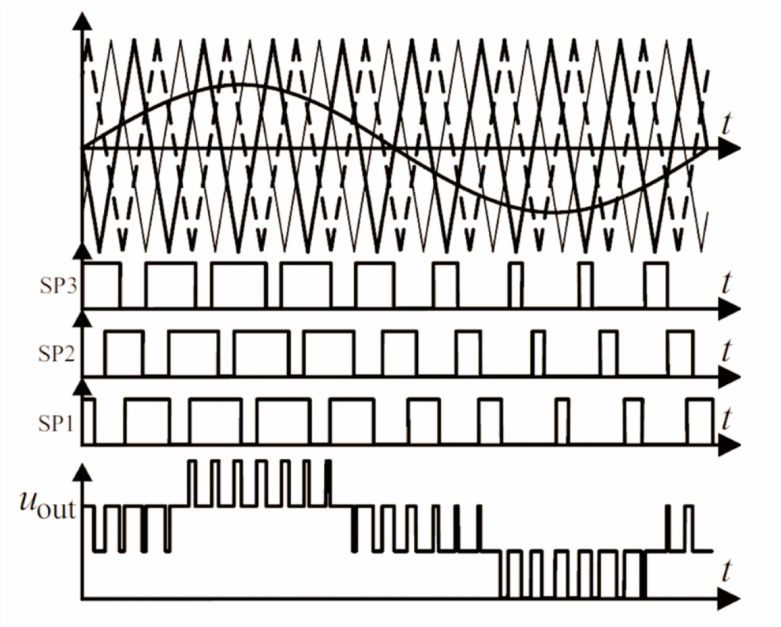


- Multiple ways to generate same output level
- Each switch has to handle maximum of V_{IN}/N
- Nice output range!

Outline

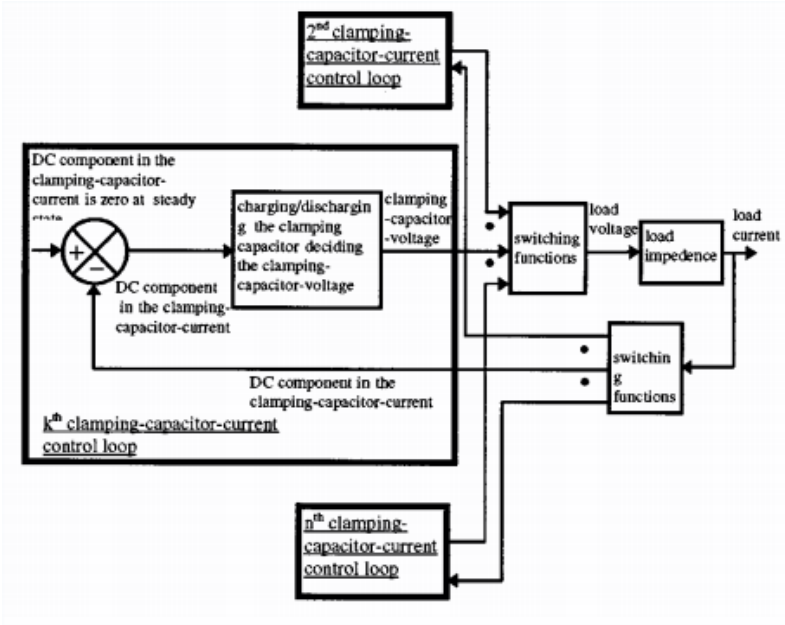
Sub-harmonic PWM modulation

- Switches are driven by PWM signal
- Control of each stage is offset by $360/N$ degrees
- Connections for same output level are alternated
- Maintains the voltage of flying capacitors



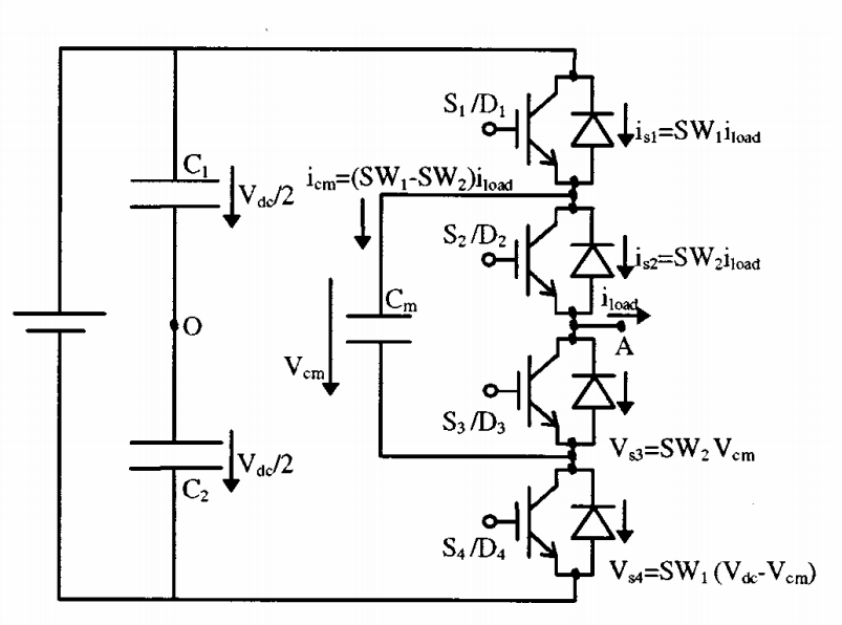
Spontaneous control loop

- Sub-harmonic PWM creates “spontaneous current control loop” in the flying capacitor
- Individual control loops are inter-connected
- Yuang et al.[1] have shown that loops hold as long as the load is not purely reactive

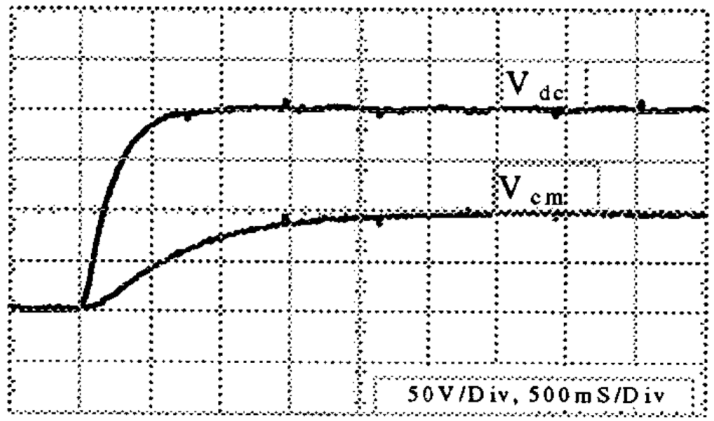


[1] Xiaoming Yuang et al., *“Self-balancing of the clamping-capacitor-voltages in the multilevel capacitor-clamping-inverter under sub-harmonic PWM modulation”*, IEEE Transactions on Power Electronics (Volume: 16 , Issue: 2 , Mar 2001)

Capacitor voltage settling



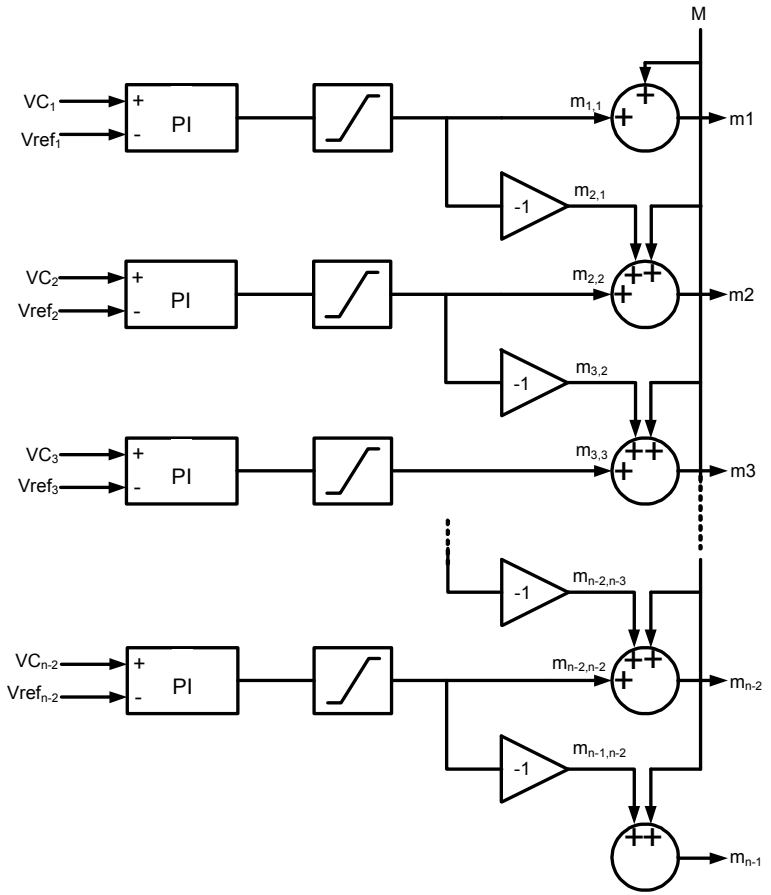
Two stage FCML converter



Settling of flying capacitor voltage

Active capacitor balancing

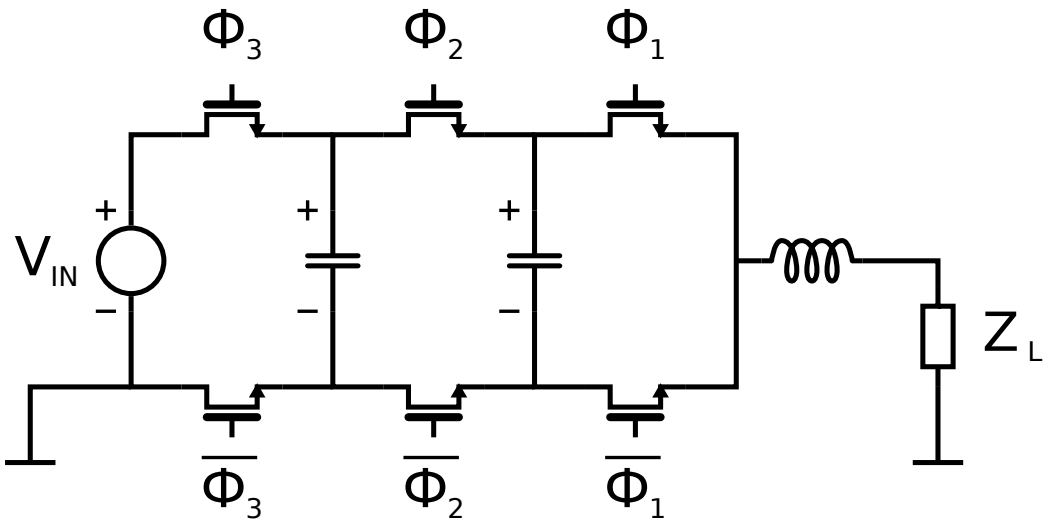
- Required under heavy load conditions to compensate voltage drift in flying capacitors
- Khazarei et al.[2] reported incorporating chained PI controllers into switch drivers (right figure)
- Controllers manipulate switching instances, thus distorting the original input signal (= trade-off)

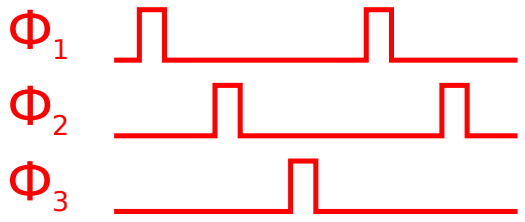


[2] Mostafa Khazarei et al., *"A generalized capacitor voltage balancing scheme for flying capacitor multilevel converters"*, 2010 Twenty-Fifth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)

Outline

Multilevel buck converter scenario

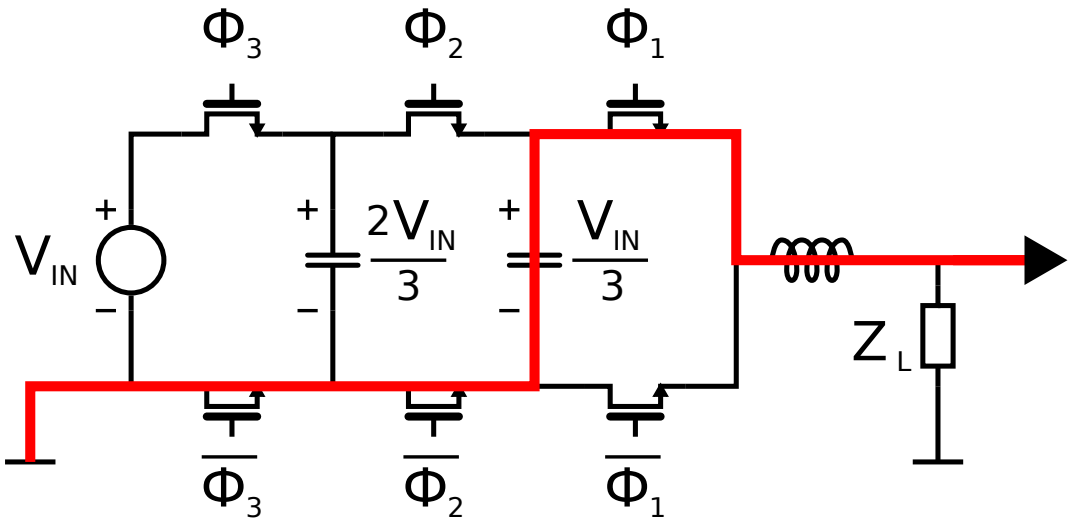


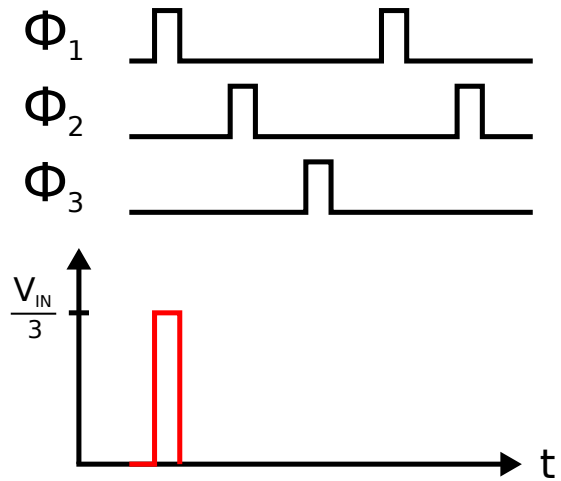


Operating conditions

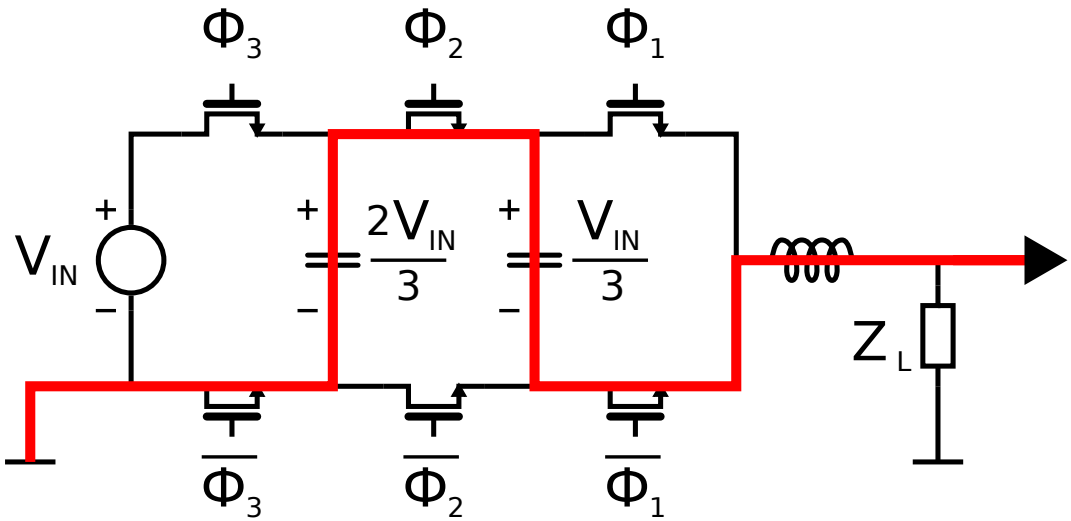
1. Define $V_{OUT} = 0.111\,V_{IN}$
2. Modulate a constant 0.111 level with subharmonic PWM

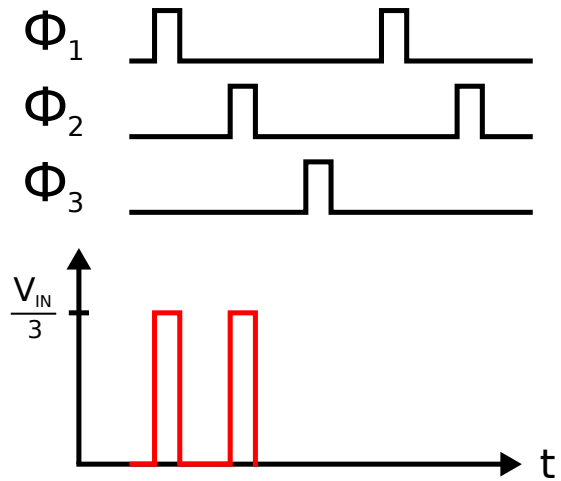
Buck regulation 1



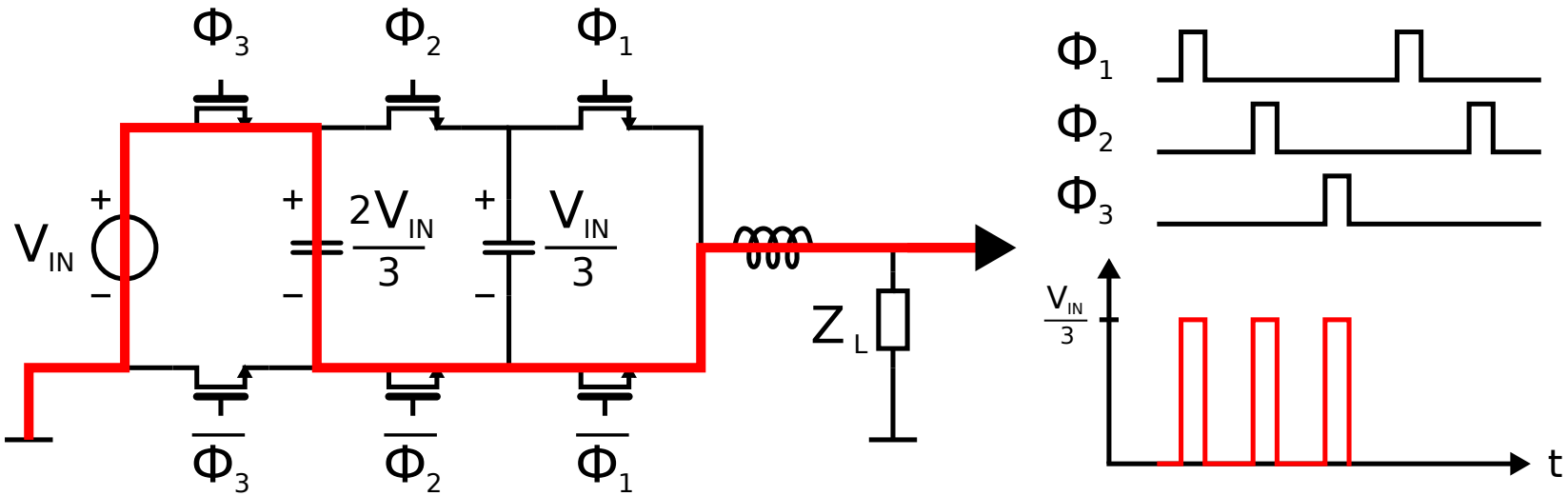


Buck regulation 2

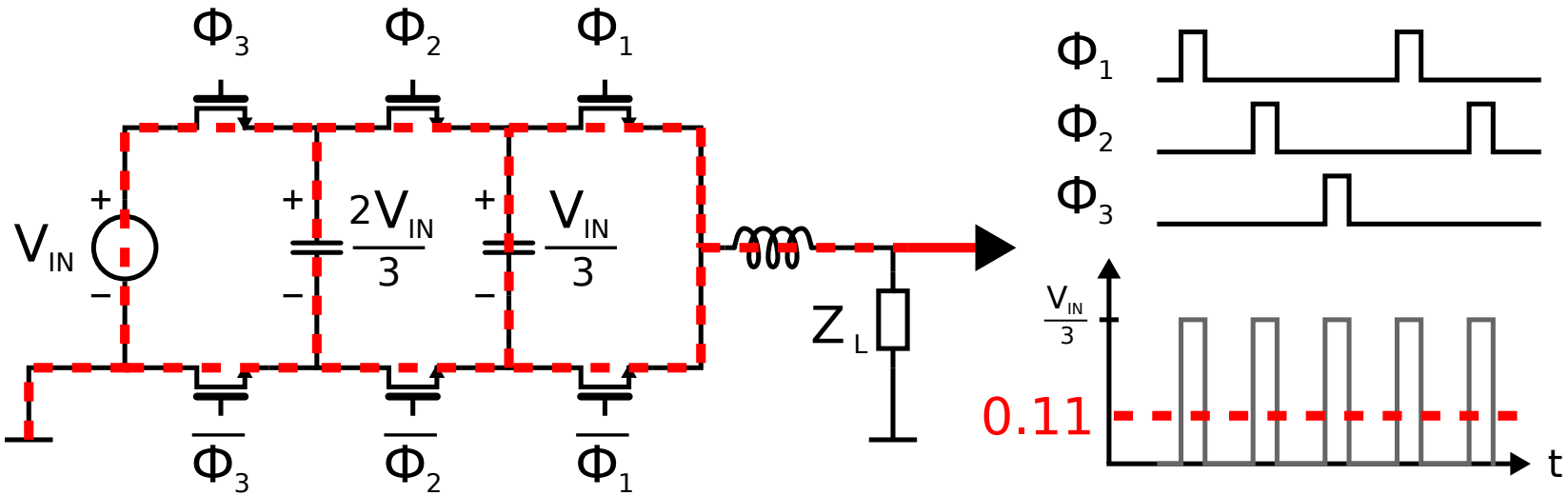




Buck regulation 3



Buck regulation – superposition



- Each flying capacitor is cycled through charge and discharge

Feasibility of FCML for converter applications

Pros

- Great output range
- Good switch rating (V_{IN}/N)
- Reduced ripple (due to multi-level)

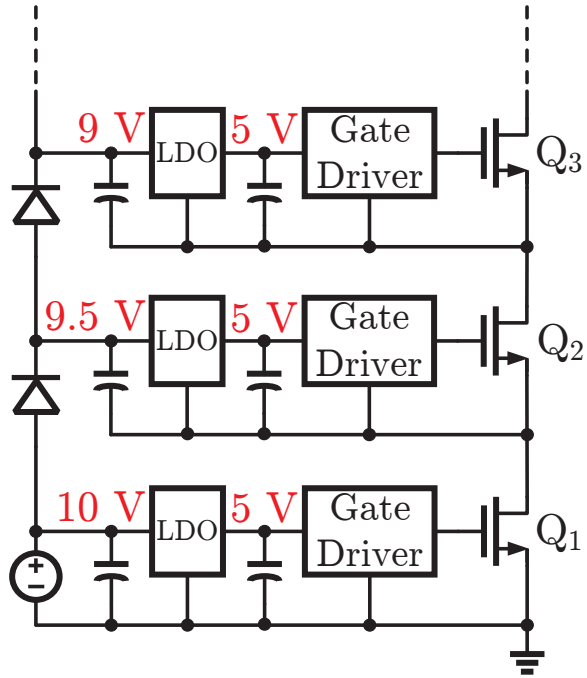
Cons

- Capacitor voltage balancing
- Startup and shutdown (switch dV/dt ?)
- Complex PWM control

Outline

Cascaded bootstrap gate driver

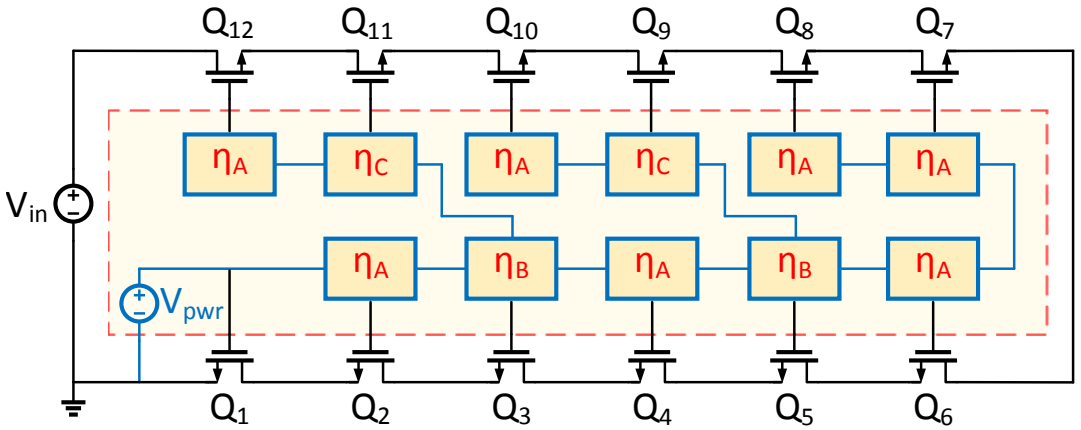
- Conventional half-bridge gate drivers can induce timing mismatch due to *bootstrap diode voltage drop in the high-side driver*
- **Affects voltage balance**
- Ye et al.[3] propose utilizing cascaded bootstrap drivers to eliminate timing mismatch
- Cascaded bootstrap ensures equal supply for all switches



[3] Zichao Ye et al., *"Investigation of capacitor voltage balancing in practical implementations of flying capacitor multilevel converters"*, 2017 IEEE 18th Workshop on Control and Modeling for Power Electronics (COMPEL)

Cascaded bootstrap gate driver

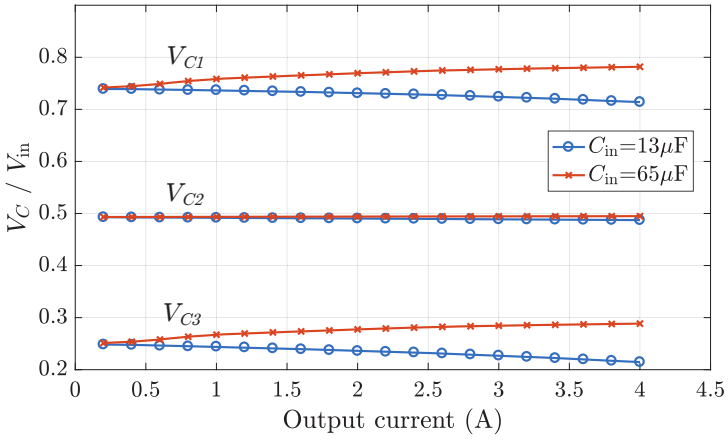
Additional gate driving techniques are proposed for GaN FCML converters with larger number of stages, ensuring reliable switching even in startup and light-load conditions.[4]



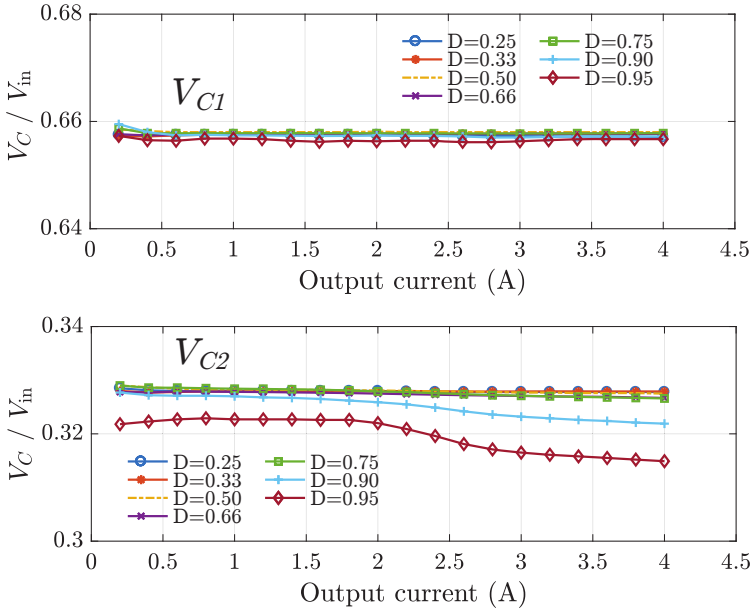
η_A: Bootstrap
η_B: Double charge pump
η_C: Gate-driven charge pump

[4] Zichao Ye et al., *" Design and implementation of a low-cost and compact floating gate drive power circuit for GaN-based flying capacitor multi-level converters "*, 2017 IEEE Applied Power Electronics Conference and Exposition (APEC)

Effect of source impedance



Capacitor voltages in 5-level FCML

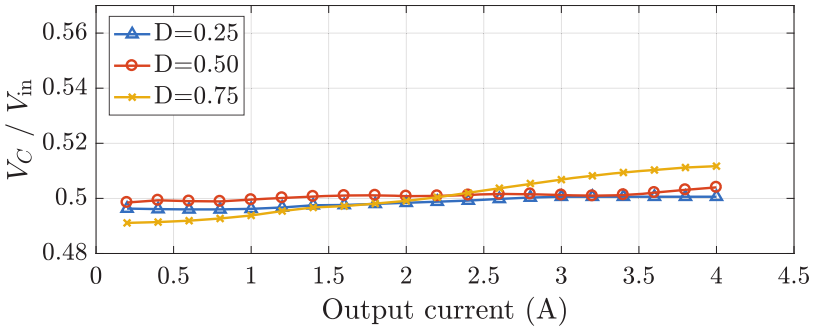


Capacitor voltages in 4-level FCML

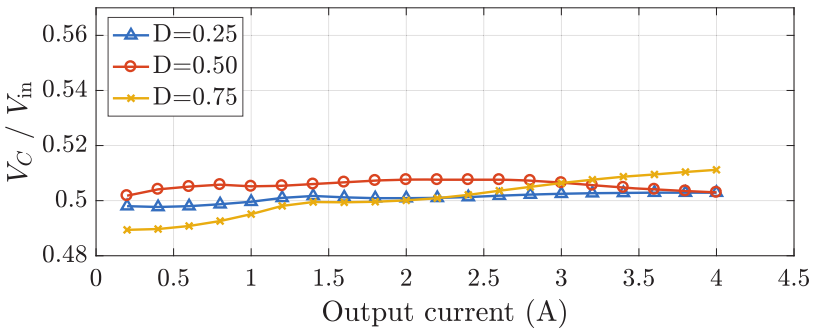
- Analytical model developed by Ye et al.
- FCML converter with an **even number of levels** is more resilient to effects of Z_{input}

Effect of on-resistance mismatch

- Ye et al. have reported experimental results on 3-level FCML converter with purposeful switch mismatch ($7m\Omega$ and $16m\Omega$)
- **Minimal voltage drift with on-resistance mismatch**



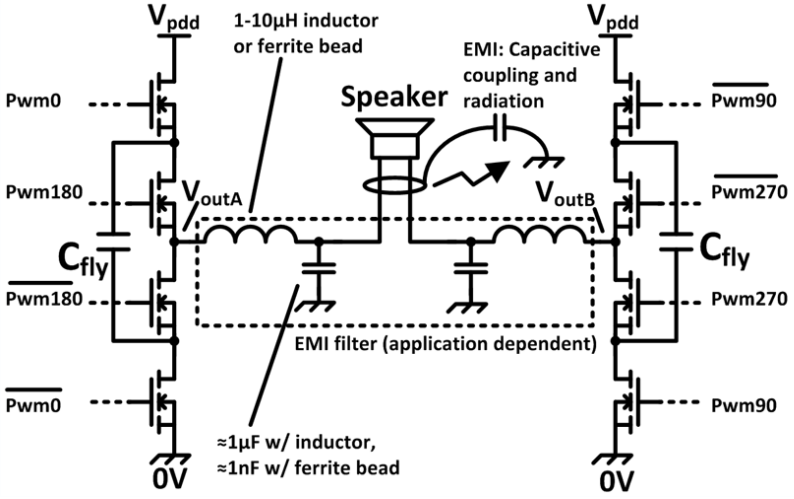
(a) no delay mismatch

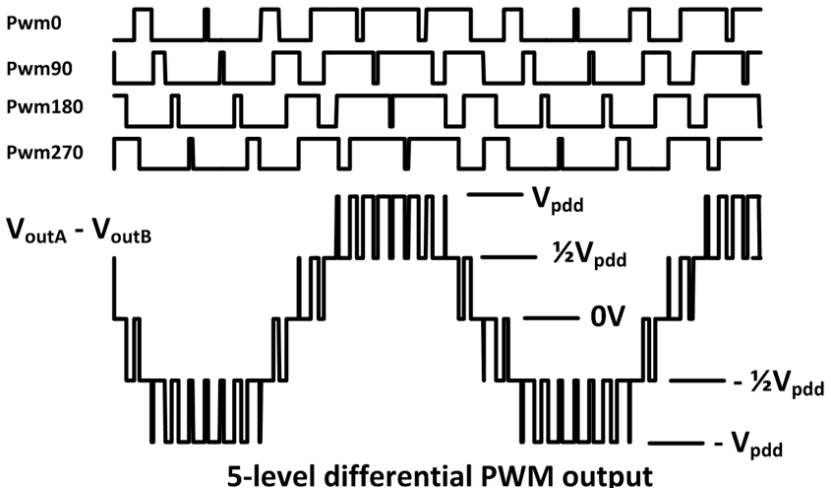


(b) no delay mismatch and different on-resistance

Outline

Example: Class D amplifier

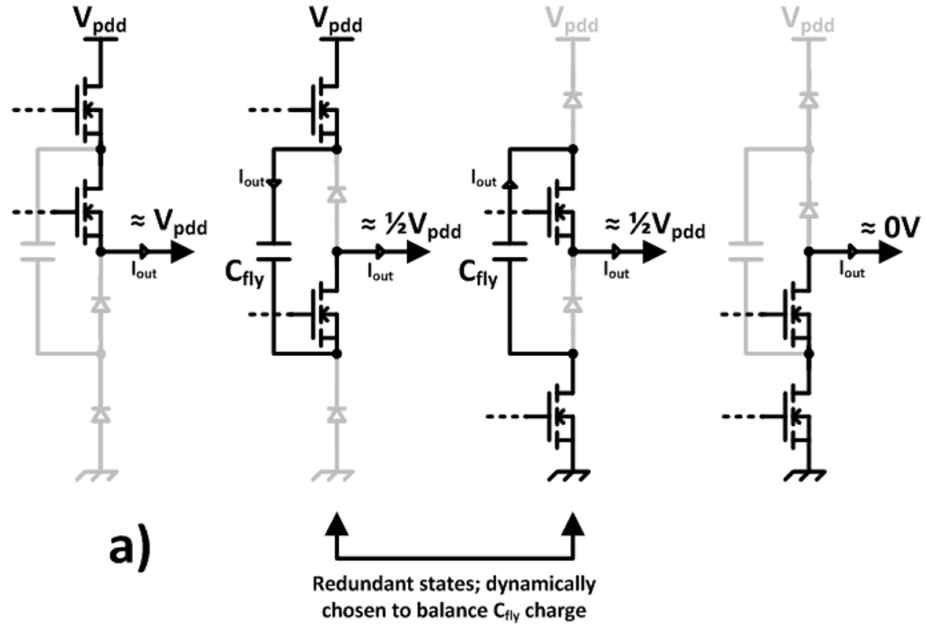




NorCAS 2018 Keynote speaker

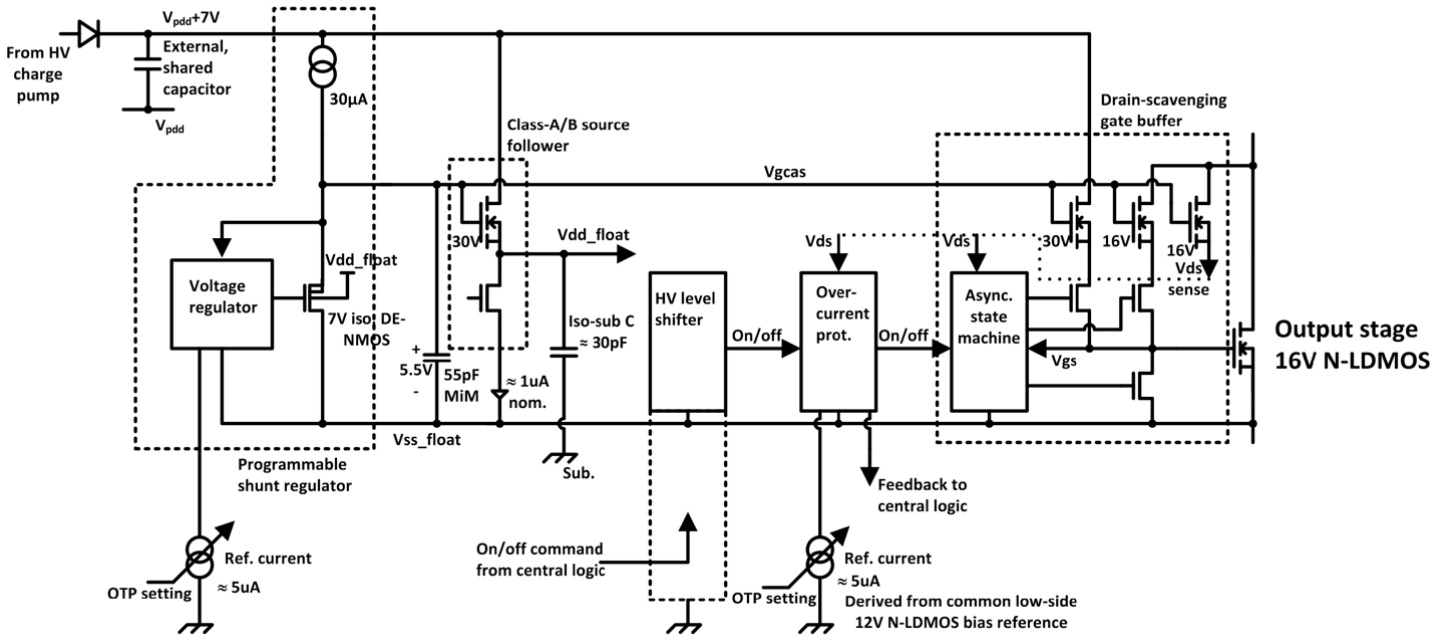
A 2x70 W Monolithic Five-Level Class-D Audio Power Amplifier in 180 nm BCD by Høyerby et al. (**Merus Audio**)

Example: Class D amplifier



- Redundant state selection (RSS) technique
- **Improves voltage balancing** without distortion
- Digitally-assisted state scrambling
- Here, 4-th order loop filter is used prior driving stage to eliminate resampling noise of analog PWM

Example: Class D amplifier

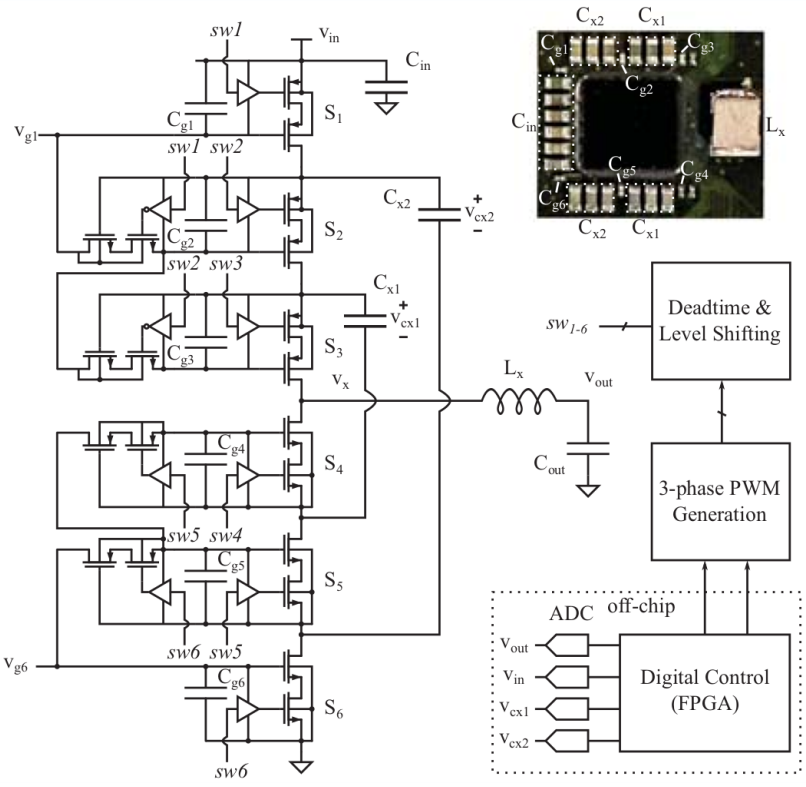


- Floating gate driver with dedicated supply regulator
- High-voltage charge pump for drive voltage generation
- Drain-scavenging gate buffer

Example: Class D amplifier

Parameter	This work, effcy. opt.	This work, perf. opt.	[20]	[8]	[5]	[13]
Half bridge topology	3-level FC		2-level	2-level	2-level	2-level
Modulation	5-level		2-level	2-level	2-level	3-level (ternary)
Power stage supply V_{pdd}	24V		80V	50V	60V	24V
Max. output power per channel	70W		45W	240W	100W	50W @21V
V_{pdd} idle cons. per channel	70mW (w. output filter)	110mW (w. output filter)	360mW (w. output filter)	2100mW (w. output filter)	1600mW (w. output filter)	380mW (w/o output filter)
Max/idle power ratio	1kW/W	630W/W	125W/W	115W/W	63.5W/W	132W/W
Efficiency at max. output power	90%	88%	91%	?	>90%	88%
THD+N	0.03% @10W, 1kHz	0.003% @10W, 1kHz	0.015% @ 9VA, 100Hz	0.04% @ 10W	0.03% @ 10W, 1kHz	0.04% @ 10W
Dynamic range	108dB	110dB	?	110dB	103dB	102dB
Feedback topology	Analog		Analog	None	Analog	Analog
Max. total output power	140W		45W	240W	200W	100W
Die size	13.4mm^2		8.5mm^2	?	22mm^2	7.04mm^2 (from X-ray)
Power/area ratio	10.4W/mm^2		5.3W/mm^2	?	9.1W/mm^2	14.2W/mm^2
Process	180nm BCD, dual-oxide		140nm SOI BCD	400nm BCD	?nm SOI BCD	?

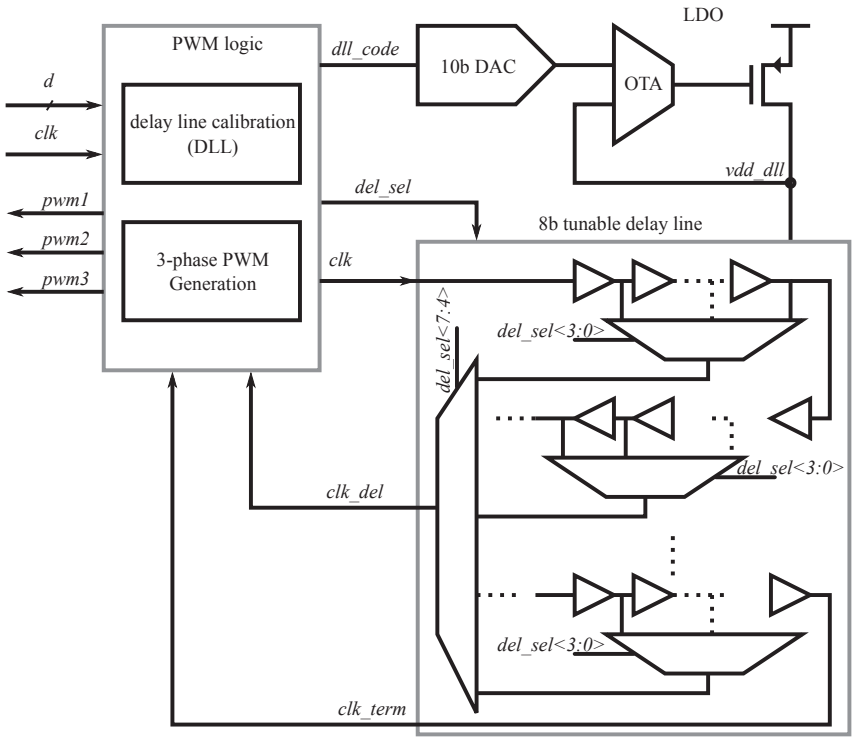
Example: FCML converter



ISSCC 2019 DC-DC converters session

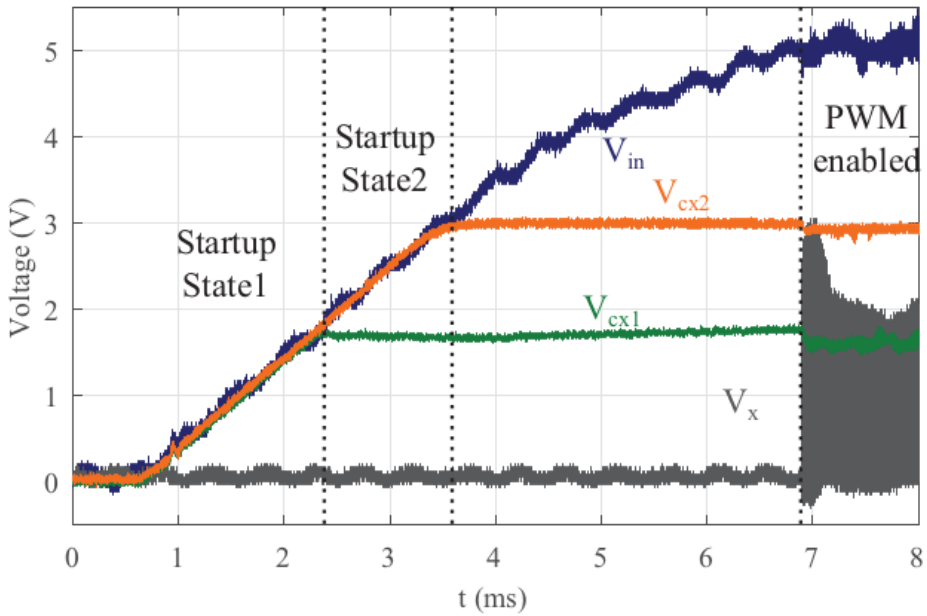
A 93.8% Peak Efficiency, 5V-Input, 10A Max ILOAD Flying Capacitor Multilevel Converter in 22nm CMOS Featuring Wide Output Voltage Range and Flying Capacitor Precharging by Christofer Chaef et al. (**Intel**)

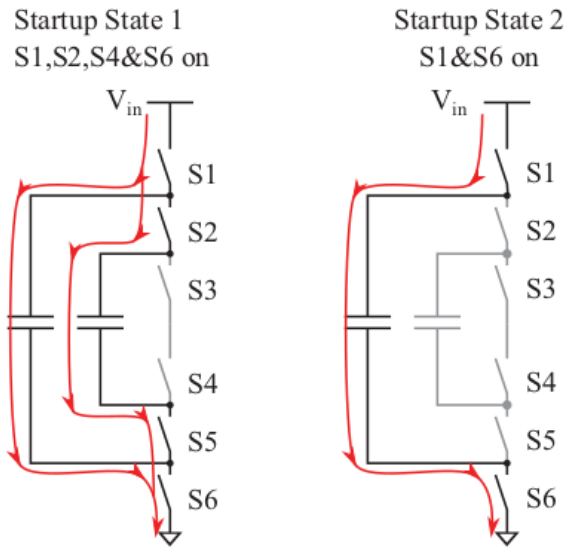
Example: FCML converter



- Delay-locked loop (DLL) for PWM generation
- LDO is calibrated to match delay line to the reference clock
- Sub-harmonic PWM is produced from a shared delay line

Example: FCML converter





Startup pre-charge sequence

Example: FCML converter

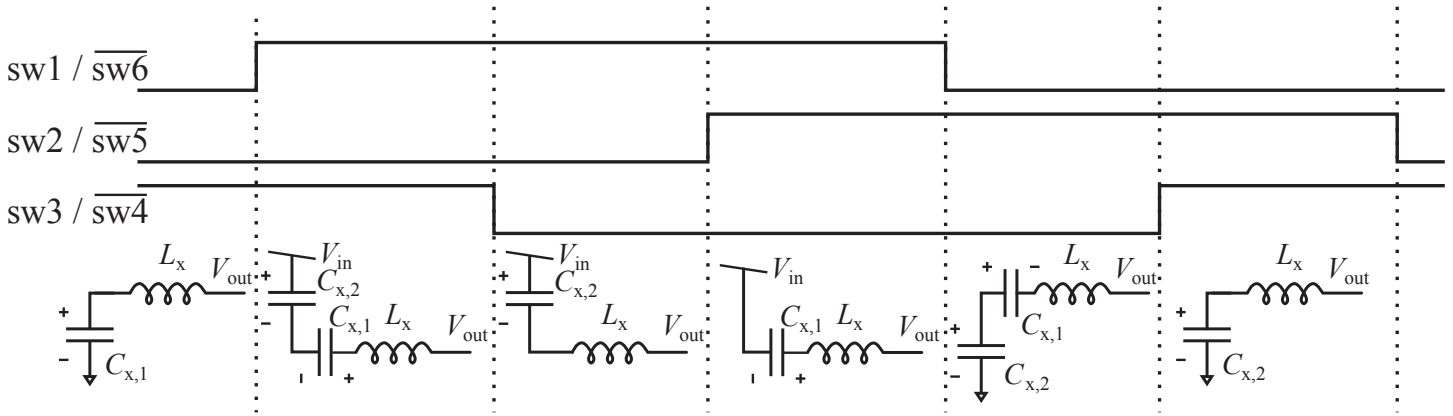
	This Work	[1]	[2]	[3]
Topology	4L FCML	4:1 Dickson	2:1 ReSC	3L FCML
Input Voltage	5 V	4.2 V	7.2 V	5 V
Output Voltage	1.8 V	1 V	3.6 V	1.5 V
Startup Precharge	Yes	No	No	No
Balancing	Yes	Yes	No	Yes
Multiple Ratios	Yes	No	No	Yes
Peak Output Current	10 A	1.05 A	1 A	0.8 A
Peak Efficiency @ I_{out}	93.8% @ 3 A	94.2% @ 0.18 A	94.8 % @ 0.3A	80%
Efficiency @ I_{max}	89.4 %	88.3 %	90.5%	78%
Inductance	10 nH	470 nH	100 nH	220 nH
Flying capacitance	2 x 13.2 µF	3 x 22 µF	2x 0.47µF	1µF
Output Decoupling	18 µF	22 µF	2 x 1 µF	2.4 µF
Sw. Frequency	5 MHz	500 kHz	1 MHz	4.4-11.8 MHz
Die Area current density	1.45 A/mm2	0.26 A/mm2	0.17 A/mm2	0.4 A/mm2
Vol. power density*	198 W/cm3	85 W/cm3	19 W/cm3	-
Total z-height	1.2 mm	3 mm**	2 mm	-

Outline

Conclusion

- Versatile topology by cost of increased complexity
- Bombastic solution for systems with dynamic supply scaling
- Inductor is indispensable
- Attractive for PA applications (e.g. speakers)

Homework (ISSCC 2019 paper)



- Find mistake on this figure
- Sketch the FCML and illustrate the mistake
- Explain your findings briefly
- Return by end of May (ilia.kempi@aalto.fi)