ELEC-E3510 Basics of IC Design

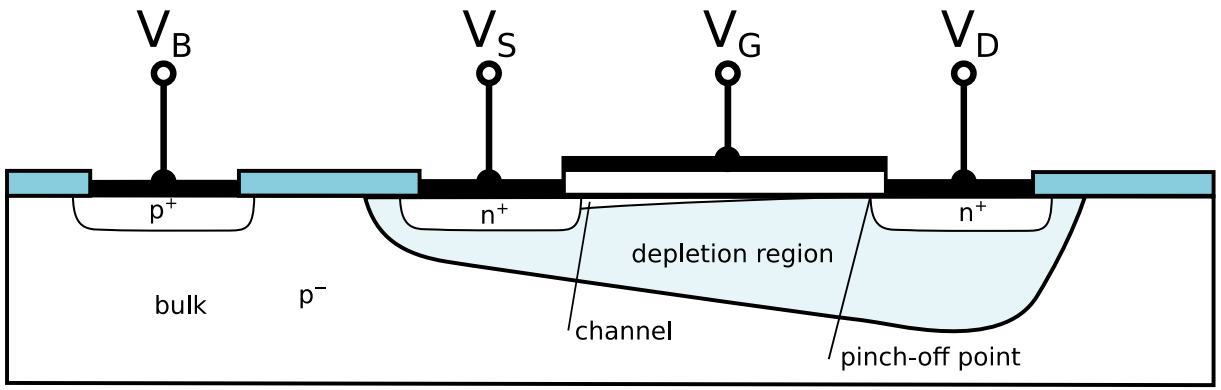
CMOS technology and layout

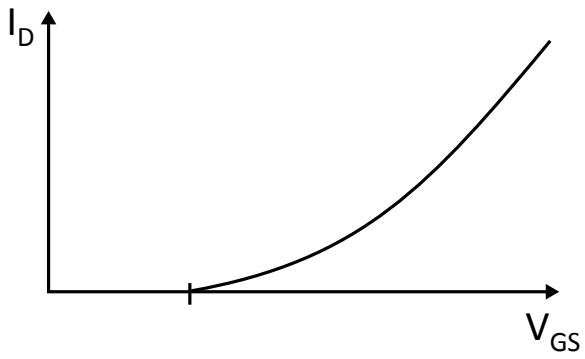
Lecture overview

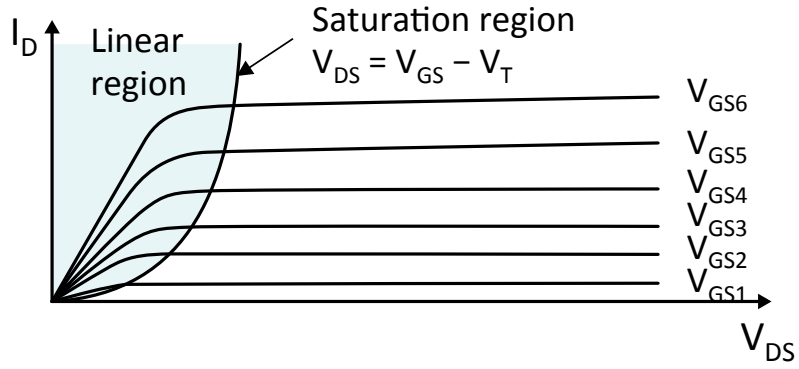
- Introduction to MOS transistor
- Introduction to CMOS technology
- Introduction to lay-out

Introduction to MOS transistor

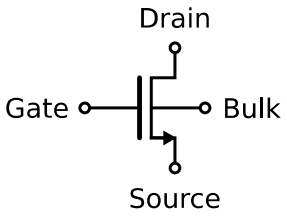
MOS transistor



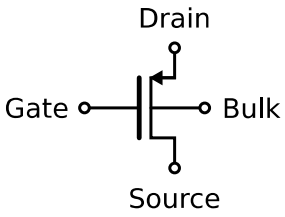




NMOS



PMOS

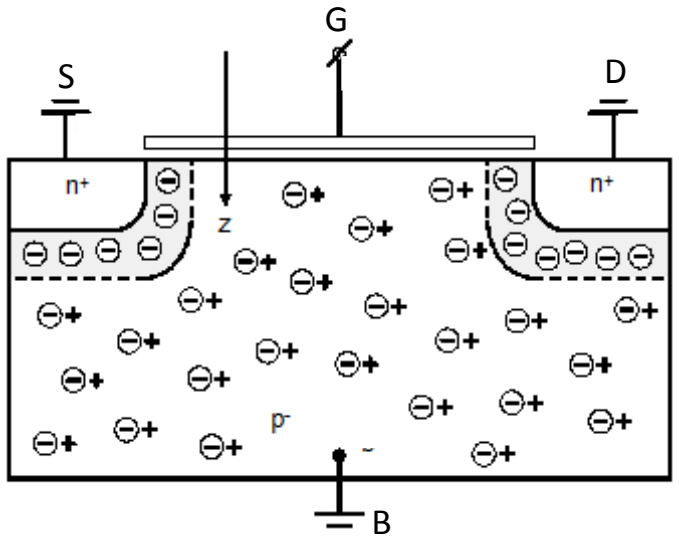


Modes of operation

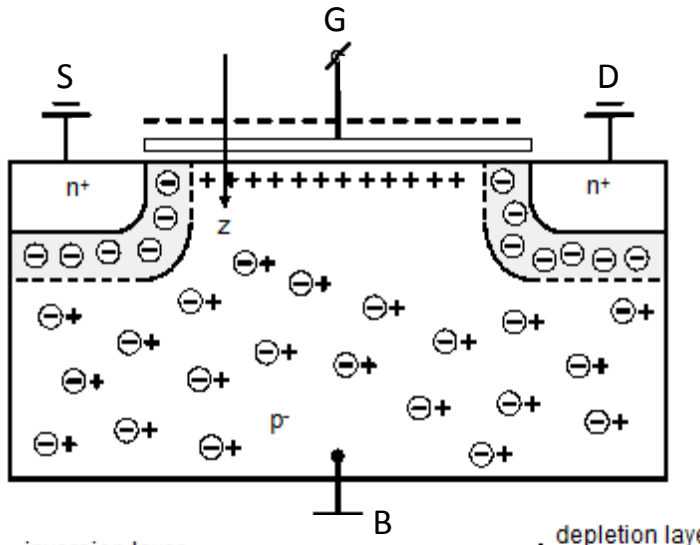
Cut-off	$V_{GS} - V_T \leq 0$	$I_{DS} = 0$
Linear region (Triode region)	$0 < V_{DS} \leq (V_{GS} - V_T)$	$I_D = \frac{\mu_0 C_{ox} W}{L}\left[(v_{GS} - V_T) - \frac{V_{DS}}{2}\right] V_{DS}(1 + \lambda V_{DS})$ $k = (K')\frac{W}{L} \cong (\mu_0 C_{ox})\frac{W}{L}$ (amps/volt^2)
Saturation	$0 < (V_{GS} - V_T) \leq V_{DS}$	$I_D = \frac{\mu_0 C_{ox} W}{2L}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$
Pinch-off	$V_{DS,SAT} = V_{GS} - V_T$	$I_{DS,LIN} = I_{DS,SAT}$

MOS transistor modes of operation

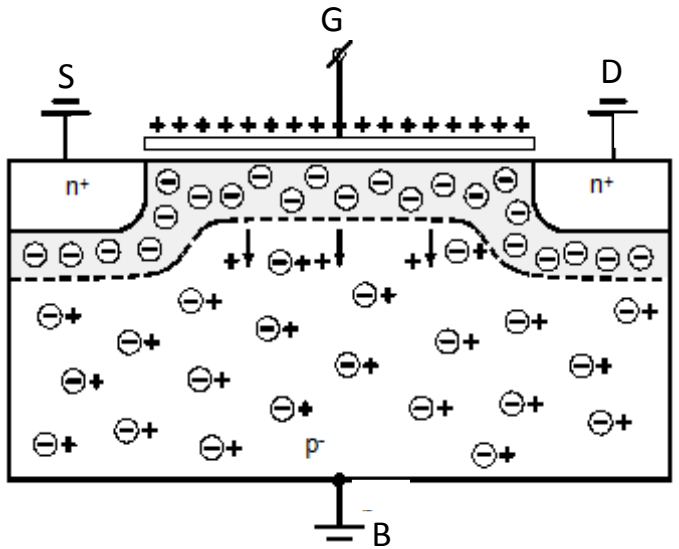
Zero-biased
$V_{GS} = 0$



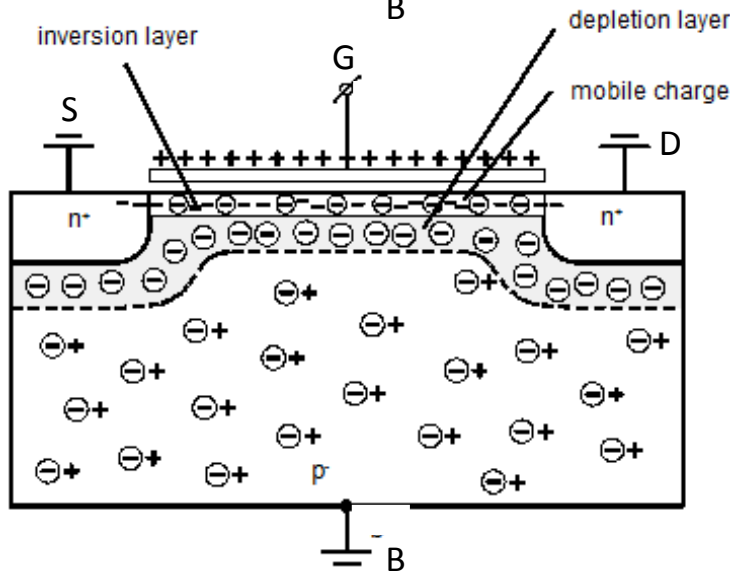
Accumulation
$V_{GS} < 0$



Depletion
$0 < V_{GS} < V_T$



Inversion
$V_{GS} > V_T$

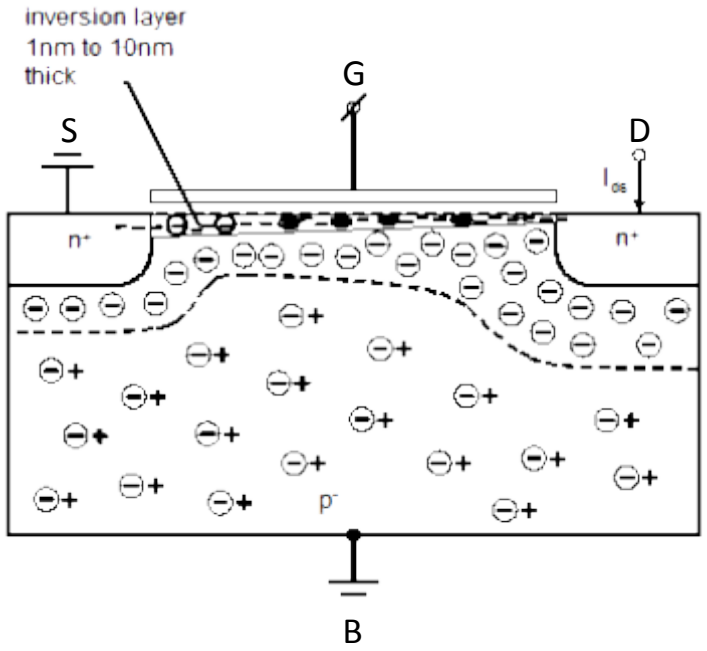


MOS transistor modes of operation

Linear region

$V_{GS} > V_T > 0$

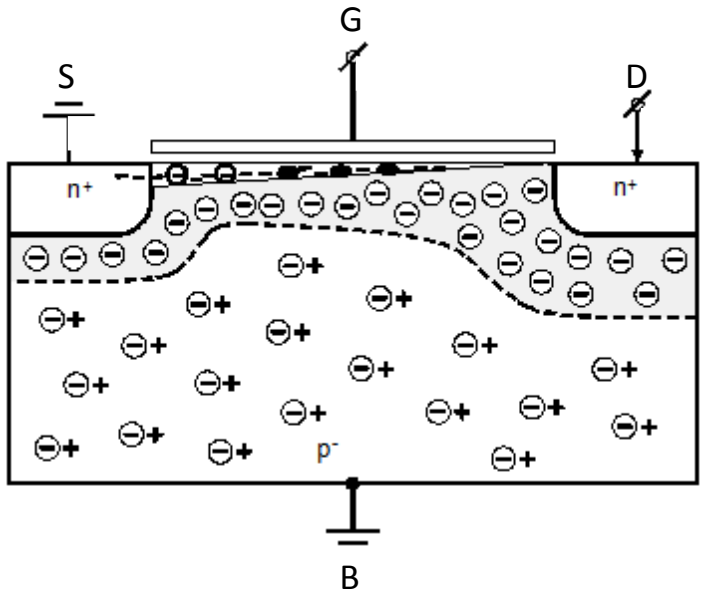
$0 < V_{DS} < V_{GS} - V_T$



Pinch-off

$V_{GS} > V_T > 0$

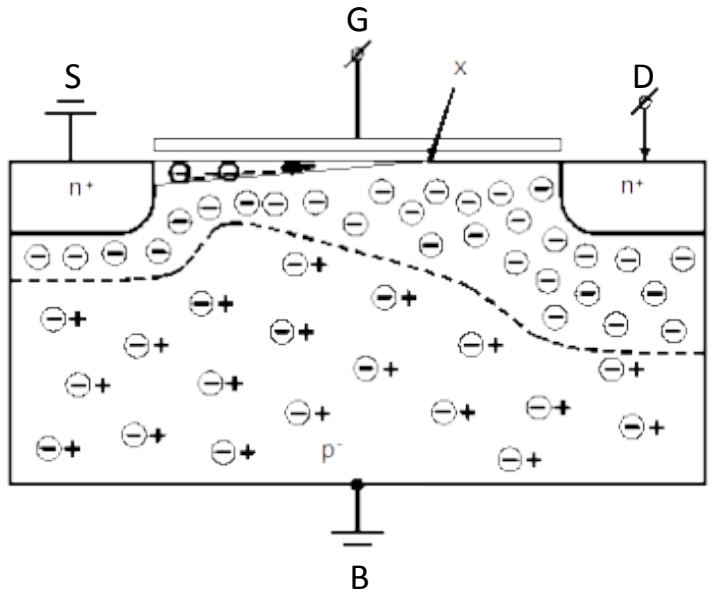
$V_{DS} > V_{GS} - V_T$



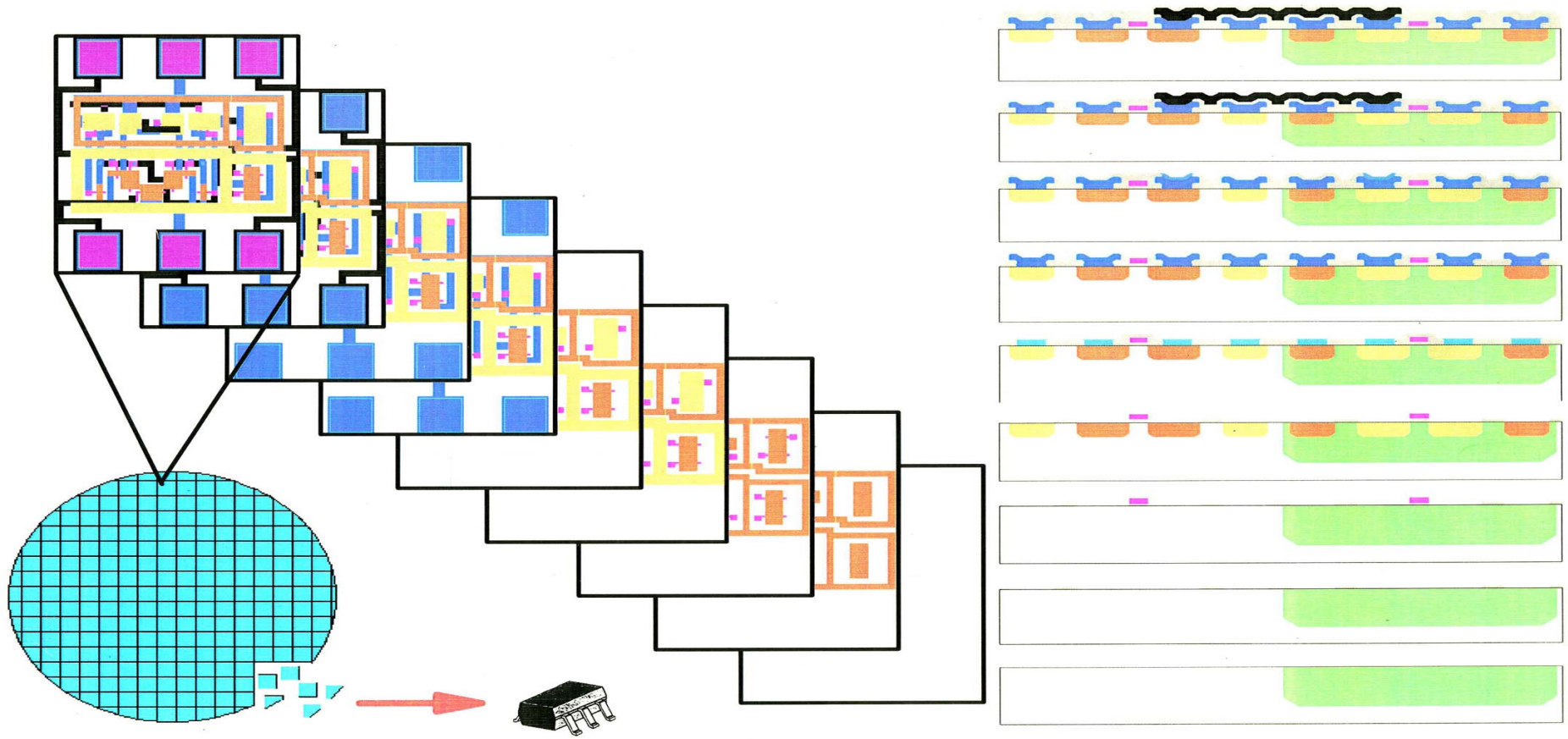
Saturation

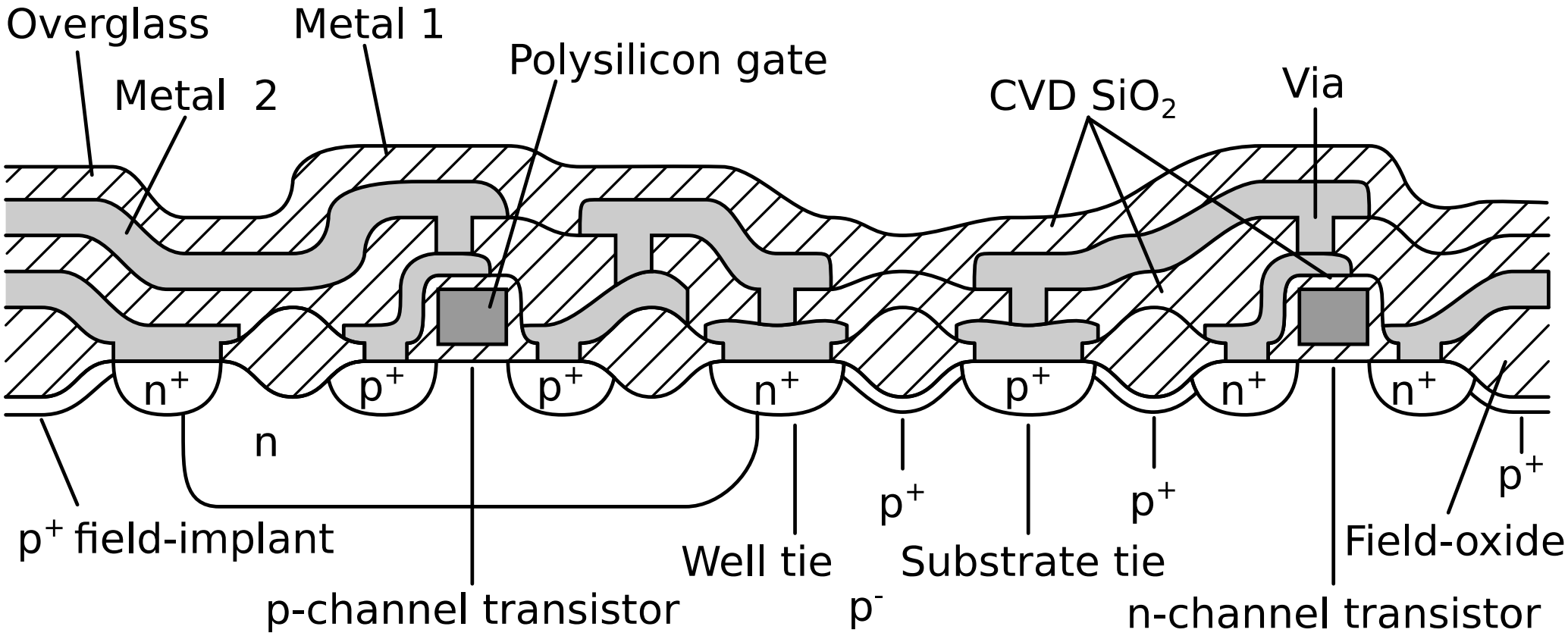
$V_{GS} > V_T > 0$

$V_{DS} > V_{GS} - V_T$



Introduction to CMOS technology





Final cross section of an example CMOS microcircuit.

Major process steps in typical n-well CMOS process

1. Clean wafer
2. GROW THIN OXIDE
3. Apply photoresist
4. PATTERN N-WELL MASK#1
5. Develop photoresist
6. Deposit and diffuse n-type impurities
7. Strip photoresist
8. Strip thin oxide
9. Grow thin oxide
10. Apply layer of Si_3N_4
11. Apply photoresist
12. PATTERN Si_3N_4 (active area definition) MASK#2
13. Develop photoresist
14. Etch Si_3N_4
15. Strip photoresist

Optional field threshold voltage adjust

A.1 Apply photoresist
A.2 PATTERN ANTIMOAT IN SUBSTRATE MASK#A1
A.3 Develop photoresist
A.4 FIELD IMPLANT (p-type)
A.5 Strip photoresist

16. GROW FIELD OXIDE
17. Strip Si_3N_4
18. Strip thin oxide
19. GROW GATE OXIDE
20. POLYSILICON DEPOSITION (POLY I)
21. Apply photoresist
22. PATTERN POLYSILICON MASK#3
23. Develop photoresist
24. ETCH POLYSILICON
25. Strip photoresist

Optional steps for double polysilicon process

B.1 Strip thin oxide
B.2 GROW THIN OXIDE
B.3 POLYSILICON DEPOSITION (POLY II)
B.4 Apply photoresist
B.5 PATTERN POLYSILICON MASK #B1
B.6 Develop photoresist
B.7 ETCH POLYSILICON
B.8 Strip photoresist
B.9 Strip thin oxide

26. Apply photoresist
27. PATTERN P-CHANNEL DRAINS AND SOURCES AND P+ GUARD RINGS (p-substrate ohmic contacts) (MASK #4)
28. Develop photoresist
29. p+ IMPLANT
30. Strip photoresist
31. Apply photoresist
32. PATTERN N-CHANNEL DRAINS AND SOURCES AND N+ GUARD RINGS (n-well ohmic contacts) (MASK #5)
33. Develop photoresist
34. n+ IMPLANT
35. Strip photoresist
36. Strip thin oxide
37. Grow oxide
38. Apply photoresist
39. PATTERN CONTACT OPENINGS (MASK #6)
40. Develop photoresist
41. Etch oxide
42. Strip photoresist
43. APPLY METAL
44. Apply photoresist
45. PATTERN METAL (MASK #7)
46. Develop photoresist
47. Etch metal
48. Strip photoresist

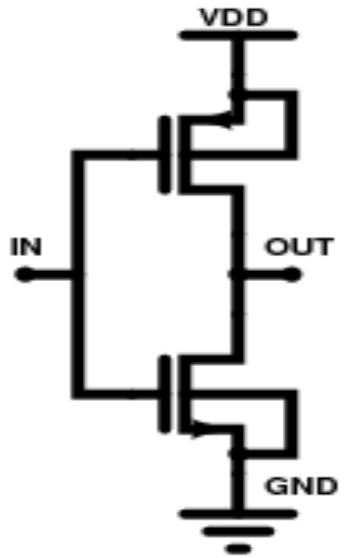
Optional steps for double metal process

C.1 Strip thin oxide
C.2 DEPOSIT INTERMETAL OXIDE
C.3 Apply photoresist
C.4 PATTERN VIAS (MASK #C1)
C.5 Develop photoresist
C.6 Etch oxide
C.7 Strip photoresist
C.8 APPLY METAL (Metal 2)
C.9 Apply photoresist
C.10 PATTERN METAL (MASK #C2)
C.11. Develop photoresist
C.12 Etch metal
C.13 Strip photoresist

49. APPLY PASSIVATION
50. Apply photoresist
51. PATTERN PAD OPENINGS (MASK #8)
52. Develop photoresist
53. Etch passivation
54. Strip photoresist
55. ASSEMBLE, PACKAGE AND TEST

Fabrication steps

- Build inverter from the bottom up

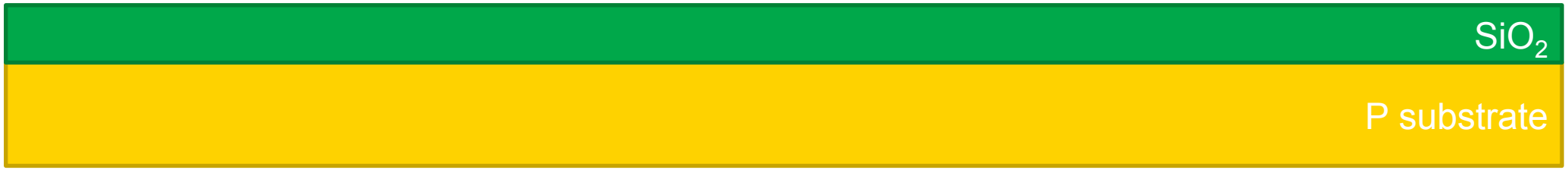


Step 1: Form N-well for the PMOS

- Start with blank wafer

Step 1: Form N-well for the PMOS

- Start with blank wafer
- Grow silicon-oxide (SiO_2) in oxidation furnace using H_2O

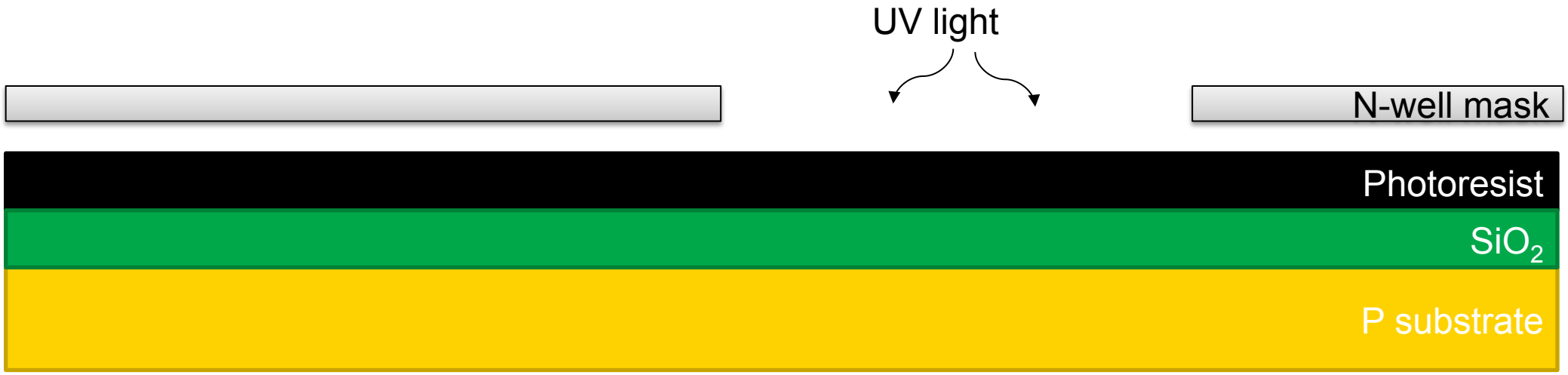


Step 1: Form N-well for the PMOS

- Start with blank wafer
- Grow silicon-oxide (SiO_2) in oxidation furnace using H_2O
- Spin on photoresist, softens when exposed to light

Step 1: Form N-well for the PMOS

- Start with blank wafer
- Grow silicon-oxide (SiO_2) in oxidation furnace using H_2O
- Spin on photoresist, softens when exposed to light
- Apply UV light through N-well mask



Step 1: Form N-well for the PMOS

- Start with blank wafer
- Grow silicon-oxide (SiO_2) in oxidation furnace using H_2O
- Spin on photoresist, softens when exposed to light
- Apply UV light through N-well mask
- Strip of exposed photoresist and etch oxide with hydrofluoric acid

Step 1: Form N-well for the PMOS

- Start with blank wafer
- Grow silicon-oxide (SiO_2) in oxidation furnace using H_2O
- Spin on photoresist, softens when exposed to light
- Apply UV light through N-well mask
- Strip of exposed photoresist and etch oxide with hydrofluoric acid
- Remove rest of the photoresist with acid mixture (Piranah etch)

Step 1: Form N-well for the PMOS

- Start with blank wafer
- Grow silicon-oxide (SiO_2) in oxidation furnace using H_2O
- Spin on photoresist, softens when exposed to light
- Apply UV light through N-well mask
- Strip of exposed photoresist and etch oxide with hydrofluoric acid
- Remove rest of the photoresist with acid mixture (Piranah etch)
- Form N-well with diffusion or ion-implantation

Step 1: Form N-well for the PMOS

- Start with blank wafer
- Grow silicon-oxide (SiO_2) in oxidation furnace using H_2O
- Spin on photoresist, softens when exposed to light
- Apply UV light through N-well mask
- Strip of exposed photoresist and etch oxide with hydrofluoric acid
- Remove rest of the photoresist with acid mixture (Piranah etch)
- Form N-well with diffusion or ion-implantation
- Remove rest of the oxide with hydrofluoric acid

Step 1: Form N-well for the PMOS

- Following steps are implemented similarly

Step 2: Polysilicon gates

- A thin silicon-oxide layer is placed

Step 2: Polysilicon gates

- A thin silicon-oxide layer is placed
- Chemical vapor deposition of silicon layer

Step 2: Polysilicon gates

- A thin silicon-oxide layer is placed
- Chemical vapor deposition of silicon layer
- Use similar procedure as in step 1 to pattern the polygates

Step 3: n+ diffusion

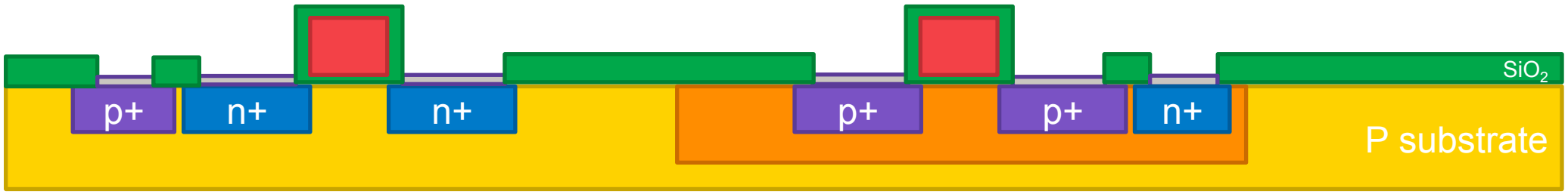
- n+ diffusion regions for NMOS source and drain
- Additionally, N-well needs to be connected to positive supply, hence the n+ diffusion region in the N-well

Step 4: p+ diffusion

- p+ diffusion regions for PMOS source and drain
- Additionally, P substrate needs to have a local connection to ground, hence the p+ diffusion region near NMOS

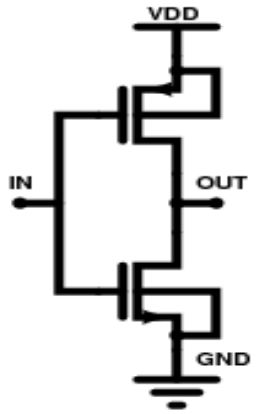
Step 5: Contacts

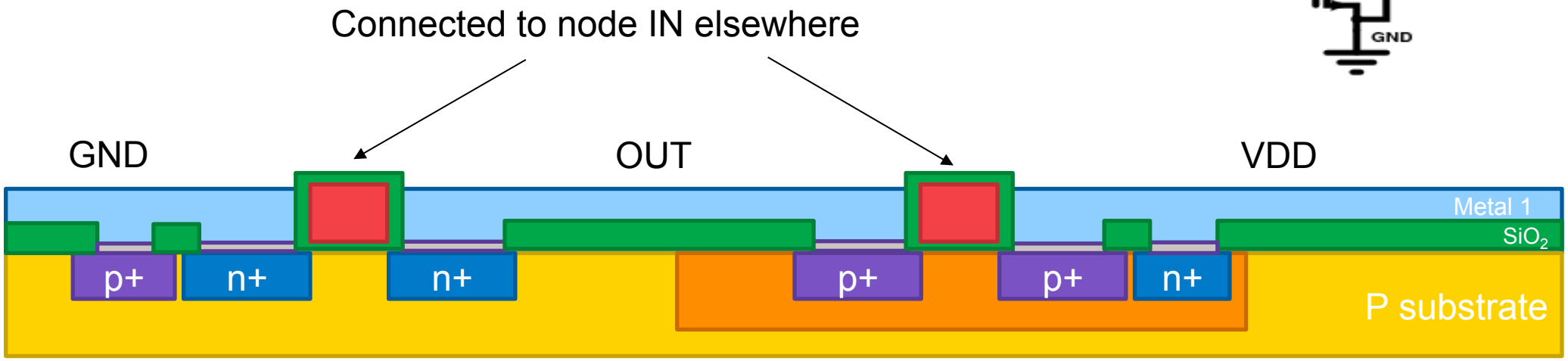
- Contacts are needed to connect to the wiring
- Rest of the surface is covered with oxide, which acts as an insulator

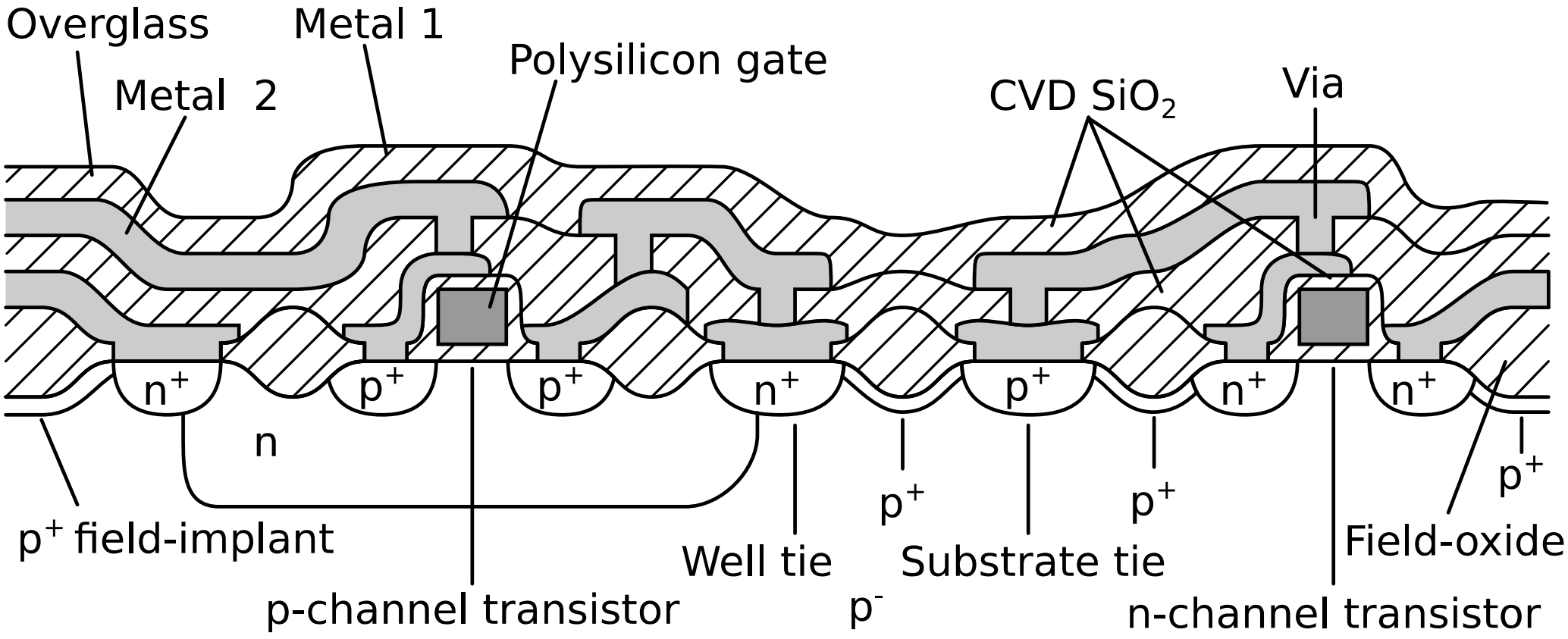


Step 5: Metal 1

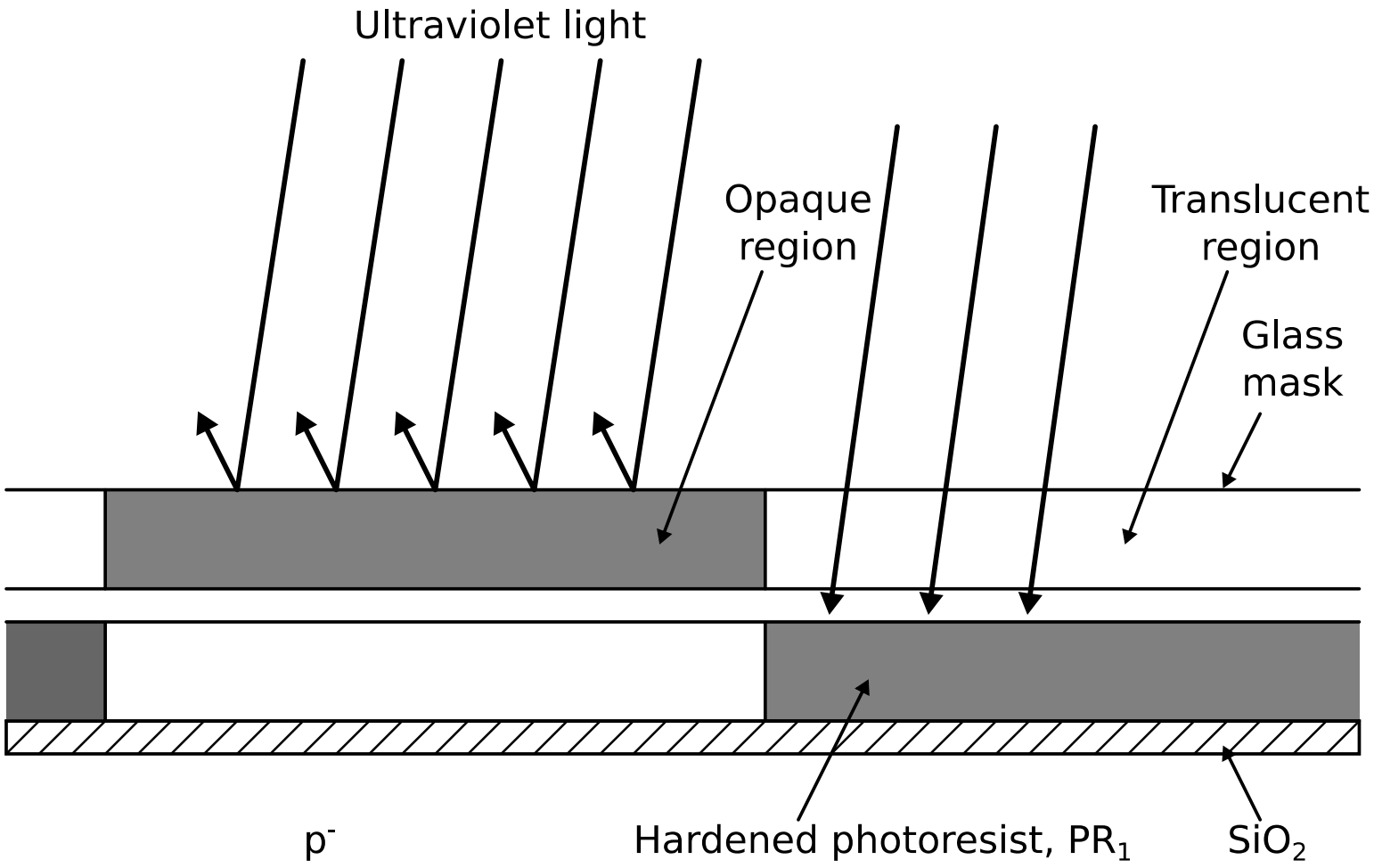
- Wiring is implemented using metal layers



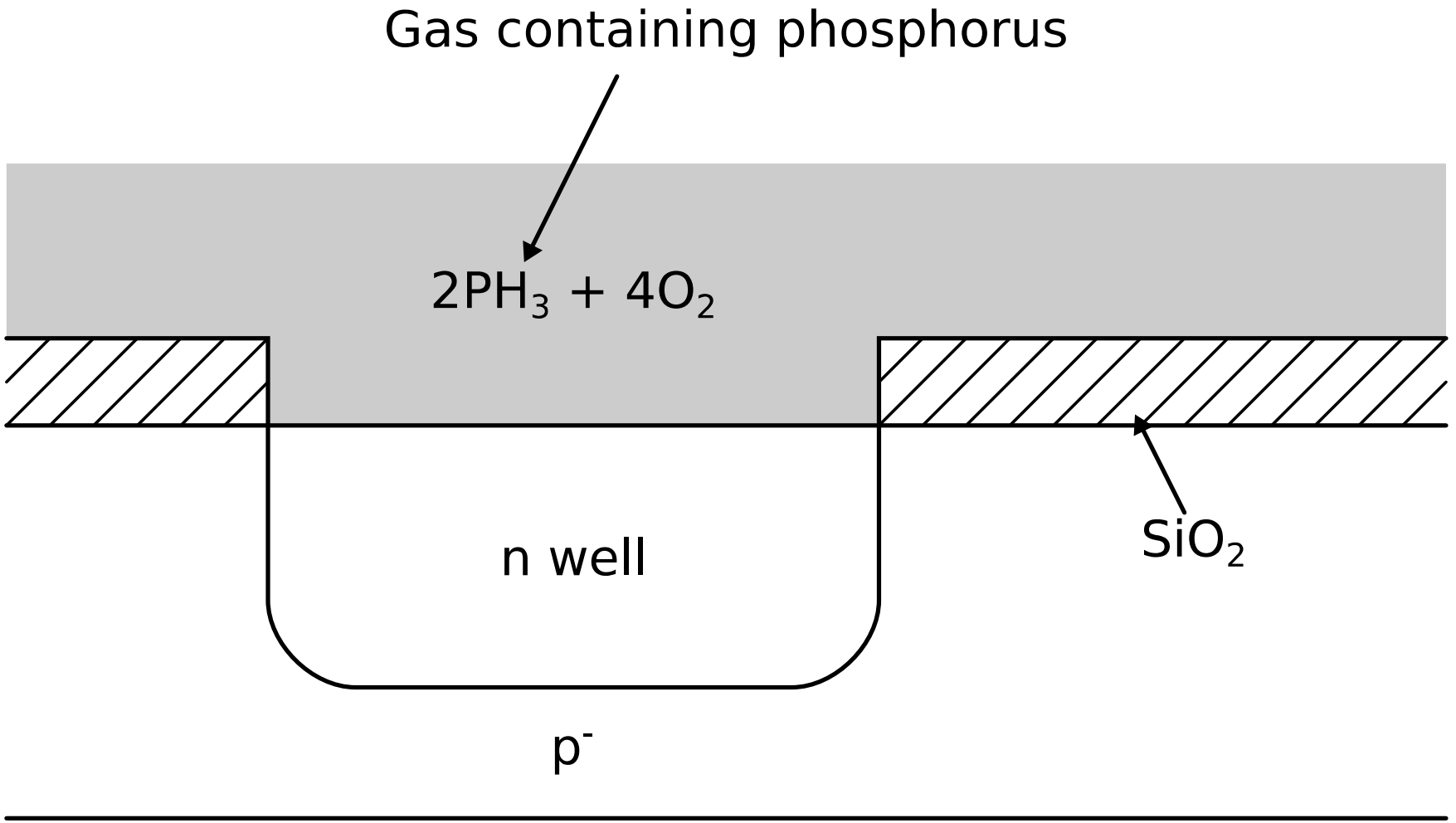




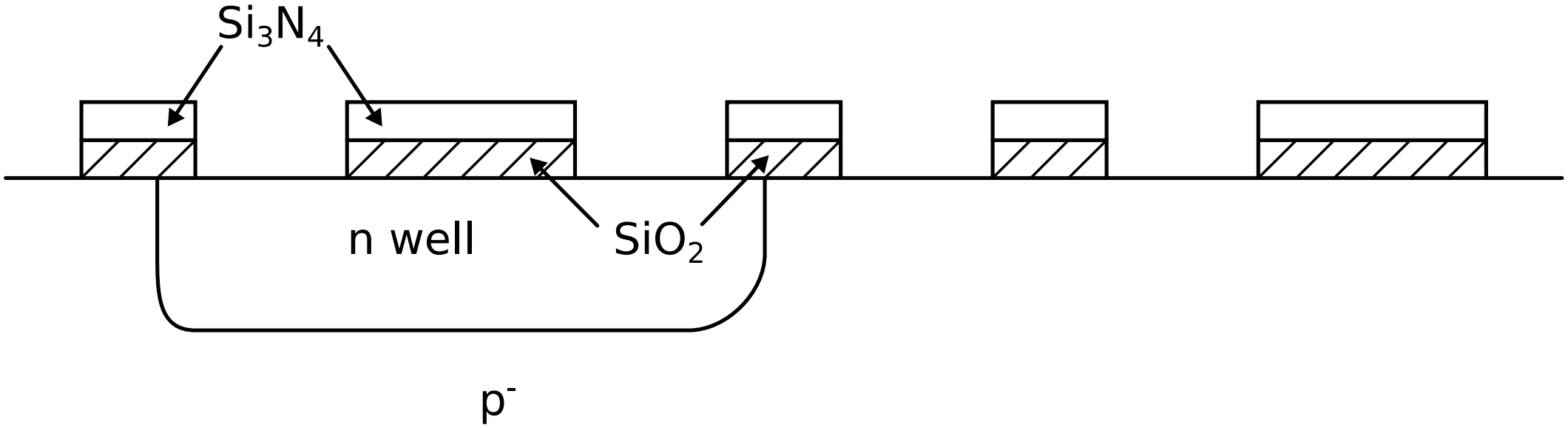
Final cross section of an example CMOS microcircuit.



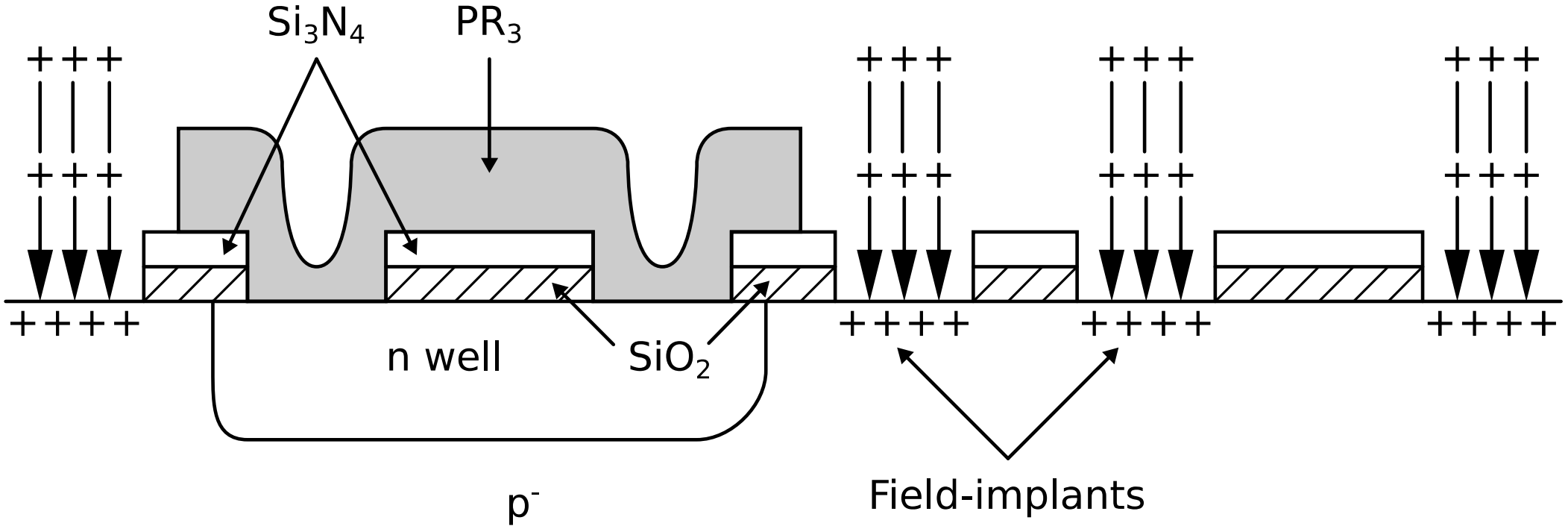
Selectively hardening a region of a photoresist using a glass mask.



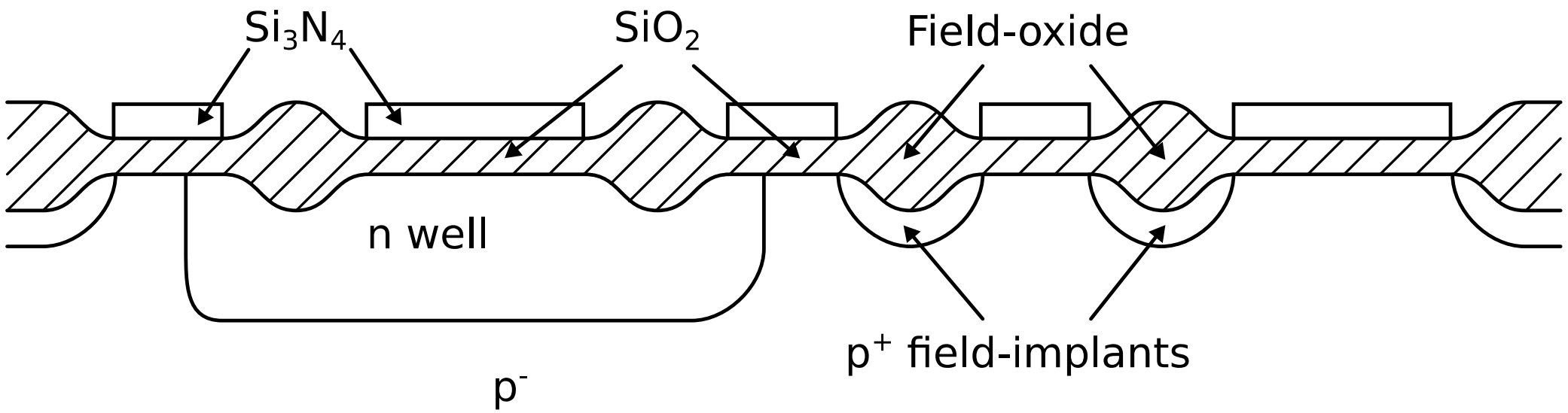
Forming an n well by diffusing phosphorus from a gas into the silicon, through the opening in the SiO_2.



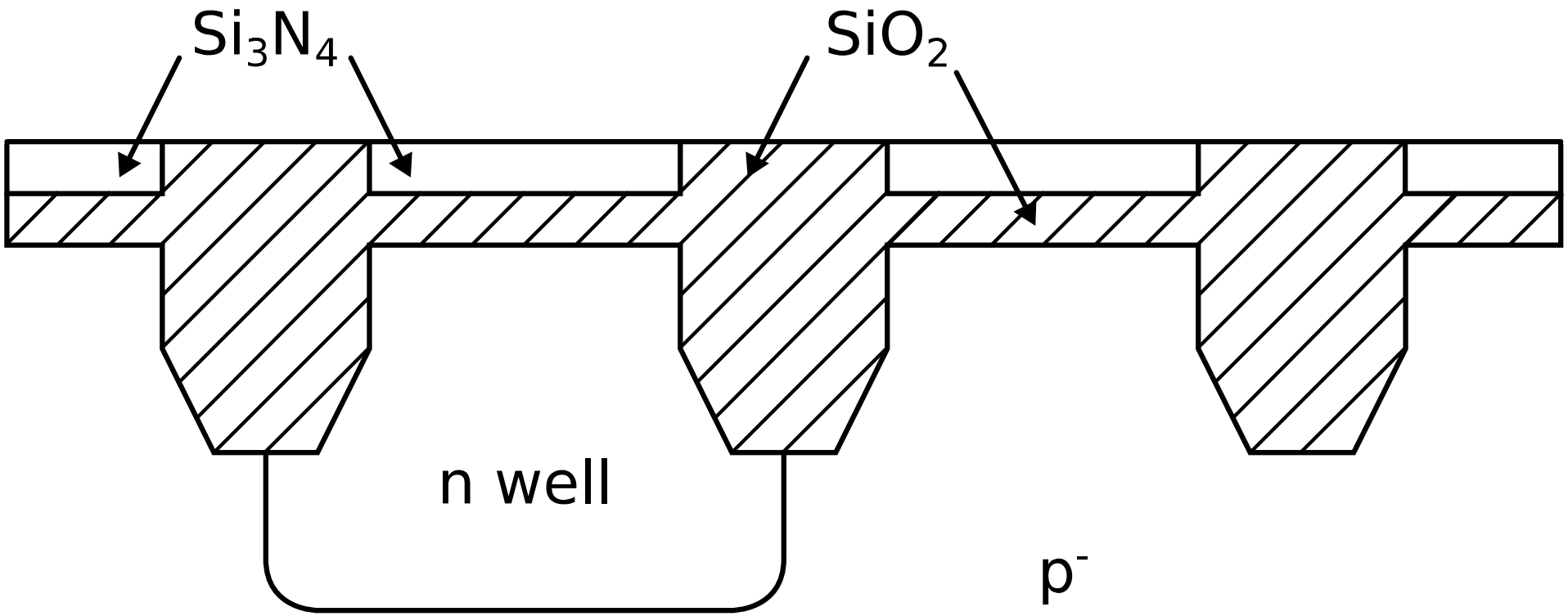
The cross section of the wafer after the oxide definition (OD) regions are patterned.



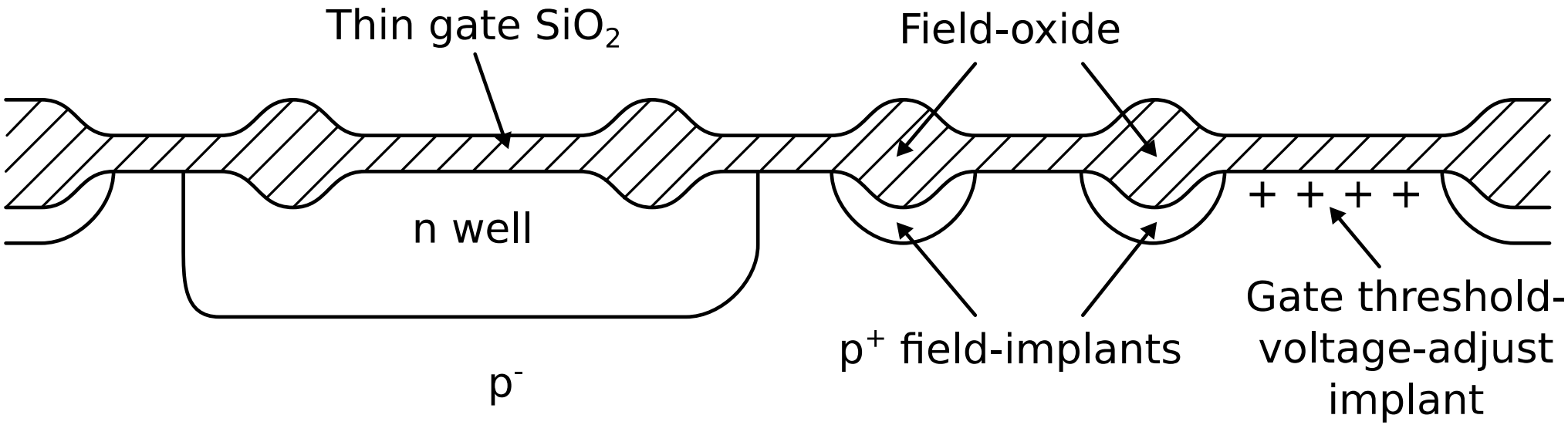
The cross section when the field-implants are being formed in a LOCOS process.



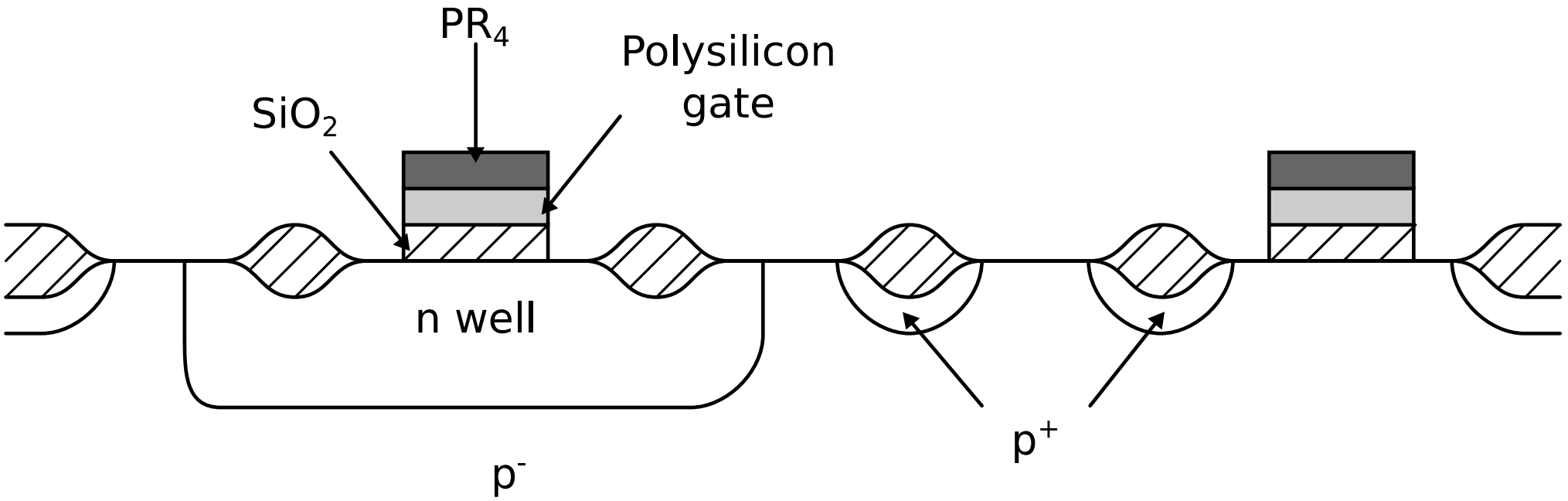
The cross section after the field-oxide has been grown in a LOCOS process.



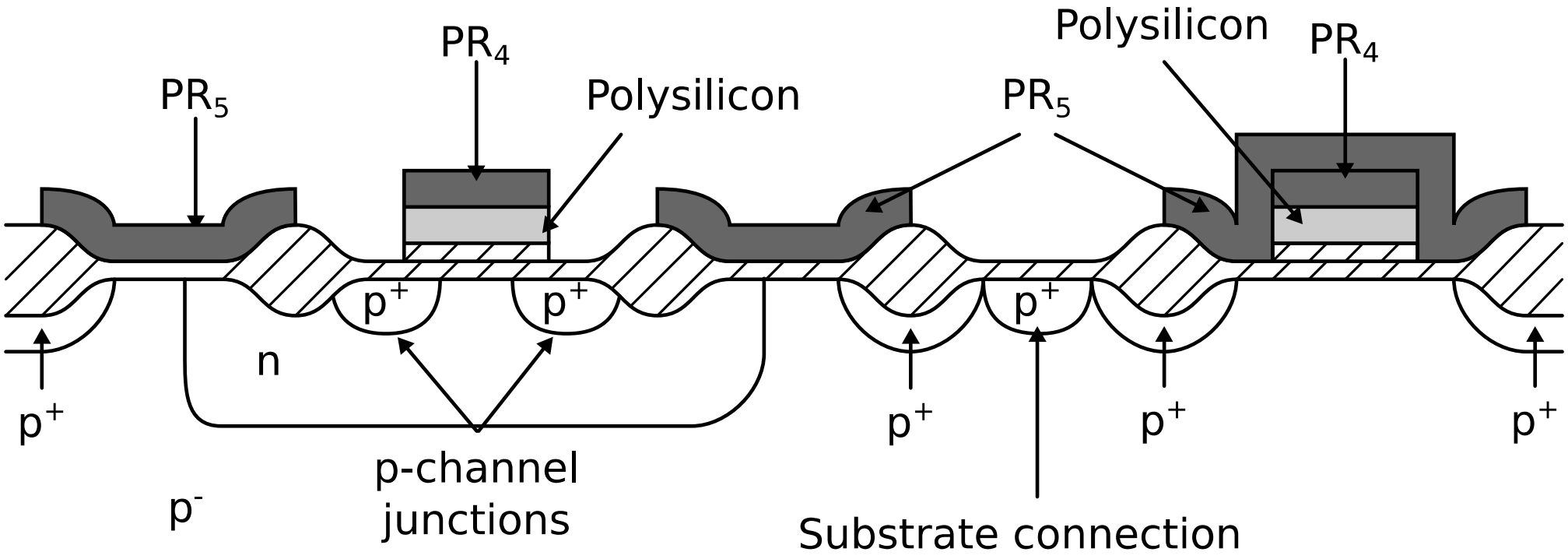
The resulting wafer cross section when shallow-trench isolation (STI) is used between transistors.



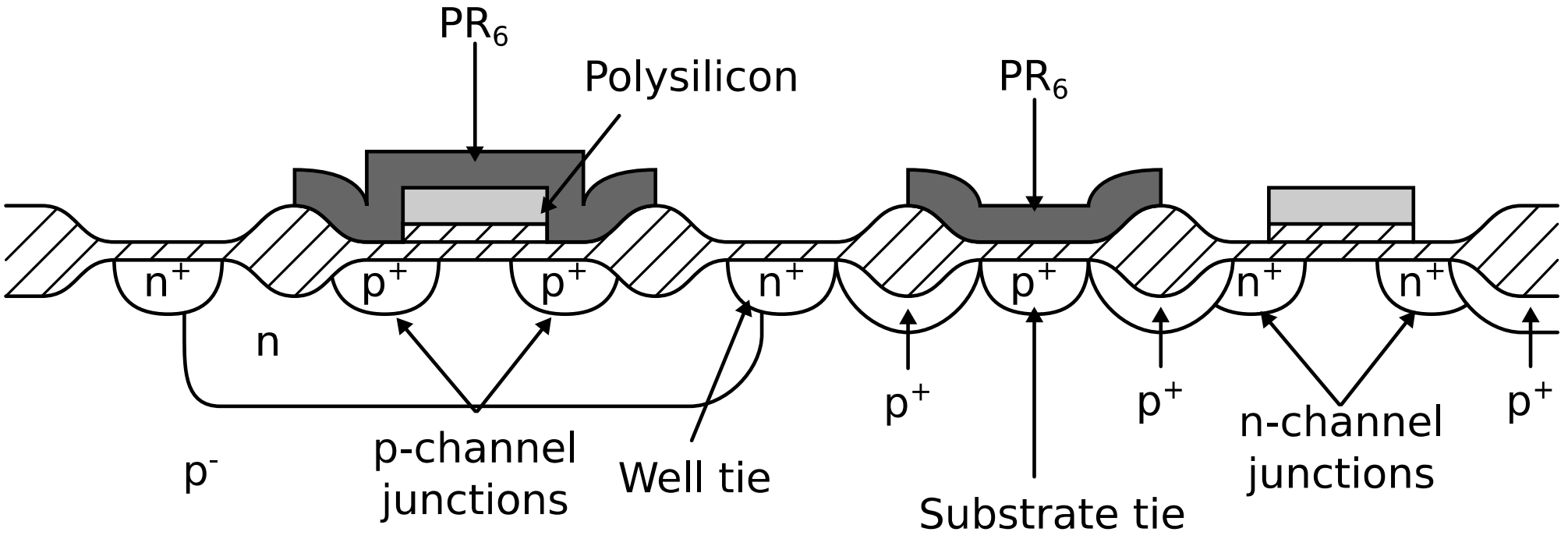
Cross section after the thin gate-oxide growth and threshold-adjust implant.



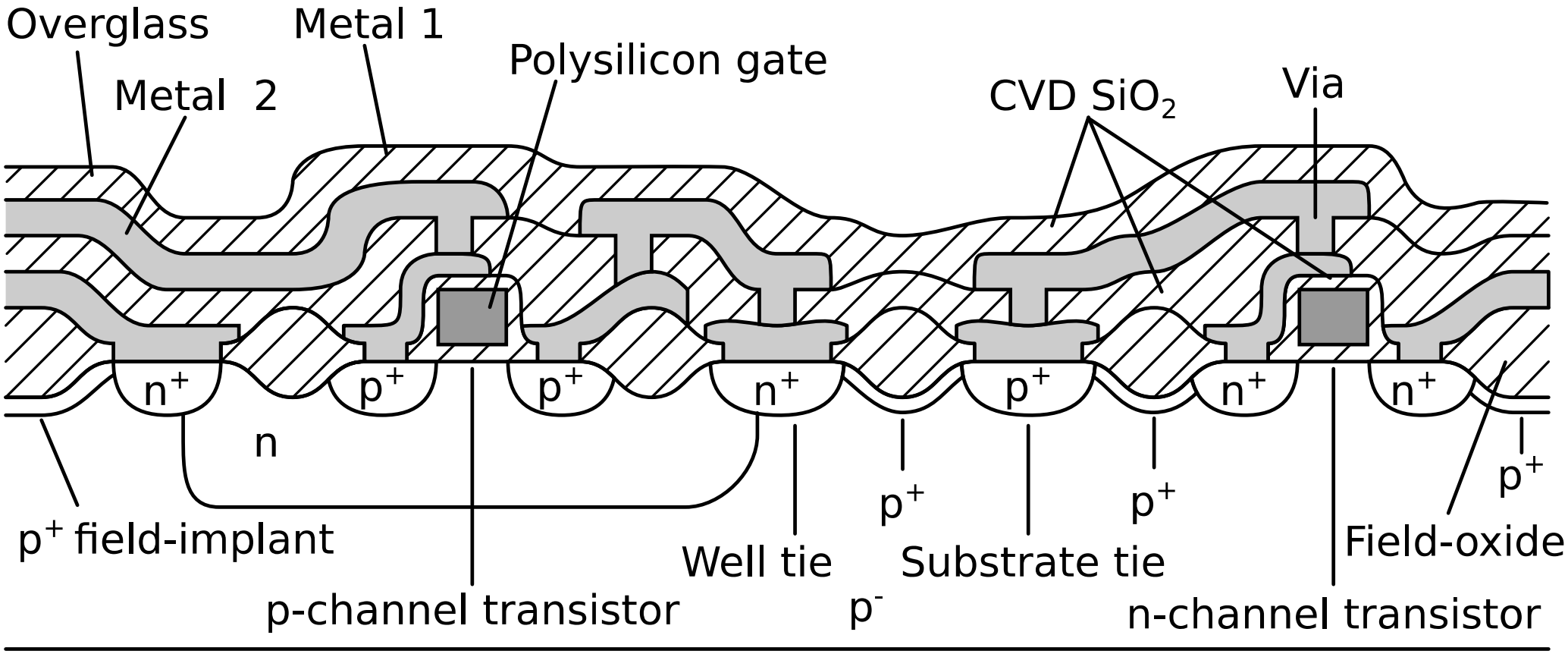
Cross section after depositing and patterning the polysilicon gates.



Cross section after ion-implanting the p^+ junctions.



Cross section after ion-implanting the n^+ junctions.



Final cross section of an example CMOS microcircuit.

Major process steps in typical p-well CMOS process

1. Clean wafer
2. GROW THIN OXIDE
3. Apply photoresist
4. PATTERN P-WELL MASK#1
5. Develop photoresist
6. Deposit and diffuse p-type impurities
7. Strip photoresist
8. Strip thin oxide
9. Grow thin oxide
10. Apply layer of Si_3N_4
11. Apply photoresist
12. PATTERN Si_3N_4 (active area definition) MASK#2
13. Develop photoresist
14. Etch Si_3N_4
15. Strip photoresist

Optional field threshold voltage adjust

A.1 Apply photoresist
A.2 PATTERN ANTIMOAT IN SUBSTRATE MASK#A1
A.3 Develop photoresist
A.4 FIELD IMPLANT (n-type)
A.5 Strip photoresist

16. GROW FIELD OXIDE
17. Strip Si_3N_4
18. Strip thin oxide
19. GROW GATE OXIDE
20. POLYSILICON DEPOSITION (POLY I)
21. Apply photoresist
22. PATTERN POLYSILICON MASK#3
23. Develop photoresist
24. ETCH POLYSILICON
25. Strip photoresist

Optional steps for double polysilicon process

B.1 Strip thin oxide
B.2 GROW THIN OXIDE
B.3 POLYSILICON DEPOSITION (POLY II)
B.4 Apply photoresist
B.5 PATTERN POLYSILICON MASK #B1
B.6 Develop photoresist
B.7 ETCH POLYSILICON
B.8 Strip photoresist
B.9 Strip thin oxide

26. Apply photoresist
27. PATTERN P-CHANNEL DRAINS AND SOURCES AND P+ GUARD RINGS (p-well ohmic contacts) (MASK #4)
28. Develop photoresist
29. p+ IMPLANT
30. Strip photoresist
31. Apply photoresist
32. PATTERN N-CHANNEL DRAINS AND SOURCES AND N+ GUARD RINGS (top ohmic contact to substrate) (MASK #5)
33. Develop photoresist
34. n+ IMPLANT
35. Strip photoresist
36. Strip thin oxide
37. Grow oxide
38. Apply photoresist
39. PATTERN CONTACT OPENINGS (MASK #6)
40. Develop photoresist
41. Etch oxide
42. Strip photoresist
43. APPLY METAL
44. Apply photoresist
45. PATTERN METAL (MASK #7)
46. Develop photoresist
47. Etch metal
48. Strip photoresist

Optional steps for double metal process

C.1 Strip thin oxide
C.2 DEPOSIT INTERMETAL OXIDE
C.3 Apply photoresist
C.4 PATTERN VIAS (MASK #C1)
C.5 Develop photoresist
C.6 Etch oxide
C.7 Strip photoresist
C.8 APPLY METAL (Metal 2)
C.9 Apply photoresist
C.10 PATTERN METAL (MASK #C2)
C.11. Develop photoresist
C.12 Etch metal
C.13 Strip photoresist

49. APPLY PASSIVATION
50. Apply photoresist
51. PATTERN PAD OPENINGS (MASK #8)
52. Develop photoresist
53. Etch passivation
54. Strip photoresist
55. ASSEMBLE, PACKAGE AND TEST

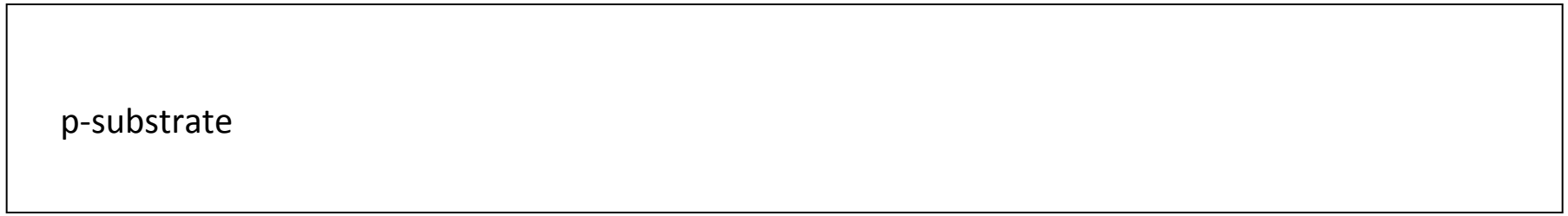
Introduction to lay-out

CMOS-INVERTER

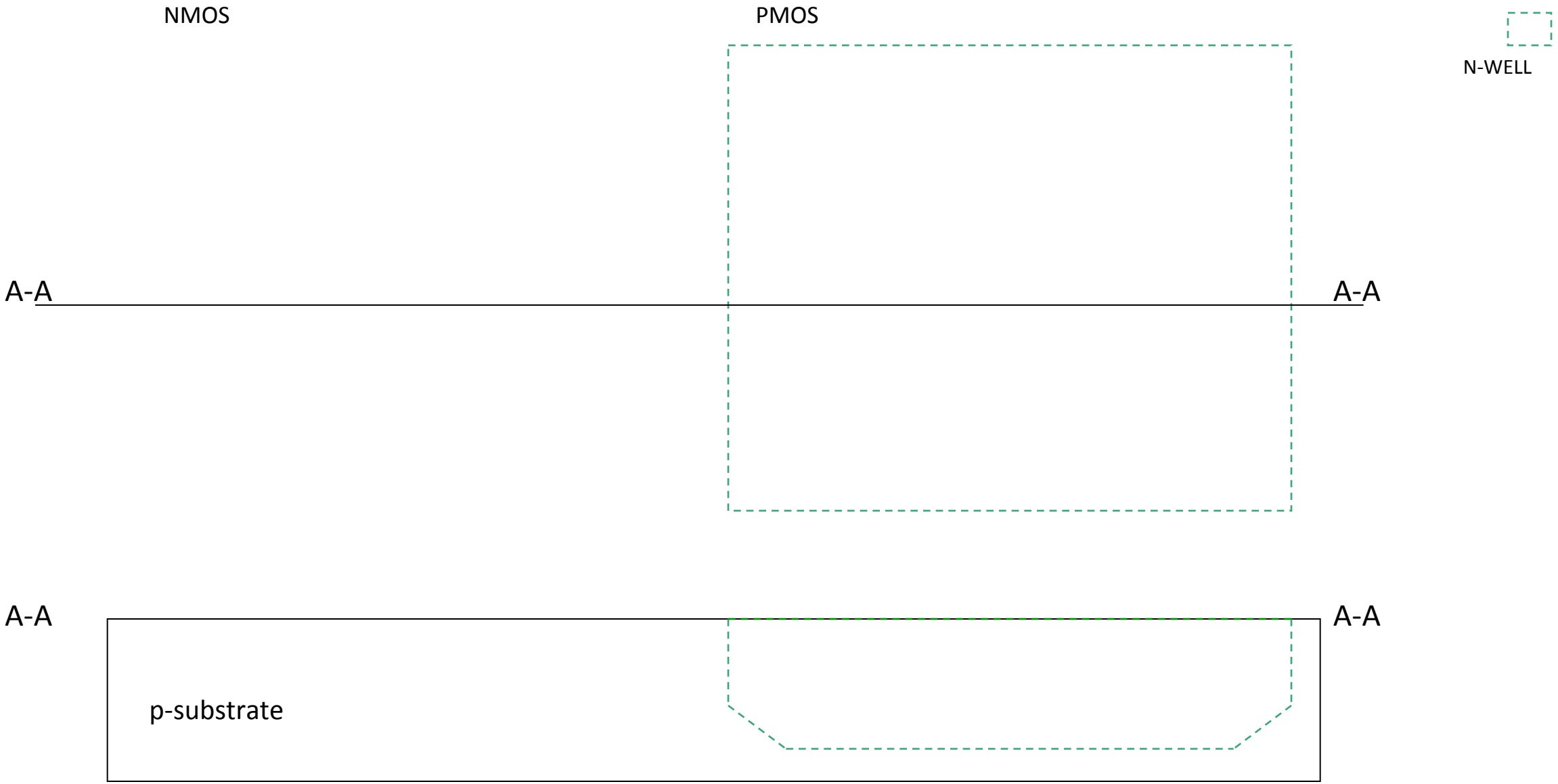
NMOS PMOS

A-A A-A

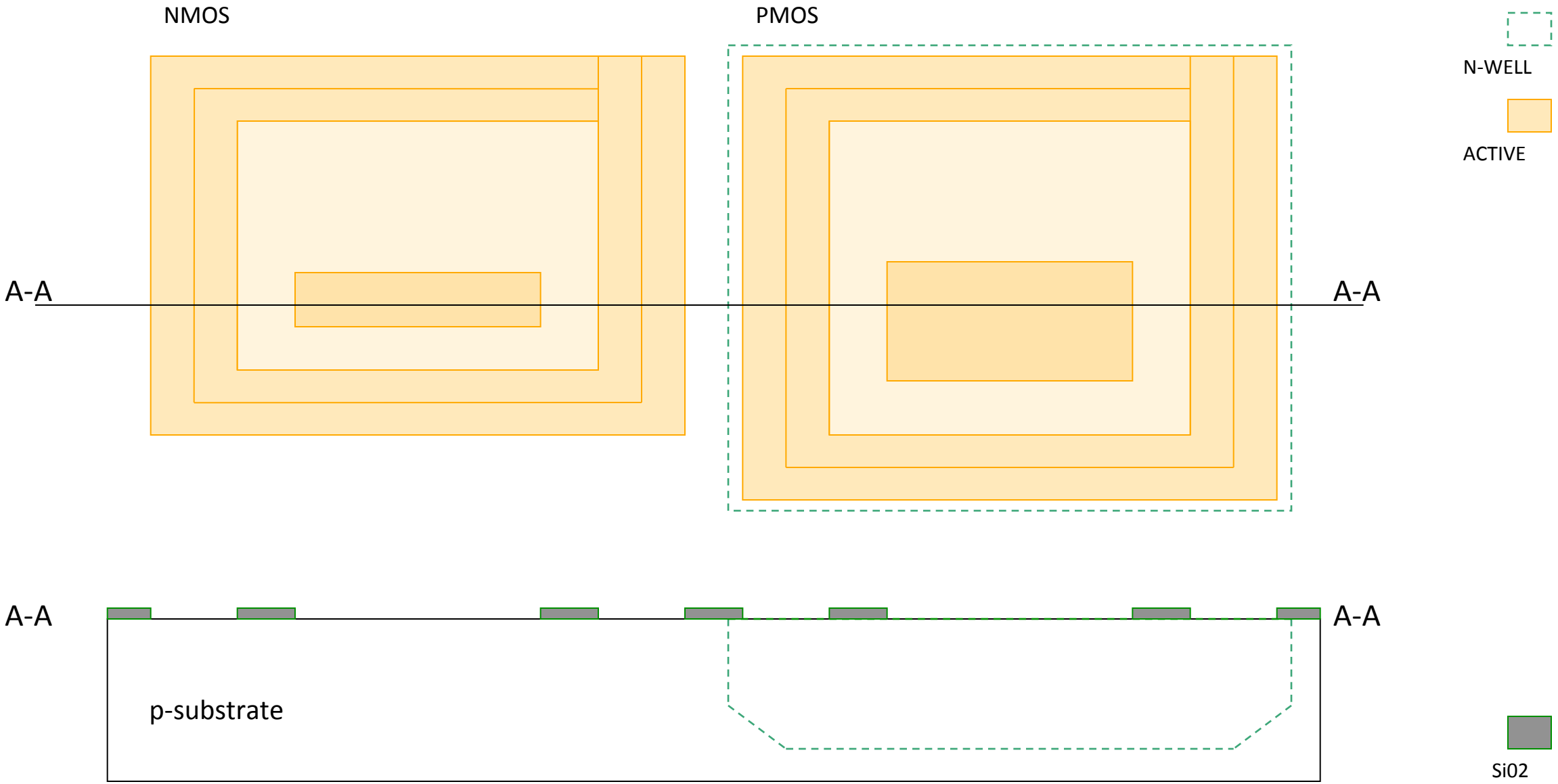
A-A A-A



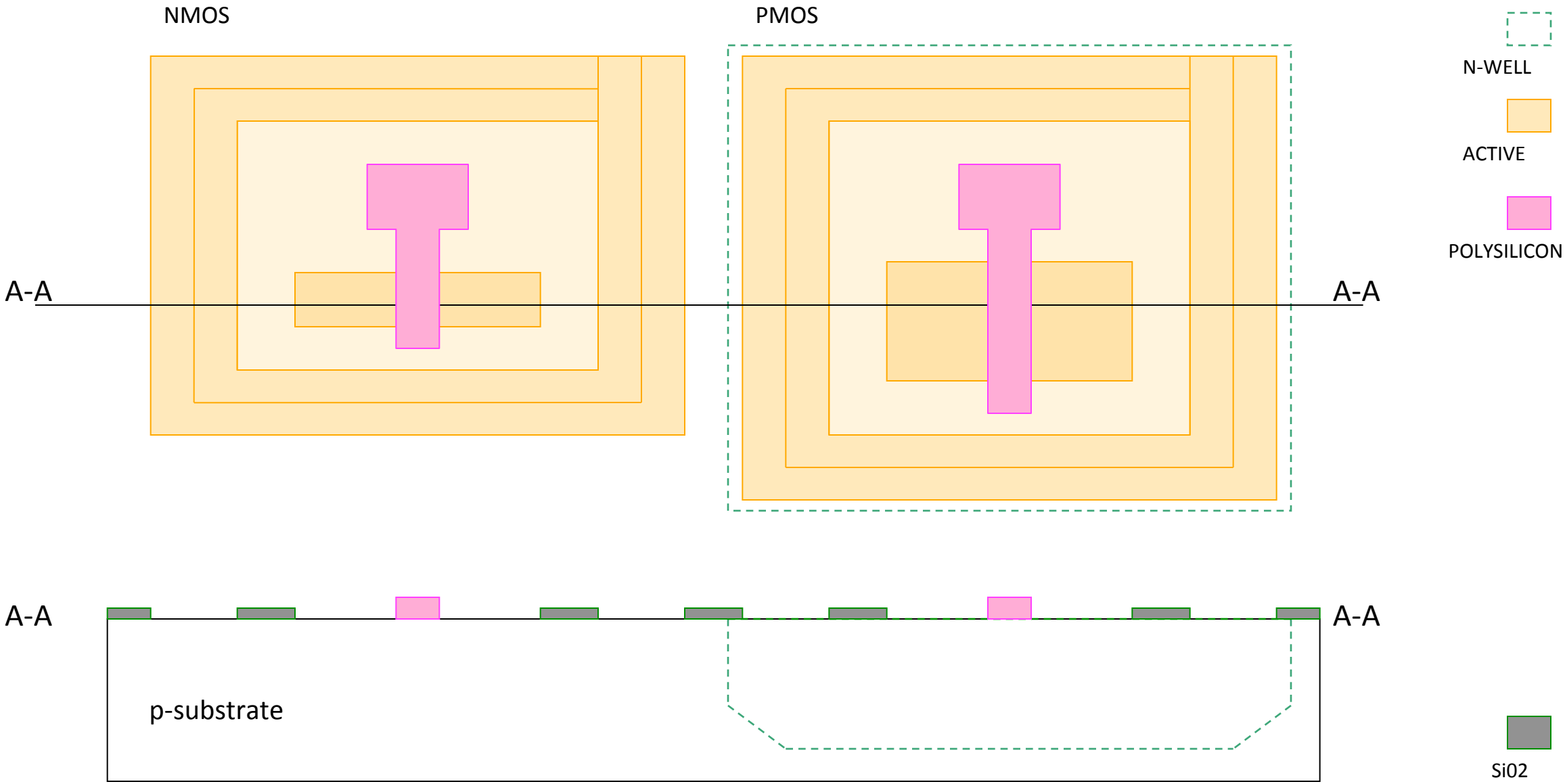
CMOS-INVERTER



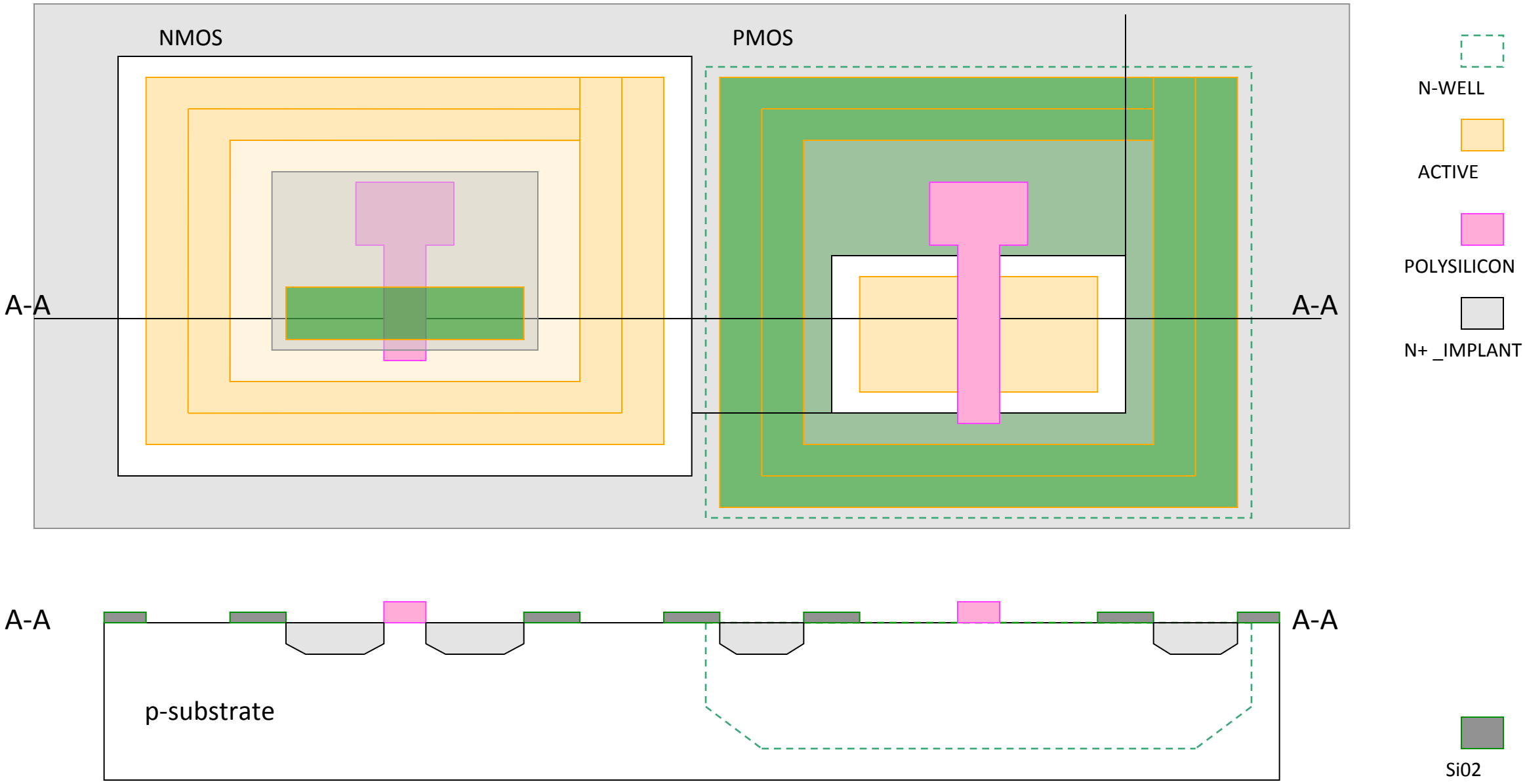
CMOS-INVERTER



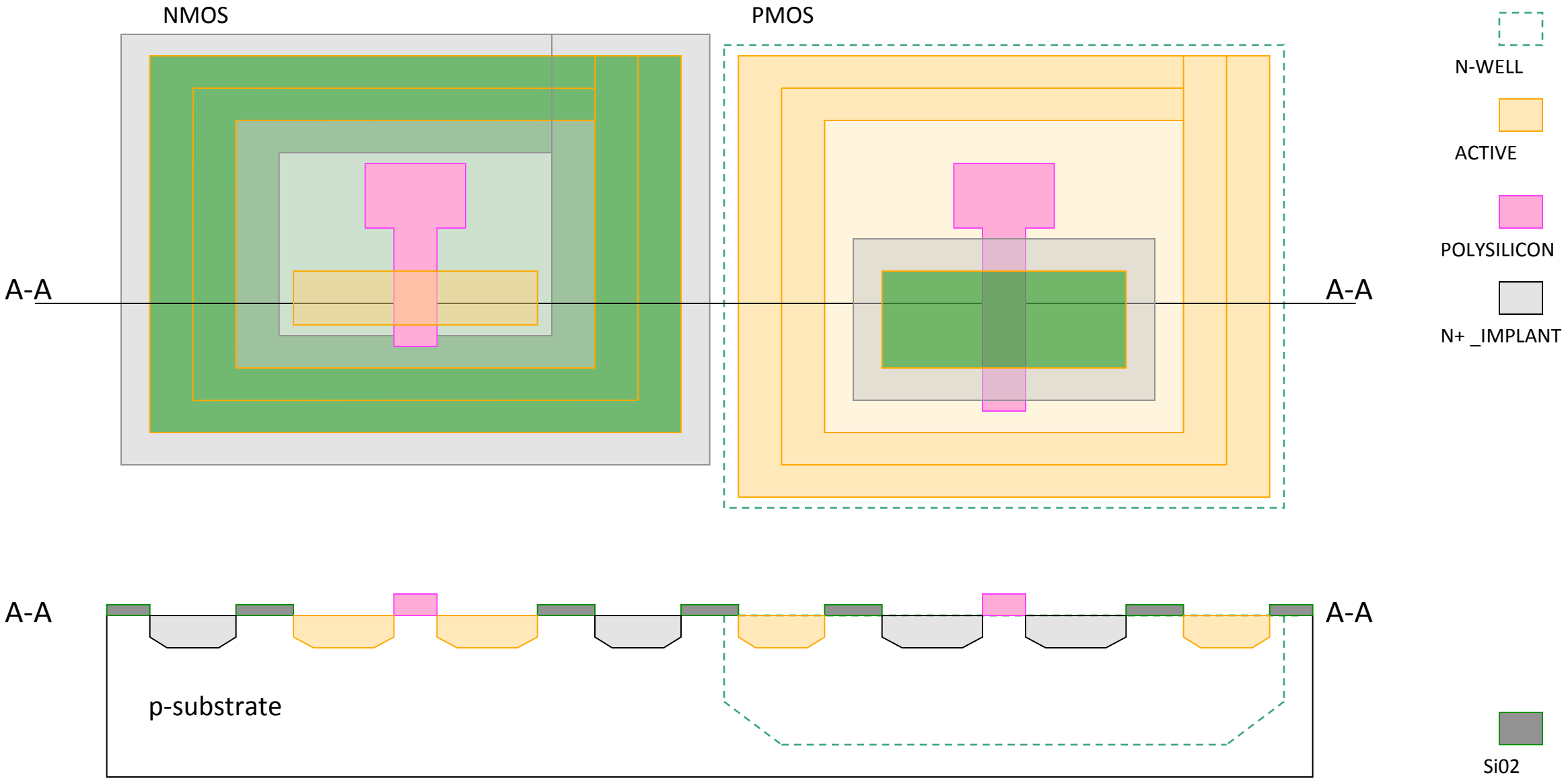
CMOS-INVERTER



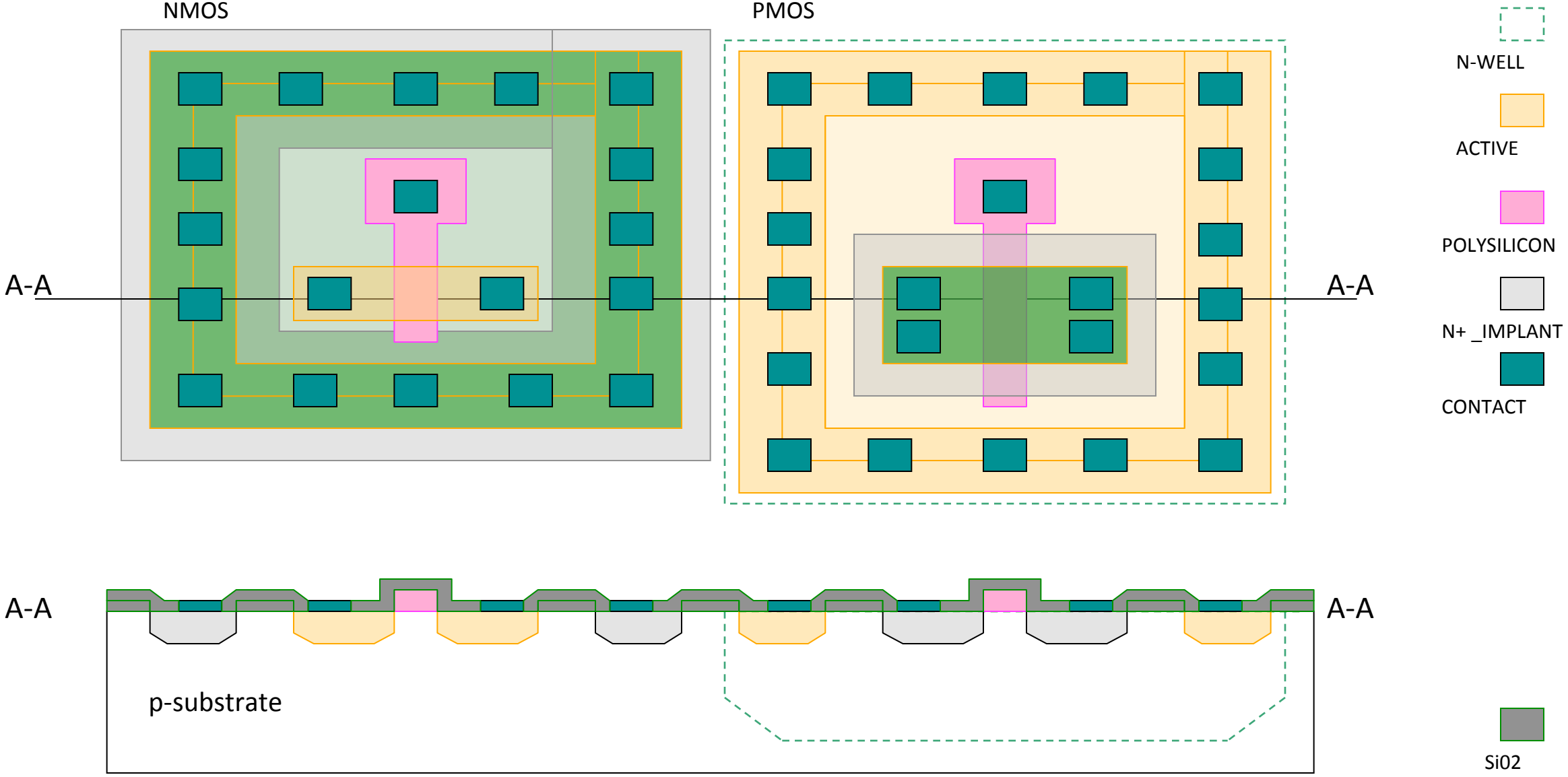
CMOS-INVERTER



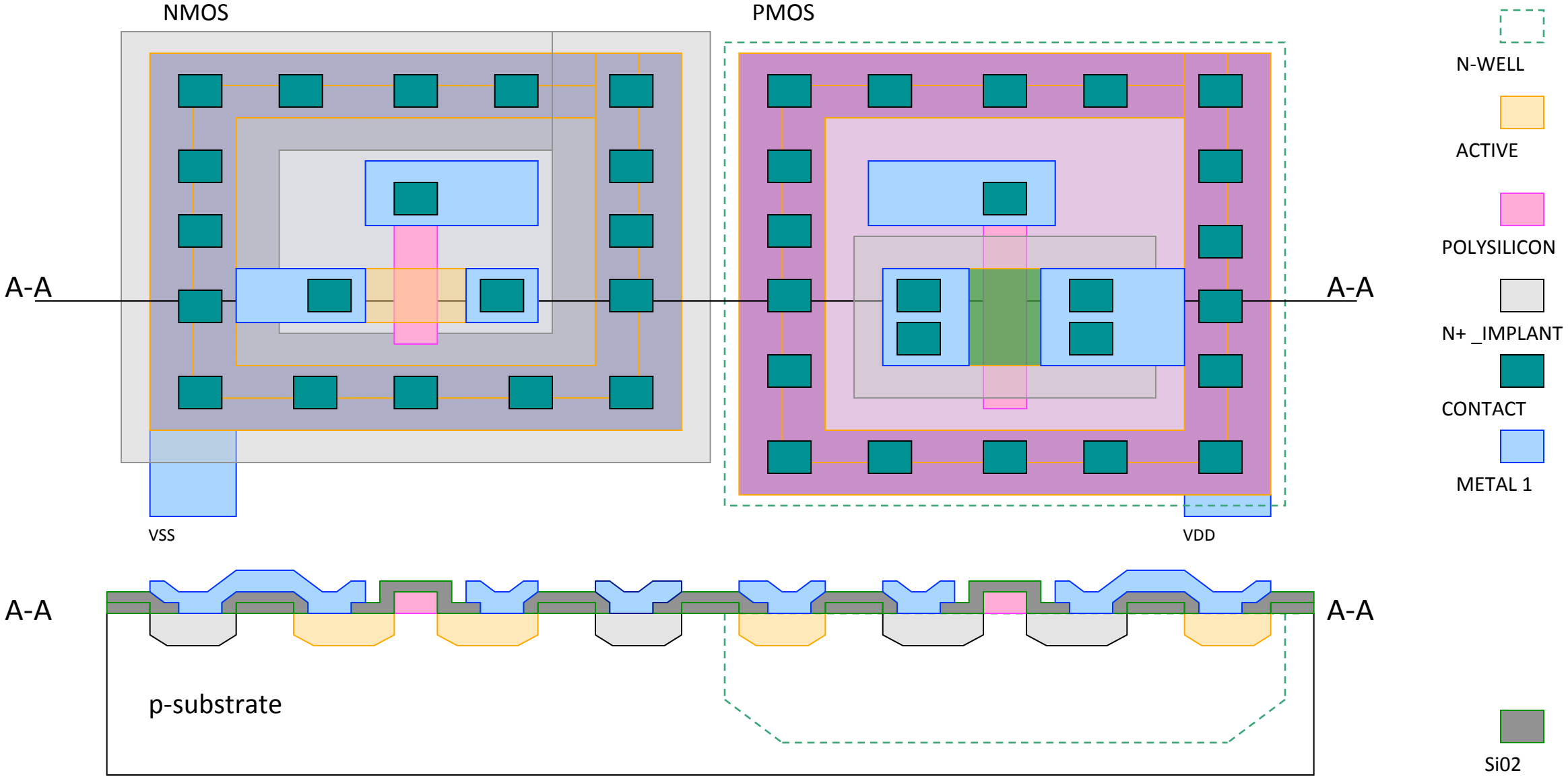
CMOS-INVERTER



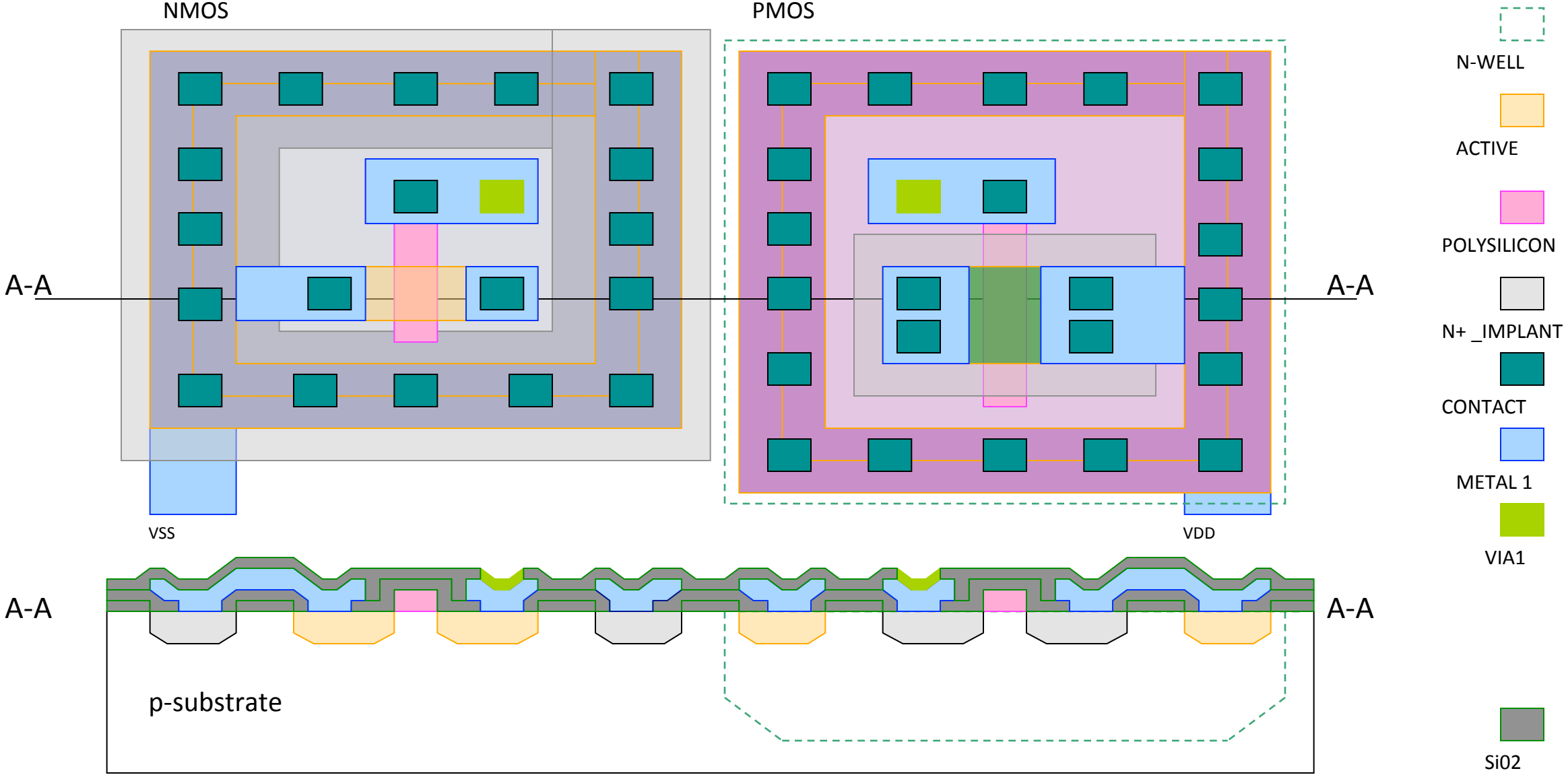
CMOS-INVERTER



CMOS-INVERTER



CMOS-INVERTER



CMOS-INVERTER