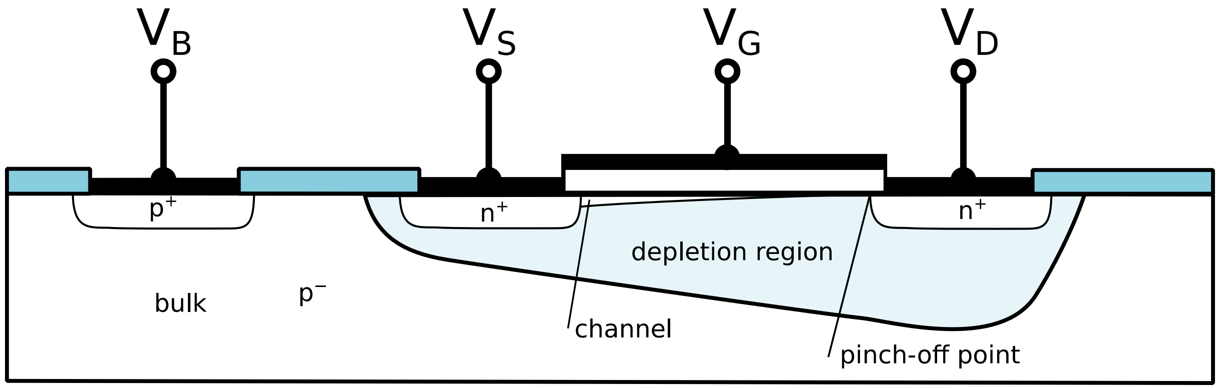
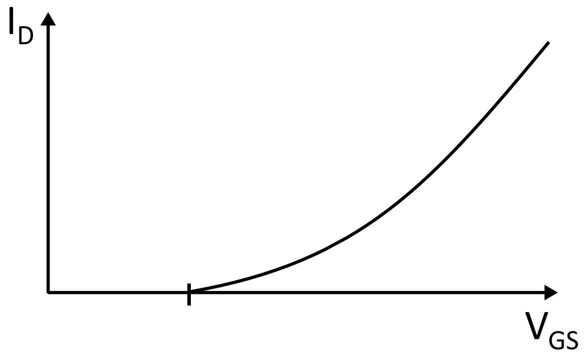
ELEC-E3510 Basics of IC Design

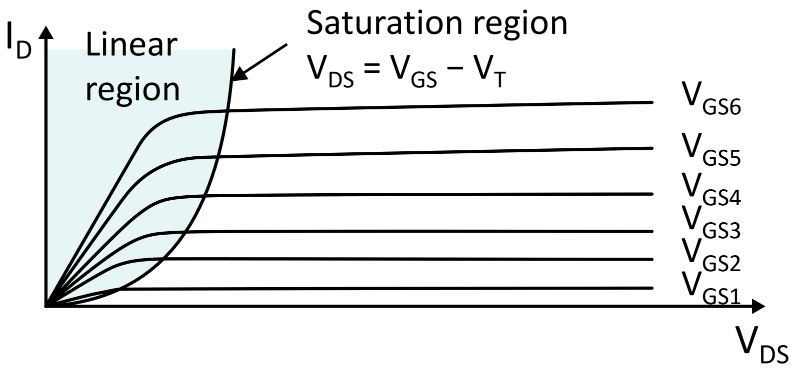
Lecture 2:
MOS transistor models

Lecture outline:
- threshold voltage of MOS transistor
- drain current equation
- parasitic capacitors and resistors
- short channel effects (extra material)
 - weak inversion
- SPICE parameters
- small signal model

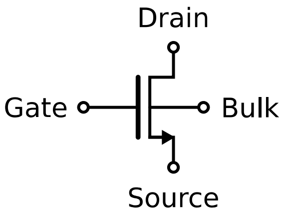
MOS transistor



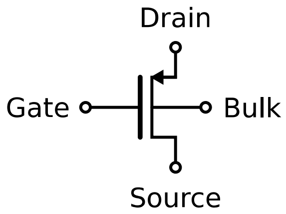




NMOS

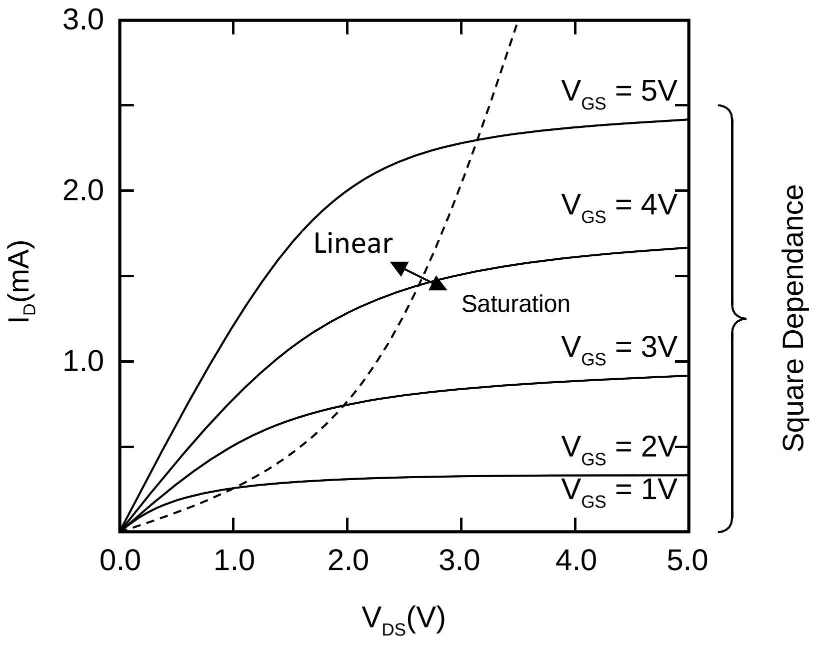


PMOS

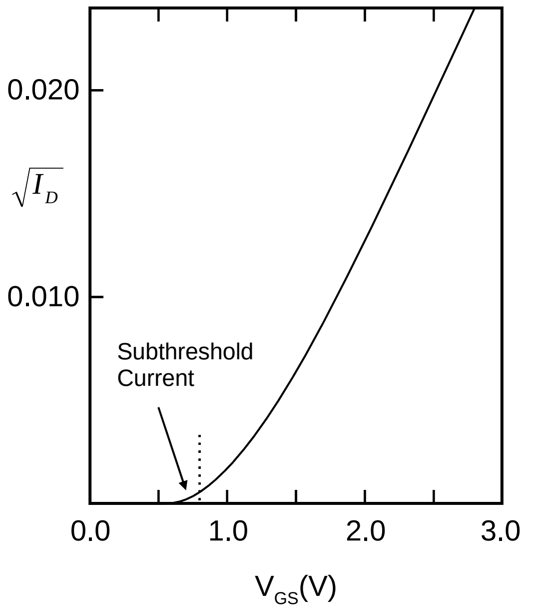


Modes of operation

Cut-off	$V_{GS} - V_T \leq 0$	$I_{DS} = 0$
Linear region (Triode region)	$0 < V_{DS} \leq (V_{GS} - V_T)$	$I_D = \frac{\mu_0 C_{ox} W}{L}\left[(v_{GS} - V_T) - \frac{V_{DS}}{2}\right] V_{DS}(1 + \lambda V_{DS})$ $k = (K')\frac{W}{L} \cong (\mu_0 C_{ox})\frac{W}{L}$ (amps/volt^2)
Saturation	$0 < (V_{GS} - V_T) \leq V_{DS}$	$I_D = \frac{\mu_0 C_{ox} W}{2L}(V_{GS} - V_T)^2 (1 + \lambda V_{DS})$
Pinch-off	$V_{DS,SAT} = V_{GS} - V_T$	$I_{DS,LIN} = I_{DS,SAT}$



a) I_D as a function of V_{DS}



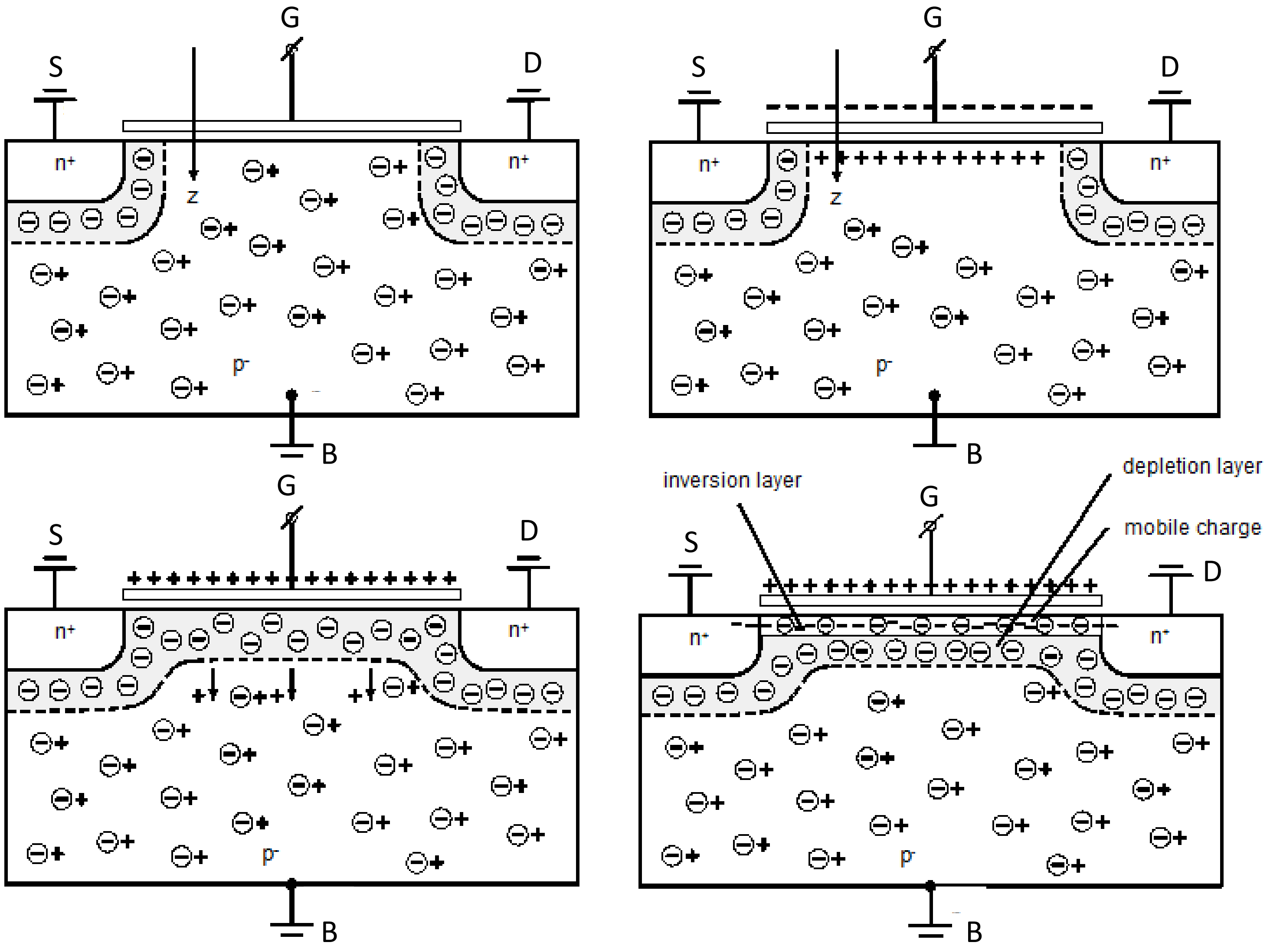
b) $\sqrt{I_D}$ as a function of V_{GS}
(for V_{DS} = 5V)

NMOS Enhancement Transistor: W = 100µm, L = 20µm

MOS transistor modes of operation

Zero-biased
$V_{GS} = 0$

Accumulation
$V_{GS} < 0$

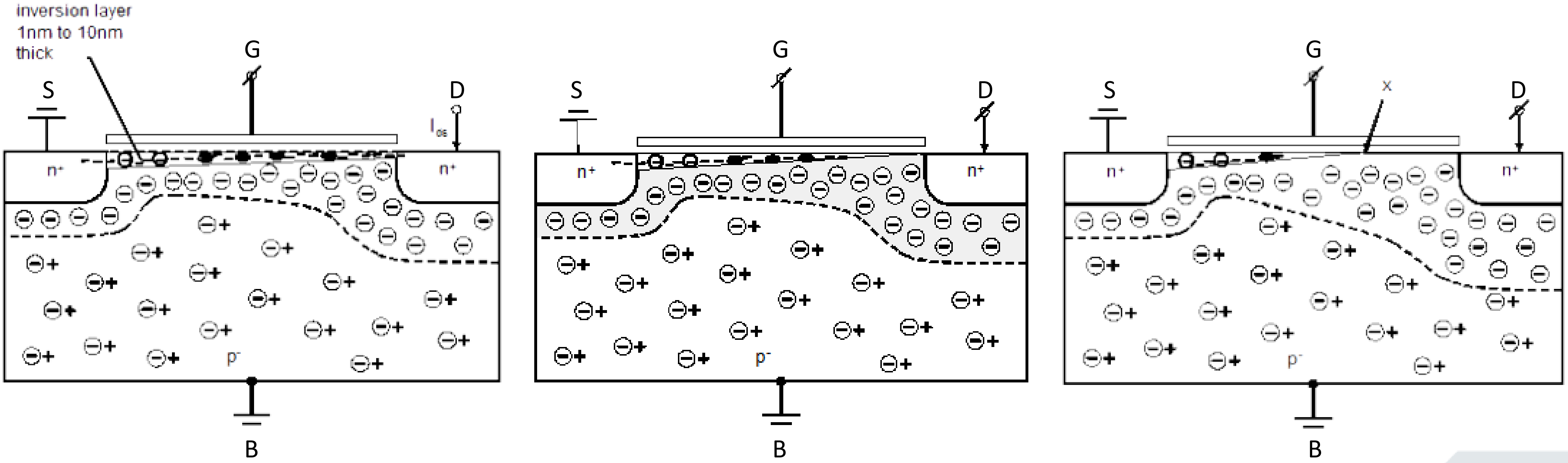


Depletion
$0 < V_{GS} < V_T$

Inversion
$V_{GS} > V_T$

MOS transistor modes of operation

Linear region	Pinch-off	Saturation
$V_{GS} > V_T > 0$	$V_{GS} > V_T > 0$	$V_{GS} > V_T > 0$
$0 < V_{DS} < V_{GS} - V_T$	$V_{DS} > V_{GS} - V_T$	$V_{DS} > V_{GS} - V_T$



Threshold voltage

gate-bulk work function diff.

formation of inversion layer

space charge of the bulk

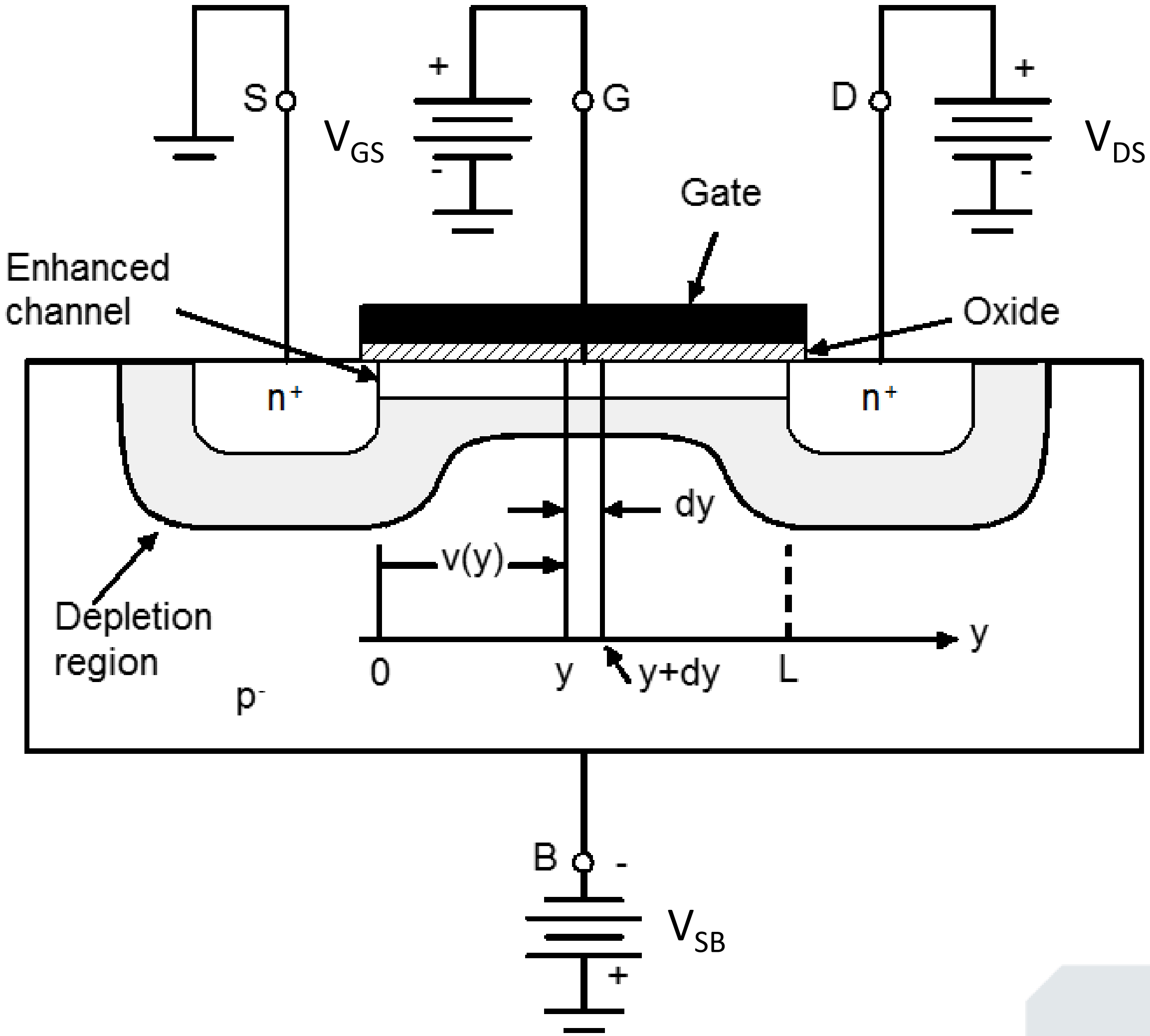
oxide charge

$$V_T = [\phi_{GB}] + \left[-2\phi_F - \frac{Q_b}{C_{ox}}\right] + \left[\frac{-Q_{ss}}{C_{ox}}\right]$$

$$= \phi_{GB} - 2\phi_F - \frac{Q_{b0}}{C_{ox}} - \frac{Q_{ss}}{C_{ox}} - \frac{Q_b - Q_{b0}}{C_{ox}}$$

Bias independent part:

$$V_{T0} = \phi_{GB} - 2\phi_F - \frac{Q_{b0}}{C_{ox}} - \frac{Q_{ss}}{C_{ox}}$$

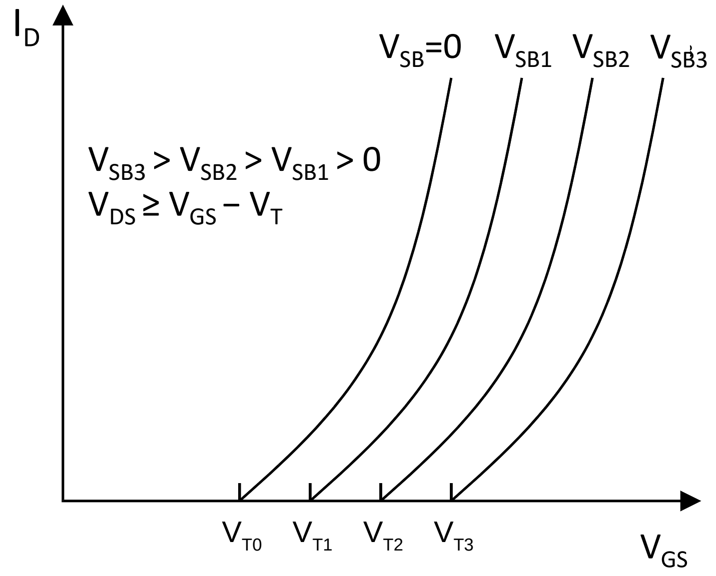


Threshold voltage

Source-bulk bias voltage dependence:

$$V_T = V_{T0} + \gamma\left(\sqrt{2|\phi_F| + V_{SB}} - \sqrt{2|\phi_F|}\right)$$

$$V_{T0} = V_T\left(V_{SB} = 0\right) = V_{FB} + 2|\phi_F| + \sqrt{\frac{2q\varepsilon_{si}N_{SUB}2|\phi_F|}{C_{OX}}}$$



$$\gamma = \text{bulk threshold parameter (volts}^{1/2}) = \frac{\sqrt{2\varepsilon_{si}qN_{SUB}}}{C_{OX}}$$

$$\phi_F = \text{strong inversion surface potential (volts)} = \frac{kT}{q}\ln\left(\frac{N_{SUB}}{n_i}\right)$$

$$V_{FB} = \text{flatband voltage (volts)} = \phi_{GB} - \frac{Q_{SS}}{Q_{OX}}$$

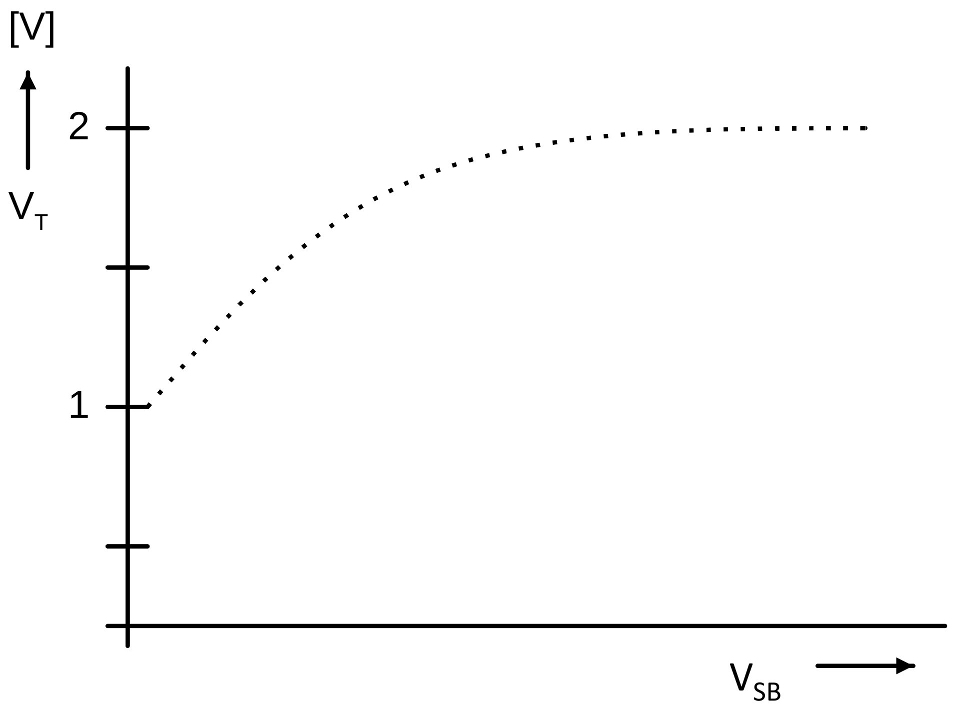
$$\phi_{GB} = \phi_F(\text{substrate}) - \phi_F(\text{gate})$$

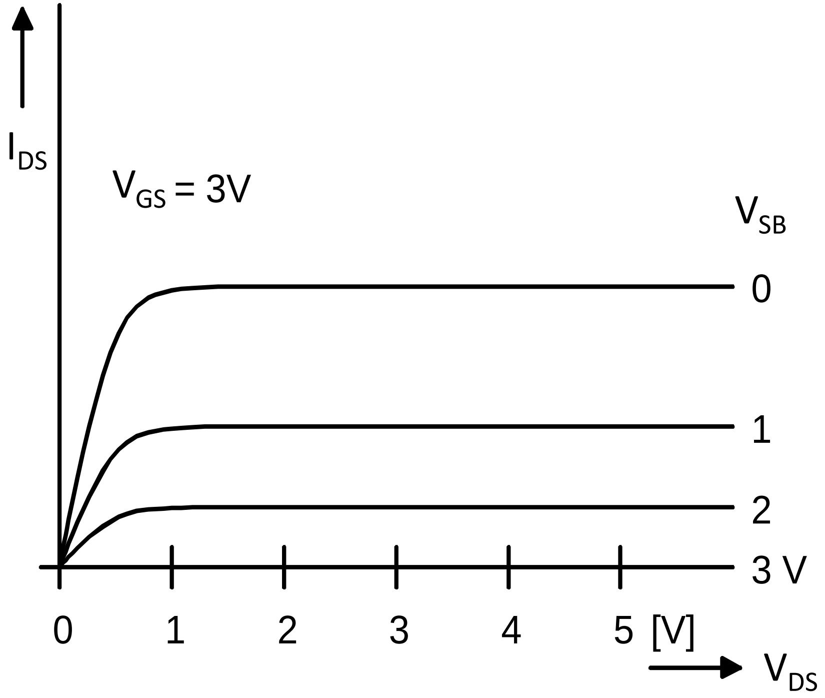
$$\phi_F(\text{substrate}) = \frac{kT}{q}\ln\left(\frac{n_i}{N_{SUB}}\right)[\text{NMOS with p - substrate}]$$

$$\phi_F(\text{gate}) = \frac{kT}{q}\ln\left(\frac{N_{GATE}}{n_i}\right)[\text{NMOS with } n^+ \text{ polysilicon gate}]$$

$$Q_{SS} = \text{oxide charge} = N_{SS}q$$

Back bias effects on MOS transistor





- Increases threshold voltage
- Decreases drain current

Derivation of drain current equation

The charge per unit area in the channel:

$$Q_1(y) = C_{OX}\left[V_{GS} - V(y) - V_T\right]$$

Resistance of the channel per unit of length:

$$dR = \frac{dy}{\mu_n Q_1(y) W} \qquad R = \frac{\rho l}{A} \quad \text{with and} \quad \rho = \frac{1}{\mu n q} \qquad A = Wz \quad , \quad nq = \frac{Q_1(y)}{z}$$

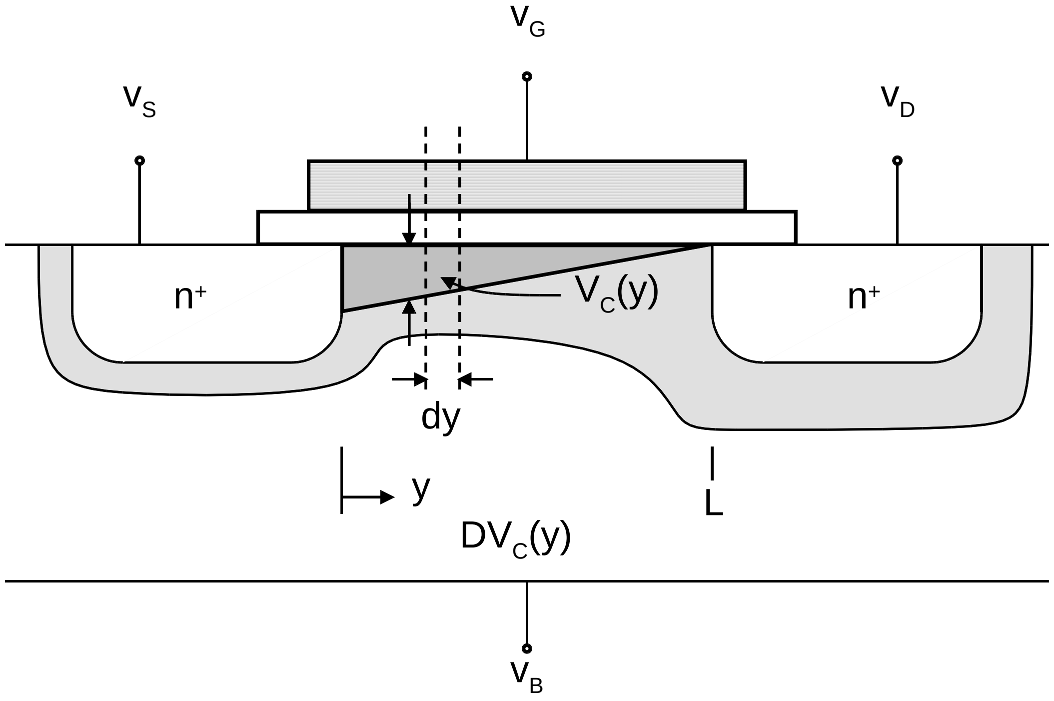
The voltage drop along the channel (y-direction):

$$dv(y) = I_D dR = \frac{I_D dy}{\mu_n Q_1(y) W} \Rightarrow I_D dy = W\mu_n Q_1(y) dv(y)$$

Integrate this from source to drain, i.e. y = 0 to y = L

$$\int_0^L I_D\, dy = \int_0^{V_{DS}} W\mu_n Q_1(y) dv(y) = \int_0^{V_{DS}} W\mu_n C_{OX}\left[V_{GS} - v(y) - V_T\right] dv(y)$$

$$\Rightarrow I_D = \frac{\mu_n C_{OX} W}{L} \Big|_0^{V_{DS}} (V_{GS} - V_T) v(y) - \frac{v(y)^2}{2}$$



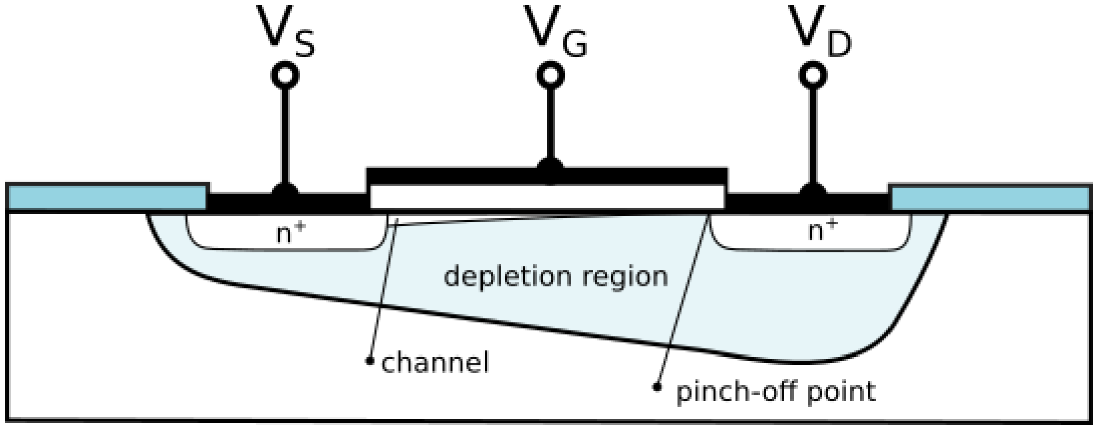
$$\Rightarrow \quad I_D = \frac{\mu_n C_{OX} W}{2L}\left[2(V_{GS} - V_T)V_{DS} - V_{DS}^2\right]$$

Pinch-off

In pinch-off inversion layer at drain end is lost due to higher V_{DS} over V_{GS}-V_T and drain current is saturated

$$I_D = \frac{\mu_o C_{ox} W}{L}\left[(V_{GS} - V_T) - \left(\frac{V_{DS}}{2}\right)\right] V_{DS}$$

$$0 < V_{DS} \leq (V_{GS} - V_T)$$



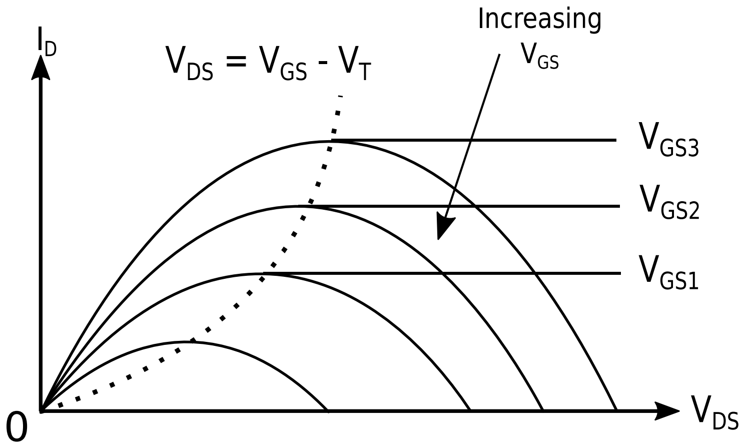
Saturation voltage

$$V_{DS,sat} = V_{GS} - V_T$$

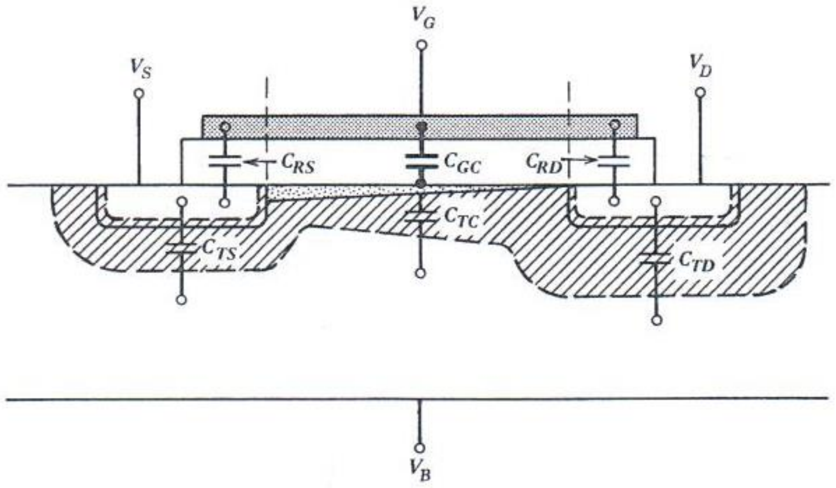
Saturation current

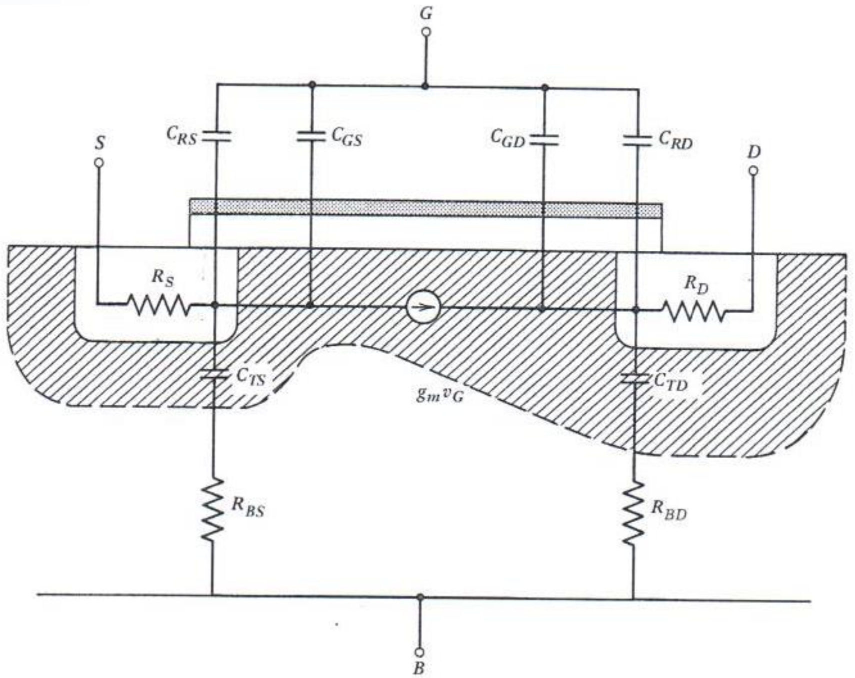
$$I_D = \frac{\mu_0 C_{ox} W}{2L}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

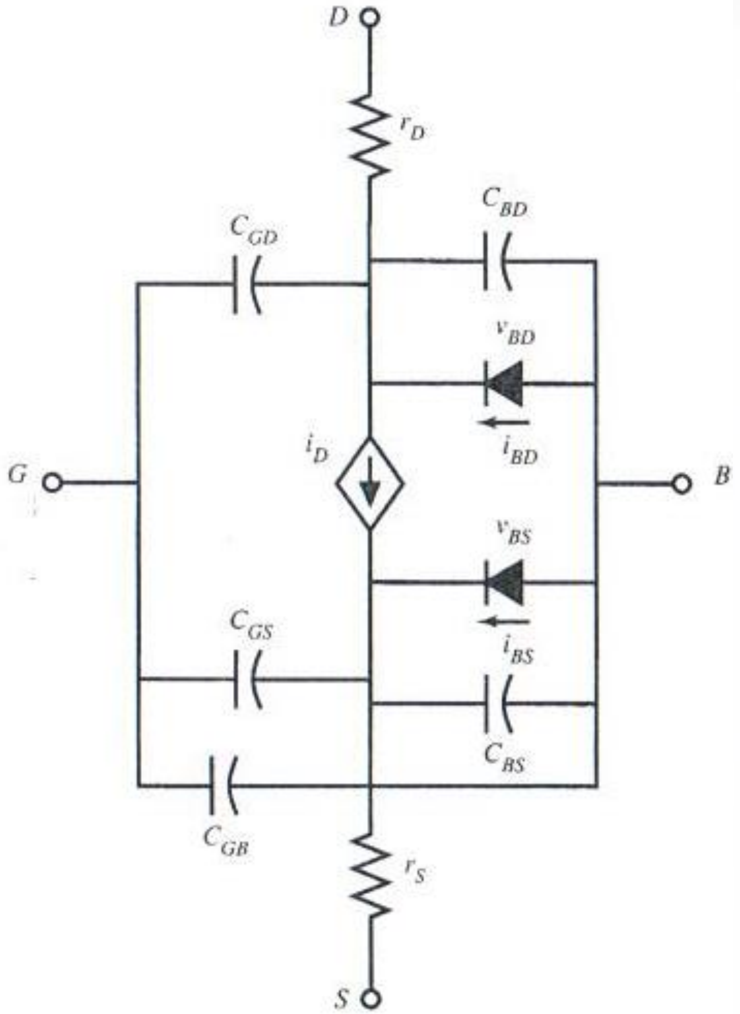
$$0 < (V_{GS} - V_T) \leq V_{DS}$$



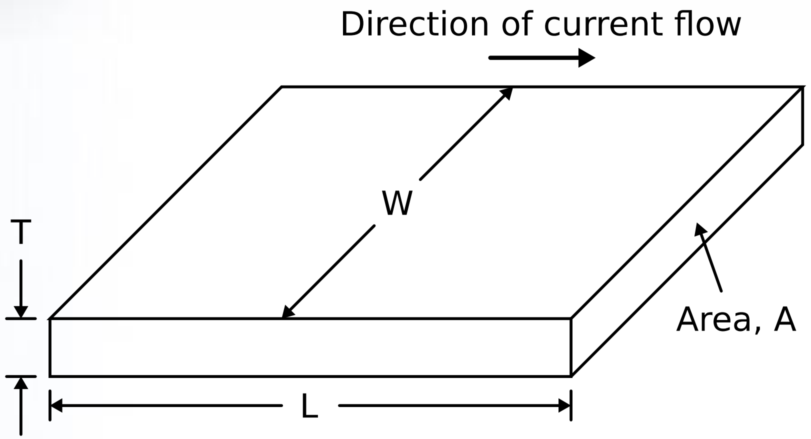
MOS Spice model (level 1)







Planar conductor resistance



Current flow in conductive bar

Resistance of a conductor

$$R = \frac{\rho L}{A} (\Omega) \quad ; \quad \rho = \frac{1}{q \mu_n n} \quad \text{resistivity}$$

Insert area A = WT

$$R = \frac{\rho L}{WT} (\Omega)$$

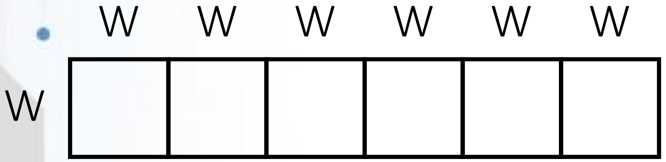
$$R = \frac{L}{W} R_{\square} \ (\Omega)$$

where resistance per square is

$$R_{\square} = \frac{\rho}{t}$$

L/W determines the number of squares

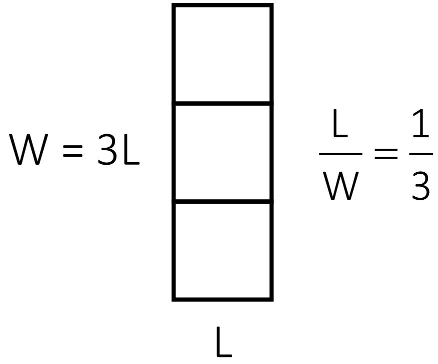
6 squares in series:



L = 6W

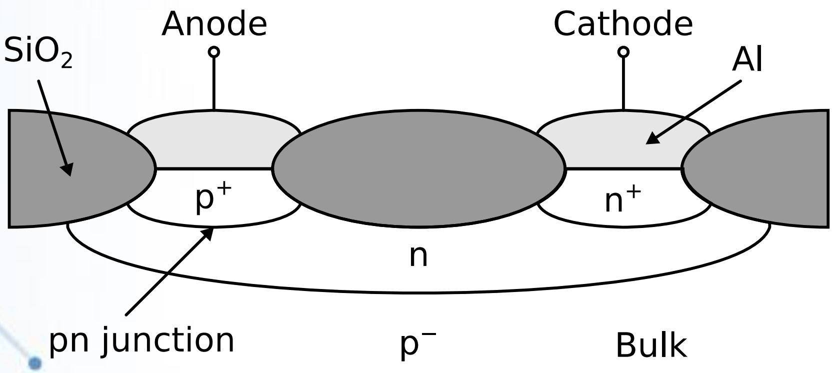
=> L/W = 6 squares

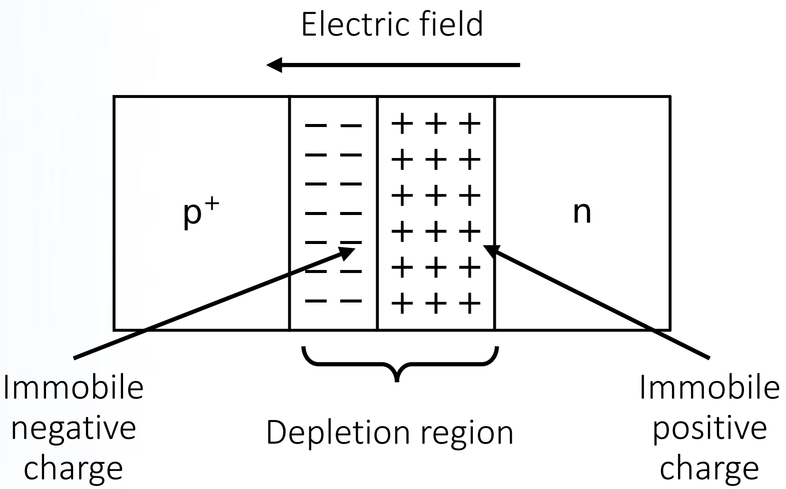
3 squares in parallel:



Capacitance of pn-diodes

Planar diode:





A simplified model of a diode

Capacitance of a reverse-biased diode (Abrupt Junction)

$$C_j = \frac{C_{j0}}{\sqrt{1 + \frac{V_R}{\Phi_0}}}$$; V_R = reverse bias voltage

, where C_{j0} is zero bias capacitance ($V_R = 0$)

$$C_{j0} = \sqrt{\frac{qK_s\varepsilon_0}{2\Phi_0}\frac{N_D N_A}{N_A + N_D}} \qquad C_{j0} = \sqrt{\frac{qK_s\varepsilon_0 N_D}{2\Phi_0}}$$, if $N_A >> N_D$

and Φ_0 is junction potential

$$\Phi_0 = \frac{kT}{q}\ln\left(\frac{N_A N_D}{n_j^2}\right)$$

Drain and source junction capacitances CDB, CSB

$$C_{BX} = C_{BX0} A_{BX} \left[1 - \left(\frac{v_{BX}}{PB} \right) \right]^{-MJ}, \quad v_{BX} \le (FC)(PB) \qquad (1)$$

A_{BX} = junction areas

$$C_{BX0} = C_{BX} \,(\text{when } v_{BX} = 0) \cong \sqrt{\frac{(q\varepsilon_{si} N_{SUB})}{PB}}$$

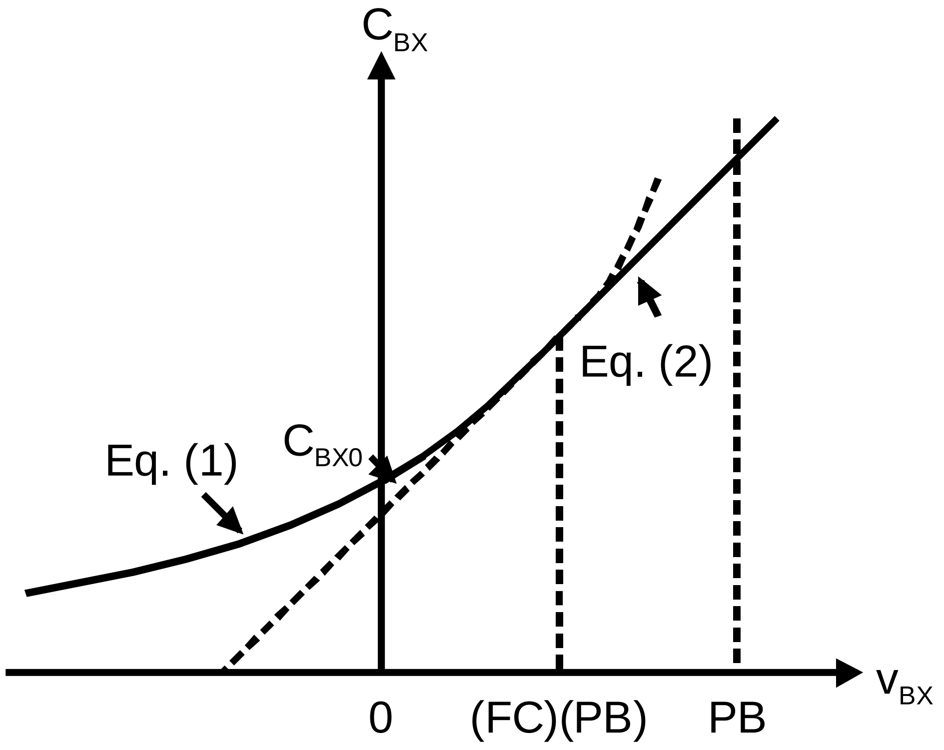
PB = bulk junction potential

FC = forward-bias nonideal junction-capacitance coefficient ($\cong 0.5$)

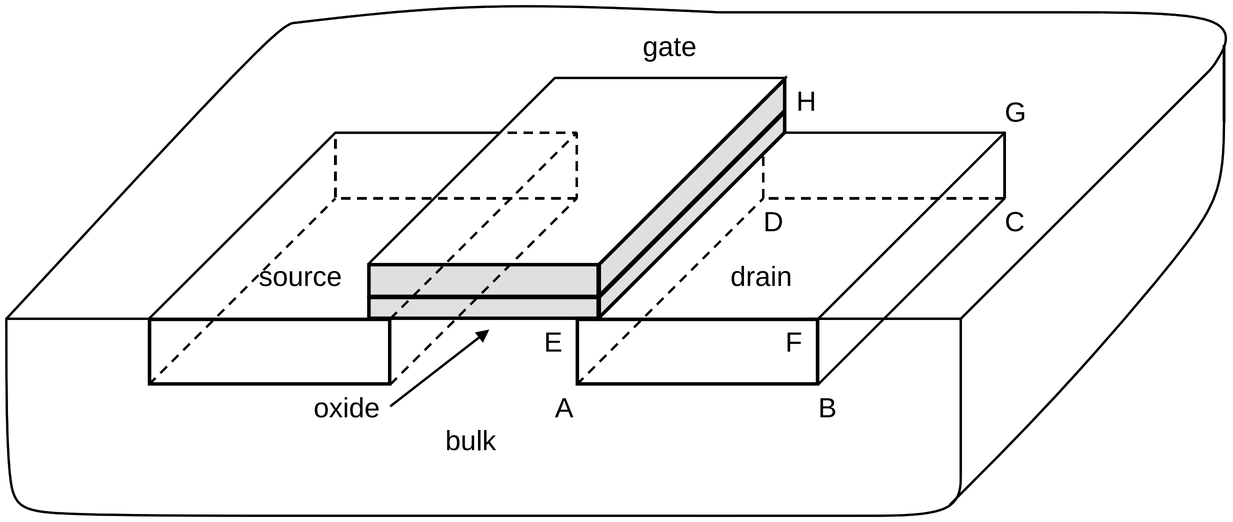
MJ = bulk-junction grading coefficient (½ for step junctions and $\frac{1}{3}$ for graded junctions)

To ease numerical solution of the simulator

$$C_{BX} = \frac{C_{BX0} A_{BX}}{(1 - FC)^{1+MJ}} \left[1 - (1 + MJ) FC + MJ \frac{v_{BX}}{PB} \right], \quad v_{BX} > (FC)(PB) \qquad (2)$$



Drain and source junction capacitances CDB, CSB



Drain bottom = ABCD

$$C_{BX} = \frac{(CJ)(AX)}{\left[1-\left(\frac{v_{BX}}{PB}\right)\right]^{MJ}} + \frac{(CJSW)(PX)}{\left[1-\left(\frac{v_{BX}}{PB}\right)\right]^{MJSW}}$$

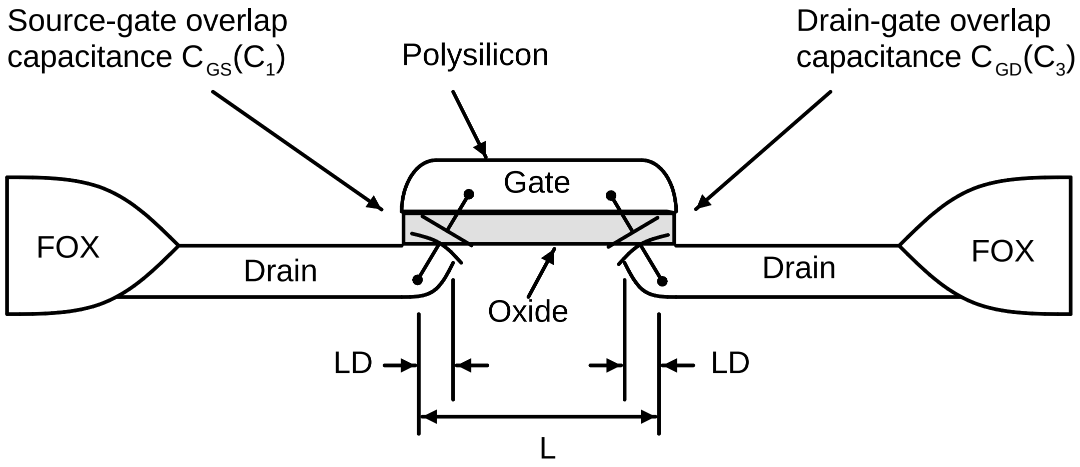
$$v_{BX} \le (FC)(PB)$$

$$C_{BX} = \frac{(CJ)(AX)}{(1-FC)^{1+MJ}}\left[1-(1+MJ)FC + MJ\frac{v_{BX}}{PB}\right] + \frac{(CJSW)(PX)}{(1-FC)^{1+MJSW}}\left[1-(1+JMSW)FC + \frac{v_{BX}}{PB}(MJSW)\right]$$

$$v_{BX} \ge (FC)(PB)$$

AX = area of the source (X = S) or drain (X = D)
PX = perimeter of the source (X = S) or drain (X = D)
CJSW = zero-bias, bulk-source/drain sidewall capacitance
MJSW = bulk-source/drain sidewall grading coefficient

MOS transistor gate capacitance

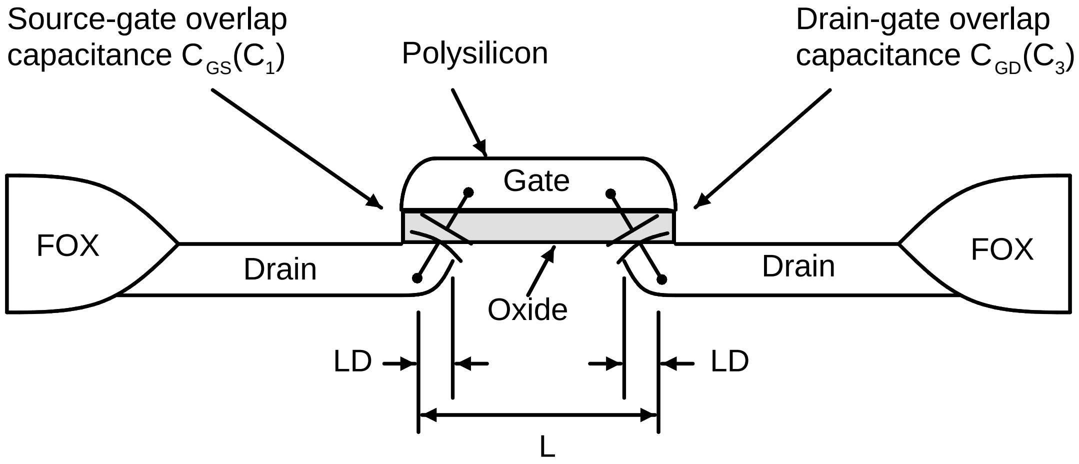


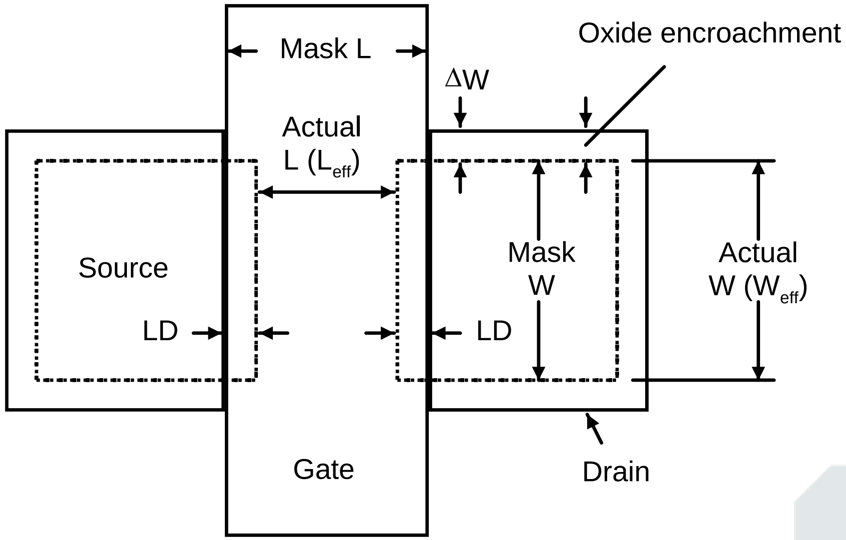
Gate capacitance (linear region)

$C_2 = W_{eff}\,(L - 2LD)\,C_{ox} = W_{eff}\,(L_{eff})C_{ox}$

Gate overlap capacitances

$C_1 = C_3 \cong LDW_{eff}C_{ox} = W_{eff}CGXO$; CGXO [F/m]= $LD \cdot C_{OX}$





MOS transistor gate capacitance

Cut-off

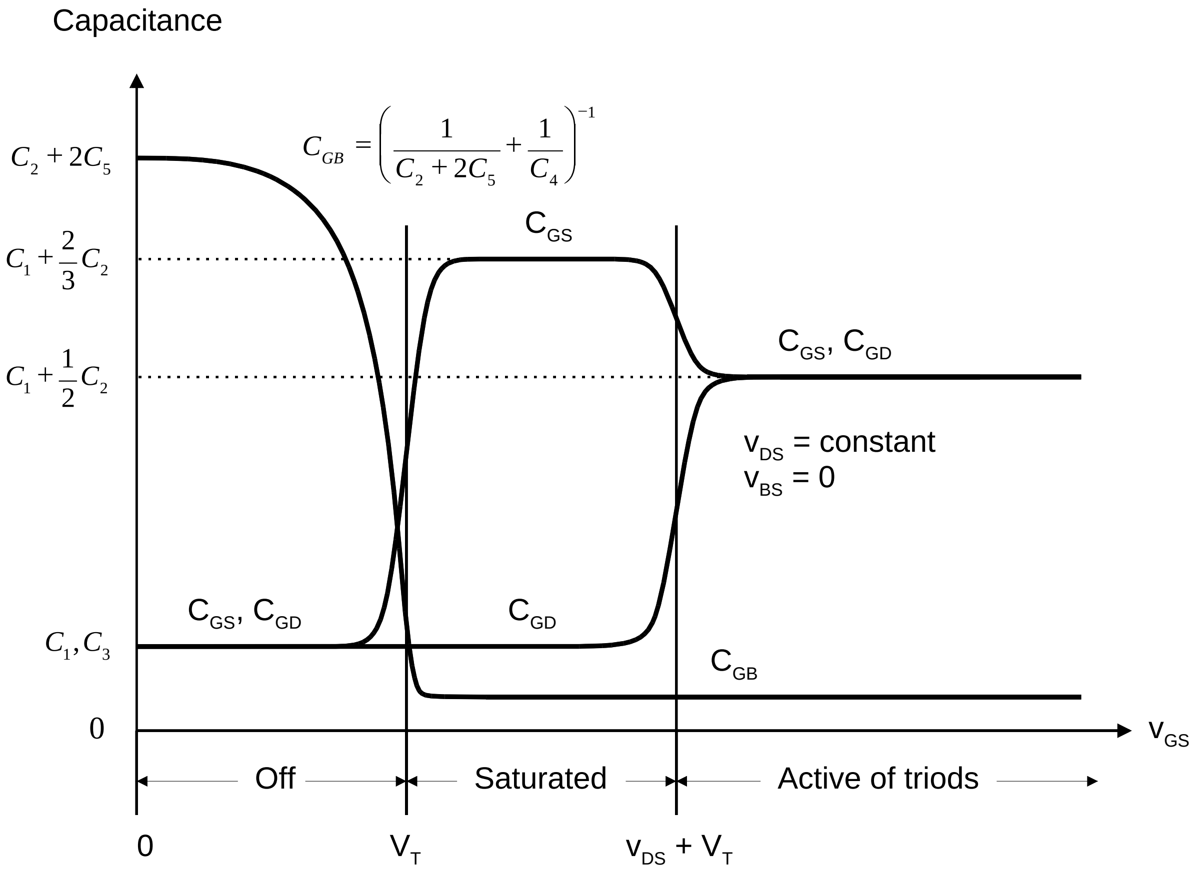
$$C_{GB} = C_2 + 2C_5 = C_{ox}(W_{eff}L_{eff}) + 2CGBO(L_{eff})$$
$$C_{GS} = C_1 \cong C_{ox}(LDW_{eff}) = CGSO(W_{eff})$$
$$C_{GD} = C_3 \cong C_{ox}(LDW_{eff}) = CGDO(W_{eff})$$

Saturation

$$C_{GB} = \frac{(C_2 + 2C_5)C_4}{C_2 + 2C_5 + C_4} \cong C_4 \cong 0$$
$$C_{GS} = C_1 + \frac{2}{3}C_2 = C_{ox}(LD + 0{,}67L_{eff})(W_{eff})$$
$$= CGSO(W_{eff}) + 0{,}67C_{ox}(W_{eff}L_{eff})$$
$$C_{GD} = C_3 \cong C_{ox}(LDW_{eff}) = CGDO(W_{eff})$$

Nonsaturated

$$C_{GB} = \frac{(C_2 + 2C_5)C_4}{C_2 + 2C_5 + C_4} \cong C_4 \cong 0$$
$$C_{GS} = C_1 + \frac{1}{2}C_2 = C_{ox}(LD + 0{,}5L_{eff})(W_{eff})$$
$$= (CGSO + 0{,}5C_{ox}L_{eff})W_{eff}$$
$$C_{GD} = C_3 + 0{,}5C_2 = C_{ox}(LD + 0{,}5L_{eff})(W_{eff})$$
$$= (CGDO + 0{,}5C_{ox}L_{eff})W_{eff}$$



Charge conservation model and short channel effects

Charge conservation model

Charge conservation model (level 2):

$$dV_C = I_d dR = \frac{I_d dy}{W\mu_n Q_n'(y)}$$

Channel change: $Q_n' = -C_{OX}'(V_G - V_T)$

Threshold voltage: $V_T = f(V_C)$

$$V_T = V_{FB} + V_C + 2|\phi_p| + \frac{1}{C_{OX}'}\sqrt{2\varepsilon_s q N_a (2|\phi_p| + V_C - V_B)}$$

Channel change: $Q_n' = f(V_C)$

$$Q_n' = -C_{OX}'(V_G - V_{FB} - 2|\phi_p| - V_C) + \sqrt{2\varepsilon_s q N_a (2|\phi_p| + V_C - V_B)}$$

Integrating:

$$dV_C = I_d dR = \frac{I_d dy}{W\mu_n Q_n'(y)}$$

$$I_D = \int_0^L dy = I_D L = -\mu W \int_{V_S}^{V_D} Q_n'(V_C) dV_C$$

Drain current equation:

$$I_D = \mu_n \frac{W}{L} C_{OX}' \Big\{ C_{OX}' \Big[V_G - V_{FB} - 2|\phi_p| - \frac{1}{2}V_D - \frac{1}{2}V_S \Big](V_D - V_S) - \frac{2}{3}\sqrt{2\varepsilon_s q N_a}\Big[(2|\phi_p| + V_D - V_B)^{\frac{2}{3}} - (2|\phi_p| + V_S - V_B)^{\frac{2}{3}} \Big]\Big\}$$

Pinch-off:

$$Q_n'(L) = 0 = -C_{OX}'(V_G - V_{FB} - 2|\phi_p| - V_{Dsat}) + \sqrt{2\varepsilon_s q N_a (2|\phi_s| + V_{Dsat} - V_B)}$$

Saturation voltage:

$$V_{Dsat} = V_G - V_{FB} - 2|\phi_p| - \frac{\varepsilon_s q N_a}{C_{OX}'^2}\left[\sqrt{1 + \frac{2C_{OX}'^2}{\varepsilon_s q N}(V_G - V_{FB} - V_B)} - 1\right]$$

Channel length modulation

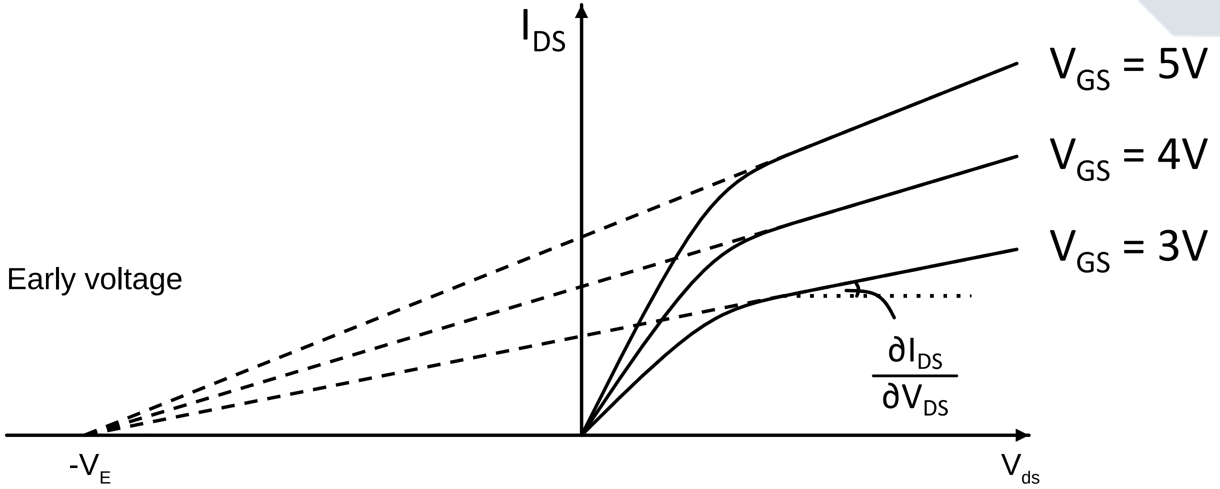
Basic model

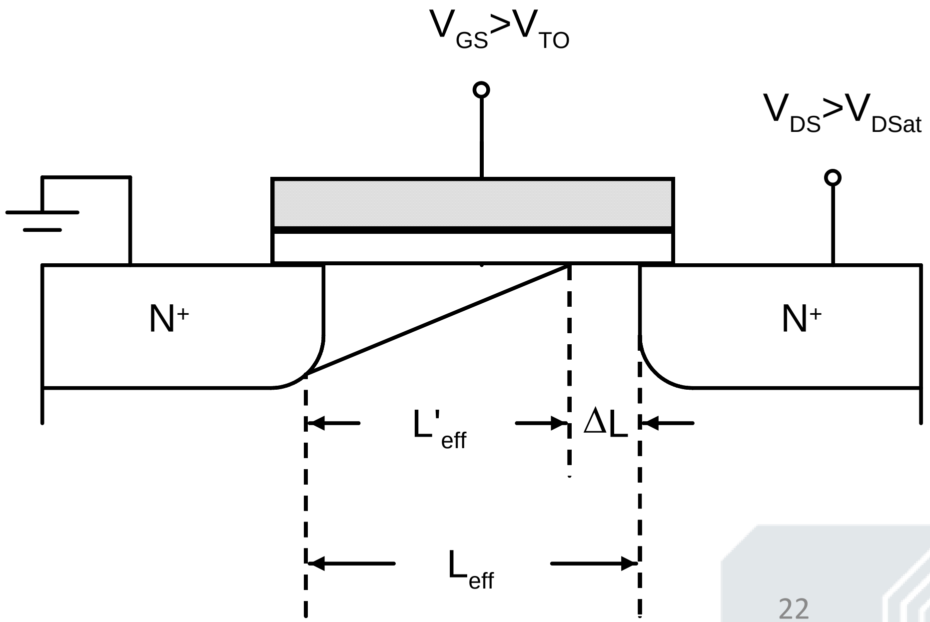
$$L_{mod} = L_{eff}\left(1 - \lambda v_{DS}\right) \qquad L_{eff} = L - 2(LD)$$

More accurate charge conservation model

$$\lambda = \frac{1}{L_{eff} v_{DS}}\left[\frac{2\varepsilon_{si}}{qN_{SUB}}\right]^{\frac{1}{2}}\left\{\frac{v_{DS} - v_{DS}(sat.)}{4} + \left[1 + \left(\frac{v_{DS} - v_{DS}(sat.)}{4}\right)^2\right]^{\frac{1}{2}}\right\}$$

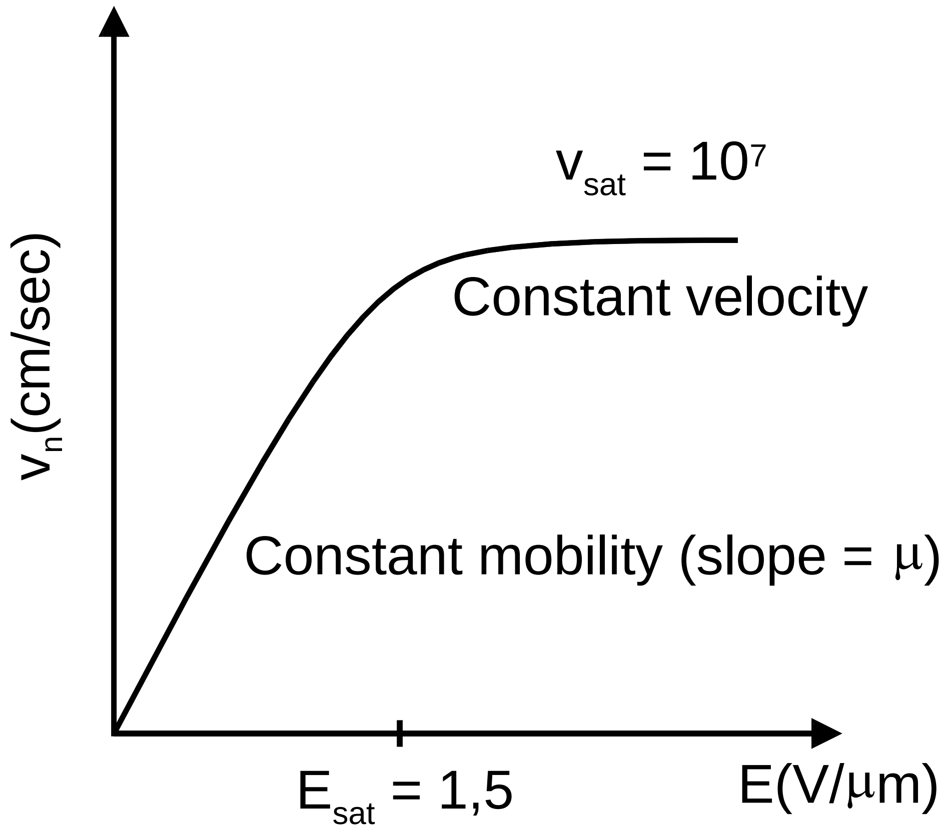
$$v_{DS}(sat.) = \frac{v_{GS} - V_{BIN}}{\theta} + \frac{1}{2}\left(\frac{\gamma s}{\theta}\right)^2\left\{1 - \left[1 + \left(\frac{2\theta}{\gamma s}\right)^2\left(\frac{v_{GS} - V_{BIN}}{\theta} + 2\left|\phi_F\right| + v_{SB}\right)\right]^{\frac{1}{2}}\right\}$$



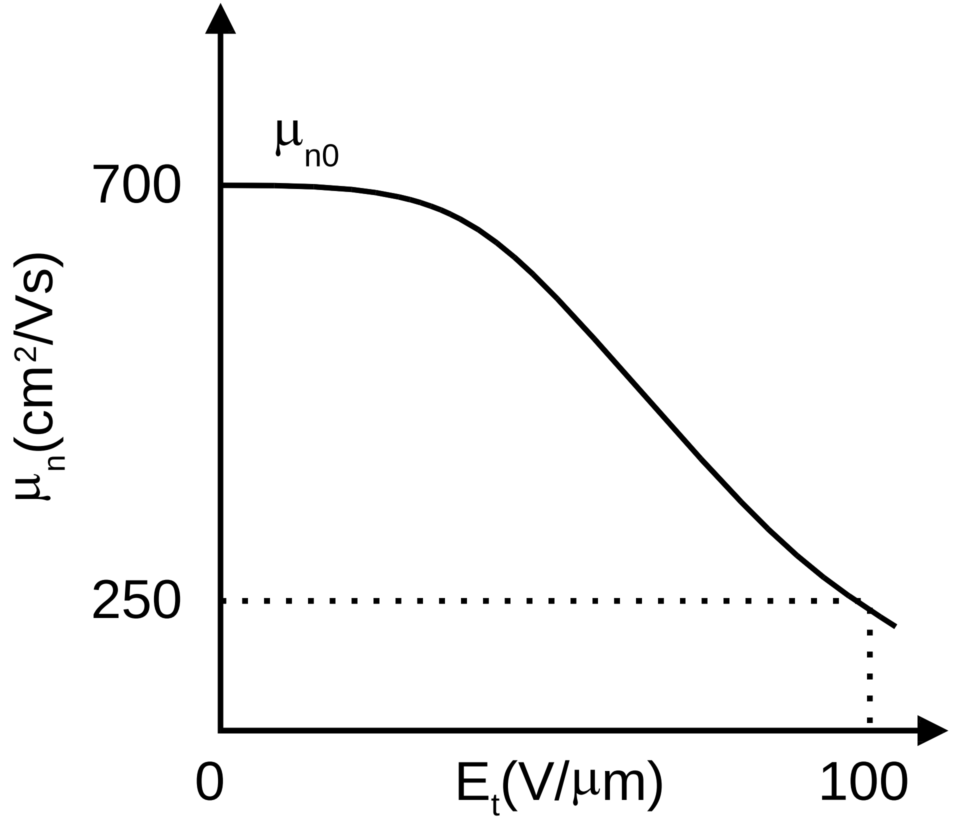


Charge carrier velocity saturation

Charge carrier velocity (NMOS):



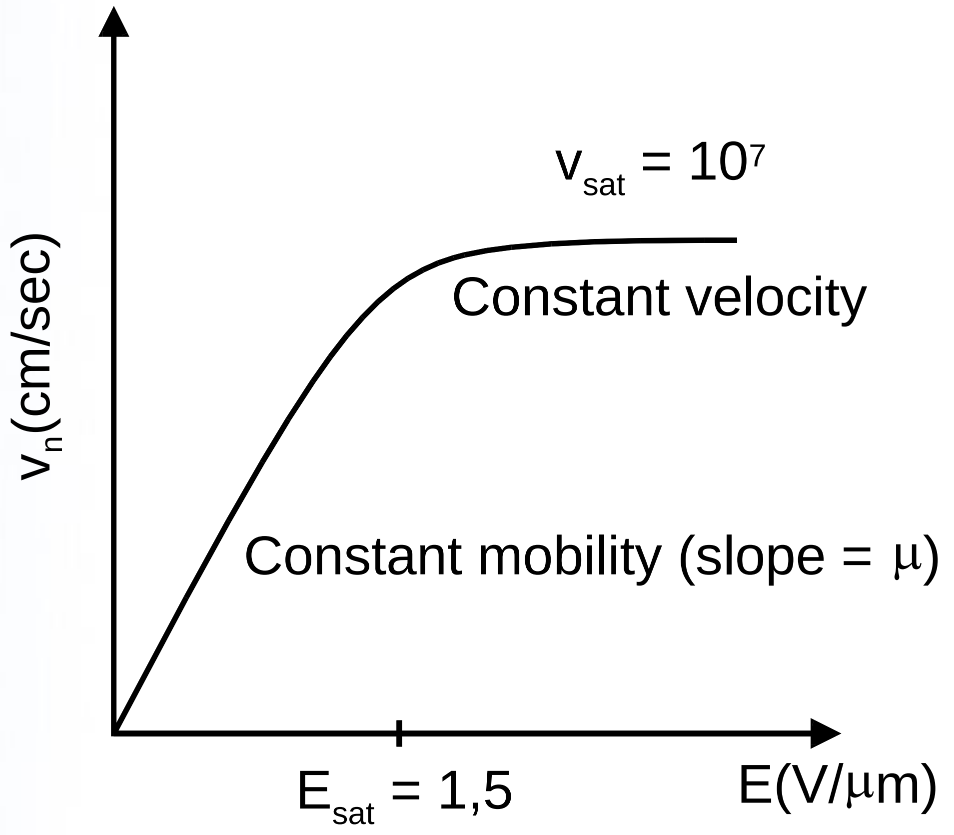
Charge carrier mobility (NMOS):



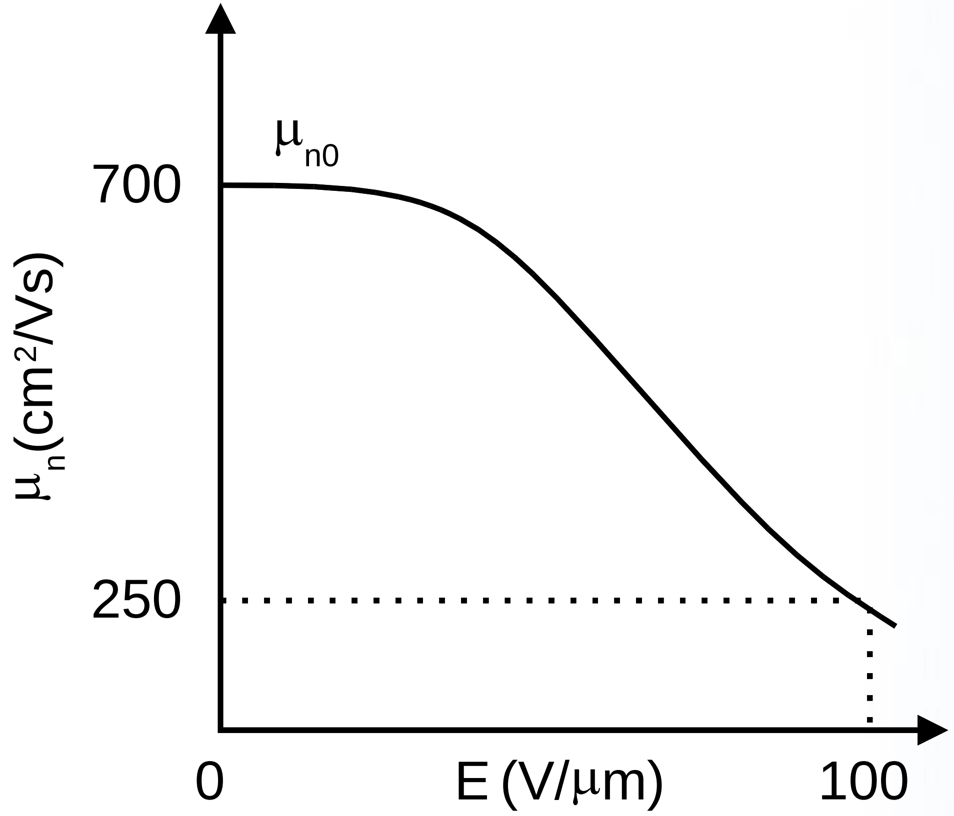
Electric field

Charge carrier velocity saturation

Charge carrier velocity (NMOS):



Charge carrier mobility (NMOS):



Electric field

Charge carrier velocity saturation

I: No velocity saturation $|\bar{E}| < E_{crit}$

$\mu_s = \mu_0$

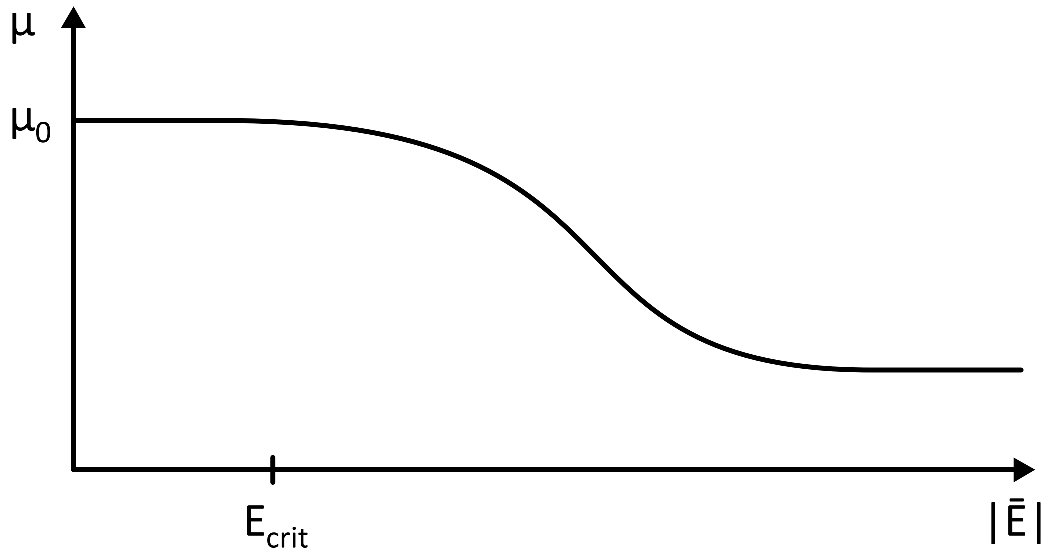
conditions

1) V_{DS} small
2) strong inversion $V_{GS} > V_T$
3) $|\bar{E}| < E_{crit}$

II: With velocity saturation $|\bar{E}| > E_{crit}$

$$\mu_s = \mu_0 \left[\frac{(U_{CRIT}) E_{si}}{C_{ox}\left[V_{GS} - V_T - (U_{TRA}) V_{DS}\right]} \right]^{U_{EXP}} \text{ when}$$

$$\frac{(U_{CRIT}) E_{si}}{C_{ox}} < V_{GS} - V_T - (U_{TRA}) V_{DS}$$



The parameters are defined as

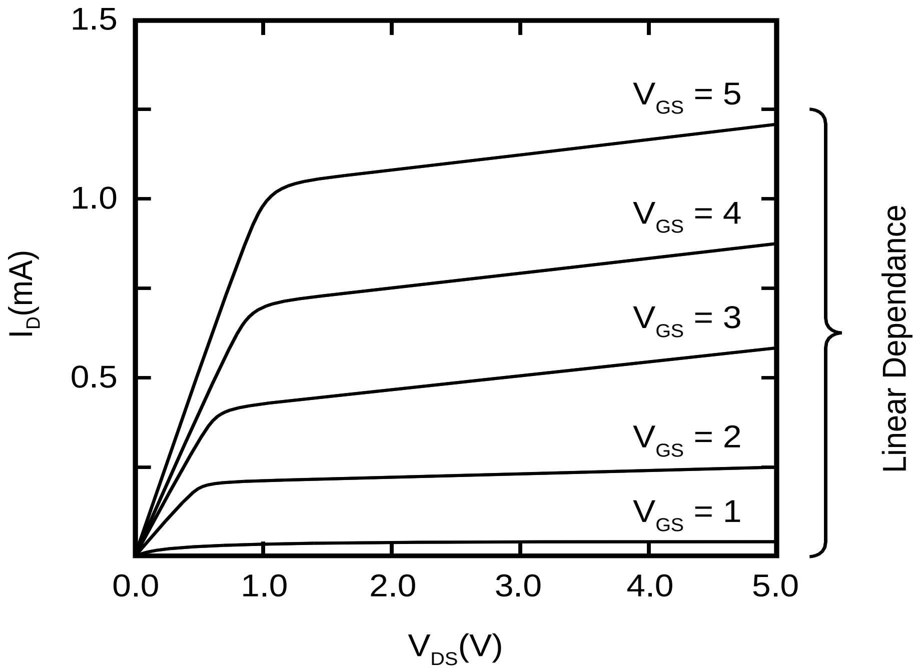
U_{CRIT} = critical field for mobility degradation and is the limit at which m_s starts decreasing.

U_{TRA} = transverse field coefficient effecting mobility.

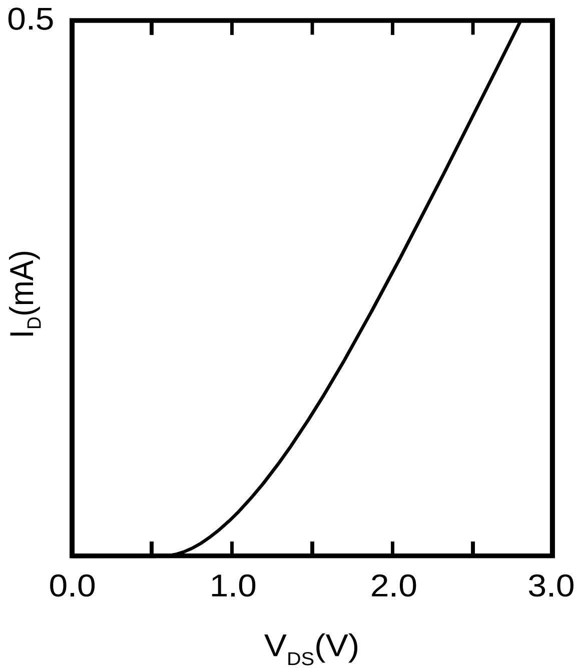
U_{EXP} = critical field exponent for mobility degradation.

Charge carrier velocity saturation

I_D as a function of V_{DS}

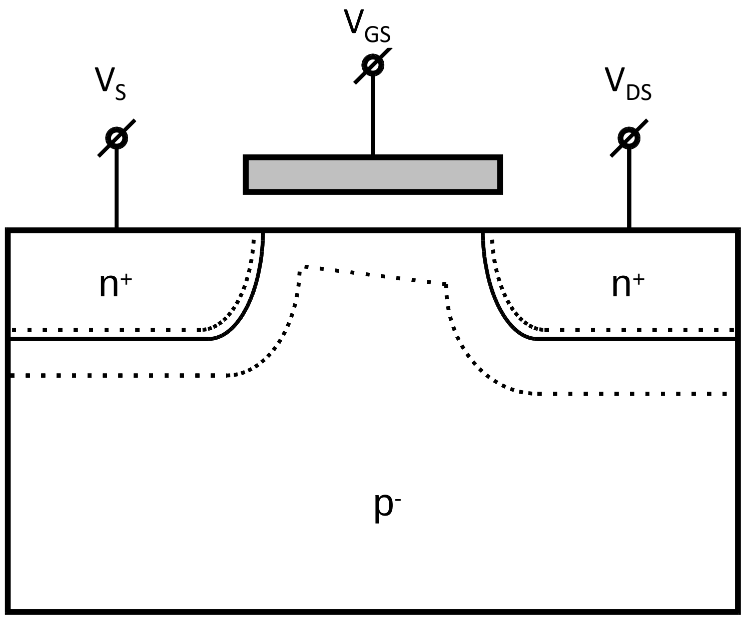


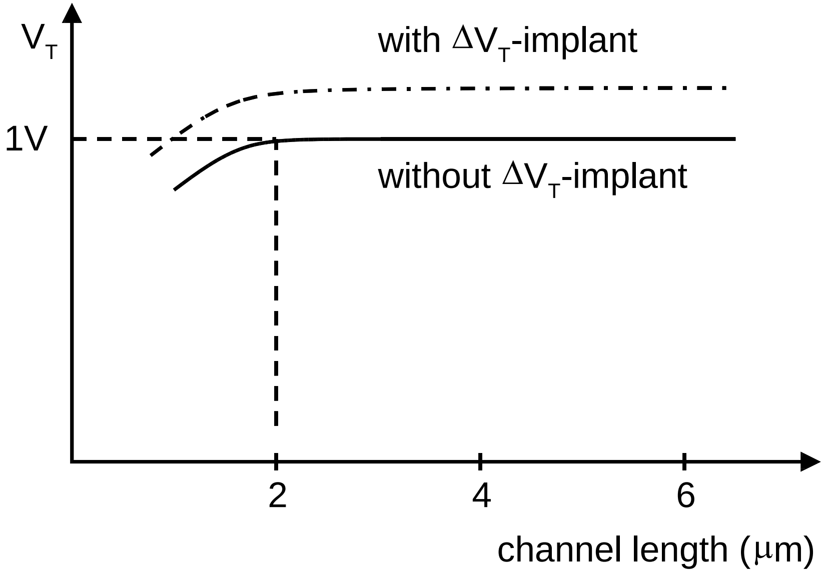
I_D as a function of V_{GS} (for V_{DS} = 5V)



Linear Dependence on V_{GS} in saturation

Short channel effects





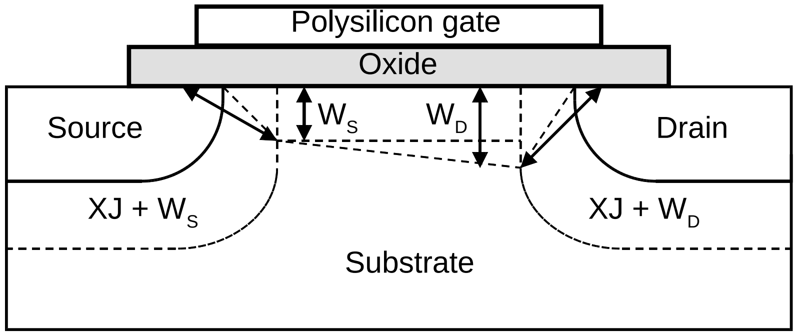
Cross section of a short channel transistor showing several depletion areas which affect each other.

Short channel effect on the threshold voltage V_T of an nMOS transistor with and without a DV_T implantation.

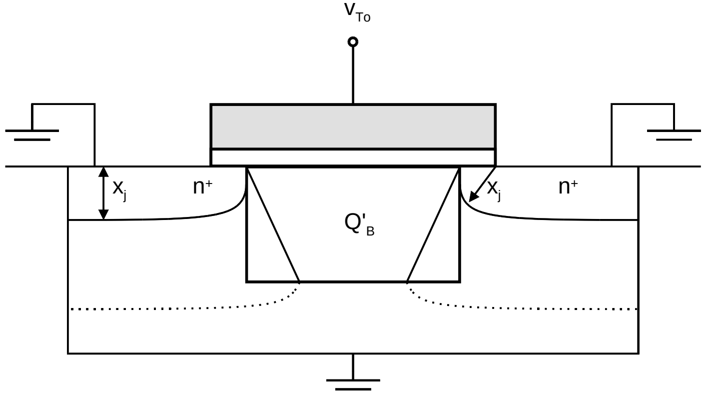
Short channel effects

$$W_S = \sqrt{\frac{2\varepsilon_{si}}{qN_{SUB}}}\sqrt{2|\phi_F| + v_{SB}}$$

$$W_D = \sqrt{\frac{2\varepsilon_{si}}{qN_{SUB}}}\sqrt{2|\phi_F| + v_{SB} + v_{DS}}$$



$$i_D = \frac{\mu_s C_{ox} W}{L_{mod}}\left\{\left[v_{GS} - V_{BIN} - \frac{\theta v_{DS}}{2}\right]v_{DS} - \frac{2}{3}\gamma s\left[\left(2|\phi_F| + v_{DS} + v_{SB}\right)^{1,5} - \left(2|\phi_F| + v_{BS}\right)^{1,5}\right]\right\}$$



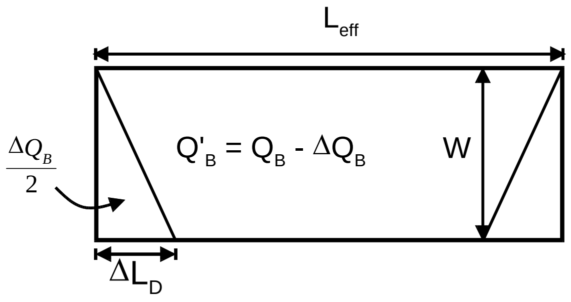
$$V_{BIN} = V_{FB} + 2|\phi_F| + \frac{\pi\varepsilon_{si}}{4C_{ox}W}\left(2|\phi_F| + v_{SB}\right)$$

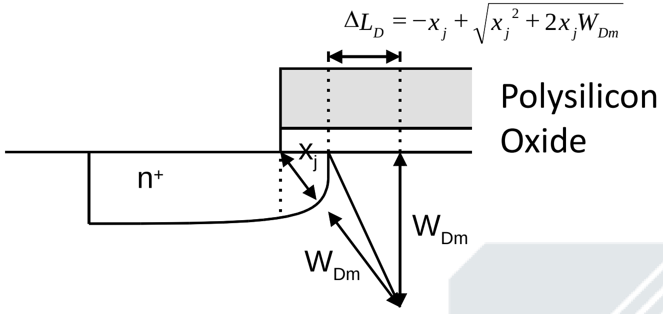
$$\theta = 1 + \frac{\pi\varepsilon_{si}}{4C_{ox}W}$$

$$\gamma_s = \gamma\left(1 - \alpha_S - \alpha_D\right)$$

$$\alpha_S = \frac{XJ}{2L}\left[\sqrt{1 + \left(\frac{2W_S}{XJ}\right)} - 1\right]$$

$$\alpha_D = \frac{XJ}{2L}\left[\sqrt{1 + \left(\frac{2W_D}{XJ}\right)} - 1\right]$$





Weak inversion behaviour

MOS transistor operates in the *'weak inversion'* region when its gate-source voltage (V_{GS}) is just below its threshold voltage (V_T).

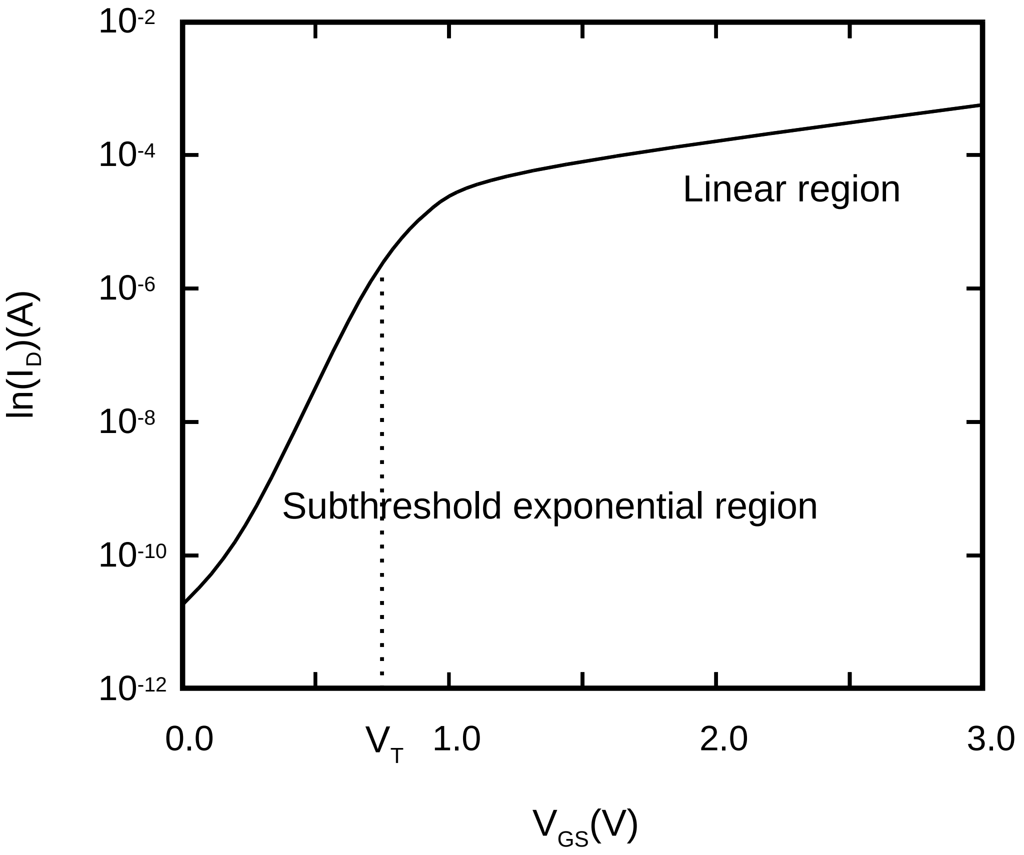
$$I_{Dsub} = \frac{W}{L} \cdot C I_D e^{\frac{V_{GB}}{mU_T}}$$

$$C = e^{\frac{-V_{SB}}{U_T}} - e^{\frac{-V_{DB}}{U_T}} \quad \text{(C is constant here)}$$

$$U_T = \frac{kT}{q} \approx 25\text{mV} \text{ at room temperature}$$

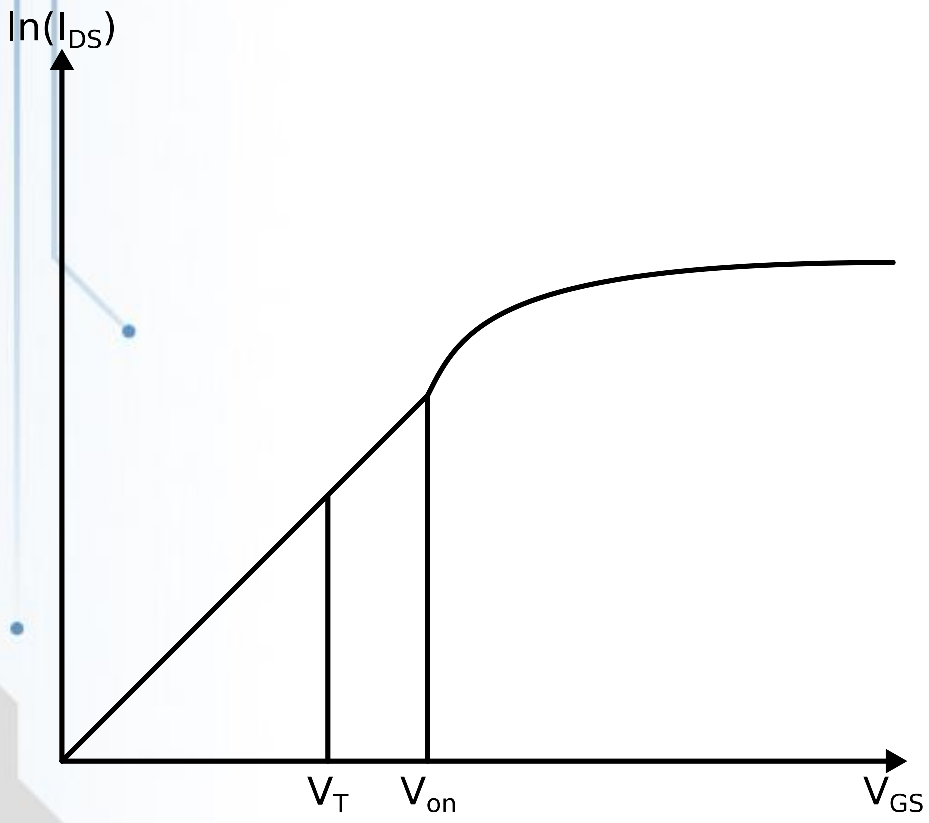
$$I_{DS0} = \text{characteristic current at } V_{GB} = 0\text{V}$$

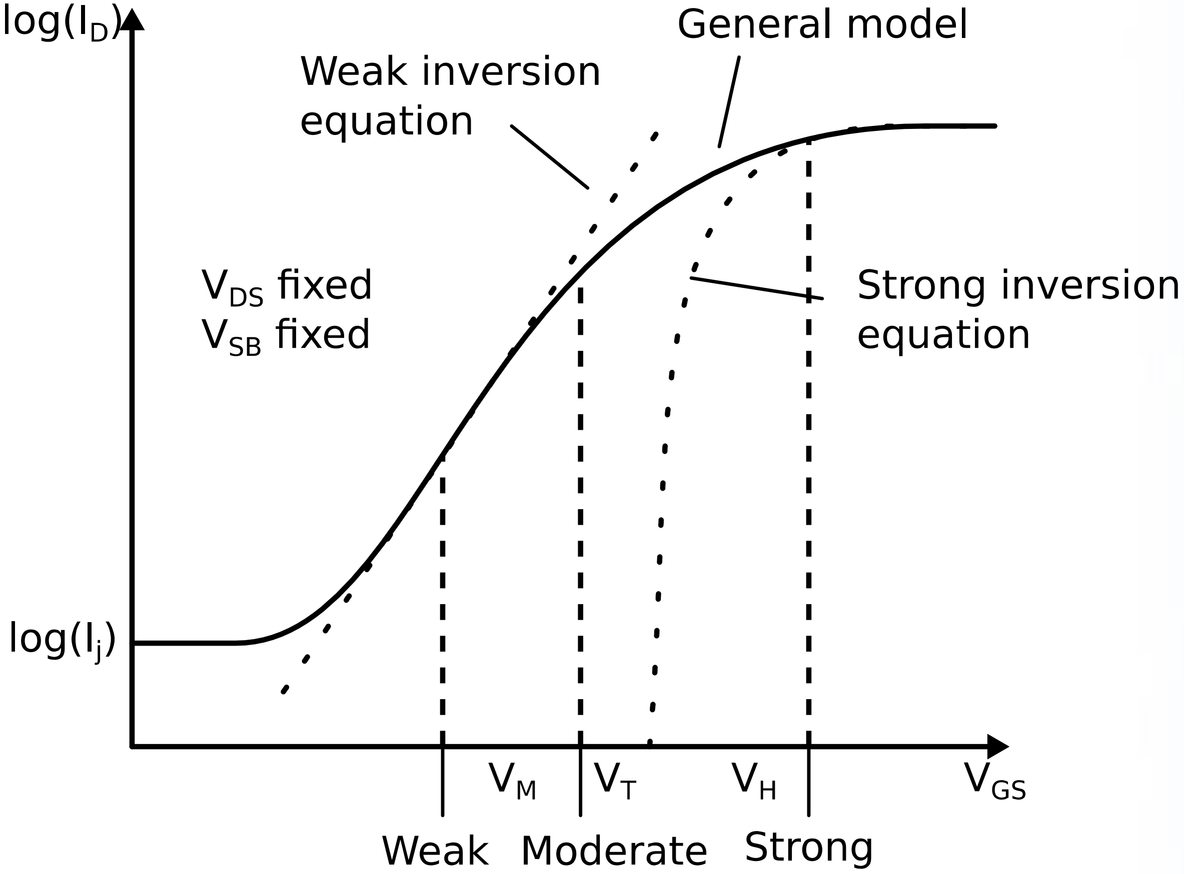
$$m = \text{slope} \approx 1{,}5$$



If V_T is low (< 0,6V) then there is always a sub-threshold current when V_{GS} = 0V. There is a considerable stand-by current.

Matching of weak and strong inversion models





Spice transistor parameters

Parameter name	Symbol	SPICE Name	Units	Default Value
Drawn Length	L	L	m	-
Effective width	W	W	m	-
Source Area	AREA	AS	m^2	0
Drain Area	AREA	AD	m^2	0
Source Perimeter	PERIM	PS	m	0
Drain Perimeter	PERIM	PD	m	0
Squares of Source Diffusion		NRS	-	1
Squares of Drain Diffusion		NRD	-	1

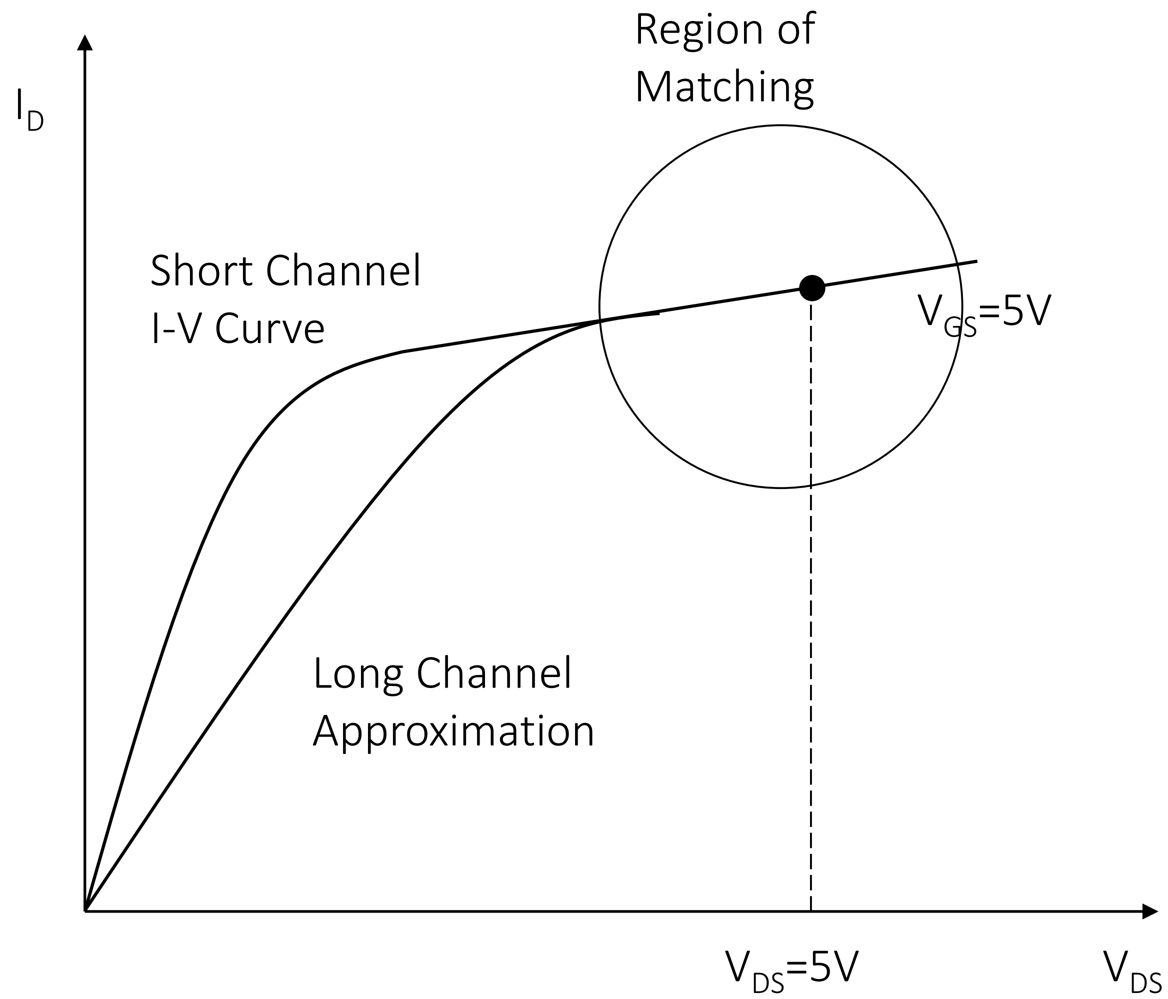
Spice parameters for parasitics

Parameter name	Symbol	SPICE Name	Units	Default Value
Source resistance	R_S	RS	Ω	0
Drain resistance	R_D	RD	Ω	0
Sheet resistance (Source/Drain)	$R_{\square}$	RSH	Ω/☐	0
Zero Bias Bulk Junction Cap	R_{J0}	CJ	F/m^2	0
Bulk Junction Grading Coeff.	m	MJ	-	0.5
Zero Bias Side Wall Junction Cap	C_{JSW0}	CJSW	F/m	0
Side Wall Grading Coeff.	m_{SW}	MJSW	-	0.3
Gate-Bulk Overlap Capacitance	C_{GBO}	CGBO	F/m	0
Gate-Source Overlap Capacitance	C_{GSO}	CGSO	F/m	0
Gate-Drain Overlap Capacitance	C_{GDO}	CGDO	F/m	0
Bulk Junction Leakage Current	I_S	IS	A	0
Bulk Junction Leakage Current Density	J_S	JS	A/m^2	1E-8
Bulk Junction Potential	ϕ_0	PB	V	0.8

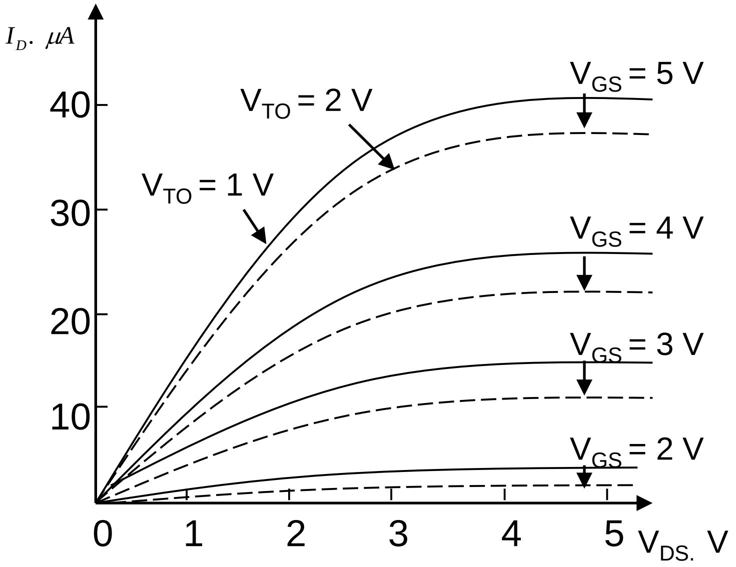
Main MOS Spice parameters

Parameter name	Symbol	SPICE Name	Units	Default Value
SPICE Model Index		LEVEL	-	1
Zero-Bias Threshold Voltage	VT0	VT0	V	0
Process Transconductance	k’	KP	A/V^2	2.E-5
Body-Bias Parameter	g	GAMMA	V0.5	0
Channel Modulation	l	LAMBDA	1/V	0
Oxide thickness	tox	TOX	m	0
Lateral Diffusion	xd	LD	m	0
Metallurgical Junction Depth	xj	XJ	m	0
Surface Inversion Potential	2|fF|	PHI	V	0.6
Substrate Doping	NA, ND	NSUB	cm^{-3}	0
Surface State Density	$Q_{ss/q}$	NSS	cm^{-3}	0
Fast Surface State Density		NFS	cm^{-3}	0
Total Channel Charge Coefficient		NEFF	-	1
Type of Gate Material		TPG	-	1
Surface Mobility	m0	U0	cm^2/Vs	600
Maximum Drift Velocity	umax	VMAX	m/s	0
Mobility Critical Field	xcrit	UCRIT	V/cm	1.0E-4
Critical Field Exponent in Mobility Degradation		UEXP	-	0
Transverse Field Exponent (mobility)		UTRA	-	0

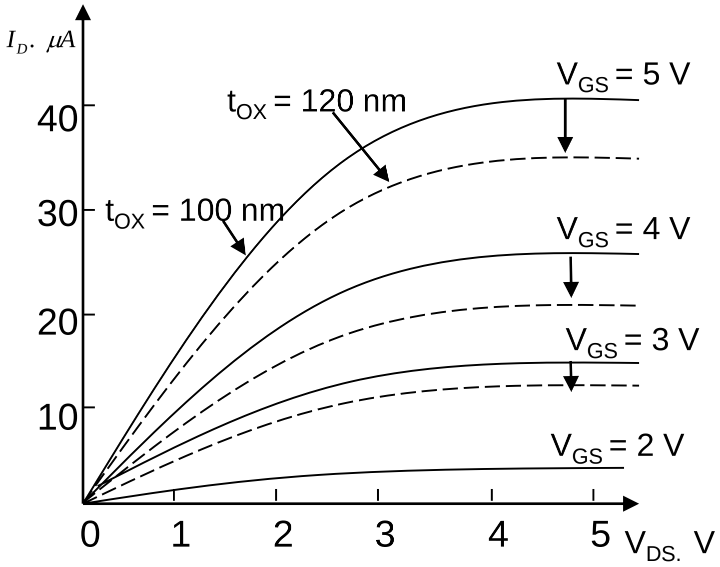
Matching manual and Spice models



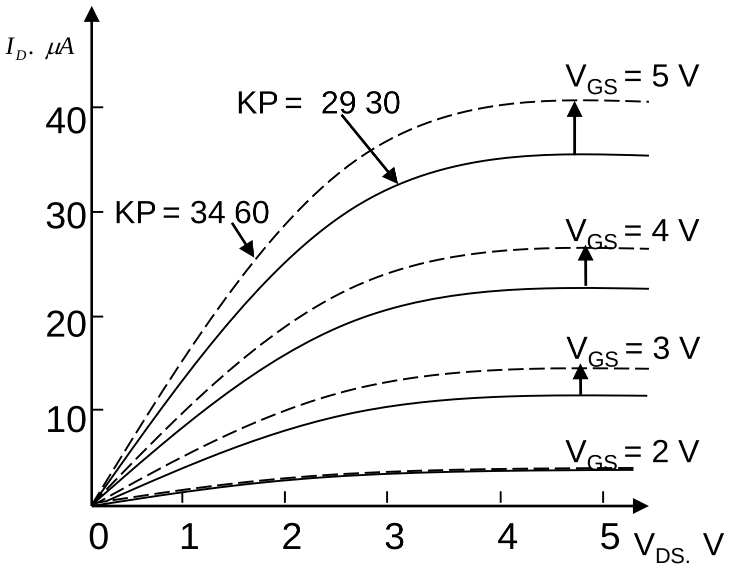
MOS transistor model characteristics



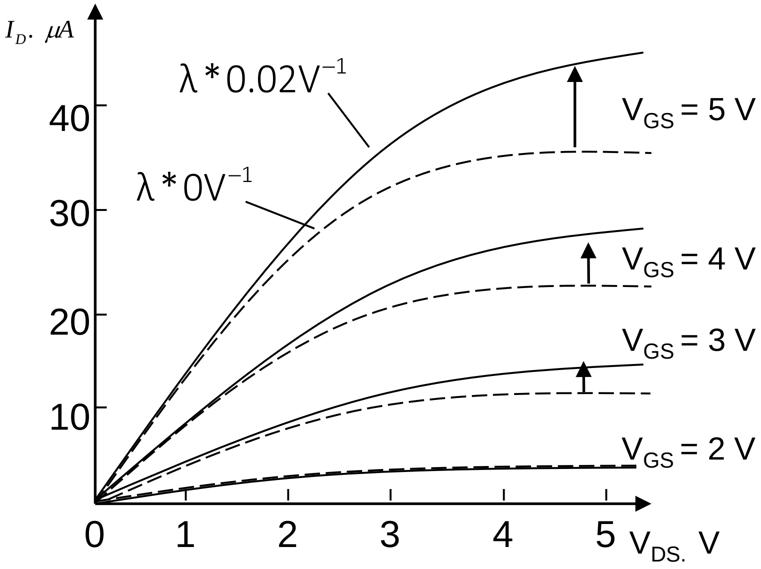
Variation of the drain current with model parameter VTO, for the LEVEL1 model.



Variation of the drain current with model parameter TOX, for the LEVEL1 model.

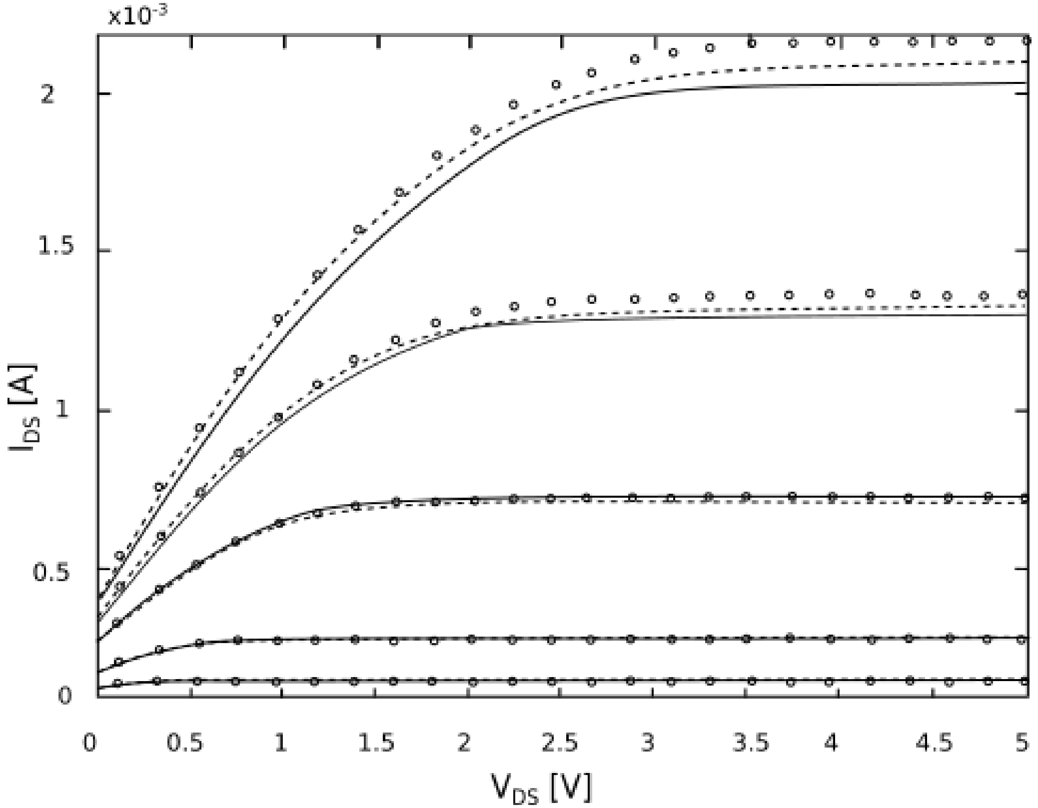


Variation of the drain current with model parameter KP, for the LEVEL1 model.

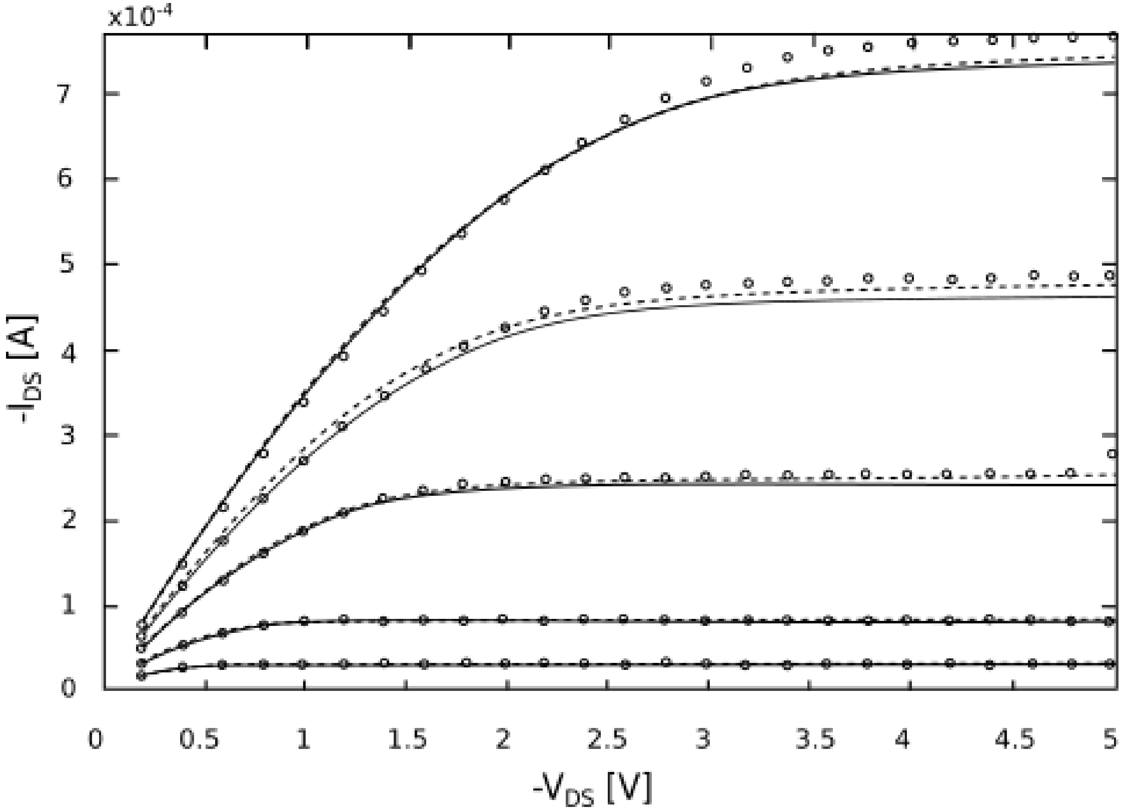


Variation of the drain current with model parameter LAMBDA, for the LEVEL1 model.

MOS transistor characteristics

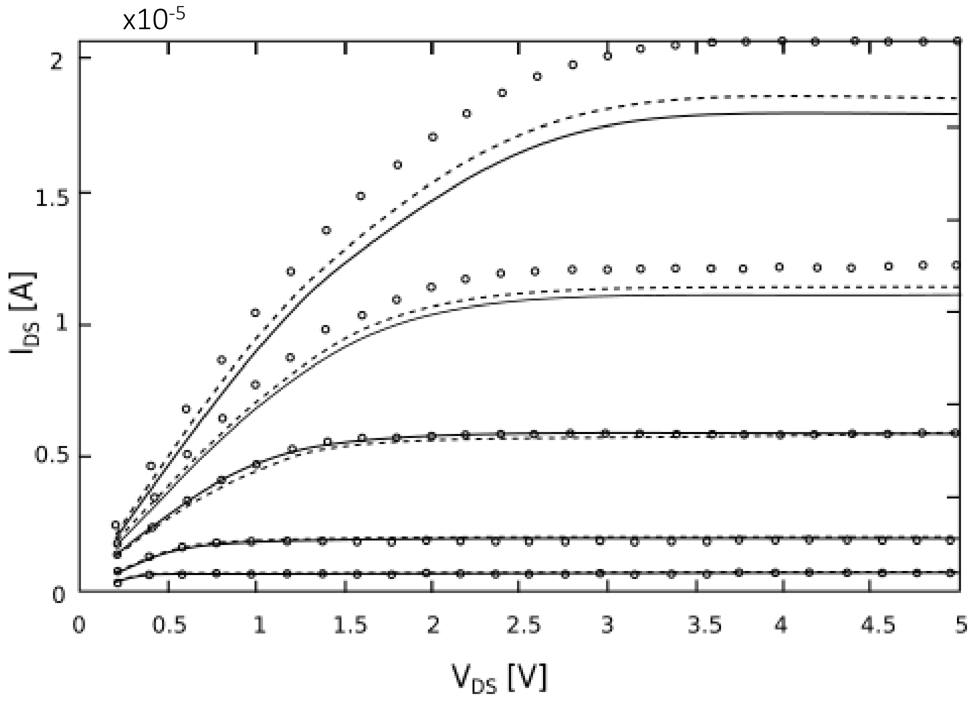


NMOS transfer characteristic of a typical wafer, W/L = 30/6, VGS = 1.5, 2, 3, 4, 5 V. o measured, solid line = MOS2 model, dashed line = AMS model.

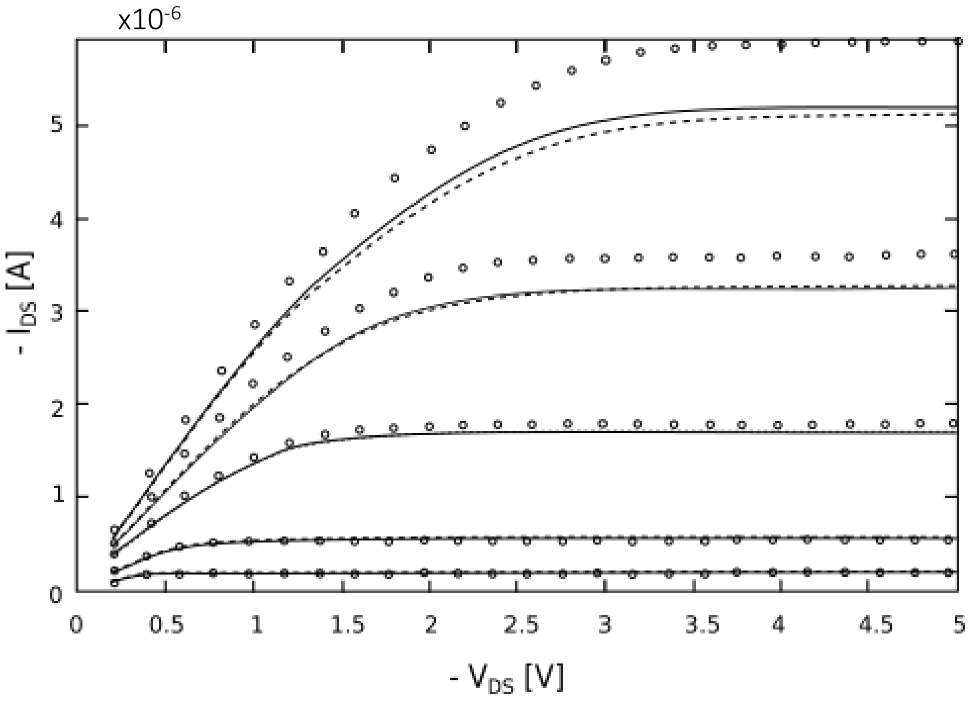


PMOS transfer characteristic of a typical wafer, W/L = 30/6, -VGS = 1.5, 2, 3, 4, 5 V. o measured, solid line = MOS2 model, dashed line = AMS model.

12 um CMOS Process Parameters

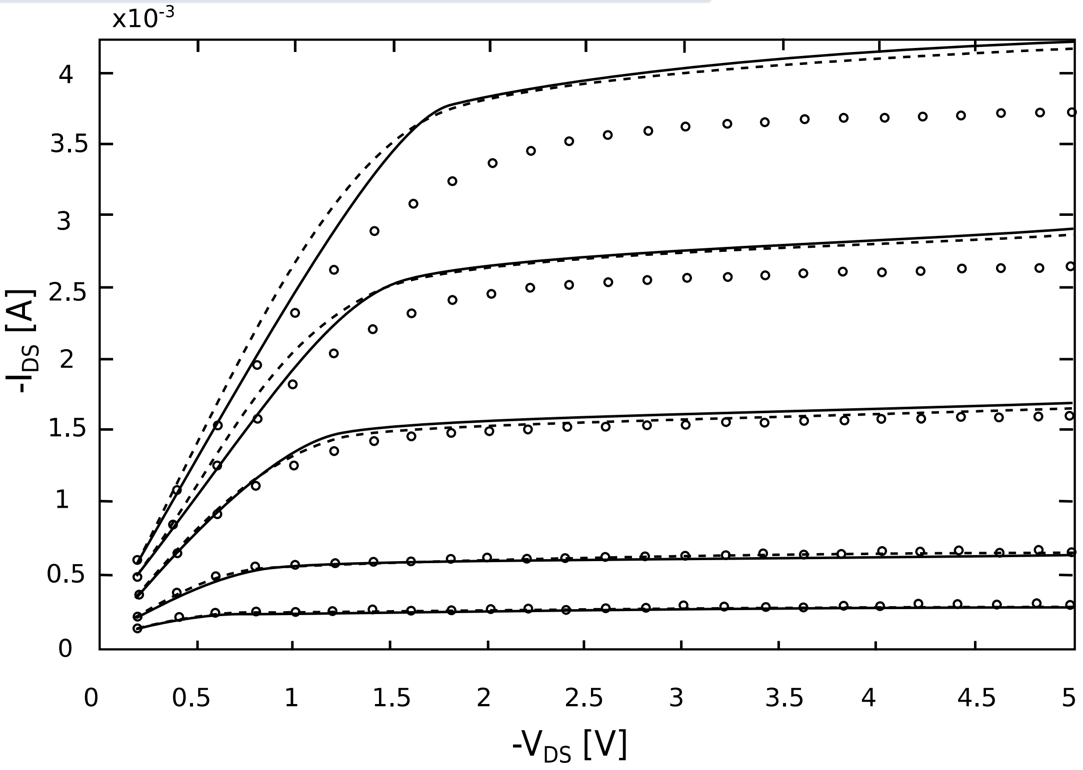


NMOS transfer characteristic of a typical wafer, W/L = 2/30, VGS = 1.5, 2, 3, 4, 5 V. o measured, solid line = MOS2 model, dashed line = AMS model.

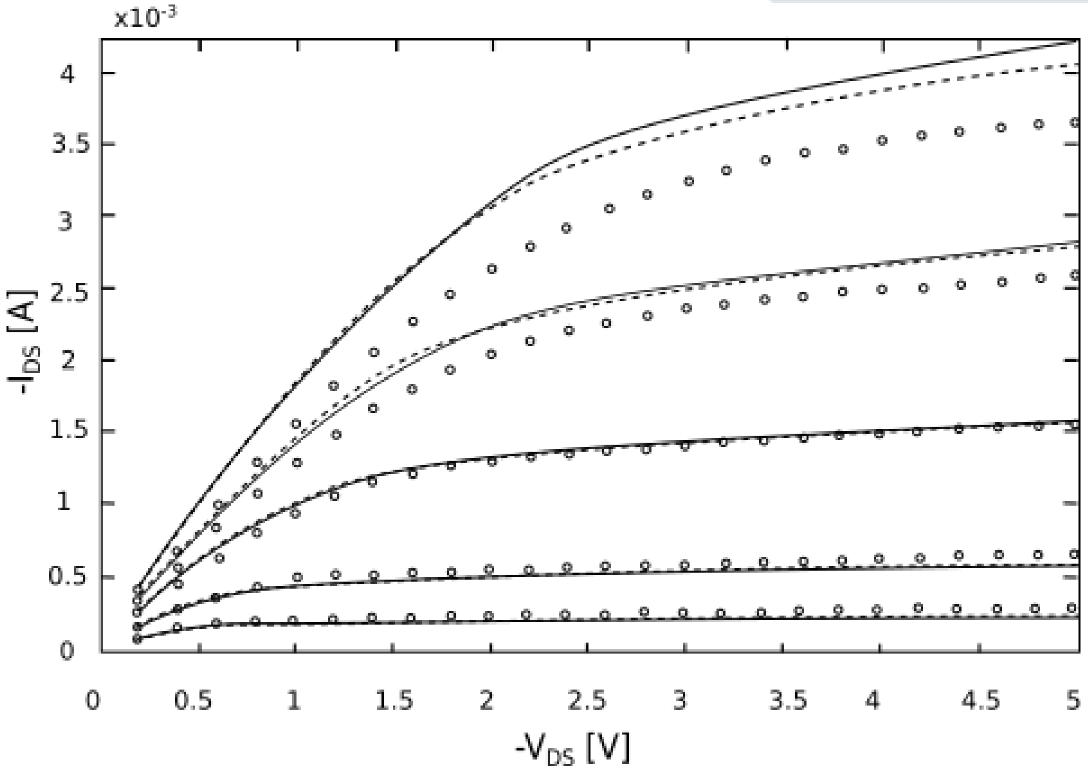


PMOS transfer characteristic of a typical wafer, W/L = 2/30, -VGS = 1.5, 2, 3, 4, 5 V. o measured, solid line = MOS2 model, dashed line = AMS model.

1.2 um CMOS Process Parameters

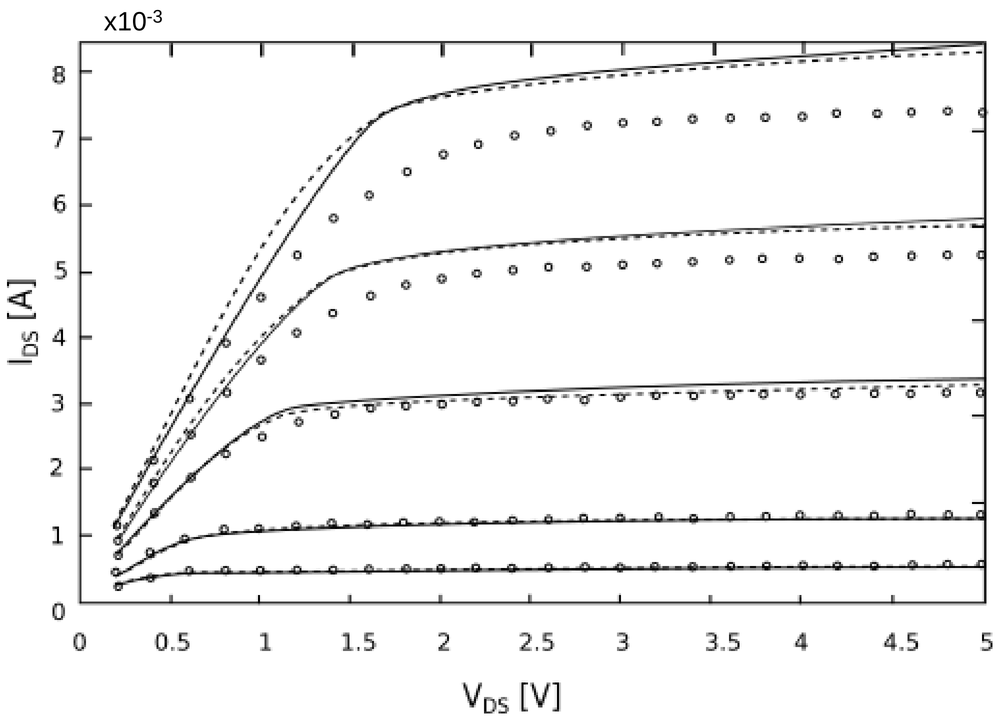


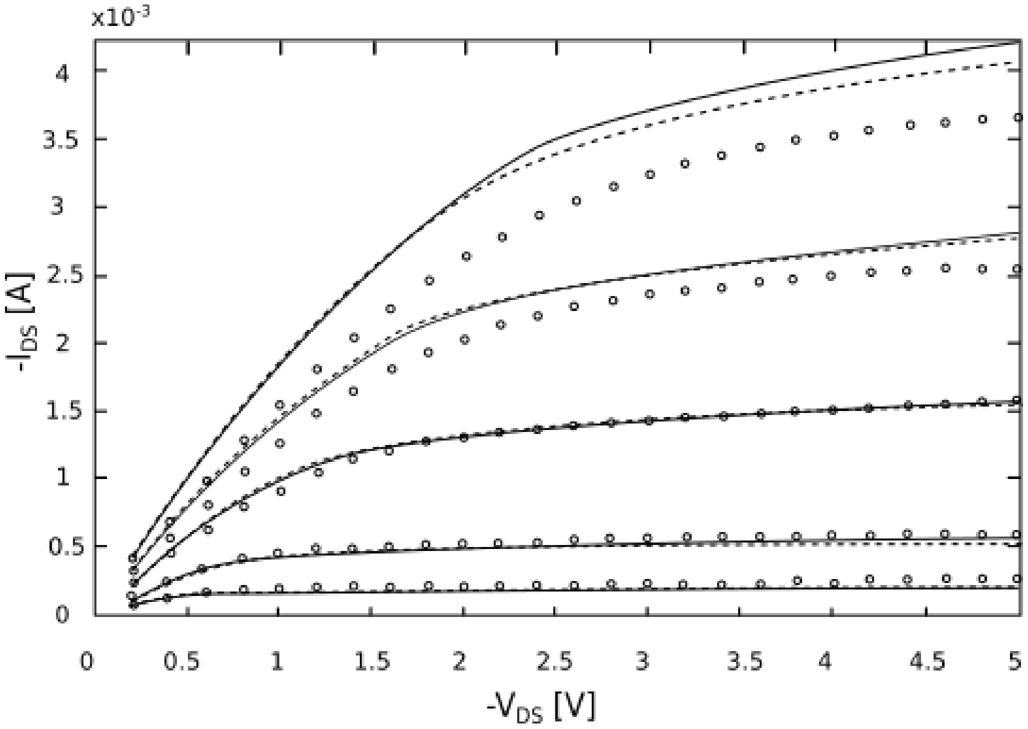
NMOS transfer characteristic of a typical wafer, W/L = 30/1.2, VGS = 1.5, 2, 3, 4, 5 V. o measured, solid line = MOS2 model, dashed line = AMS model.



PMOS transfer characteristic of a typical wafer, W/L = 30/1.2, -VGS = 1.5, 2, 3, 4, 5 V. o measured, solid line = MOS2 model, dashed line = AMS model.

1.2 um CMOS Process Parameters





NMOS transfer characteristic of a typical wafer, W/L = 30/1.2, VGS = 1.5, 2, 3, 4, 5 V. o measured, solid line = MOS2 model, dashed line = AMS model.

PMOS transfer characteristic of a typical wafer, W/L = 30/1.2, -VGS = 1.5, 2, 3, 4, 5 V. o measured, solid line = MOS2 model, dashed line = AMS model.

Small-signal model

Small signal model

Small-signal model is a linearised model at the operating point

Transconductance: $g_m = \frac{\partial i_D}{\partial v_{GS}}$ (at the quiescent point)

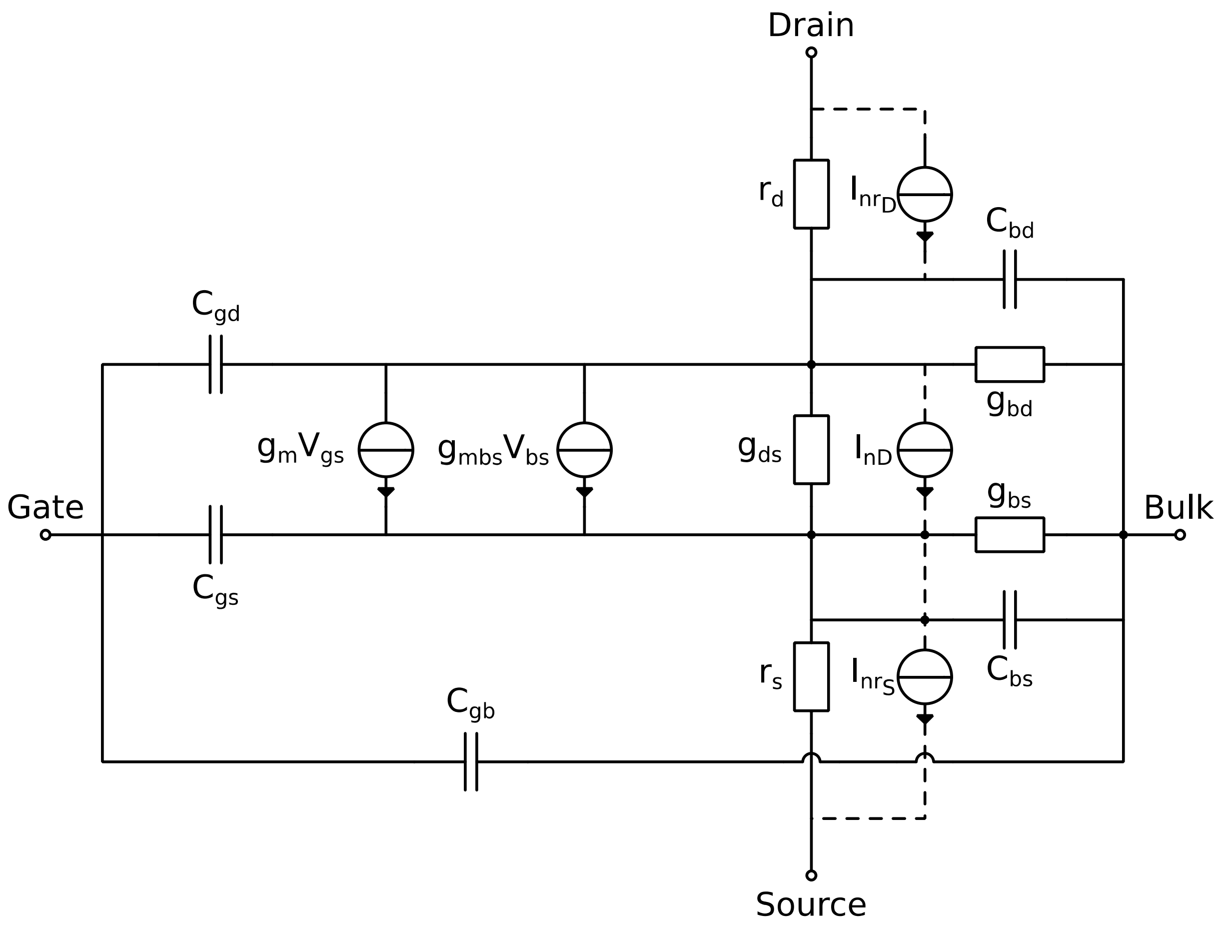
Drain-source conductance: $g_{ds} = \frac{\partial i_D}{\partial v_{DS}}$ (at the quiescent point)

Bulk modulation: $g_{mbs} = \frac{\partial i_D}{\partial v_{BS}}$ (at the quiescent point)

Drain and source diode conductances:

$$g_{bd} = \frac{\partial i_{BD}}{\partial v_{BD}} \text{ (at the quiescent point)} \approx 0$$

$$g_{bs} = \frac{\partial i_{SB}}{\partial v_{SB}} \text{ (at the quiescent point)} \approx 0$$



Modes of operation

Cut-off	$v_{GS} - V_T \leq 0$	$i_D = 0$
Linear region	$0 < v_{DS} \leq (v_{GS} - V_T)$	$i_D = \frac{\mu_0 C_{ox} W}{L}\left[(v_{GS} - V_T) - \frac{v_{DS}}{2}\right] v_{DS}(1 + \lambda v_{DS})$ $\beta = (K') \frac{W}{L} \cong (\mu_0 C_{ox}) \frac{W}{L}$ (amps/volt^2)
Saturation	$0 < (v_{GS} - V_T) \leq v_{DS}$	$i_D = \frac{\mu_0 C_{ox} W}{2L}(v_{GS} - V_T)^2 (1 + \lambda v_{DS})$
Pinch-off	$v_{DS}(\text{sat.}) = v_{GS} - V_T$	

Saturation region

$$i_D = \frac{\mu_O C_{OX} W}{2L}(v_{GS} - V_T)^2(1+\lambda v_{DS})$$

$$V_T = V_{T0} + \gamma\left(\sqrt{\left|-2\phi_F + v_{SB}\right|} - \sqrt{\left|-2\phi_F\right|}\right)$$

Transconductance:

$$g_m = \frac{\partial i_D}{\partial v_{GS}} = \frac{\overbrace{\mu_O C_{OX}}^{k'} W}{2L} 2(v_{GS} - V_T)(1+\lambda v_{DS})$$

$$g_m = \sqrt{(2K'W/L)|I_D|(1+\lambda V_{DS})} \cong \sqrt{(2K'W/L)|I_D|}$$

$$k' = \mu * C_{OX}$$

Drain-source conductance:

$$g_{ds} = \frac{\partial i_D}{\partial v_{DS}}$$

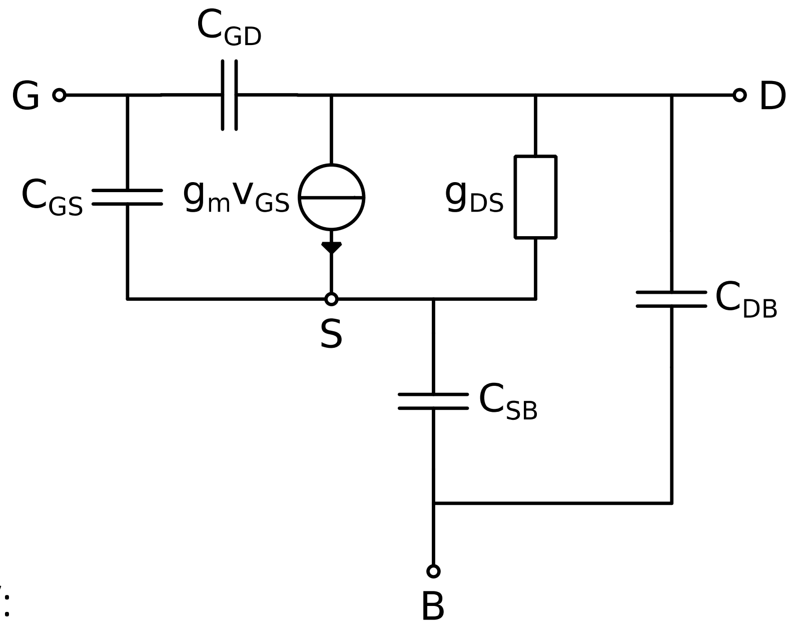
$$g_{ds} = g_o = \frac{I_D \lambda}{1+\lambda V_{DS}} \approx I_D \lambda \qquad \lambda \propto \frac{1}{L}$$

Bulk modulation:

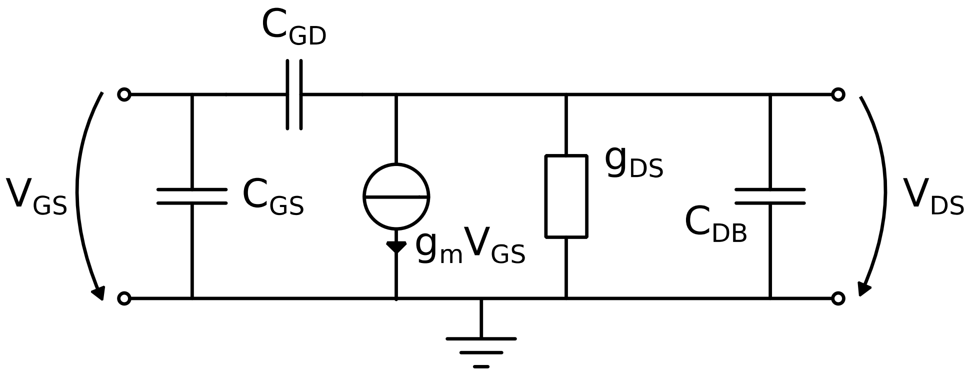
$$g_{mbs} = \frac{\partial i_D}{\partial v_{SB}} = \left(\frac{\partial i_D}{\partial V_T}\right)\left(\frac{\partial V_T}{\partial v_{SB}}\right) \qquad \frac{\partial i_D}{\partial V_T} = \left(\frac{-\partial i_D}{\partial v_{GS}}\right)$$

$$g_{mbs} = g_m \frac{\gamma}{2(2|\phi_F| + V_{SB})^{1/2}} = \eta g_m$$

MOS transistor small signal model



V_{SB} = 0V:



$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \sqrt{2\mu_O C_{OX} I_D \frac{W}{L}}$$

;V_E is the normalised Early voltage relative to L

$$g_{DS} = \frac{\partial I_D}{\partial V_{DS}} = \frac{I_D}{L * V_E^{'}} = I_D \lambda$$

;L ~ 3-10 μ

$$C_{GS} = \frac{2}{3} WL * C_{OX}$$

;$C_{OX} = \frac{\varepsilon_{OX}}{t_{OX}}$

$$C_{GD} = W\Delta\Delta * C_{OX}$$

;ΔL = lateral diffusion 0,1-0,2μ

$$C_{DB} = WC_{DB}^{'} \Big/ \sqrt{V_{DB} + 2\phi_p}$$

$$C_{SB} = WC_{SB}^{'} \Big/ \sqrt{V_{SB} + 2\phi_p}$$