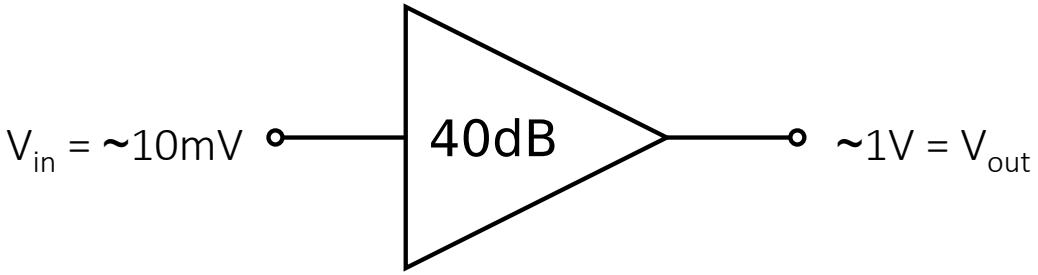
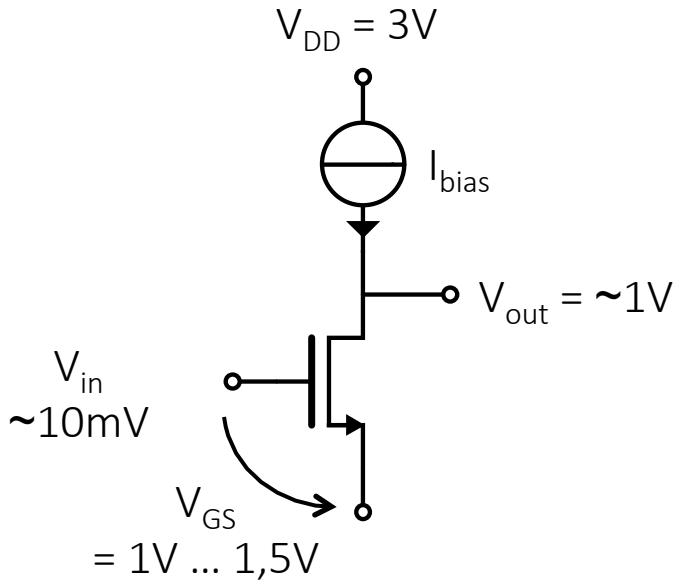
ELEC-E3510 Basics of IC Design

Lecture 3:
Single stage amplifiers

Small-signal model

Why small signal model:

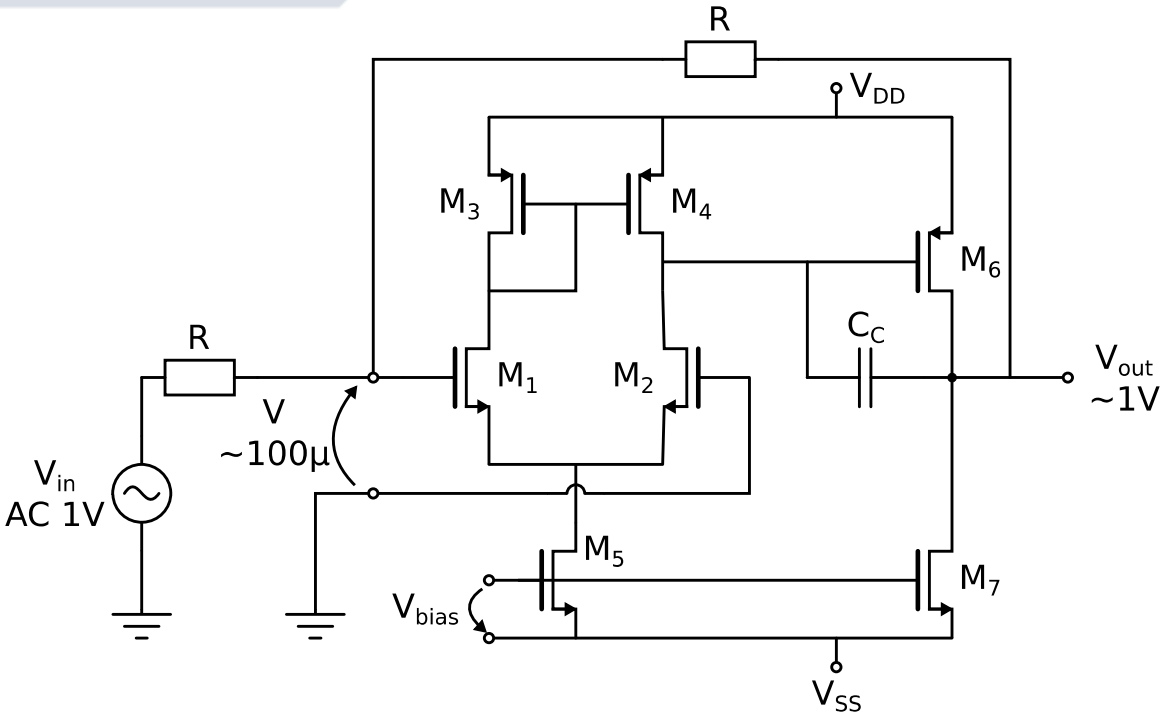




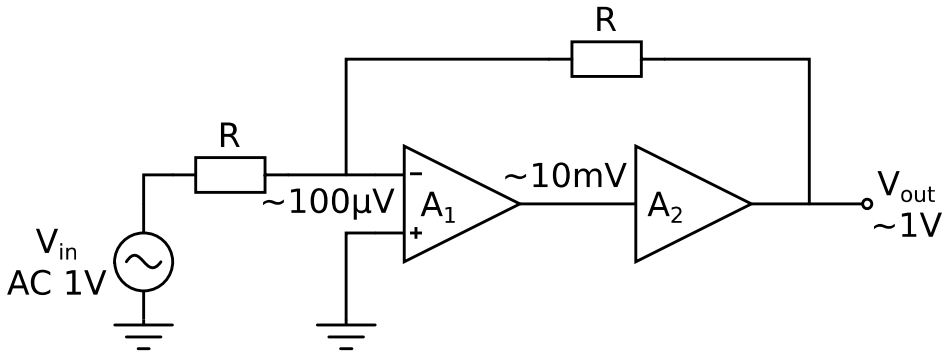
Only 1% variation in V_{GS}
$I_D = f(V_{GS})$ negligible variation in I_D

$g_m = f(I_D)$
$g_{DS} = f(I_D)$

Why small signal model:

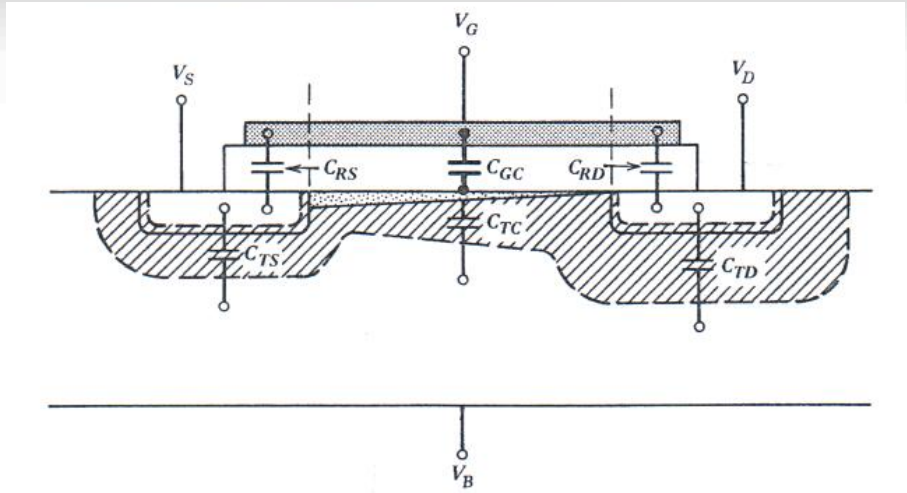


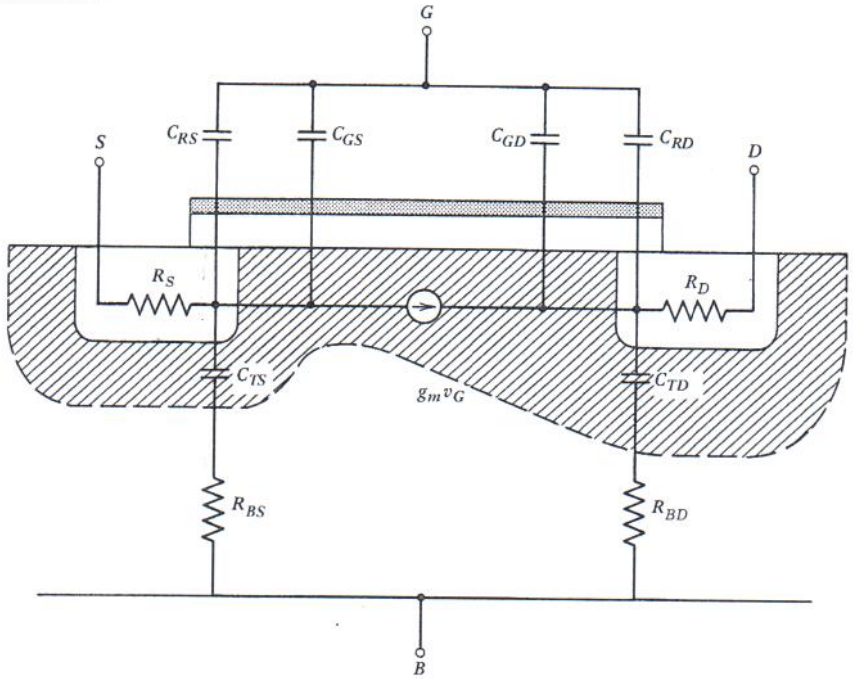
- Large signal i.e. AC=1V only at the output node
- Small signal 100µV…10mV<<1V at input and all internal nodes

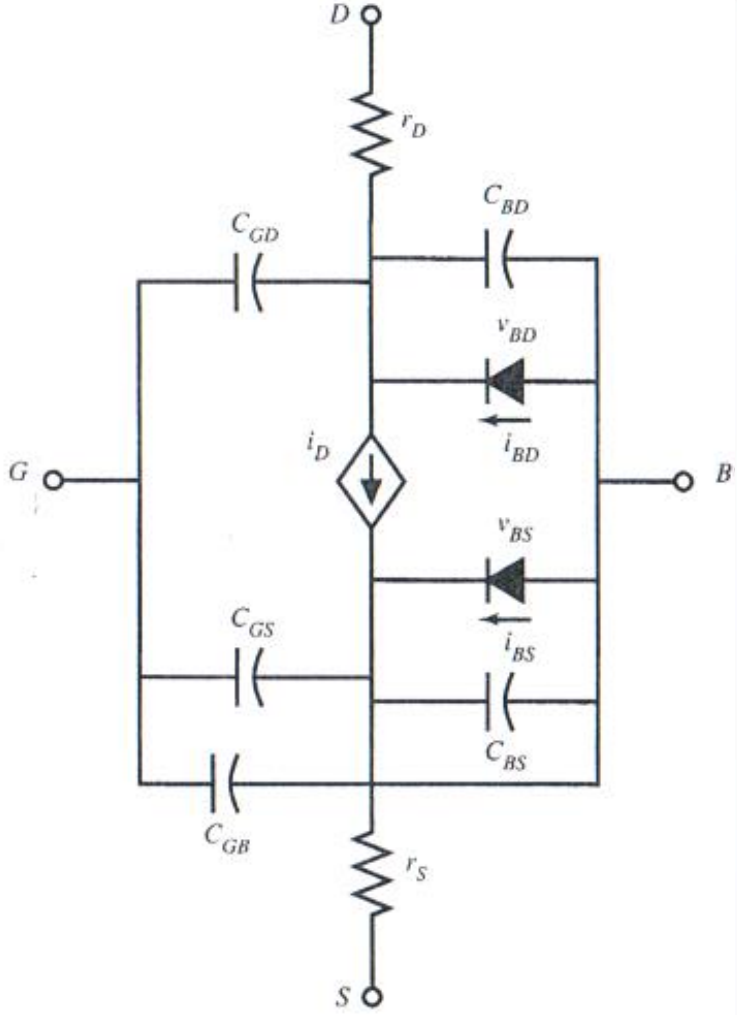


$A_1 = A_2 = 40dB$

MOS Spice model (level 1)







Small signal model

Small signal model is a linearised transistor model at the operating point.
Small signal model is used to analyse amplifier gain and noise characteristics

Transconductance: $g_m = \frac{\partial i_D}{\partial v_{GS}}$ (at the quiescent point)

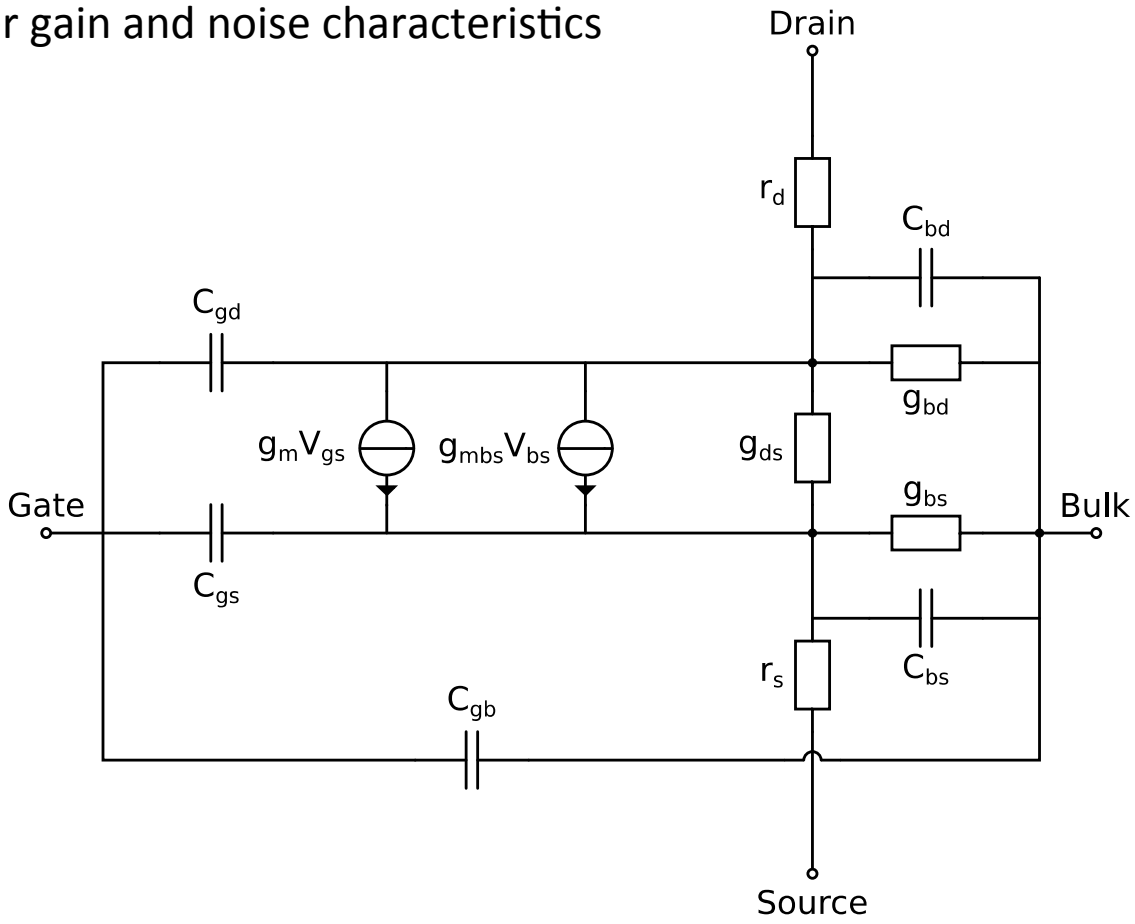
Drain-source conductance: $g_{ds} = \frac{\partial i_D}{\partial v_{DS}}$ (at the quiescent point)

Bulk modulation: $g_{mbs} = \frac{\partial i_D}{\partial v_{BS}}$ (at the quiescent point)

Drain and source diode conductances:

$g_{bd} = \frac{\partial i_{BD}}{\partial v_{BD}}$ (at the quiescent point) 0

$g_{bs} = \frac{\partial i_{SB}}{\partial v_{SB}}$ (at the quiescent point) 0



Modes of operation

Cut-off	$v_{GS} - V_T \leq 0$	$i_D = 0$
Linear region	$0 < v_{DS} \leq (v_{GS} - V_T)$	$i_D = \frac{\mu_0 C_{ox} W}{L}\left[(v_{GS} - V_T) - \frac{v_{DS}}{2}\right] v_{DS}(1 + \lambda v_{DS})$ $\beta = (K') \frac{W}{L} \cong (\mu_0 C_{ox}) \frac{W}{L}$ (amps/volt^2)
Saturation	$0 < (v_{GS} - V_T) \leq v_{DS}$	$i_D = \frac{\mu_0 C_{ox} W}{2L}(v_{GS} - V_T)^2(1 + \lambda v_{DS})$
Pinch-off	$v_{DS}(\text{sat.}) = v_{GS} - V_T$	

Saturation region

$$i_D = \frac{\mu_O C_{OX} W}{2L}(v_{GS} - V_T)^2(1 + \lambda v_{DS})$$

$$V_T = V_{T0} + \gamma\left(\sqrt{|-2\phi_F + v_{SB}|} - \sqrt{|-2\phi_F|}\right)$$

Transconductance:

$$g_m = \frac{\partial i_D}{\partial v_{GS}} = \frac{\overbrace{\mu_O C_{OX}}^{k'} W}{2L} 2(v_{GS} - V_T)(1 + \lambda v_{DS})$$

$$g_m = \sqrt{(2K'W/L)|I_D|}(1 + \lambda V_{DS}) \cong \sqrt{(2K'W/L)|I_D|}$$

$$k' = \mu * C_{OX}$$

Drain-source conductance:

$$g_{ds} = \frac{\partial i_D}{\partial v_{DS}}$$

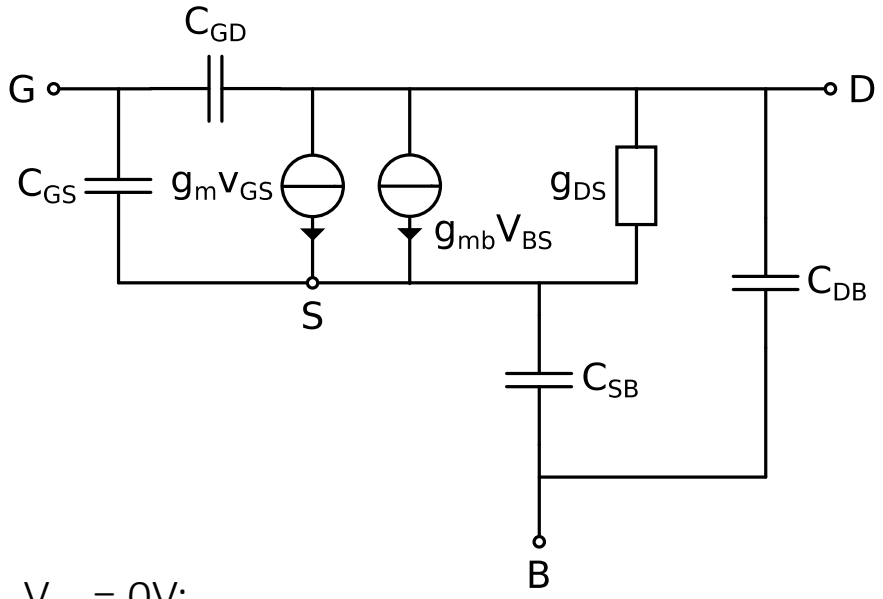
$$g_{ds} = g_o = \frac{I_D \lambda}{1 + \lambda V_{DS}} \approx I_D \lambda \qquad \lambda \propto \frac{1}{L}$$

Bulk modulation:

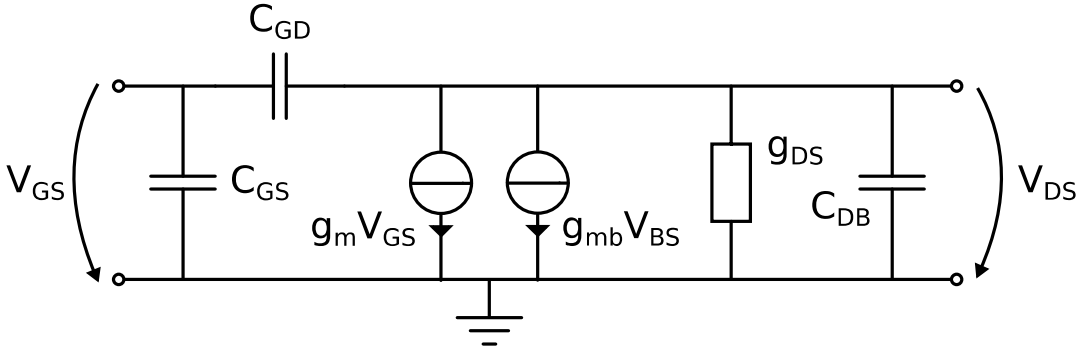
$$g_{mbs} = \frac{\partial i_D}{\partial v_{SB}} = \left(\frac{\partial i_D}{\partial V_T}\right)\left(\frac{\partial V_T}{\partial v_{SB}}\right) \qquad \frac{\partial i_D}{\partial V_T} = \left(\frac{-\partial i_D}{\partial v_{GS}}\right)$$

$$g_{mbs} = g_m \frac{\gamma}{2\left(2|\phi_F| + V_{SB}\right)^{1/2}} = \eta g_m$$

MOS transistor small signal model



V_{SB} = 0V:



$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \sqrt{2\mu_O C_{OX} I_D \frac{W}{L}}$$

$$g_{mb} = \frac{\partial I_D}{\partial V_{BS}} = \eta g_m$$

$$g_{DS} = \frac{\partial I_D}{\partial V_{DS}} = \frac{I_D}{L * V_E'} = I_D \lambda$$

$$C_{GS} = \frac{2}{3} WL * C_{OX}$$

$$C_{GD} = W\Delta L * C_{OX}$$

$$C_{DB} = WC_{DB}' \Big/ \sqrt{v_{DB} + 2\phi_p}$$

$$C_{SB} = WC_{SB}' \Big/ \sqrt{v_{SB} + 2\phi_p}$$

;V_E is the normalised Early voltage relative to L

;L 3-10 µm

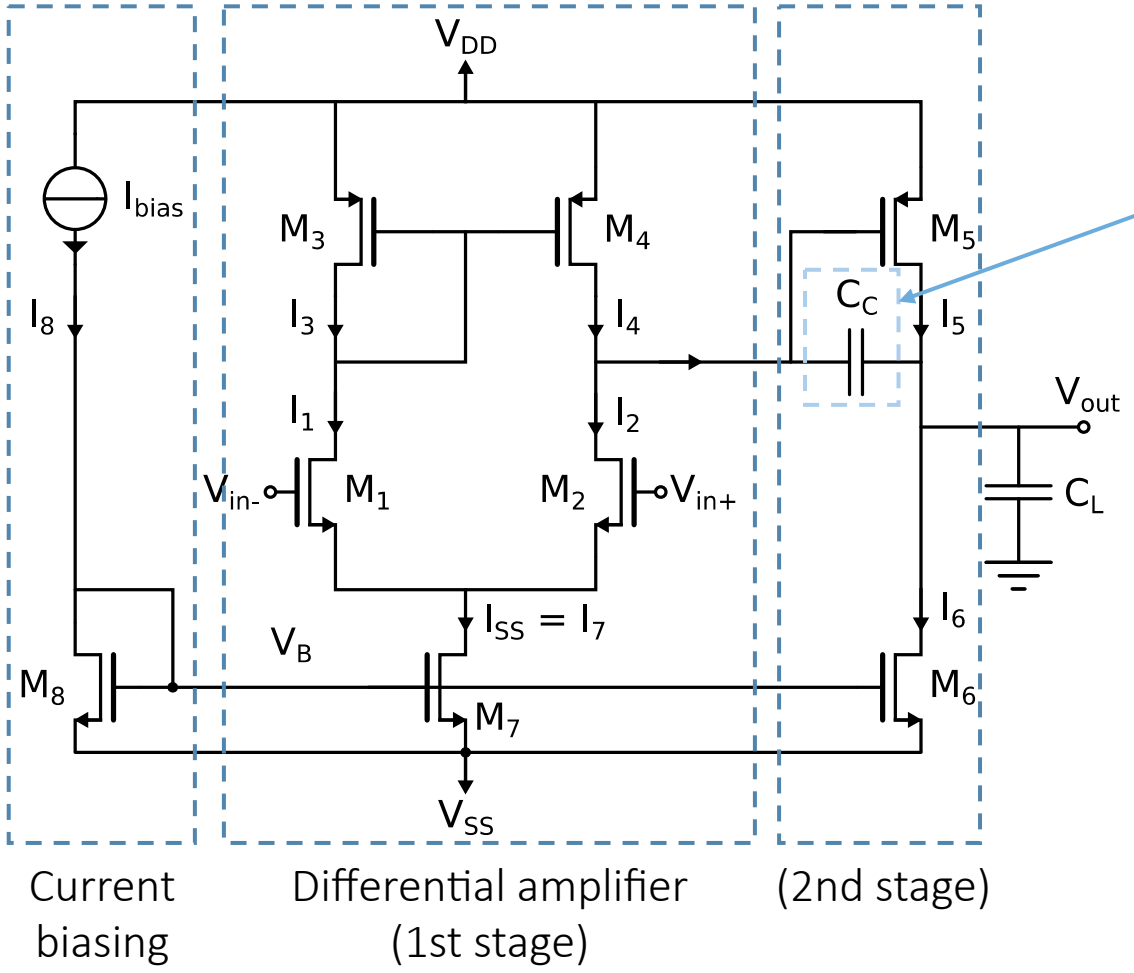
;$C_{OX} = \frac{\varepsilon_{OX}}{t_{OX}}$

;ΔL = lateral diffusion 0,1-0,2µm

Outline of single stage amplifiers:

- general analysis with resistive load
- diode loaded amplifier
- current source loaded amplifier
- push-pull CMOS inverter
- source follower
- cascode amplifier (extra material)
- amplifier design trade-offs (extra material)

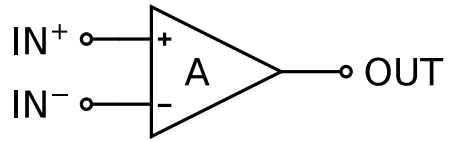
Operational amplifier



Compensation

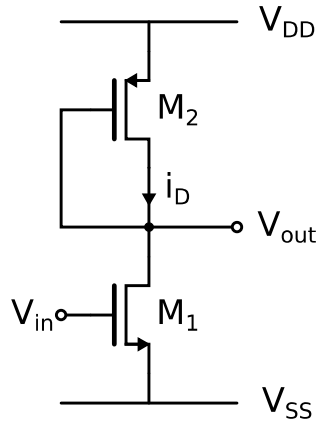
- 2 gain stages (80…120dB)
- Differential input stage
- Miller compensation
- Current biasing

Symbol:

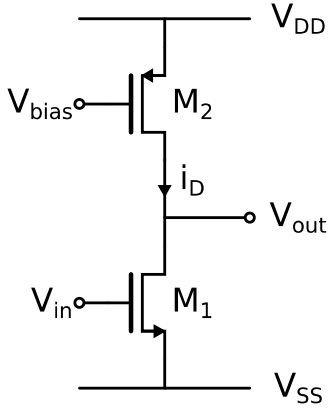


Single stage CMOS amplifiers

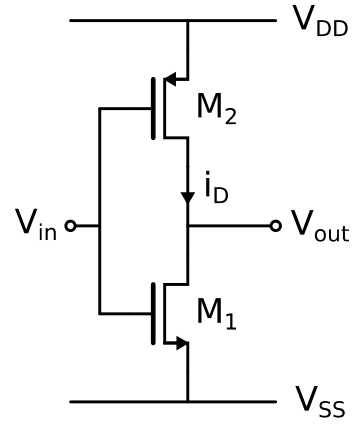
Amplifier with diode load



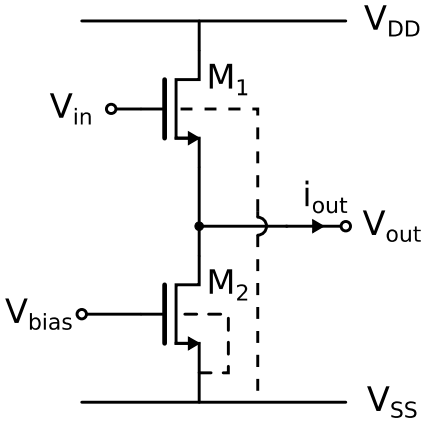
Amplifier with current source biasing



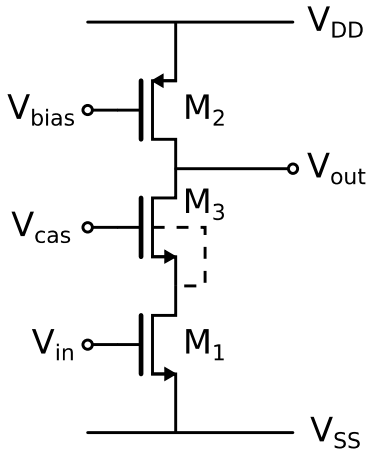
Push-pull inverter



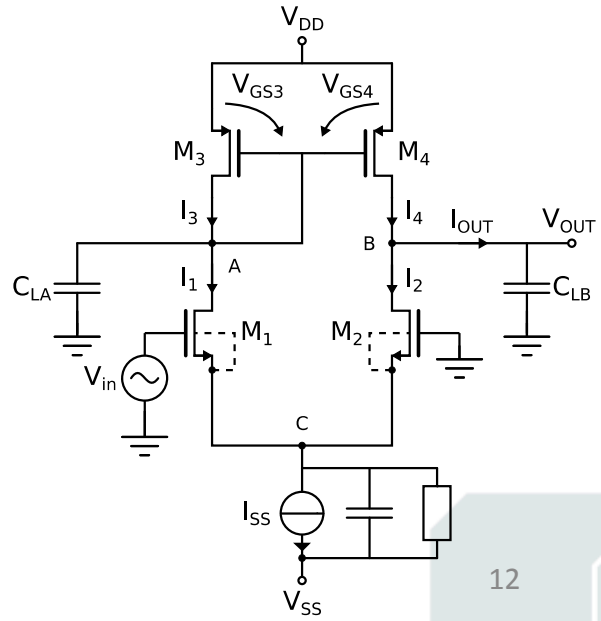
Source follower



Cascode amplifier

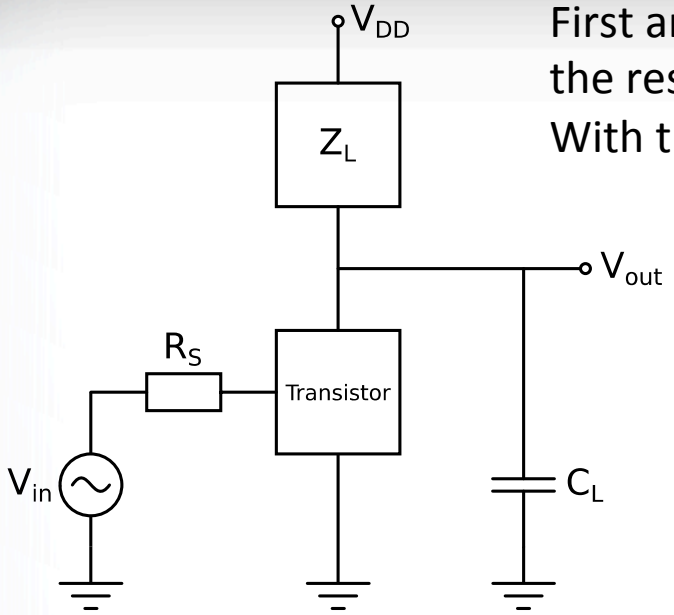


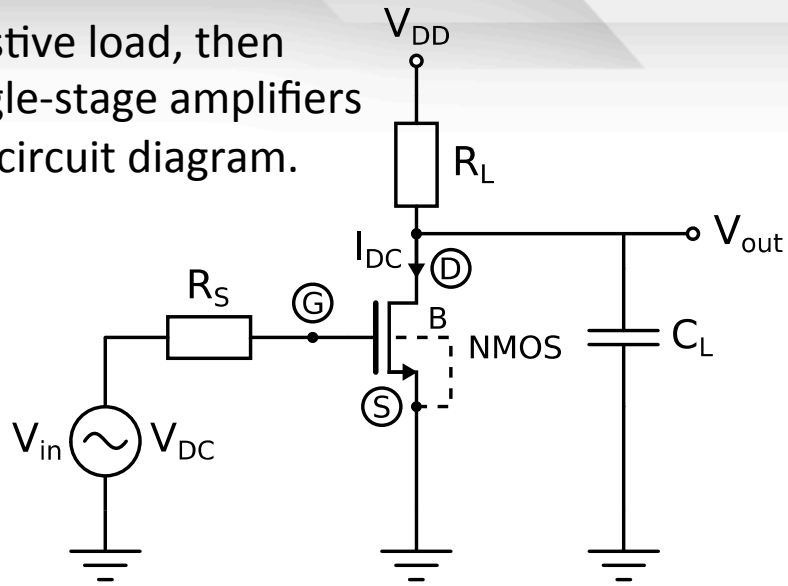
Differential amplifier

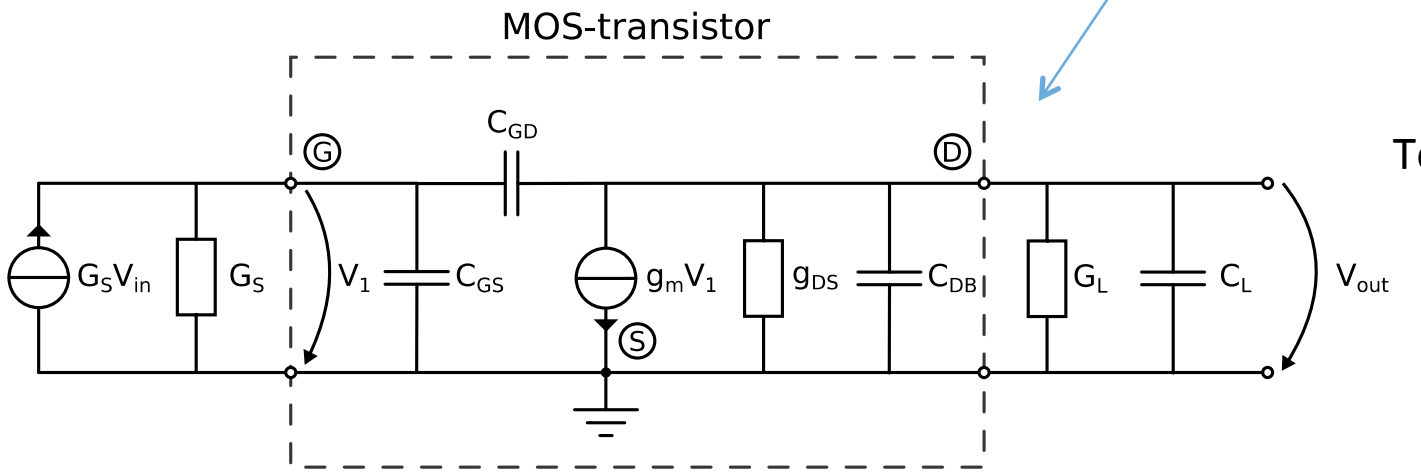


General single stage transistor amplifier

First analysed with the resistive load, then the results are used for single-stage amplifiers With the same small signal circuit diagram.





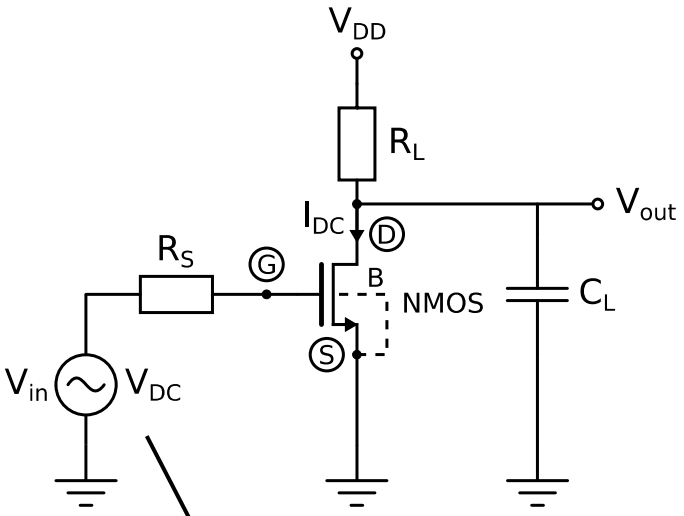


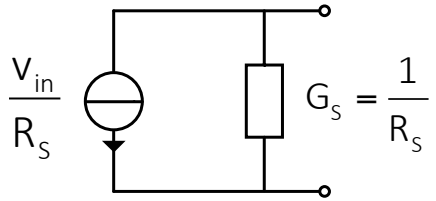
Total load:

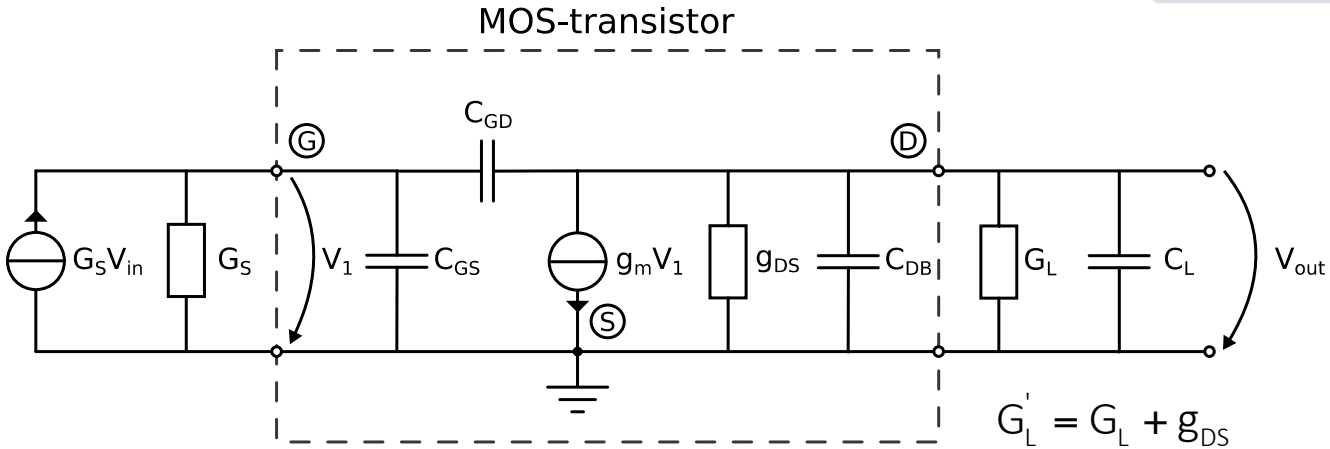
$$G_L' = G_L + g_{DS}$$

$$C_L' = C_L + C_{DB}$$

Single stage amplifier with resistive load







$$G_L' = G_L + g_{DS}$$

$$C_L' = C_L + C_{DB}$$

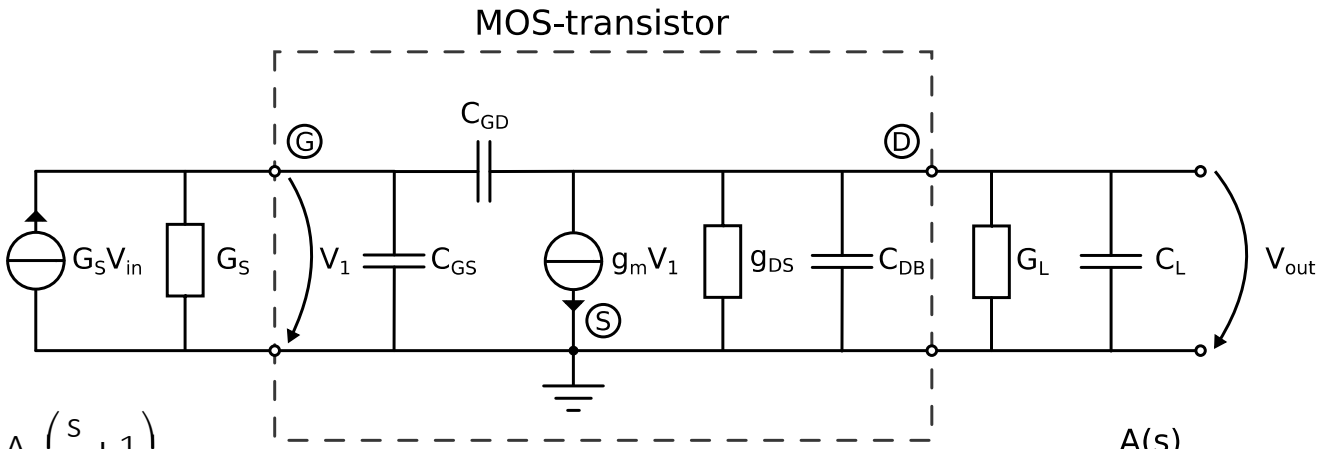
Current equations at nodes G and D

$$\begin{array}{ll} G & G_s v_{in} = v_1(G_S + sC_{GS}) + (v_1 - v_{out})sC_{GD} \\ D & g_m v_1 + (v_{out} - v_1)sC_{GD} + v_{out}(G_L' + sC_L') = 0 \end{array} \Big| : v_{in}$$

$$\Rightarrow \begin{cases} G_s = \frac{v_1}{v_{in}}(G_s + s(C_{GS} + C_{GD})) - \frac{v_{out}}{v_{in}} sC_{GD} \\ (g_m - sC_{GD})\frac{v_1}{v_{in}} + (s(C_{GD} + C_L) + G_L)\frac{v_{out}}{v_{in}} = 0 \end{cases}$$

Solve gain-transferfunction V_{out}/V_{in} by eliminating V_1/V_{in}

$$A(s) = \frac{v_{out}}{v_{in}} = \frac{G_s(sC_{GD} - g_m)}{s^2\left(C_{GS}C_{GD} + C_{GD}C_L' + C_{GS}C_L'\right) + s\left[G_s(C_{GD} + C_L) + G_L'(C_{GS} + C_{GD}) + g_m C_{GD}\right] + G_s G_L'}$$



Total load:

$$G_L^{'} = G_L + g_{DS}$$

$$C_L^{'} = C_L + C_{DB}$$

$$A(s) = \frac{K_0(s+z)}{(s+p_1)(s+p_2)} = \frac{A_0\left(\frac{s}{z}+1\right)}{\left(\frac{s}{p_1}+1\right)\left(\frac{s}{p_2}+1\right)}$$

$$\text{DC-gain:} \quad A(s=0) = -\frac{g_m}{G_L^{'}} = -\frac{g_m}{G_L + g_{DS}} \Rightarrow \max|A| = \left|-\frac{g_m}{g_{DS}}\right|$$

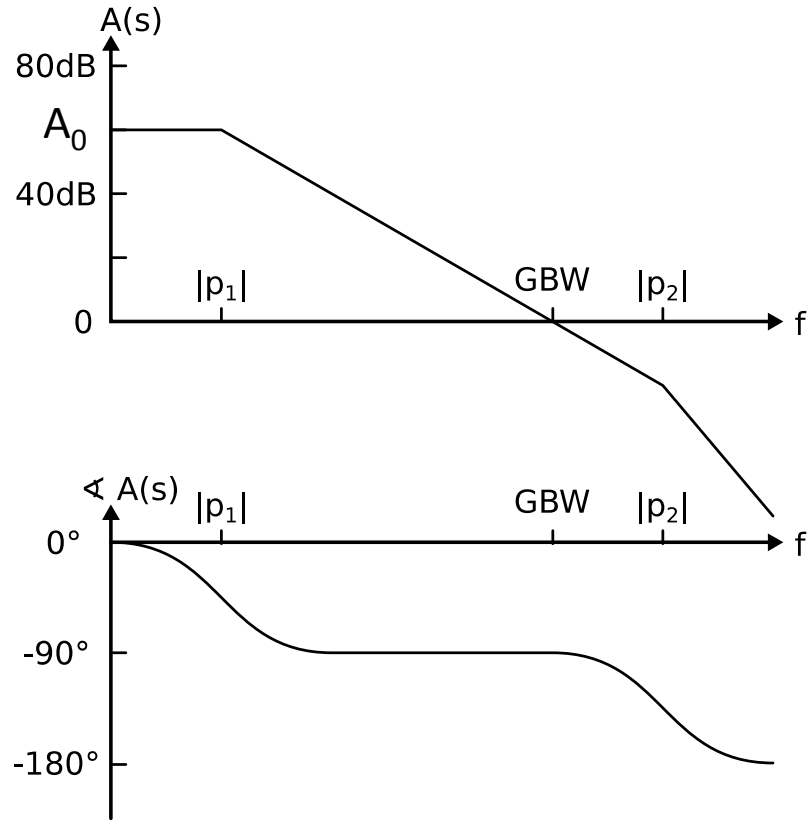
$$\text{zero:} \quad z = \frac{g_m}{C_{GD}}$$

$$\text{poles:} \quad P_{1,2} = \frac{-C_{GD}g_m - G_L(C_{GS}+C_{GD}) - G_S(C_{GD}+C_L)}{2(C_{GS}C_{GD}+C_{GS}C_L+C_{GD}C_L)}$$

$$\pm \frac{\sqrt{\left[C_{GD}g_m + G_L(C_{GS}+C_{GD}) + G_S(C_{GD}+C_L)\right]^2 - 4(C_{GS}C_{GD}+C_{GS}C_L+C_{GD}C_L)G_SG_L}}{2(C_{GS}C_{GD}+C_{GS}C_L+C_{GD}C_L)}$$

unity-gain bandwidth (GBW):

$$\left[GBW = |A(s=0)p_L| = \frac{g_m}{G_L^{'}} * \frac{G_L^{'}}{C_L^{'}} = \frac{g_m}{C_L^{'}}\right]$$



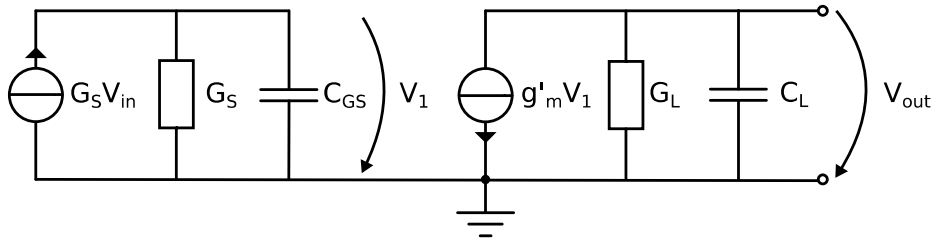
These results are used to characterise the other single stage amplifiers.

Approximative solutions for poles

In electronics approximative solutions are useful due to the complexity of circuits.
Three general methods are presented to solve the poles of the amplifier:

1) Assume: $C_{GD} << C_{GS}, C_L$

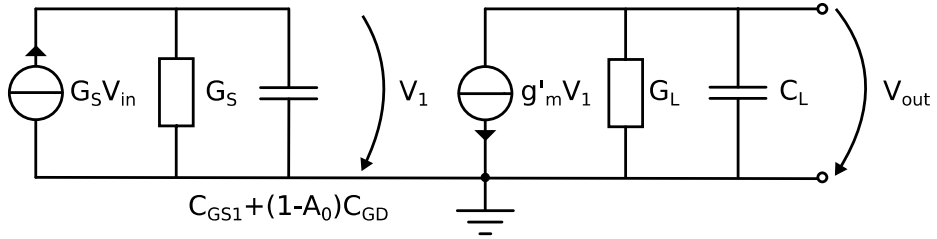
poles: $P_{in} = \frac{-G_s}{C_{GS}}$, $P_L = \frac{-G_L}{C_L}$



$g_m^{'} = g_m - sC_{GD}$

2) Miller theorem:

poles: $P_{in} = \frac{-G_s}{C_{GS} + \left(1 + \frac{g_m}{G_L}\right)C_{GD}}$, $P_L = \frac{-G_L}{C_L + C_{GD}}$



$g_m^{'} = g_m - sC_{GD}$

3) Separate poles: assume $|p_2| >> |p_1|$ (i.e. dominant pole approximation)

$$s^2 + s(p_1 + p_2) + p_1 p_2 \Rightarrow (s + p_1)(s + p_2) \approx s^2 + sp_2 + p_1 p_2$$

$$p_2 = \frac{-(C_{GD}g_m + G_L(C_{GS} + C_{GD}) + G_S(C_{GD} + C_L))}{C_{GS}C_{GD} + C_{GS}C_L + C_{GD}C_L} \quad , \quad p_1 = \frac{-G_S G_L}{C_{GD}g_m + G_L(C_{GS} + C_{GD}) + G_S(C_{GD} + C_L)}$$

Dominant pole approximation

$$A(s) = \frac{A_0}{1 + \frac{s}{p_1}}$$

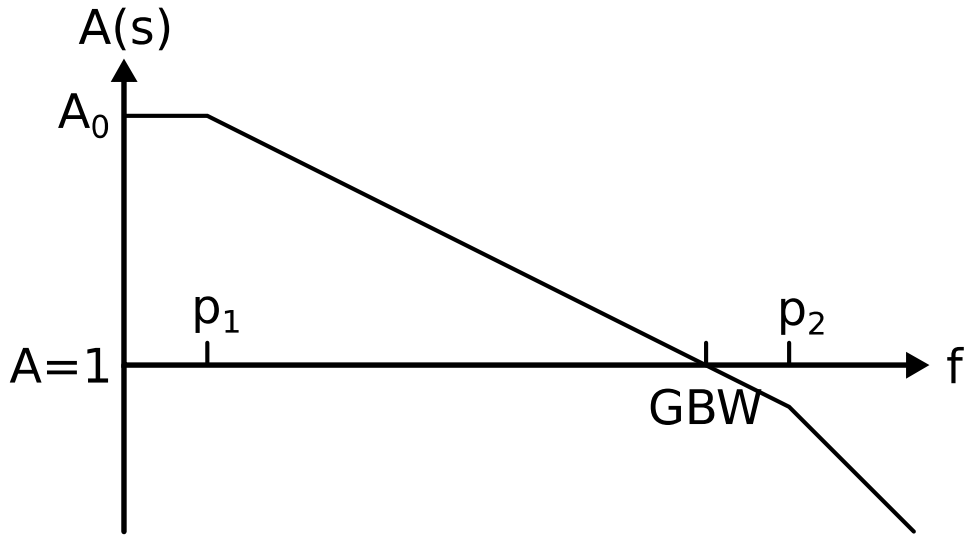
assume: $s >> p_1$

$$\Rightarrow A(s) = \frac{A_0}{s/p_1}$$

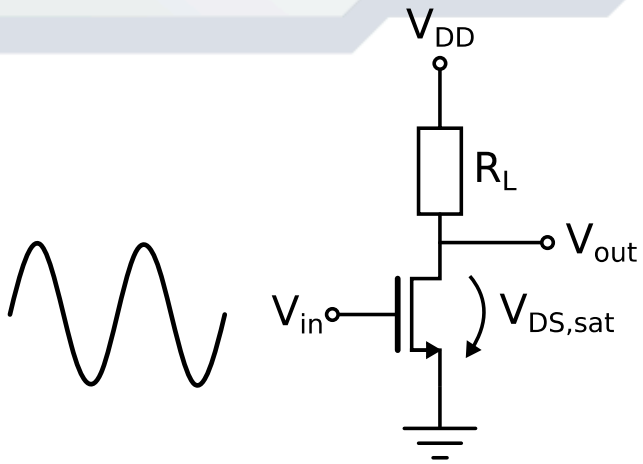
$$|A(GBW)| = 1$$

$$\Rightarrow GBW = A_0 p_1$$

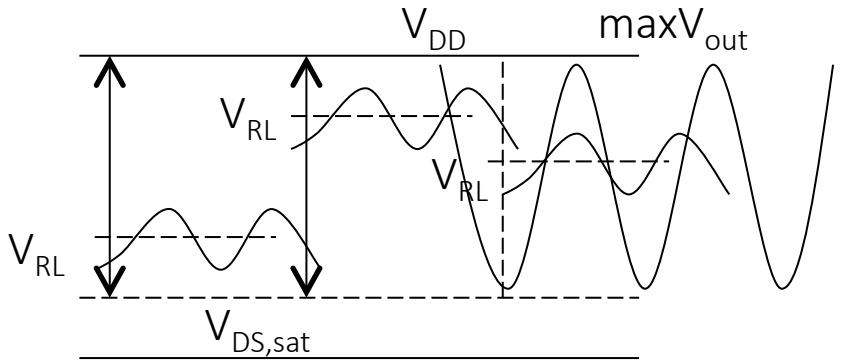
”gain bandwidth product”



Signal linear range



Output linear range depends on output biasing point:

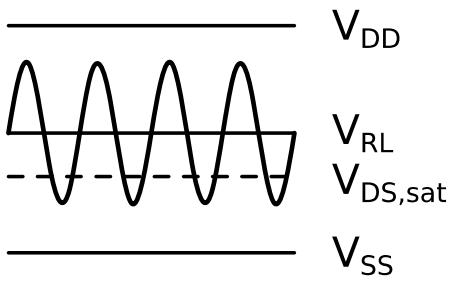


V_{SS}

Linear range maximised when biased half way between supply and transistor saturation limit.

Transistor saturation voltage limited:

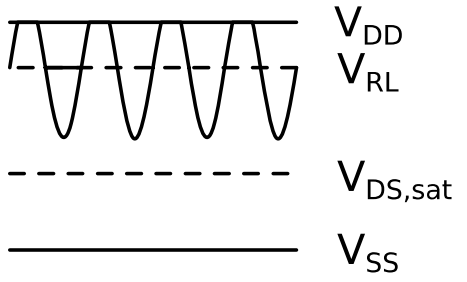
$V_{OUT} > V_{RL}-V_{DS,SAT}$:



⇒ Distortion

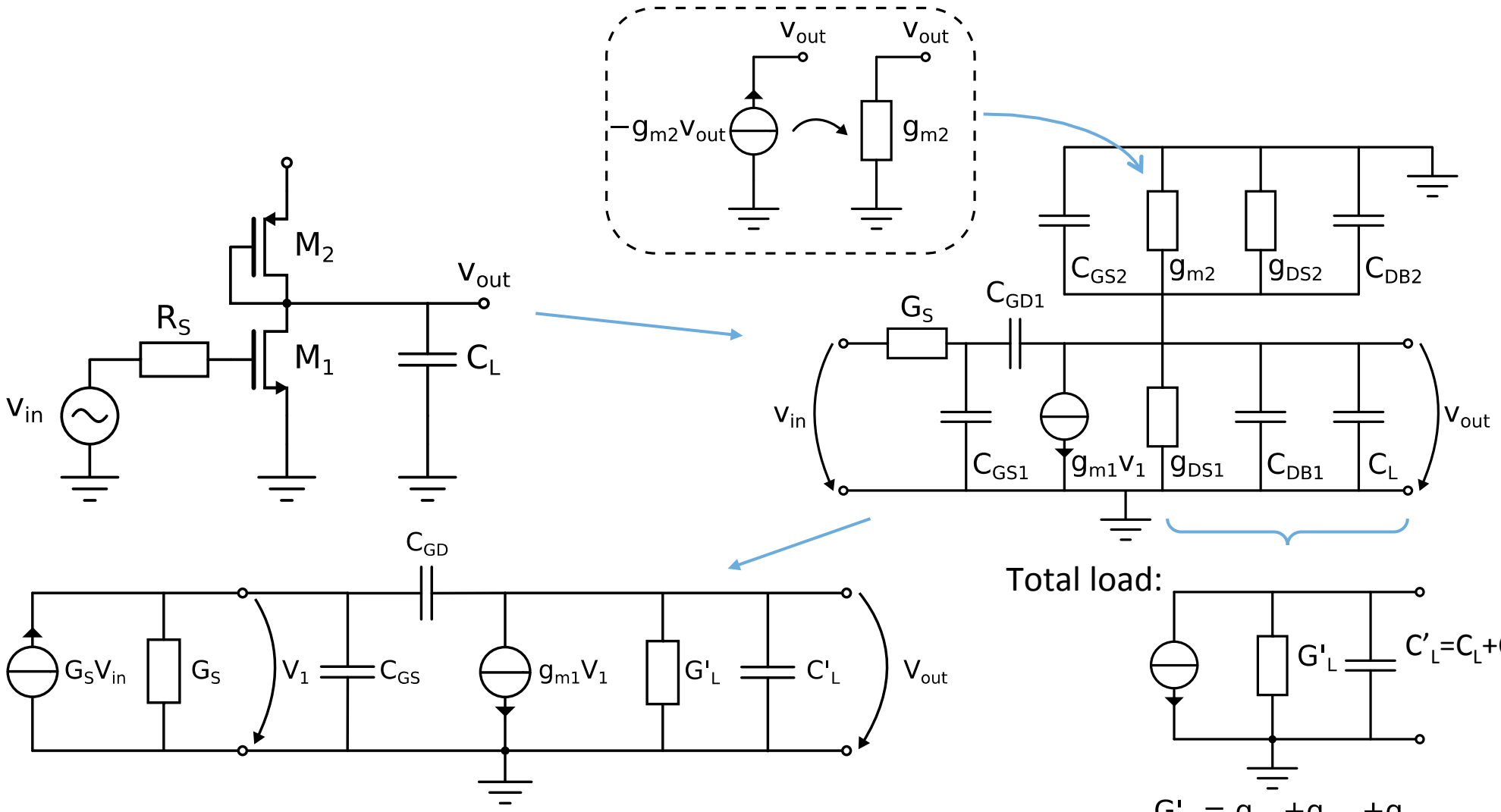
Supply voltage limited:

$V_{OUT} > V_{DD}-V_{RL}$:



⇒ Clipping!

Diode loaded amplifier



Total load:

$G'_L = g_{m2}+g_{DS1}+g_{DS2}$

Results of the resistive loaded case can be used to characterise the diode loaded amplifier:

$$A(s) = \frac{A_0\left(\frac{s}{z}+1\right)}{\left(\frac{s}{p_1}+1\right)\left(\frac{s}{p_2}+1\right)}$$

$$A_0 = \frac{-g_{m1}}{G_L'} = \frac{-g_{m1}}{g_{m2}+g_{DS1}+g_{DS2}} \approx \frac{-g_{m1}}{g_{m2}} \approx \sqrt{\frac{\mu_n\left(\frac{W}{L}\right)_1}{\mu_p\left(\frac{W}{L}\right)_2}}$$

$$\text{zero}: z = \frac{g_{m1}}{C_{GD1}}$$

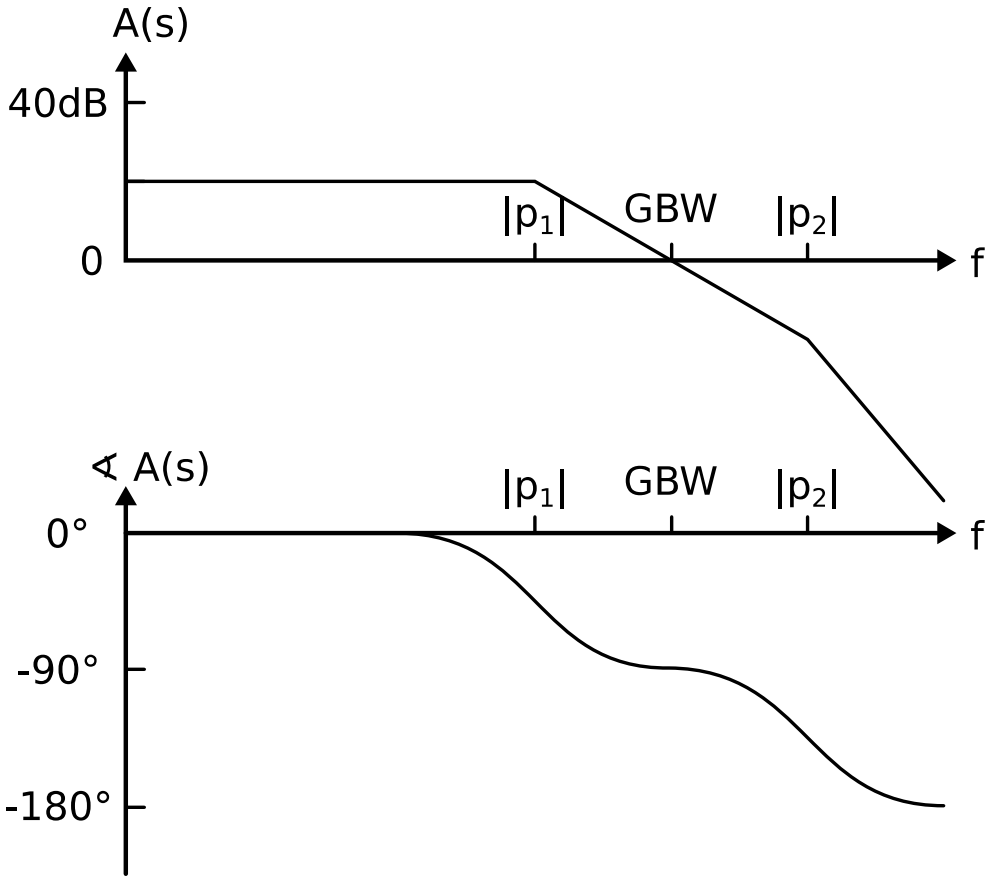
Poles (according to Miller theorem):

$$P_{in} = \frac{-G_s}{C_{GS1}+\left(1+\frac{g_{m1}}{g_{m2}}\right)C_{GD1}} \approx \frac{-G_s}{C_{GS1}}$$

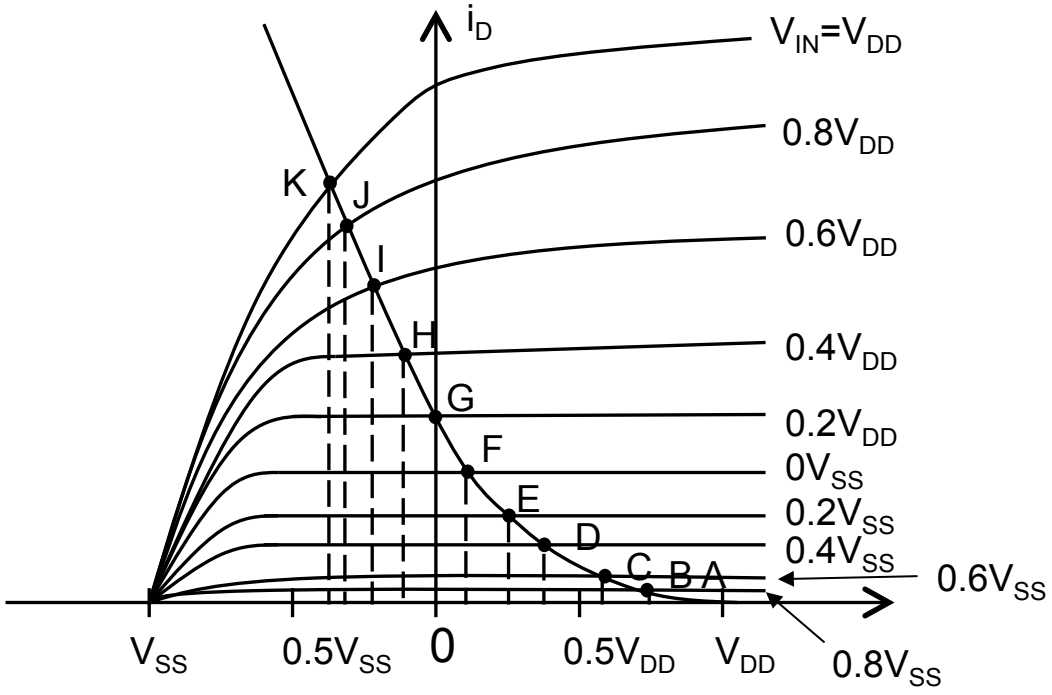
$$P_L = \frac{-\left(g_{m2}+g_{DS1}+g_{DS2}\right)}{C_L+C_{GS2}+C_{DB1}+C_{DB2}+C_{GD1}} \approx \frac{-g_{m2}}{C_L'}$$

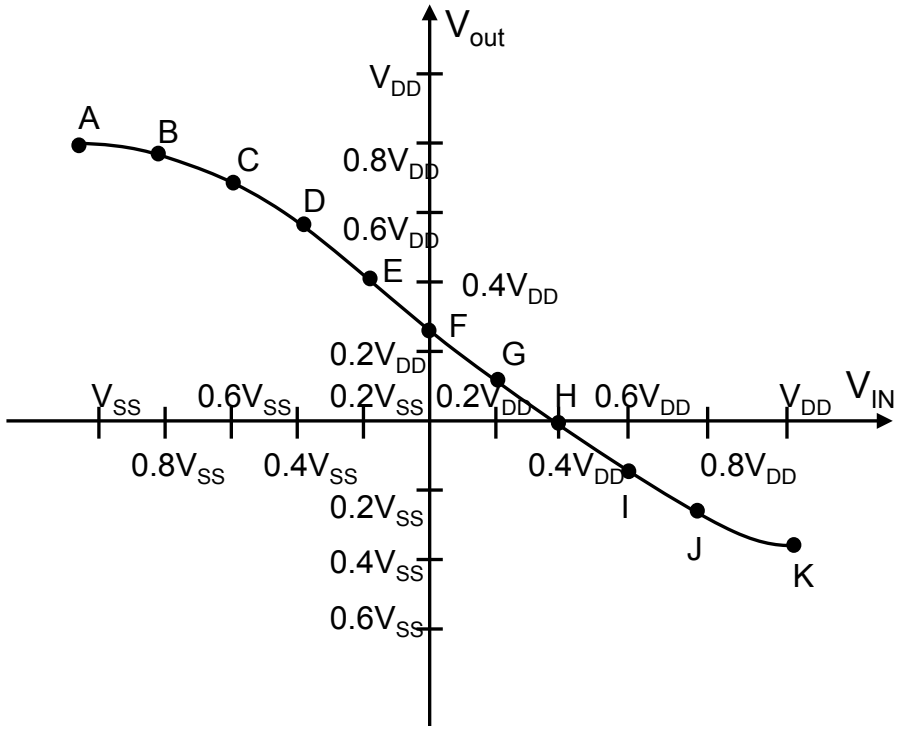
Assume: $p_L << p_{in}$ (in fig. $p_1=p_L$ and $p_2=p_{in}$)

$$GBW = A_0 \bullet p_L = \frac{g_{m1}}{C_L'}$$



Transfer curve of diode loaded amplifier





Transfer curve of diode loaded amplifier

Assume: M1 and M2 in saturation:

$$I_1 = k_1 (V_{in} - V_T)^2$$
$$I_2 = k_2 (V_{DD} - V_{out} - V_T)^2$$
$$I_1 = I_2$$
$$k_1 (V_{in} - V_T)^2 = k_2 (V_{DD} - V_{out} - V_T)^2$$
$$\sqrt{k_1} (V_{in} - V_T) = \sqrt{k_2} (V_{DD} - V_{out} - V_T)$$
$$\Rightarrow V_{out} = \frac{-\sqrt{k_1}}{\sqrt{k_2}} V_{in} + V_{DC} \quad \Rightarrow$$

This is a linear relationship

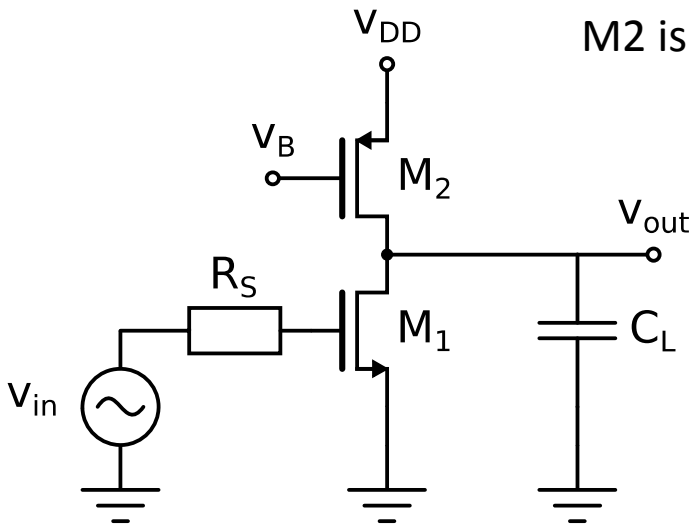
Channel length modulation causes nonlinearity

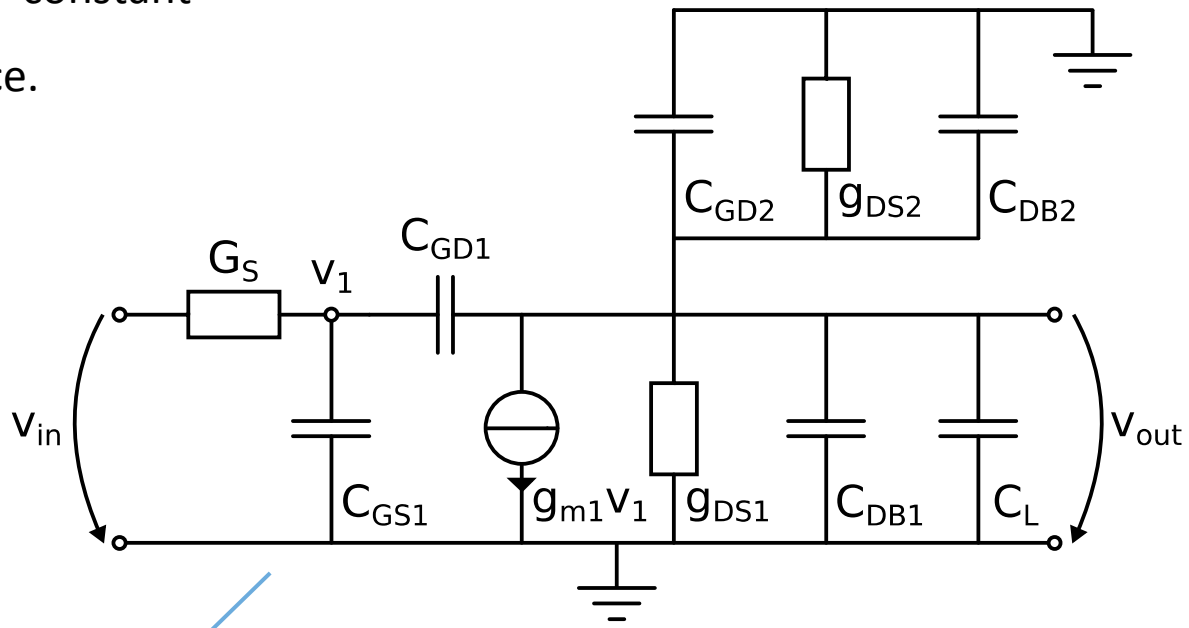
$$I_1 = k_1 (V_{in} - V_T)^2 (1 + \lambda V_{out})$$
$$I_2 = k_2 (V_{DD} - V_{out} - V_T)^2 (1 + \lambda (V_{DD} - V_{out}))$$

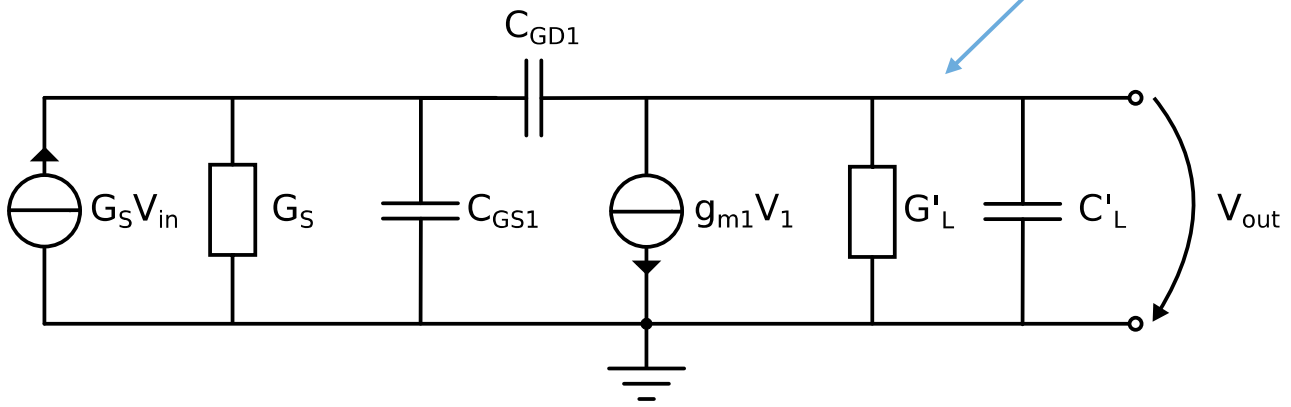
Current source load

V_B = constant $\Rightarrow$ I_{D2} = constant

M2 is a current source.







Total load:

$G'_L = g_{DS1} + g_{DS2}$

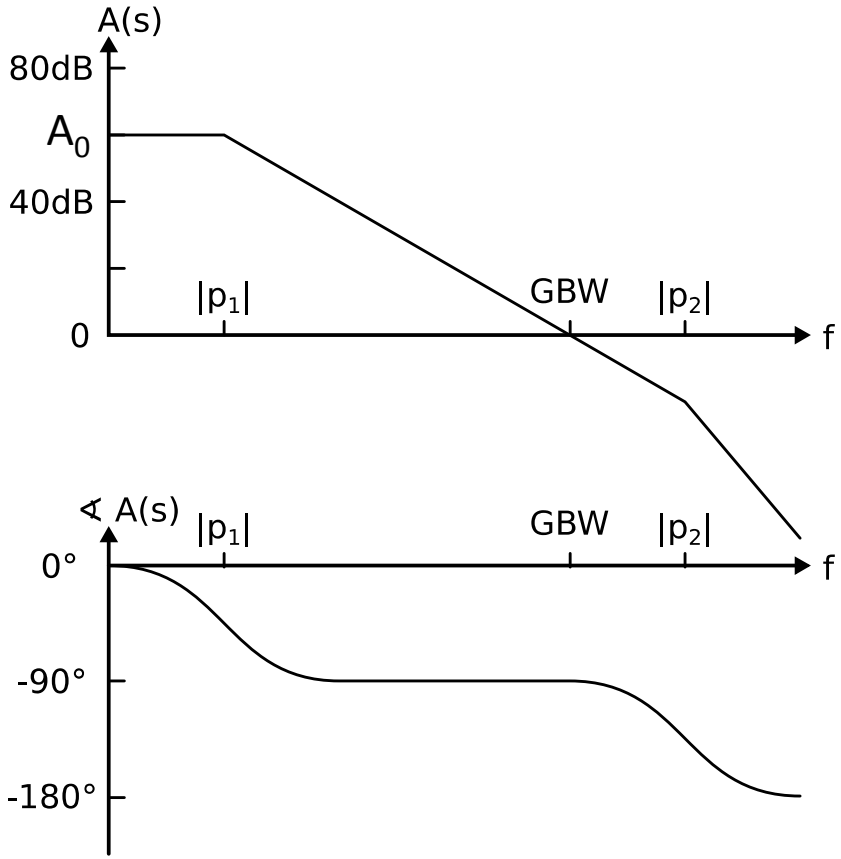
$C'_L = C_L + C_{DB1} + C_{GD2} + C_{DB2}$

Results of the resistive loaded case are used to characterise the current source biased amplifier:

$$A(s) = \frac{A_0\left(\frac{s}{z}+1\right)}{\left(\frac{s}{p_1}+1\right)\left(\frac{s}{p_2}+1\right)}$$

$$A_0 = \frac{-g_{m1}}{G_L'} = \frac{-g_{m1}}{g_{DS1}+g_{DS2}}$$

$$\text{Zero}: Z = \frac{g_{m1}}{C_{GD1}}$$



Poles (approximation with Miller theorem):

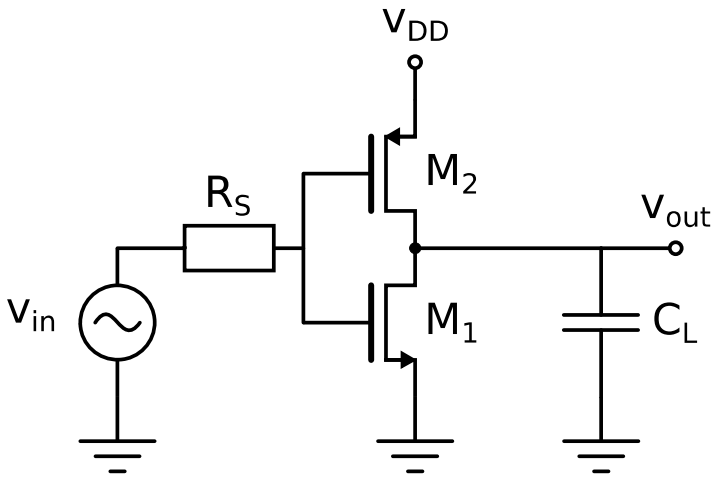
$$P_{in} = \frac{-G_s}{C_{GS1}+\left(1+\frac{g_{m1}}{g_{DS1}+g_{DS2}}\right)C_{GD1}}$$

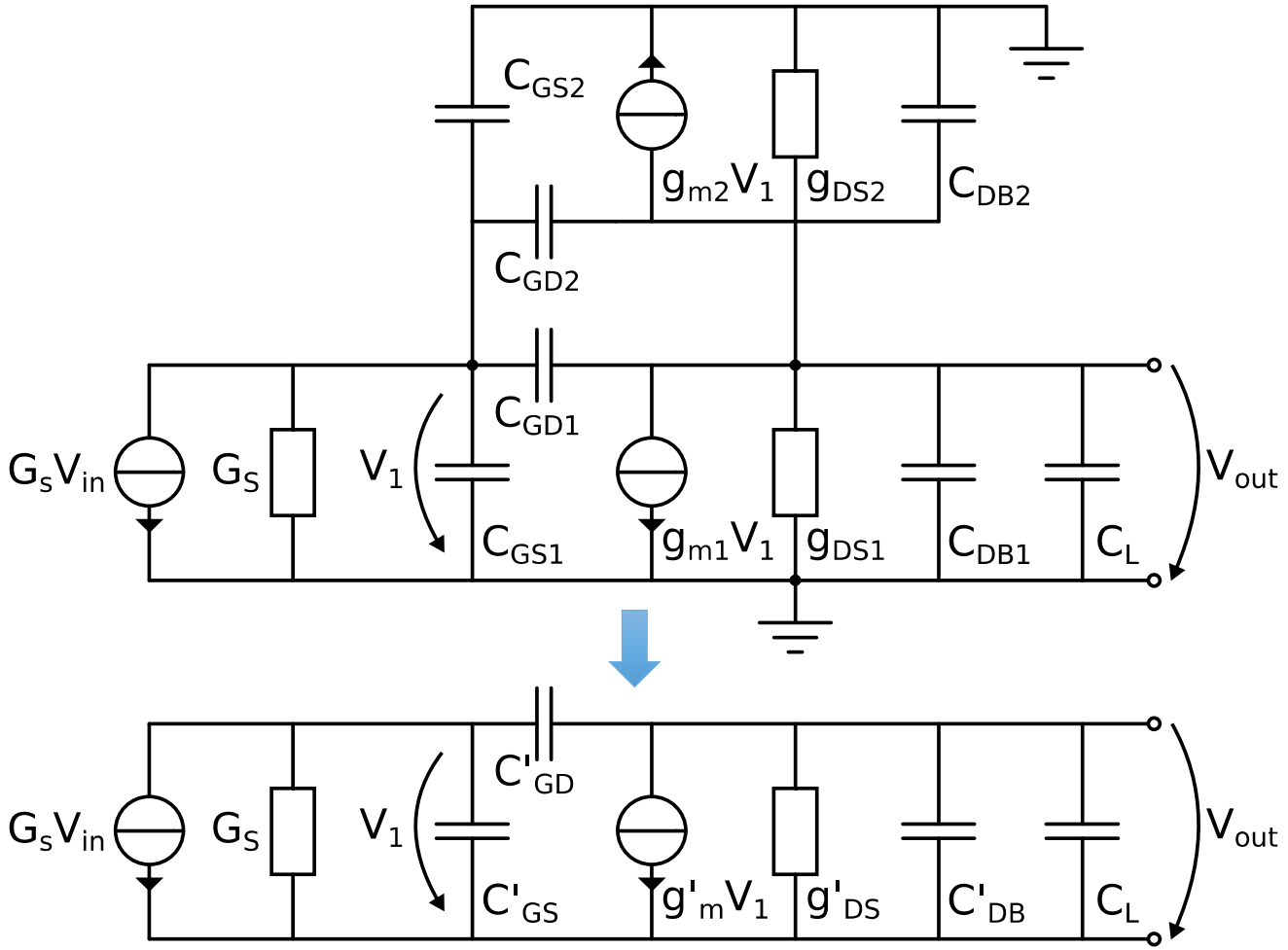
$$P_L = \frac{-\left(g_{DS1}+g_{DS2}\right)}{C_L'}$$

Assume: $p_L << p_{in}$ (in fig. $p_1=p_L$ and $p_2=p_{in}$)

$$GBW = A_0 p_L = \frac{g_{m1}}{C_L'}$$

PUSH-PULL SINGLE STAGE AMPLIFIER





$$g'_m = g_{m1} + g_{m2}$$

$$C'_{GS} = C_{GS1} + C_{GS2}$$

$$C'_{GD} = C_{GD1} + C_{GD2}$$

$$g'_{DS} = g_{DS1} + g_{DS2}$$

$$C'_{DB} = C_{DB1} + C_{DB2}$$

Results of the resistive loaded case are used to characterise the push-pull amplifier:

$$A(s) = \frac{-A_0\left(1+\frac{s}{s_Z}\right)}{\left(1+\frac{s}{p_{in}}\right)\left(1+\frac{s}{p_L}\right)}$$

DC amplification:

$$A_0 = \frac{g_{m1}+g_{m2}}{g_{DS1}+g_{DS2}} = \frac{-g_m'}{G_L'}$$

Poles (Millers theorem):

$$P_{in} = \frac{-G_s}{C_{GS1}+C_{GS2}+\left(1+\frac{g_{m1}+g_{m2}}{g_{DS1}+g_{DS2}}\right)\left(C_{GD1}+C_{GD2}\right)}$$

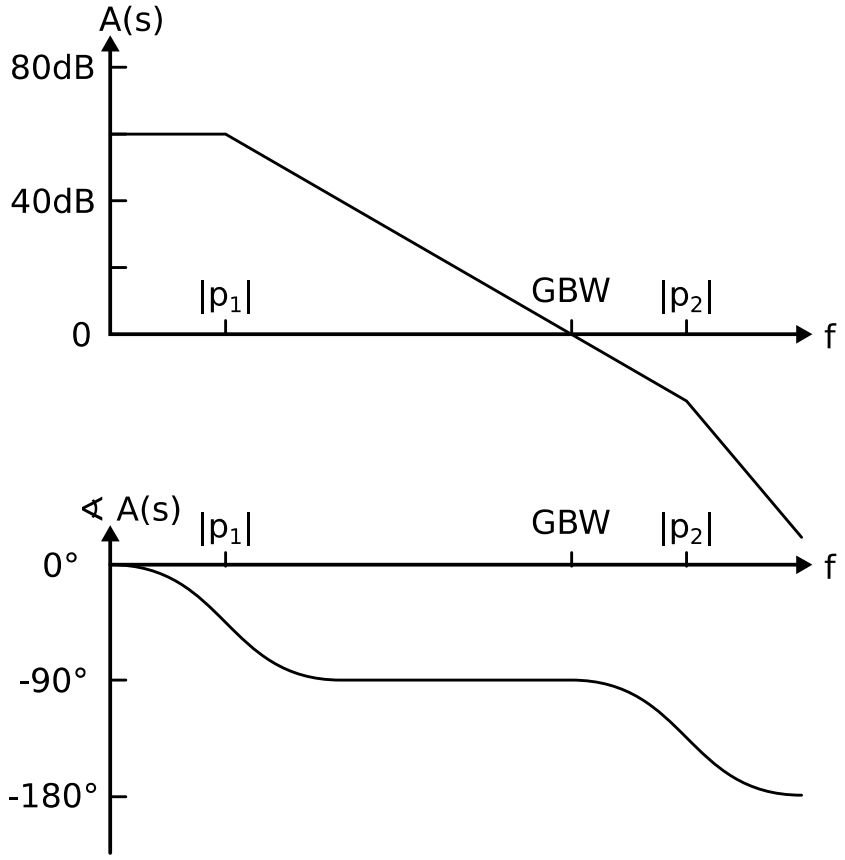
$$p_L = \frac{-\left(g_{DS1}+g_{DS2}\right)}{C_L'} = \frac{-\left(g_{DS1}+g_{DS2}\right)}{C_L+C_{DB1}+C_{DB2}}$$

Zero:

$$Z = \frac{g_{m1}+g_{m2}}{C_{GD1}+C_{GD2}} = \frac{g_m'}{C_{GD1}'}$$

Gain bandwidth:

$$GBW = \frac{g_{m1}+g_{m2}}{C_L'} (= A_0|p_L|)$$



Due to double g_m the gain and gain-bandwidth are doubled compared with the current source biased case. Here both transistors are active.

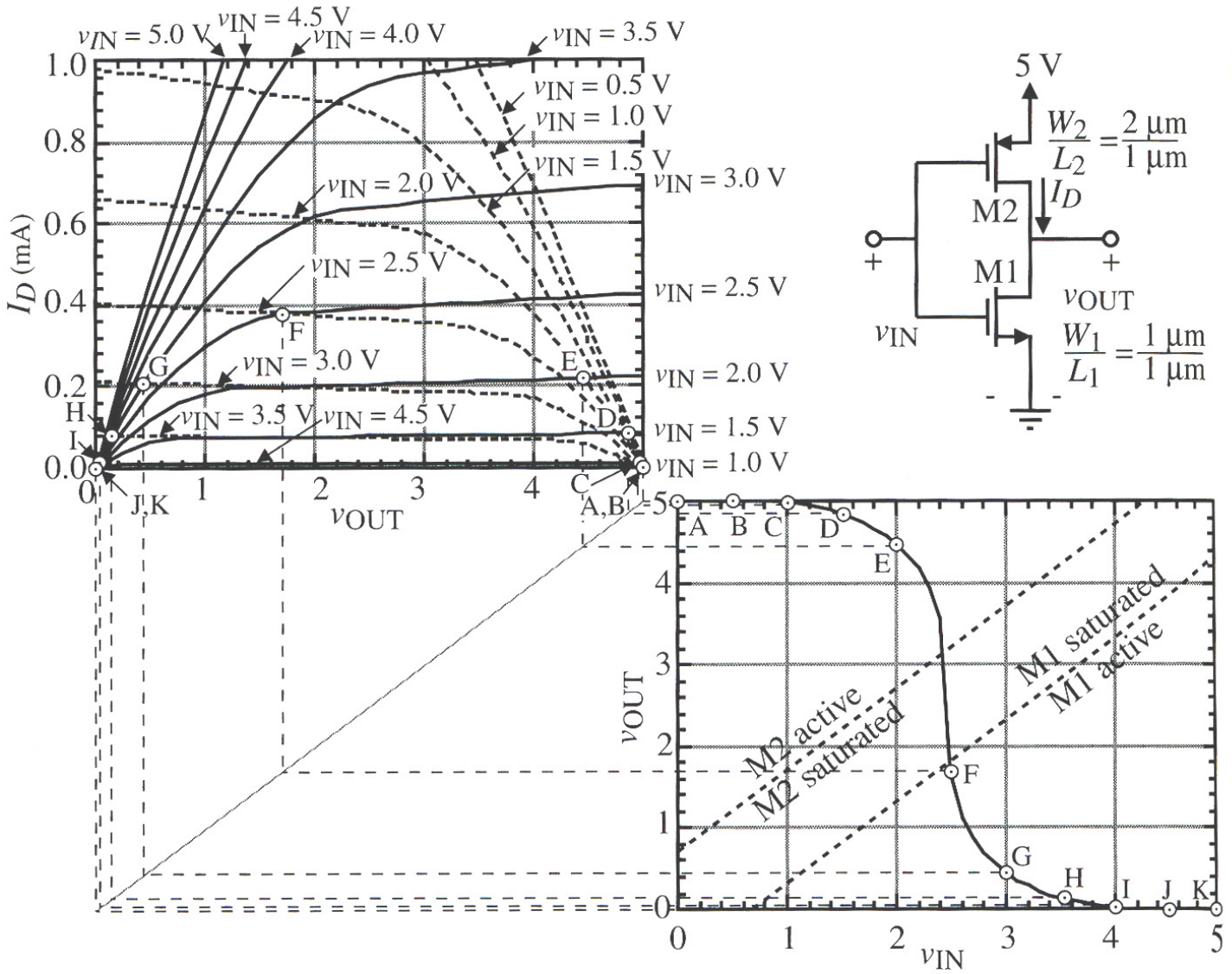
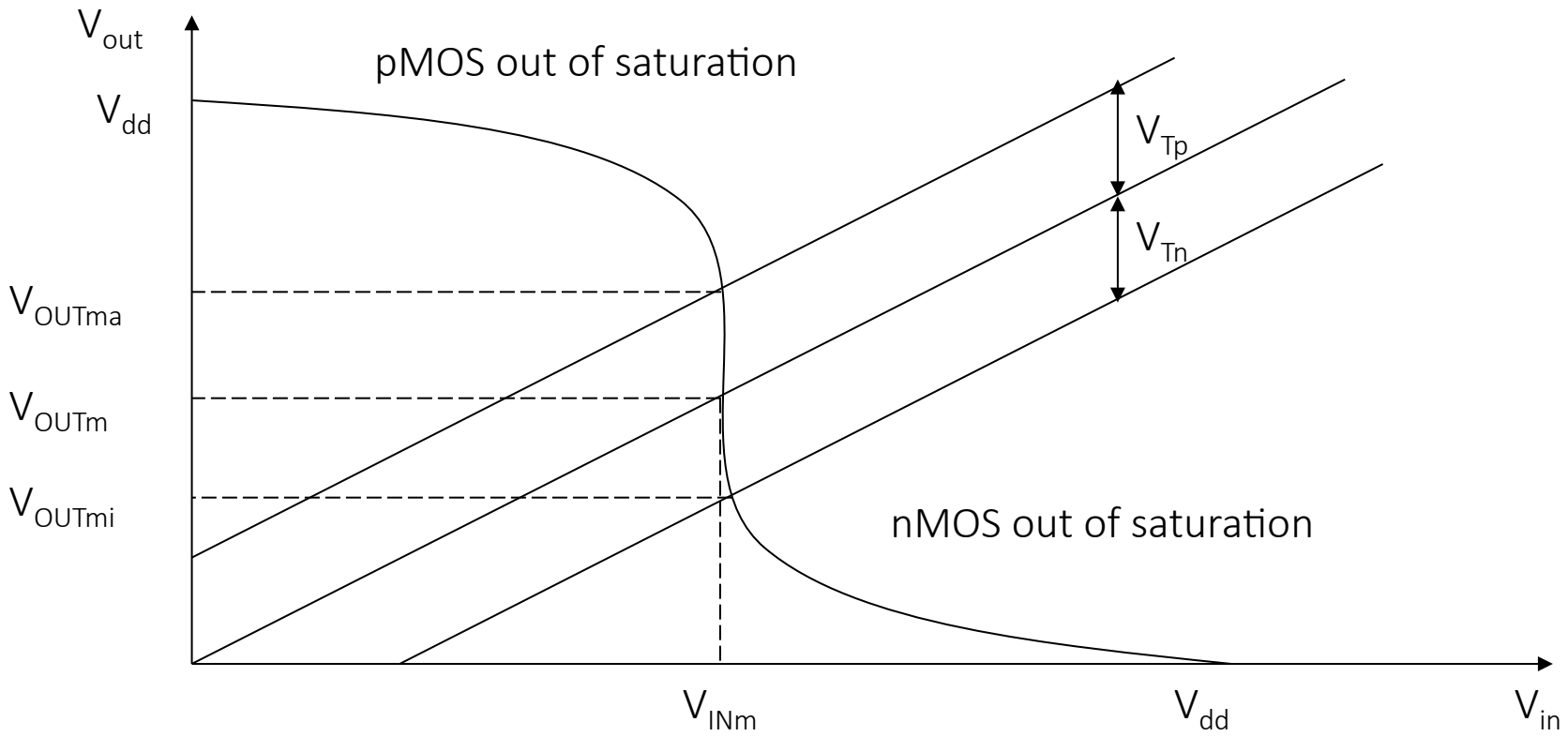


Figure 5.1-8 Graphical illustration of the voltage-transfer function for the push–pull inverter.


V_out
V_dd
pMOS out of saturation
V_Tp
V_Tn
V_OUTma
V_OUTm
V_OUTmi
nMOS out of saturation
V_INm
V_dd
V_in

Push-pull inverter output range

Maximum linear output signal range:

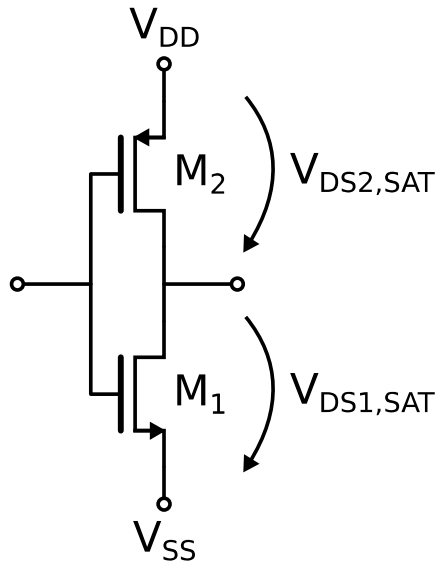
$$\max\{\Delta V_{OUT}\} = \frac{1}{2}\left(V_{DD} - V_{DS1,SAT} - V_{DS2,SAT}\right)$$

$$V_{DS1,SAT} = V_{GS} - V_{T1} = \frac{1}{2}V_{DD} - V_{T1}$$

$$V_{DS2,SAT} = V_{GS} - V_{T2} = \frac{1}{2}V_{DD} - V_{T2}$$

$$\max\{\Delta V_{OUT}\} = \frac{1}{2}\left(V_{DD} - \frac{1}{2}V_{DD} + V_{T1} - \frac{1}{2}V_{DD} + V_{T2}\right)$$

$$= \frac{1}{2}\left(V_{T1} + V_{T2}\right) \approx V_{T1} = V_{T2}$$



How to increase the output range:

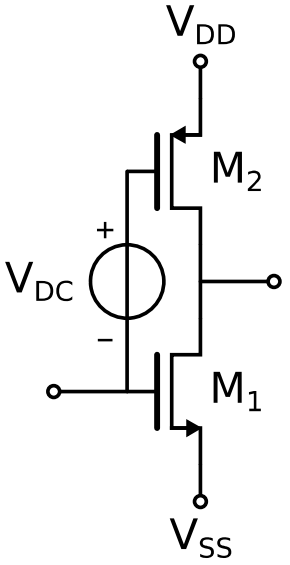
$$V_{GS1} + V_{GS2} = V_{DD} - V_{DC}$$

$$\max\{\Delta V_{out}\} = \frac{1}{2}\left(V_{DD} - \left(V_{GS1} - V_{T1}\right) - \left(V_{GS2} - V_{T2}\right)\right)$$

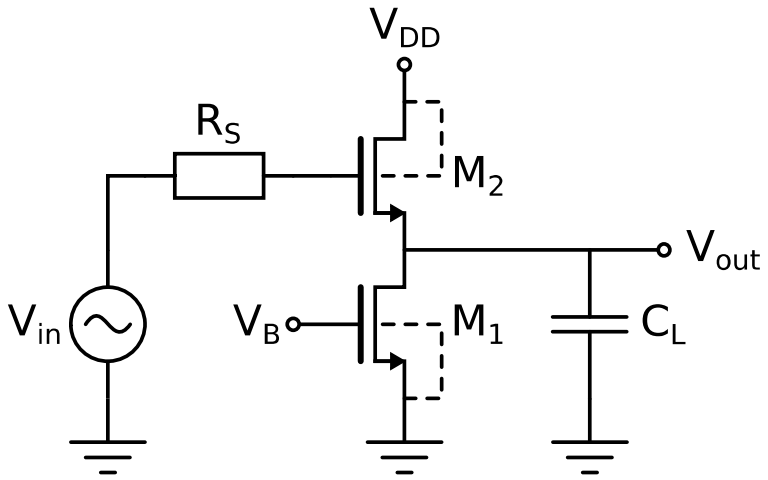
$$= \frac{1}{2}\left(V_{DD} - \left(V_{GS1} + V_{GS2}\right) + V_{T1} + V_{T2}\right)$$

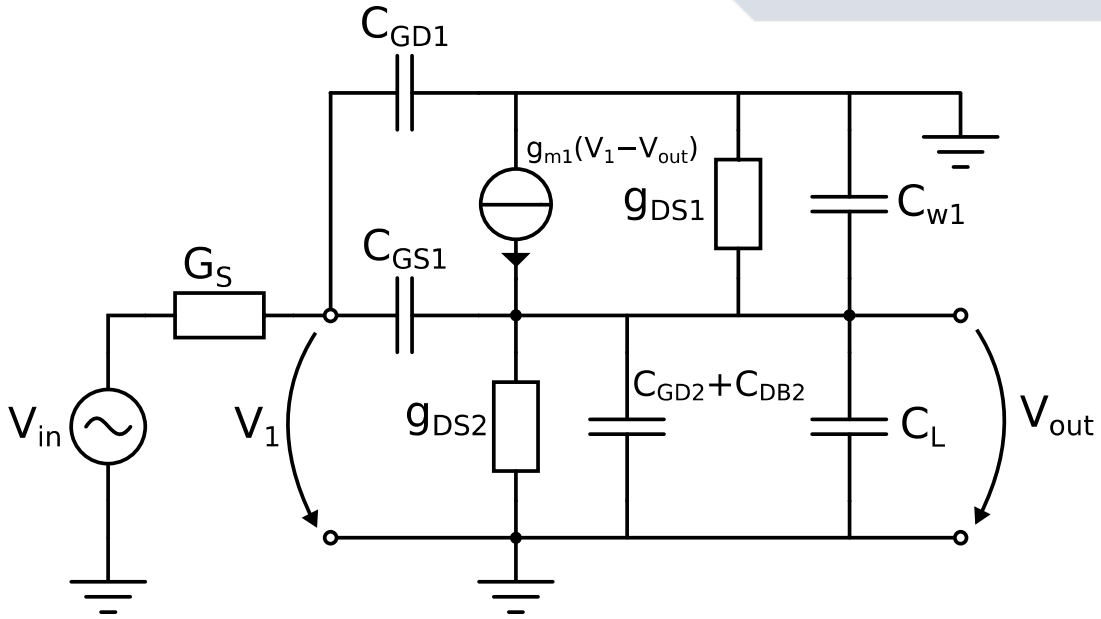
$$= \frac{1}{2}\left(V_{DD} - V_{DD} + V_{DC} + V_{T1} + V_{T2}\right)$$

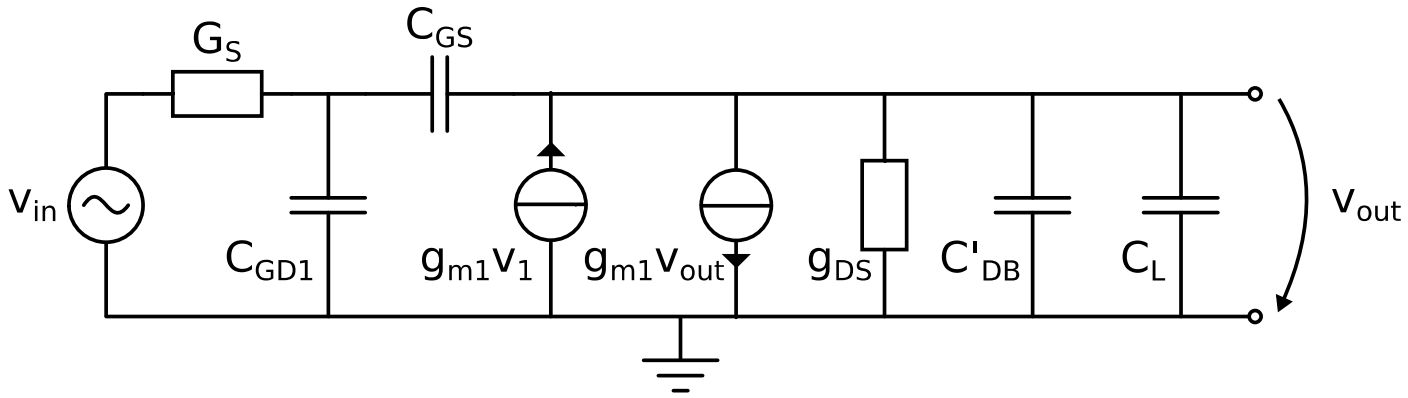
$$= \frac{1}{2}\left(V_{DC} + V_{T1} + V_{T2}\right) = \frac{1}{2}V_{DC} + V_T \quad , V_{T1} = V_{T2}$$



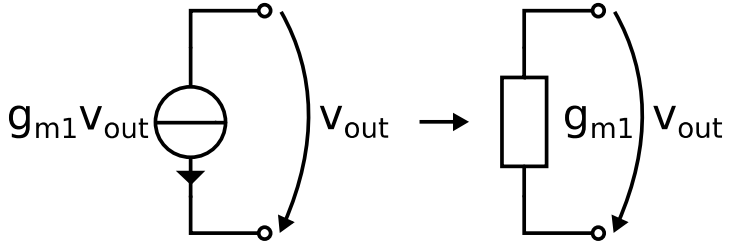
SOURCE FOLLOWER







Replace:



Results of the resistive loaded case are used to characterise the source follower (small signal circuit diagram is same):

$$A(s) = \frac{A_0\left(1+\frac{s}{s_Z}\right)}{\left(1+\frac{s}{p_{in}}\right)\left(1+\frac{s}{p_L}\right)}$$

Gain: $A_0 = \frac{g_{m1}}{g_{m1}+g_{DS1}+g_{DS2}} \le 1$

Zero: $z = \frac{g_{m1}}{C_{GS1}}$

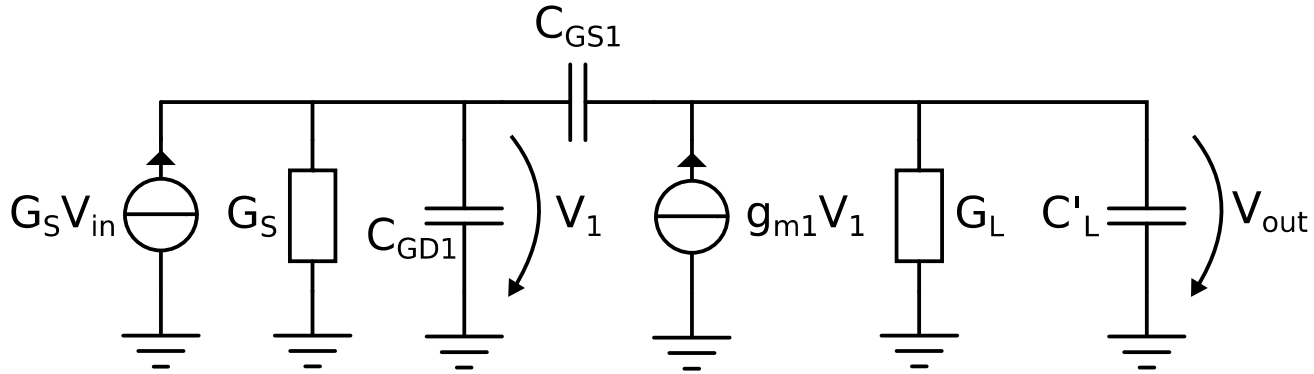
Poles: $p_{in} = \frac{-G_S}{C_{GD1}+C_{GS1}}$

Miller capacitor C_{GD} has no effect, as

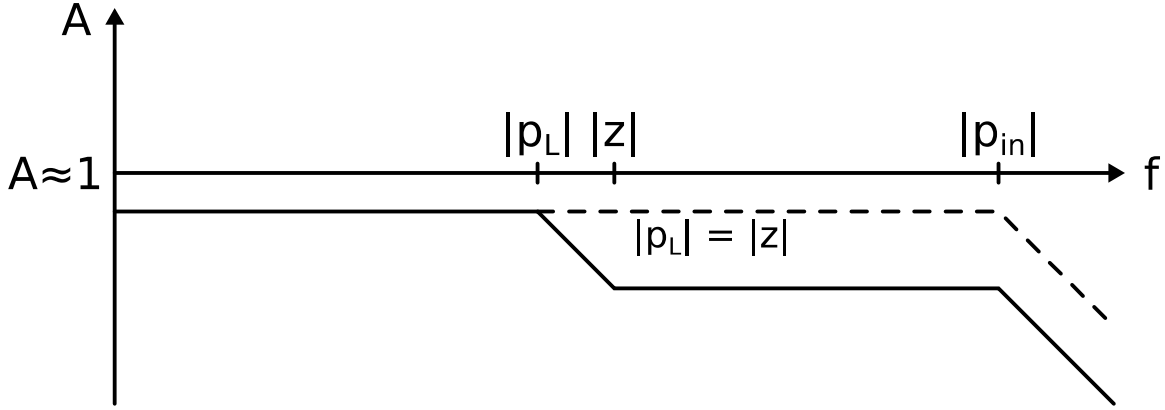
$$p_L = \frac{-(g_{m1}+g_{DS1}+g_{DS2})}{C_L+C_{GS1}+C_{DB2}+C_w}$$

Unity gain bandwidth:

$$GBW = A_0 p_L = \frac{g_{m1}}{C_L'}$$

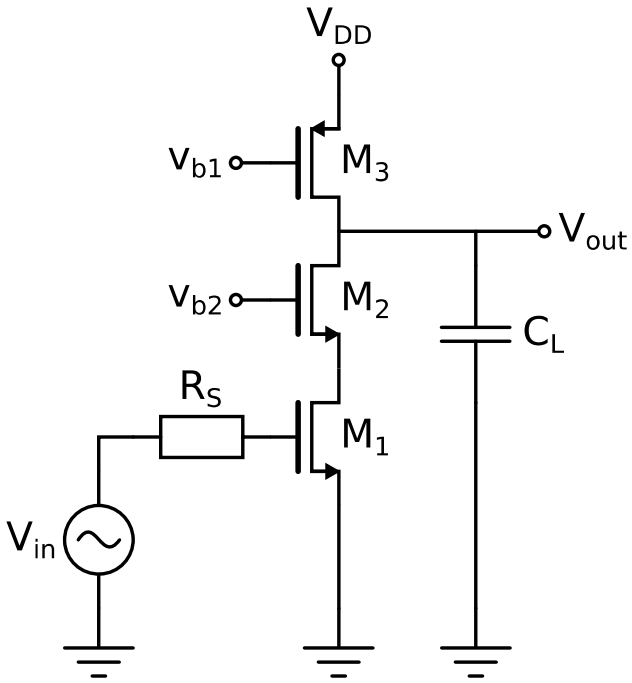


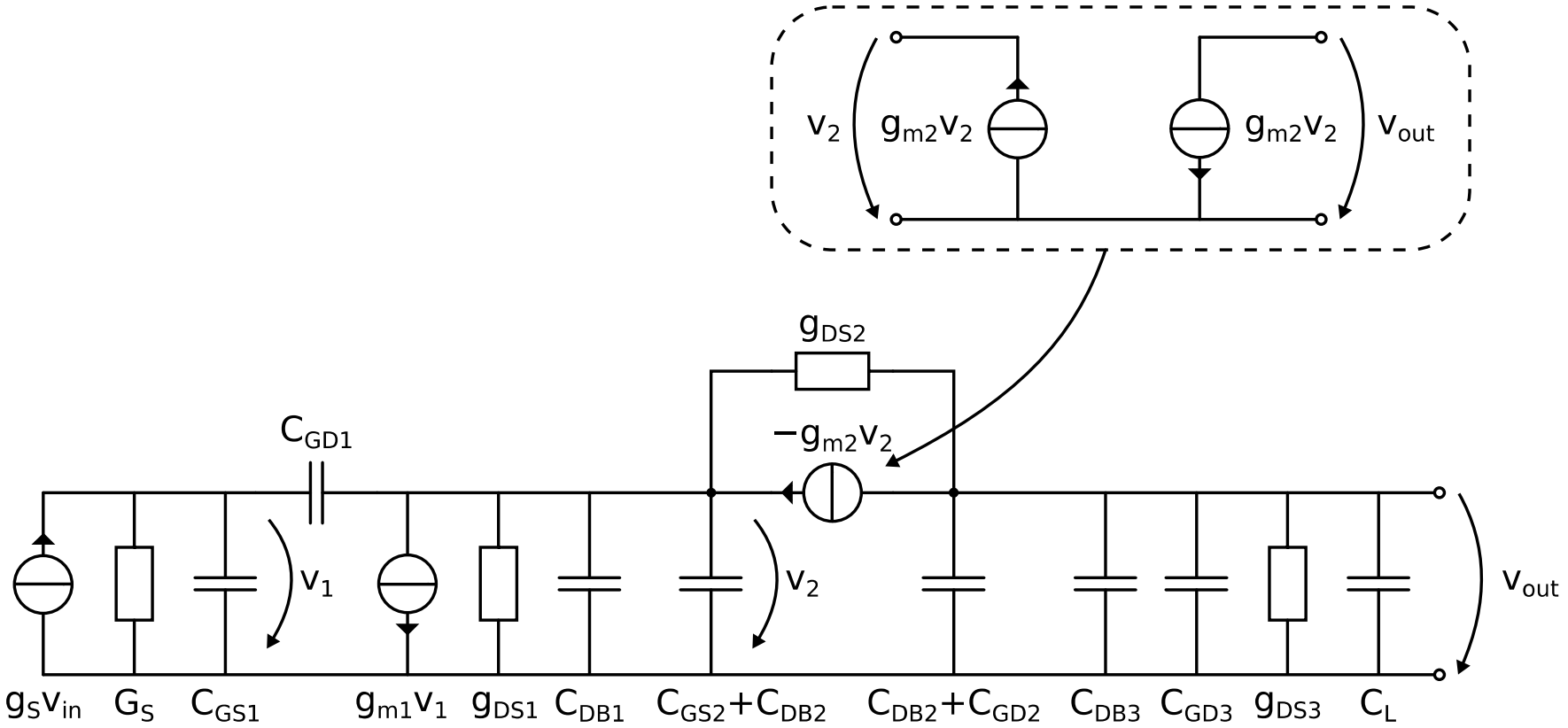
$G_L = g_{DS1}+g_{DS2}+g_{m1}$



$p_L = z \Longrightarrow GBW \longrightarrow \infty$

CASCODE AMPLIFIER





Transferfunction:

$$A(s) = \frac{-A_0\left(1+\frac{s}{s_z}\right)}{\left(1+\frac{s}{p_{in}}\right)\left(1+\frac{s}{p_2}\right)\left(1+\frac{s}{p_L}\right)}$$

Gain:

$$A_0 = \frac{g_{m1}}{g_{DS1}+g_{m2}} * \frac{g_{m2}}{g_{DS3}} \approx \frac{g_{m1}}{g_{DS3}}$$

Poles:

$$P_{in} = \frac{-G_s}{C_{GS1}+\frac{g_{m1}}{g_{m2}}C_{GD1}} \approx \frac{-G_s}{C_{GS1}}$$

$$P_2 = \frac{g_{m2}}{C_{DB1}+C_{DB2}+C_{GS2}}$$

$$P_L = -\frac{g_{DS3}}{C_L'}$$

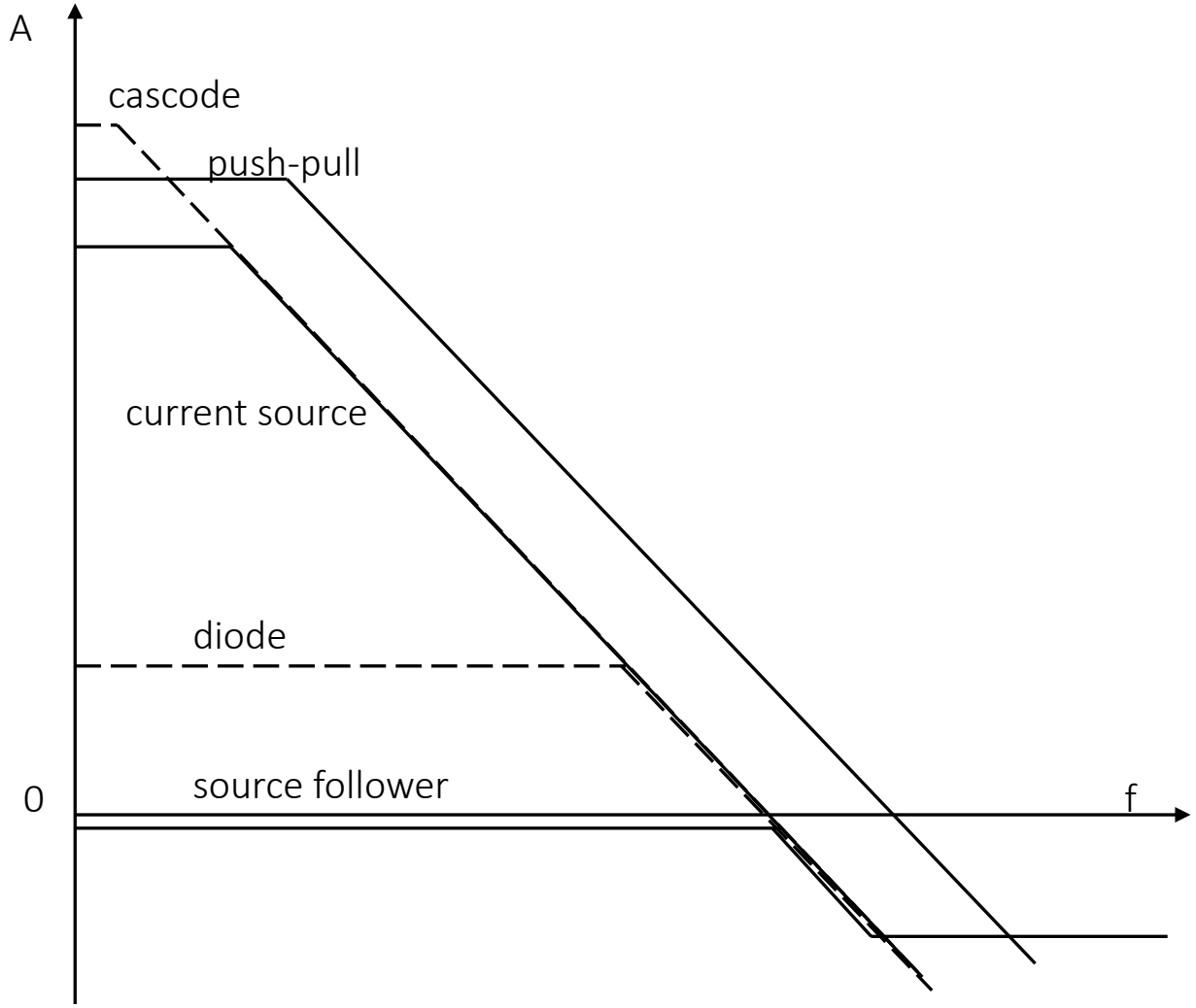
Zero:

$$Z = \frac{g_{m1}}{C_{GD1}}$$

Unity gain bandwidth:

$$GBW = A_0|p_L| = \frac{g_{m1}}{C_L'}$$

Comparison of single stage amplifiers



Design trade-offs in single stage amplifiers

Gain $A_0 = f(W,L,I_D)$

In general $A_0 = \dfrac{-g_m}{G_L}$

1) Diode loaded: $G_L \approx g_{m2}$

$$g_m = \sqrt{2\mu C_{OX} I_D \frac{W}{L}}$$

$$A_0 = \frac{-g_m}{g_{m2}} = -\sqrt{\frac{\mu_n (W/L)_1}{\mu_p (W/L)_2}}$$

$A_0 = 10$

$$\Rightarrow \frac{(W/L)_1}{(W/L)_2} \approx 100$$

2) Current source load:

$G_L = g_{DS1} + g_{DS2}$

$g_{DS} = \dfrac{I_D}{LV_E}$; V'_E=Early voltage (normalized with L)

assume $L_1 = L_2 = L$

$$\boxed{A_o = \frac{-\sqrt{2\mu C_{OX} W_1 L V'_E}}{2\sqrt{I_D}}}$$

$|A_o| \uparrow \Rightarrow I_D \downarrow$ or $W_1 \uparrow$ or $L \uparrow$

$I_D \downarrow : \Rightarrow$ Transistor enters the weak inversion region :

$g_m = \dfrac{qI_D}{2kT}$

$$\boxed{A_o = \frac{-gLV'_E}{2kT}}$$

Unity gain bandwidth GBW = f(W,L,I_d)

$$GBW = \frac{g_{m1}}{C_L''}$$

$$g_{m1} = \sqrt{2\mu_n C_{ox} I_D \left(\frac{W}{L}\right)_1}$$

$$C_L'' = C_{DB1} + C_{DB2} + C_L + C_{GS2}$$

$$= W_1 C_{DB}' + W_2 C_{DB}' + W_2 L_2 C_{ox} + C_{LO}$$

$$= W_1 C_{DB}' + C_L'$$

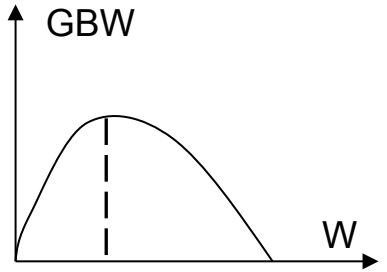
$$\Rightarrow GBW = \frac{\sqrt{2\mu_n C_{ox} I_D \left(\frac{W}{L}\right)_1}}{W_1 C_{DB}' + C_L'}$$

$GBW \uparrow \Rightarrow \left(\frac{W}{L}\right)_1 \uparrow$ tai $I_D \uparrow$

assume $L_1 = \min\{L\}$

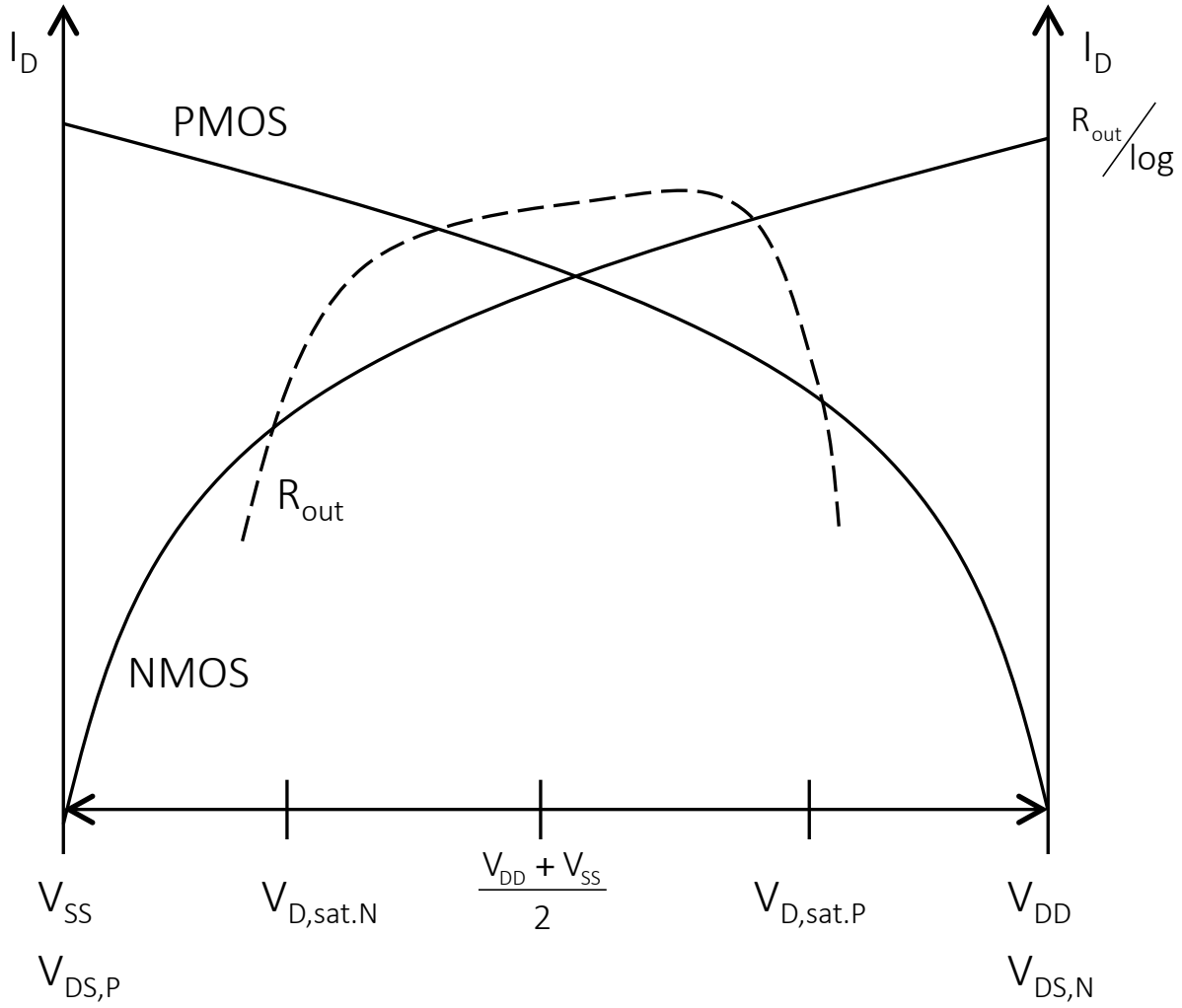
$\underline{\underline{W}} \uparrow : (I_D = \text{constant})$

$$\max\{GBW\} = GBW\Big|_{W_1 = \frac{C_L'}{C_{DB}'}} = \frac{\sqrt{\mu_n C_{ox} I_D / L_1}}{2\sqrt{C_L' C_{DB}'}}$$



$$W = \frac{C_L'}{C_{DB}'}$$

Gain linearity



$$\underline{\underline{I_D \uparrow}}: \quad \Rightarrow V_{D,SAT} = \sqrt{\frac{2I_D}{\mu C_{ox}\left(\frac{W}{L}\right)_1}} \quad \uparrow$$

$\Rightarrow$ linear range shrinks!

maintain linear range:

$$V_{D,SAT} = \text{constant} \Rightarrow I_D' = aI_D \Rightarrow W' = aW \quad \text{assume } L = \min\{L\}$$

$$GBW = \frac{a\sqrt{2\mu C_{OX} I_D \left(\frac{W}{L}\right)_1}}{aW_1 C_{DB}' + C_L'}$$

$$\Rightarrow \max\{GBW\} = \lim_{a\to\infty} GBW = \frac{\mu C_{OX} V_{D,SAT}}{2L_1 C_{DB'}}$$