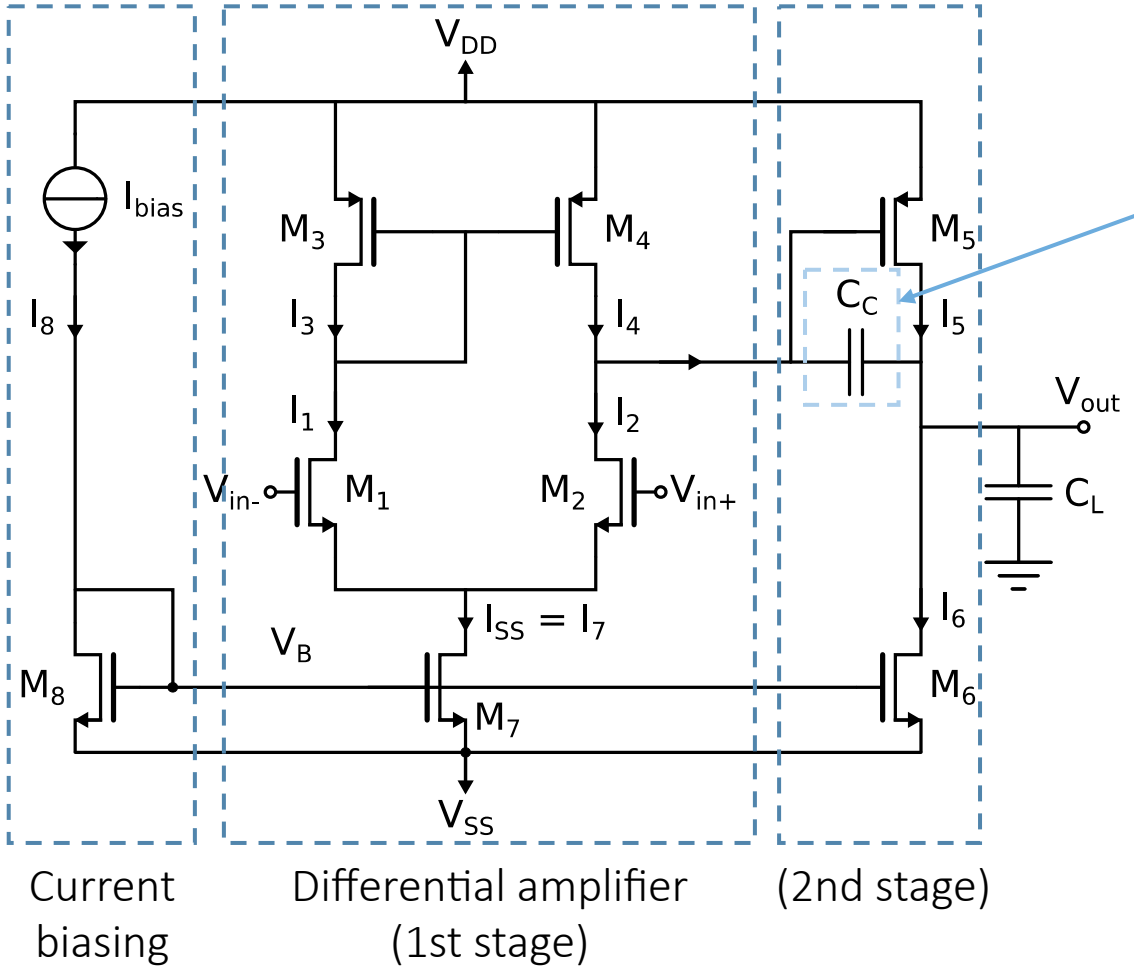
ELEC-E3510 Basics of IC Design

Lecture 4:
Differential amplifier and
Current sources

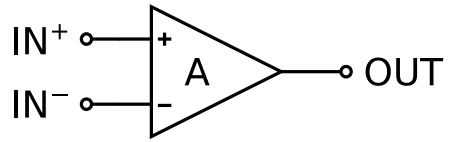
Operational amplifier



Compensation

- 2 gain stages (80…120dB)
- Differential input stage
- Miller compensation
- Current biasing

Symbol:



Differential amplifier

Source-coupled pair

Assume M1 and M2 are equal and in saturation

$$I_D = k(V_{GS} - V_T)^2 \qquad k = \frac{\mu C_{ox}}{2} \cdot \frac{W}{L}, \; k_1 = k_2$$

Current and voltage equations:

$$\begin{cases} I_1 + I_2 = I_{SS} \\ V_{in} = V_{GS1} - V_{GS2} \\ I_1 = k(V_{GS1} - V_T)^2 \\ I_2 = k(V_{GS2} - V_T)^2 \end{cases}$$

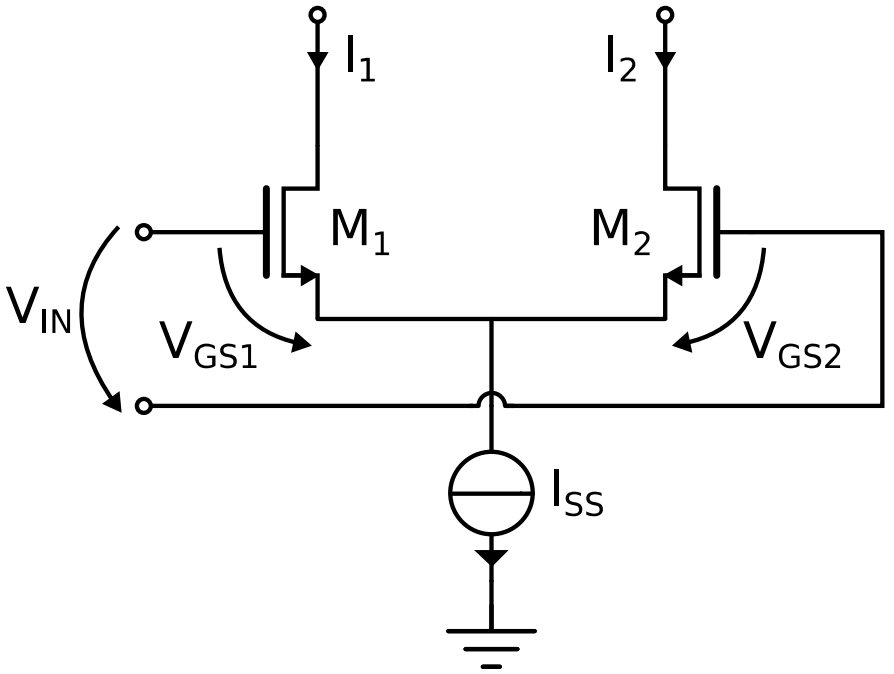
Solve I_1 and I_2

$$I_1 = \frac{k}{2}\left(\sqrt{\frac{I_{SS}}{k} - \frac{V_{in}^2}{2}} + \frac{V_{in}}{\sqrt{2}}\right)^2$$

$$I_2 = \frac{k}{2}\left(\sqrt{\frac{I_{SS}}{k} - \frac{V_{in}^2}{2}} - \frac{V_{in}}{\sqrt{2}}\right)^2$$

Output difference current

$$\Delta I = I_1 - I_2 = kV_{in}\sqrt{\frac{2I_{SS}}{k} - V_{in}^2}$$



when $V_{in} = 0$ then $I_1 = I_2 = \frac{I_{SS}}{2}$

with large input voltages

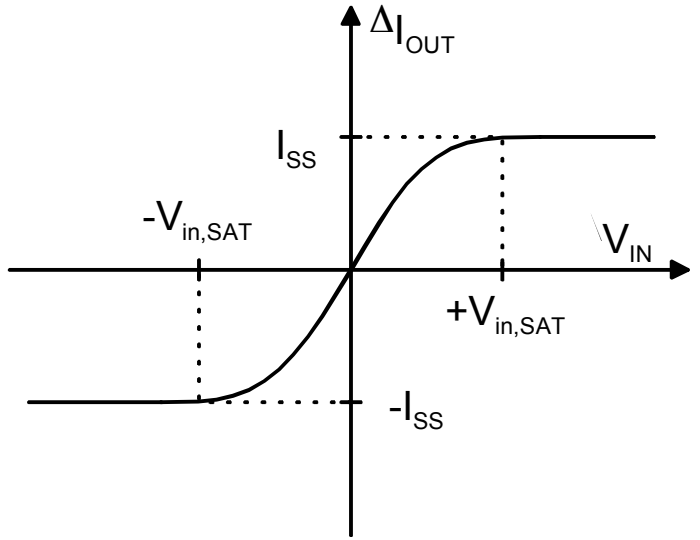
saturation: either $I_1 = I_{SS}, I_2 = 0$

or $I_1 = 0, \quad I_2 = I_{SS}$

All bias current flows through M_1 (or M_2) and M_2 (or M_1) are closed

Input saturation voltage

$$V_{in,SAT} = \pm\sqrt{\frac{I_{SS}}{k}} = \pm\sqrt{2}V_{DS_1SAT_1M1}$$



with small input voltage i.e.

$$V_{in} << \sqrt{\frac{I_{SS}}{k}}$$

$$\Rightarrow \quad \Delta I_{OUT} \approx kV_{in}\sqrt{\frac{2I_{SS}}{k}}$$

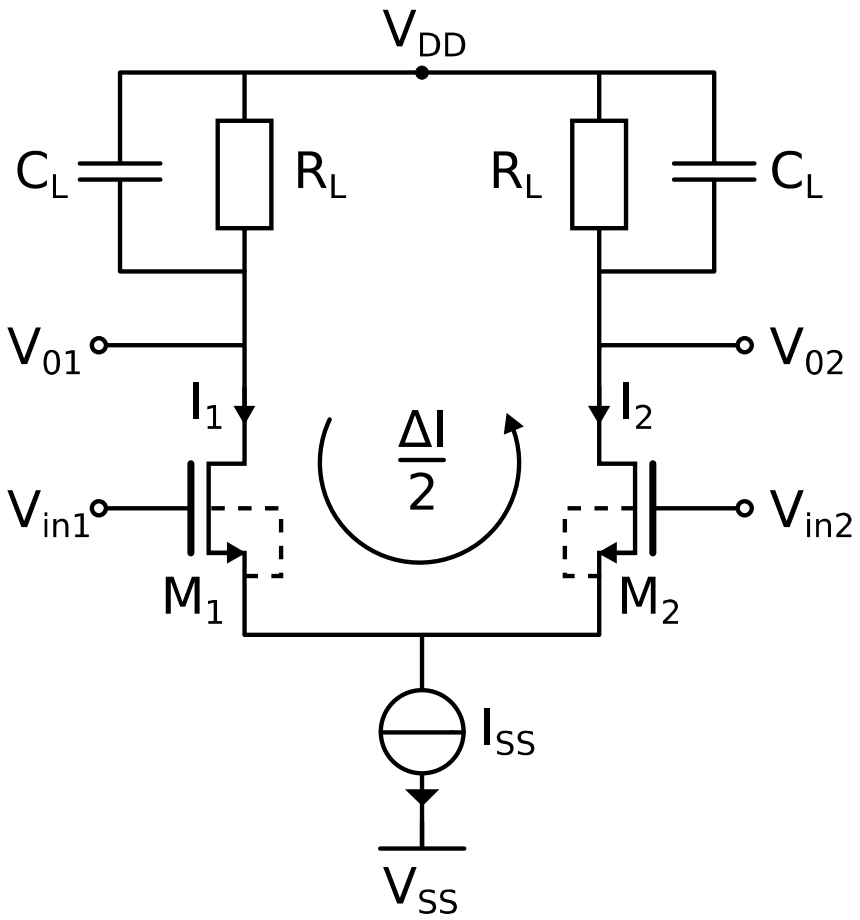
$$= \sqrt{2k \cdot I_{SS}} \cdot V_{in}$$

$$\Delta I_{OUT} = g_{m1} \cdot V_{in}$$

$$;g_{m1} = \sqrt{2\mu C_{OX}\frac{W}{L}\frac{I_{SS}}{2}}$$

$$k = \frac{1}{2}\mu C_{OX}\frac{W}{L}$$

Gain of source-coupled pair



Assume $V_{in}=V_{in1}-V_{in2}$ is small and assign

$$V_{in1} = \frac{V_{in}}{2} \text{ ja } V_{in2} = -\frac{V_{in}}{2}$$

$$I_1 \approx \frac{I_{SS}}{2} + g_{m1}\frac{V_{in}}{2} = \frac{I_{SS}}{2} + \frac{\Delta I}{2}$$

$$I_2 \approx \frac{I_{SS}}{2} - g_{m2}\frac{V_{in}}{2} = \frac{I_{SS}}{2} - \frac{\Delta I}{2}$$

$$g_{m1} = g_{m2} = g_m$$

No signal current flows into tail current source

$\Rightarrow$ ”virtual ground”

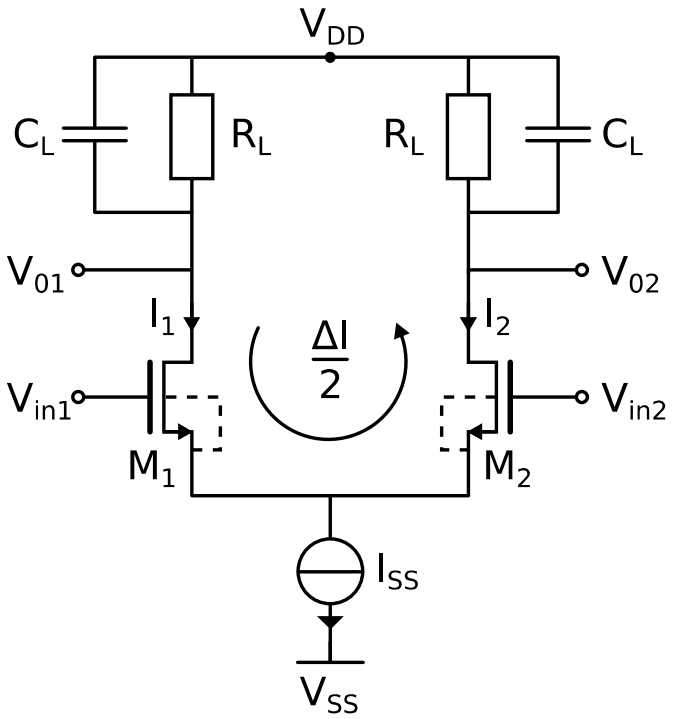
Small signal gain with load resistor R_L

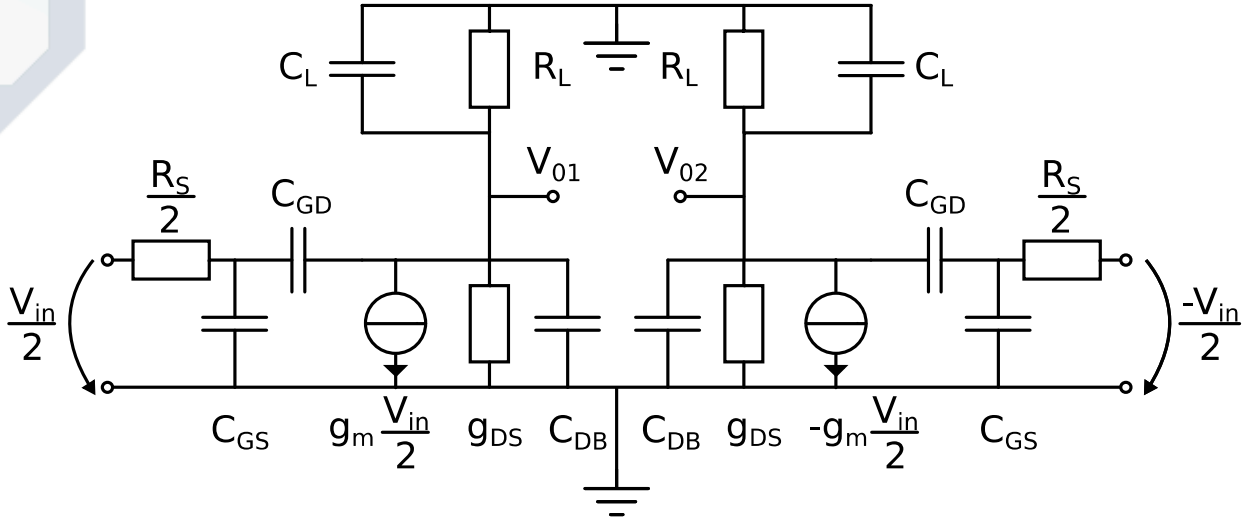
$$\begin{aligned}\Delta V_{OUT} &= I_1 R_L - I_2 R_L \\ &= (I_1 - I_2) R_L \\ &= g_{m1} V_{in} R_L\end{aligned}$$

Solve for gain

$$\Rightarrow A_0 = \frac{\Delta V_{OUT}}{V_{in}} = g_{m1} R_L$$

AC analysis





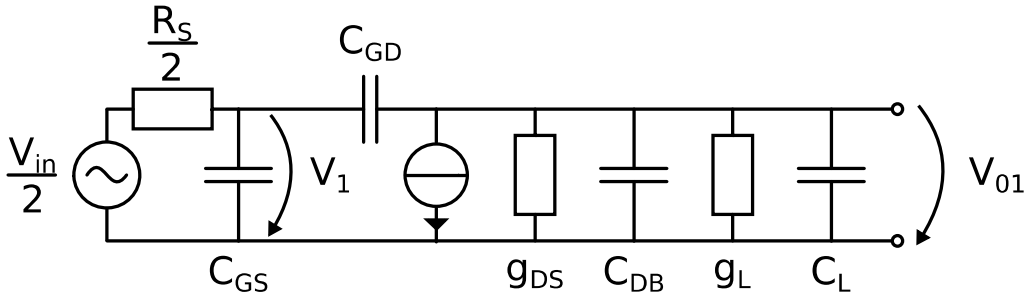
No current flow into tail current source I_{SS} $\Rightarrow$ "virtual ground"

Assign $V_{in1} = \frac{V_{in}}{2}$ and $V_{in2} = -\frac{V_{in}}{2}$

M1 drives current $\frac{\Delta I}{2}$ into virtual ground

M2 draws current $\frac{\Delta I}{2}$ from virtual ground

It is adequate to study only left or right half circuit



$$V_{O1} = A(s)\frac{V_{in}}{2}$$

$$V_{O2} = A(s)\left(-\frac{V_{in}}{2}\right)$$

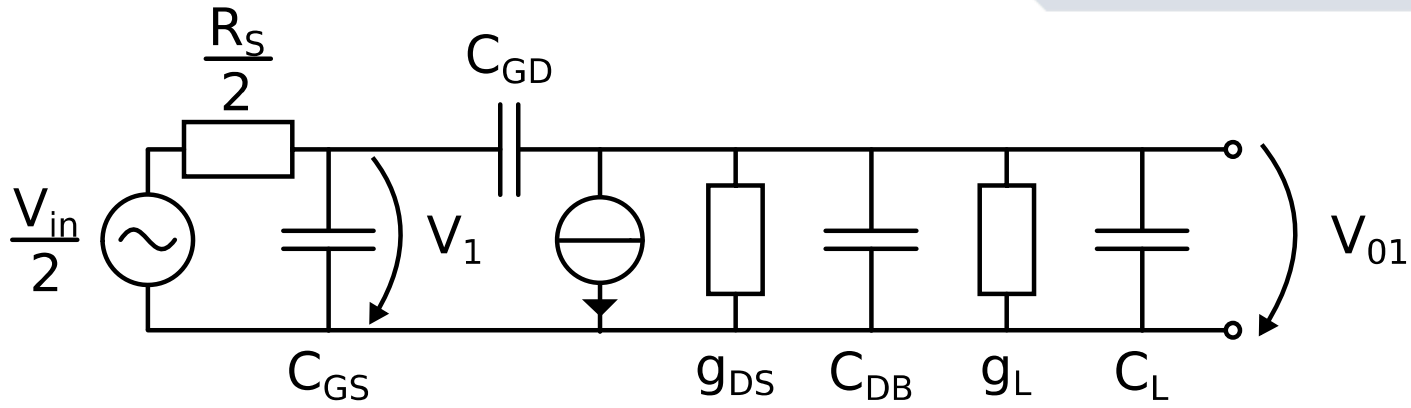
$$V_{OUT} = V_{O1} - V_{O2} \quad \Rightarrow \quad V_{OUT} = A(s)V_{in}$$

Small signal analysis

Single stage amplifier analysis

Gain transferfunction

$$A(s) = -\frac{g_{m1} - sC_{GD}}{(1 + sC_{GS}R_S)(g_{DS} + g_L + sC_L)}$$



Gain:

$$A_o = -\frac{g_{m1}}{g_{DS} + g_L}$$

Poles:

$$p_{in} = -\frac{1}{C_{GS}R_S}$$

$$p_L = -\frac{g_{DS} + g_L}{C_L'}$$

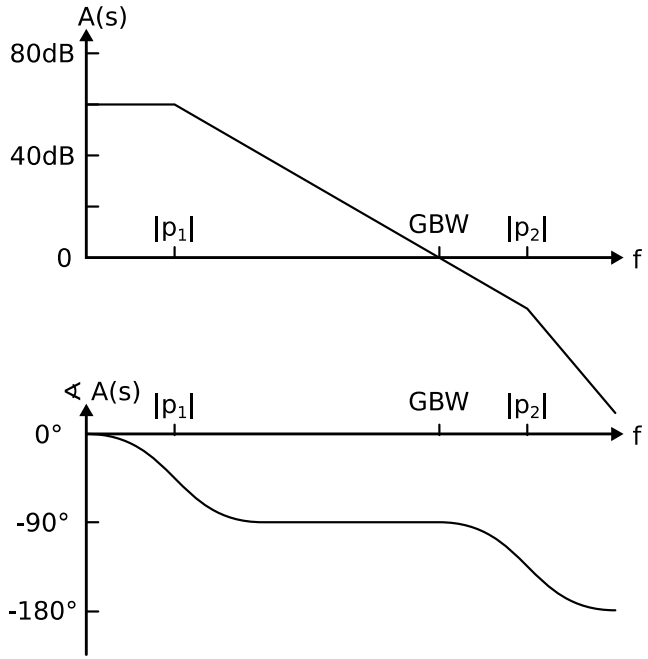
Zero:

$$z = \frac{g_{m1}}{C_{GD}}$$

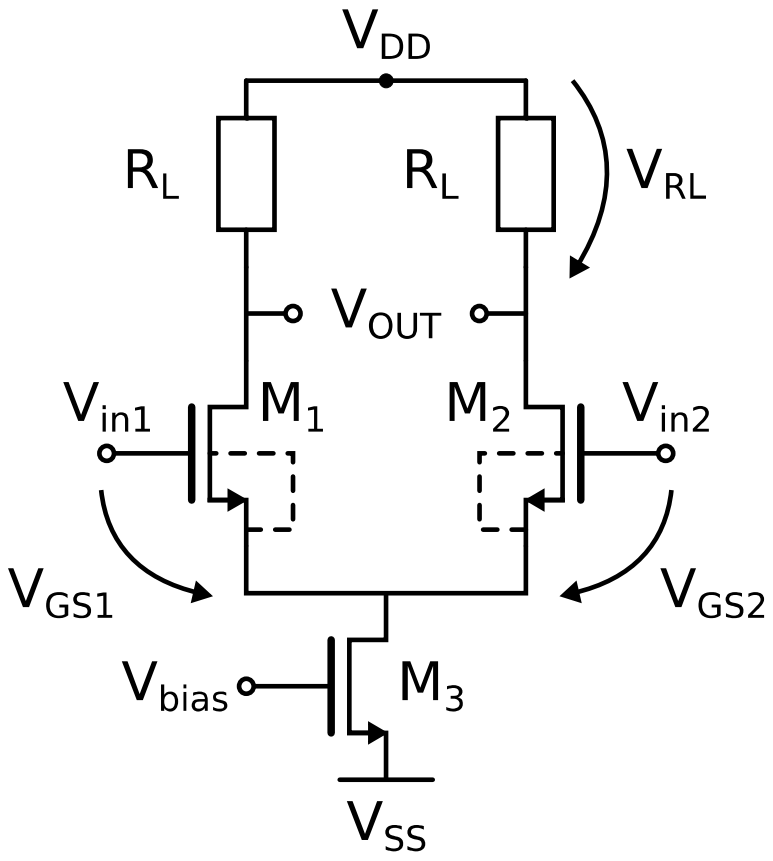
Unity gain bandwidth:
(in fig. p_1=p_L and p_2=p_{in})

$$GBW = \frac{g_{m1}}{C_L'}$$

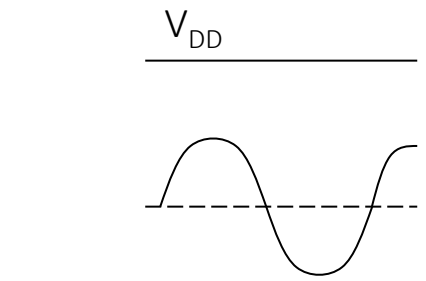
(assume p_L<<p_{in})



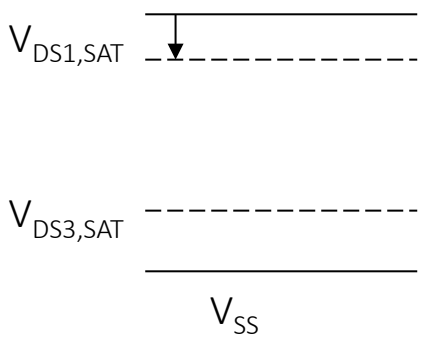
Common-mode and signal ranges



Assume source-coupled pair not saturated



$$V_{DD} - V_{RL} = V_{DD} - R_L \cdot \frac{I_{SS}}{2}$$



$$V_{in,CM} - V_{T1,2} = V_{DS1,SAT} + V_{S1,2}$$

$$V_{in,CM} - V_{GS1,2} = V_{in,CM} - \left(V_{DS1,SAT} + V_{T1,2}\right)$$

$$= V_{S1,2}$$

$$V_{DS3,SAT} = \sqrt{\frac{I_{SS}}{k_3}}$$

$$V_{DS1,SAT} = \sqrt{\frac{I_{SS}}{2k_1}} = V_{DS2,SAT}$$

Output signal range:

$$\max\{V_{OUT}\} = V_{DD}$$

$$\min\{V_{OUT}\} = V_{in,CM} - V_{T1}$$

$$\Delta V_{OUT} = V_{DD} - V_{in,CM} - V_{T1}$$

Input common-mode range:

maximum common-mode level:

$$V_{in,CM,MAX} - V_{T1} = V_{DD} - V_{RL} = V_{DD} - R_L \cdot \frac{I_{SS}}{2}$$

$$V_{in,CM,MAX} = V_{DD} - V_{RL} + V_{T1} = V_{DD} - R_L \cdot \frac{I_{SS}}{2} + V_{T1}$$

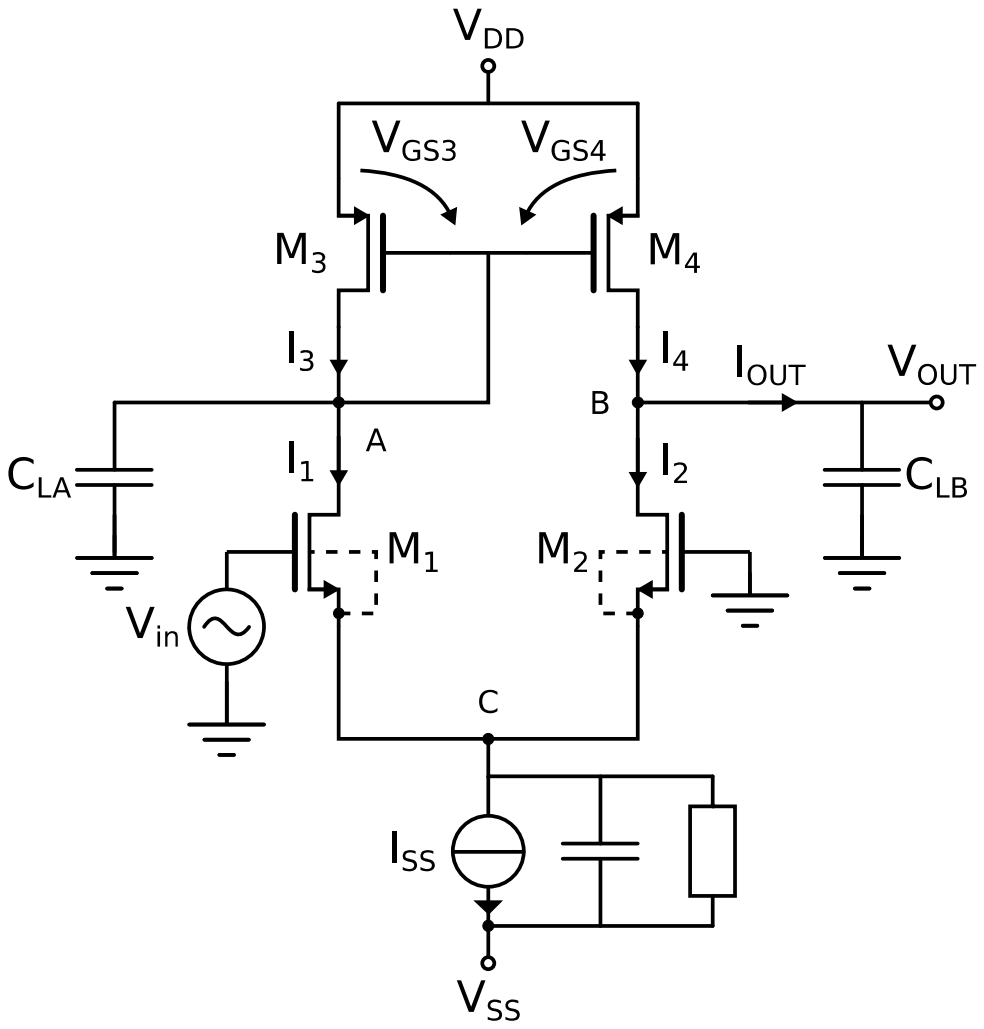
minimum common-mode level:

$$V_{in,CM,MIN} - V_{GS1} = V_{DS3,SAT} + V_{SS}$$

$$V_{in,CM,MIN} = V_{GS1} + V_{DS3,SAT} + V_{SS}$$

$$= V_{DS1,SAT} + V_{T1} + V_{DS3,SAT} + V_{SS}$$

Differential to single-ended conversion



Differential to single-ended conversion can be performed with a current mirror load M_3 and M_4
Assume a small input signal

$$\Delta I = I_1 - I_2 = g_m \Delta V_{in}$$

$$I_1 = \frac{I_{SS} + \Delta I}{2}$$

$$I_2 = \frac{I_{SS} - \Delta I}{2}$$

Assume equal transistors M_3 and M_4

$$V_{GS3} = V_{GS4}$$

$$\Rightarrow I_4 = I_3 = I_1$$

Current equation at output

$$I_{OUT} = I_4 - I_2 = I_1 - I_2$$

$$= \frac{I_{SS} + \Delta I}{2} - \frac{I_{SS} - \Delta I}{2}$$

$$= \Delta I$$

$$I_{OUT} = g_m \Delta V_{in}$$

Current equations at nodes A and B

$$(A)\quad g_{m1}\bullet\frac{V_{in}}{2}=-\left(g_{m3}+g_{DS1}+g_{DS3}+sC'_{LA}\right)V_A$$

$$(B)\quad -g_{m2}\left(-\frac{V_{in}}{2}\right)-g_{m4}V_A=\left(g_{DS2}+g_{DS4}+sC'_{LB}\right)V_B$$

$C_{LA}' = C_{LA} + C_{DB1}$ and $C_{LB}' = C_{LB} + C_{DB2}$

Eliminate V_A and assign $V_{out} = V_B$

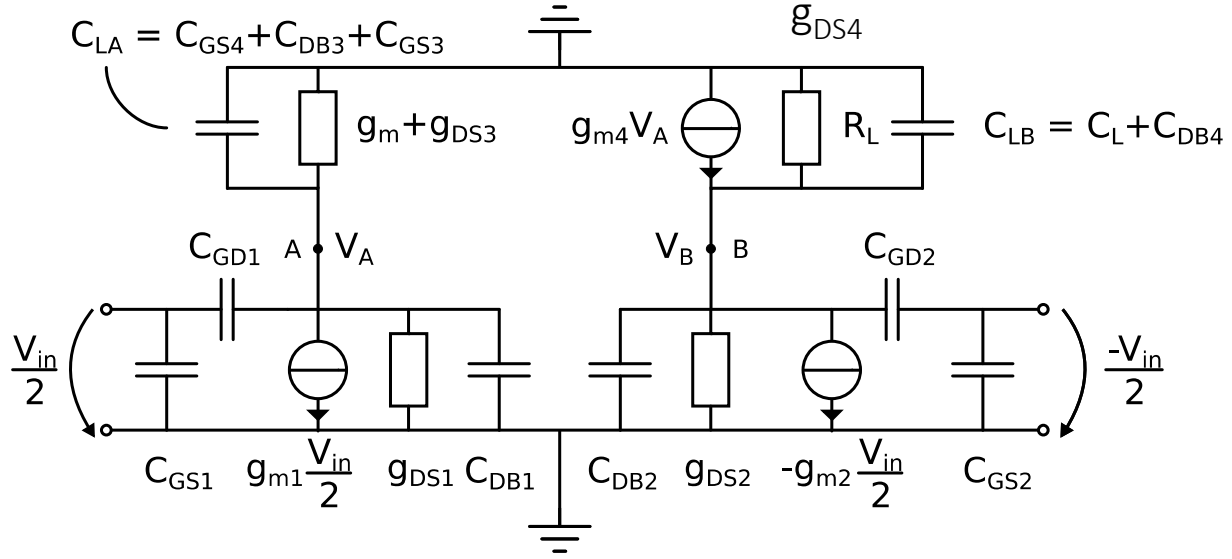
$$\frac{V_B}{V_{in}}=\frac{V_{out}}{V_{in}}=\frac{1}{2}\frac{g_{m3}+g_{m4}+g_{DS1}+g_{DS3}}{g_{m3}+g_{DS1}+g_{DS3}}$$

$$\bullet\left(\frac{1+s\dfrac{C'_{LA}}{2g_{m3}}}{1+s\dfrac{C'_{LA}}{g_{m3}}}\right)\frac{g_{m1}}{g_{DS2}+g_{DS4}+sC'_{LB}}$$

$g_{m3} = g_{m4}$ and $g_{m3} >> g_{DS1}, g_{DS3}$

$$\frac{V_{out}}{V_{in}}=\left(\frac{1+s\dfrac{C'_{LA}}{2g_{m3}}}{1+s\dfrac{C'_{LA}}{g_{m3}}}\right)\frac{g_{m1}}{g_{DS2}+g_{DS4}+sC'_{LB}}$$

$$A(s)\approx\frac{g_{m1}}{g_{DS2}+g_{DS4}+sC'_{LB}}$$



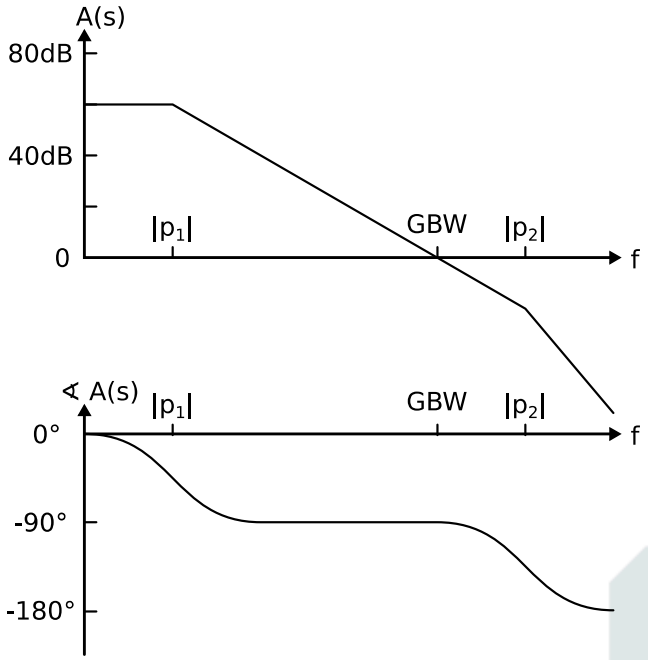
$$\text{gain}:(s=0)\quad\Rightarrow A_0=\frac{g_{m1}}{g_{DS2}+g_{DS4}}$$

$$\text{poles}:\quad p_A=\frac{g_{m3}}{C'_{LA}}$$

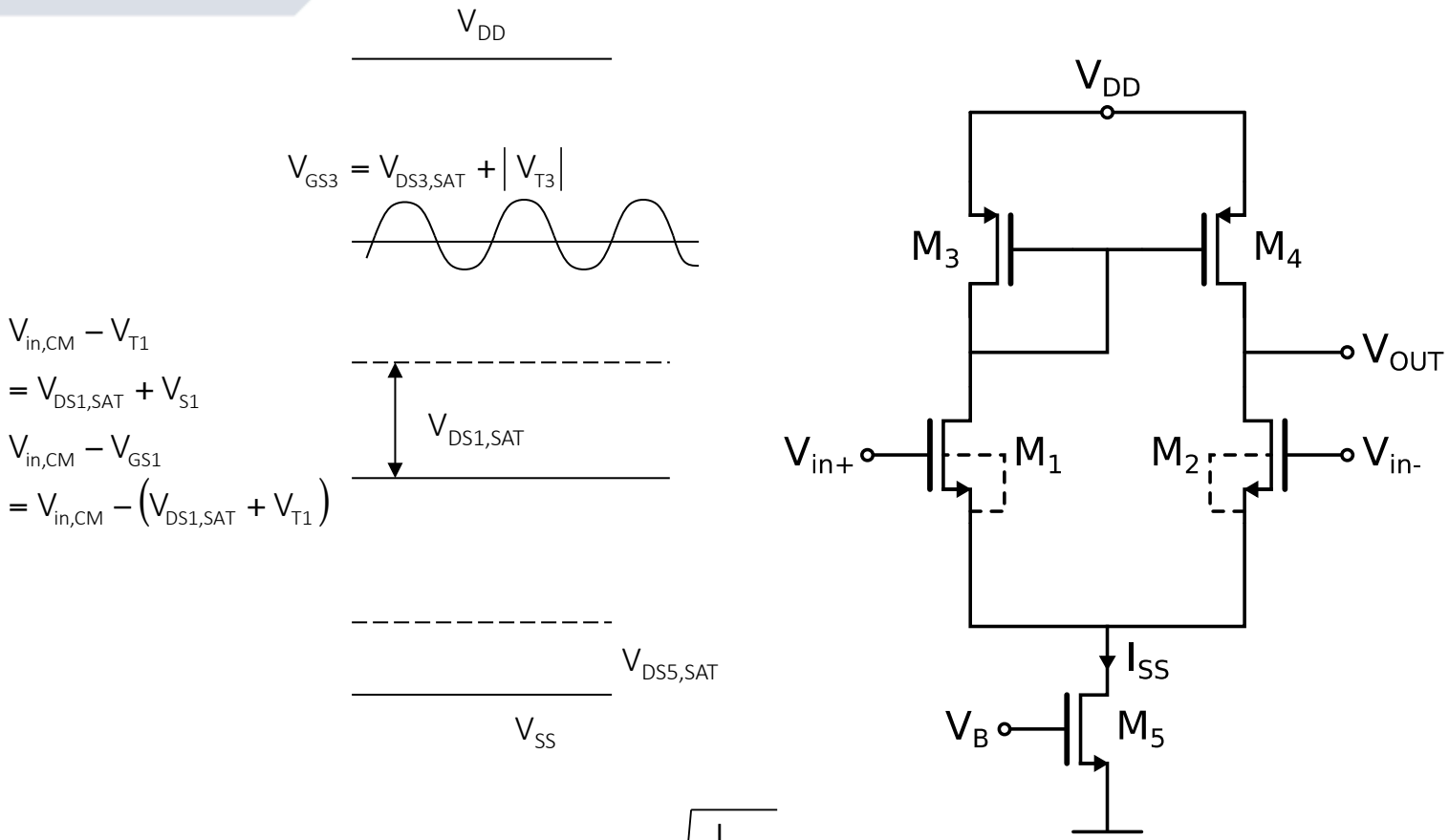
$$p_B=\frac{g_{DS2}+g_{DS4}}{C'_{LB}}$$

$$\text{zero}:\quad z=\frac{2g_{m3}}{C'_{LA}}$$

$$GBW=\frac{g_{m1}}{C'_{LB}}$$

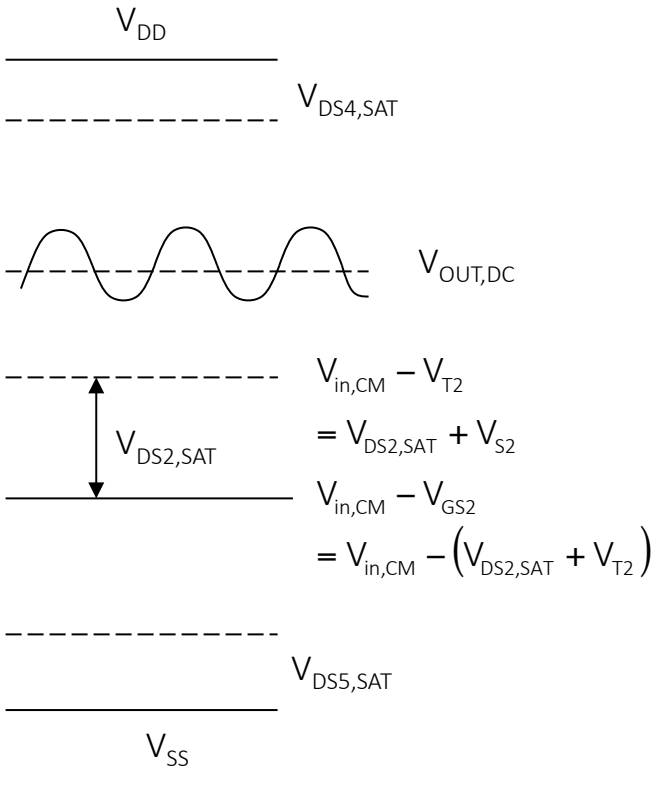


Common-mode and signal ranges



$$V_{DS1,SAT} = V_{DS2,SAT} = \sqrt{\frac{I_{SS}}{2k_{1,2}}}$$

$$V_{S1} = V_{S2}$$



$$V_{DS4,SAT} = \sqrt{\frac{I_{SS}}{2k_4}} = V_{DS3,SAT}$$

$$V_{DS5,SAT} = \sqrt{\frac{I_{SS}}{k_5}}$$

Output signal range:

$$\max\{V_{OUT}\} = V_{DD} - V_{DS4,SAT}$$
$$\min\{V_{OUT}\} = V_{in,CM} - V_{T1}$$

$$\Delta V_{OUT} = V_{DD} - V_{DS4,SAT} - V_{in,CM} - V_{T1}$$

Input common-mode range:

maximum common-mode level:

$$V_{in,CM,MAX} - V_{T1} = V_{DD} - V_{GS3} = V_{DD} - V_{DS3,SAT} - |V_{T3}|$$
$$\Rightarrow V_{in,CM,MAX} = V_{DD} - V_{DS3,SAT} - |V_{T3}| + V_{T1}$$

minimum common-mode level:

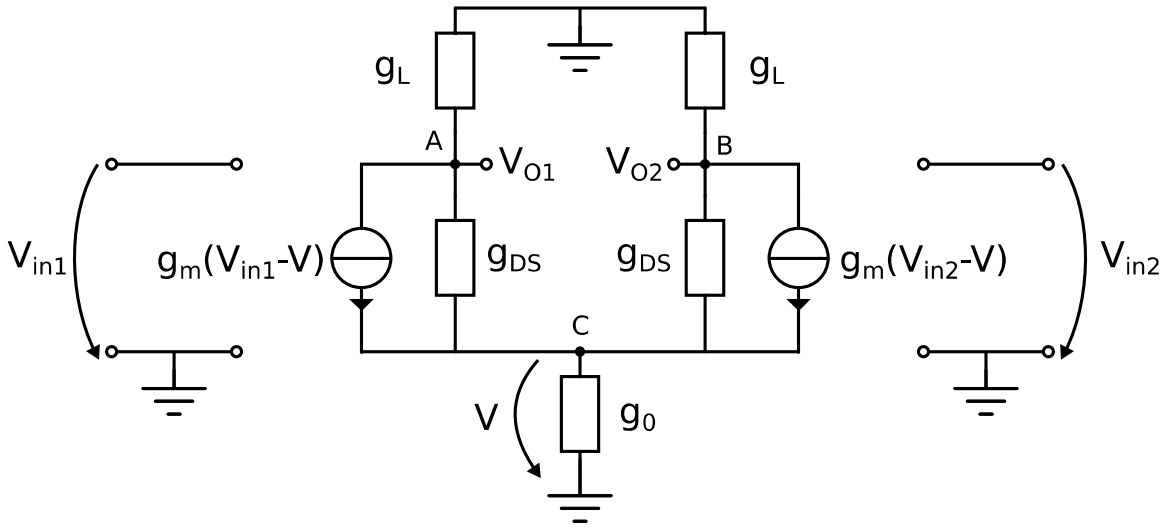
$$V_{in,CM,MIN} - V_{GS1} = V_{DS5,SAT} + V_{SS}$$
$$V_{in,CM,MIN} = V_{DS1,SAT} + V_{T1} + V_{DS5,SAT} + V_{SS}$$

Common-mode rejection ratio (CMRR)

Common-mode rejection

- Ideal tail current source with infinite source impedance blocks the common mode signal

- common mode signal is transferred to the output when curren source impedance is finite.



assume equal transistors M1 and M2

$g_m = g_{m1} = g_{m2}$ $\quad g_L = g_{L1} = g_{L2}$

$g_{DS} = g_{DS1} = g_{DS2}$

current equations at nodes A, B and C

A $\quad v_{o1}g_L + (v_{o1} - V)g_{DS} + g_m(V_{in1} - V) = 0$

B $\quad v_{o2}g_L + (v_{o2} - V)g_{DS} + g_m(V_{in2} - V) = 0$

C $\quad (v - v_{o1})g_{DS} - g_m(V_{in1} - v) + Vg_o + (V - V_{o2})g_{DS} - (V_{in2} - V)g_m = 0$

solve for V_{o1} and V_{o2}

$$V_{o1} = -\frac{g_L g_m (g_D + g_m)(V_{in1} - V_{in2}) + g_o g_m (g_L + g_D)V_{in1}}{(g_L + g_D)\left[2g_L(g_D + g_m) + g_o(g_L + g_D)\right]}$$

$$V_{o2} = -\frac{g_L g_m (g_D + g_m)(V_{in2} - V_{in1}) + g_o g_m (g_L + g_D)V_{in2}}{(g_L + g_D)\left[2g_L(g_D + g_m) + g_o(g_L + g_D)\right]}$$

Differential mode signal gain:

$$\Delta V_{in} = V_{in1} - V_{in2}$$

$$\Delta V_{OUT} = V_{out1} - V_{out2}$$

$$A_{diff} = \frac{V_{out1} - V_{out2}}{V_{in1} - V_{in2}} = \frac{2g_L g_m \left(g_m + g_{DS}\right) + g_m g_o \left(g_L + g_{DS}\right)}{\left(g_L + g_{DS}\right)\left[2g_L \left(g_{DS} + g_m\right) + g_o \left(g_L + g_{DS}\right)\right]} \quad \text{assume } g_m >> g_{DS}, g_o$$

$$\approx -\frac{g_m}{g_L + g_{DS}}$$

Common-mode signal gain:

$$V_{in,cm} = \frac{V_{in1} + V_{in2}}{2}$$

$$V_{out,cm} = \frac{V_{out1} + V_{out2}}{2}$$

$$A_{cm} = \frac{\frac{V_{out1} + V_{out2}}{2}}{\frac{V_{in1} + V_{in2}}{2}} = -\frac{g_m g_o}{2g_L \left(g_m + g_{DS}\right) + g_o \left(g_L + g_{DS}\right)} \quad \text{assume } g_m >> g_{DS}, g_o$$

$$\approx \frac{-g_o}{2\left(g_L + g_{DS}\right)}$$

Common-mode signal rejection:

$$\text{CMRR} = \left|\frac{A_{diff}}{A_{cm}}\right| = 1 + 2\frac{g_L}{g_o}\frac{g_m + g_{DS}}{g_L + g_{DS}} \approx \frac{2g_m}{g_o}$$

CMRR frequency response

Add capacitors in parallel of g_0 and g_L

$$g_L \rightarrow y_L = g_L + sC_L$$
$$g_o \rightarrow y_o = g_o + sC_o$$

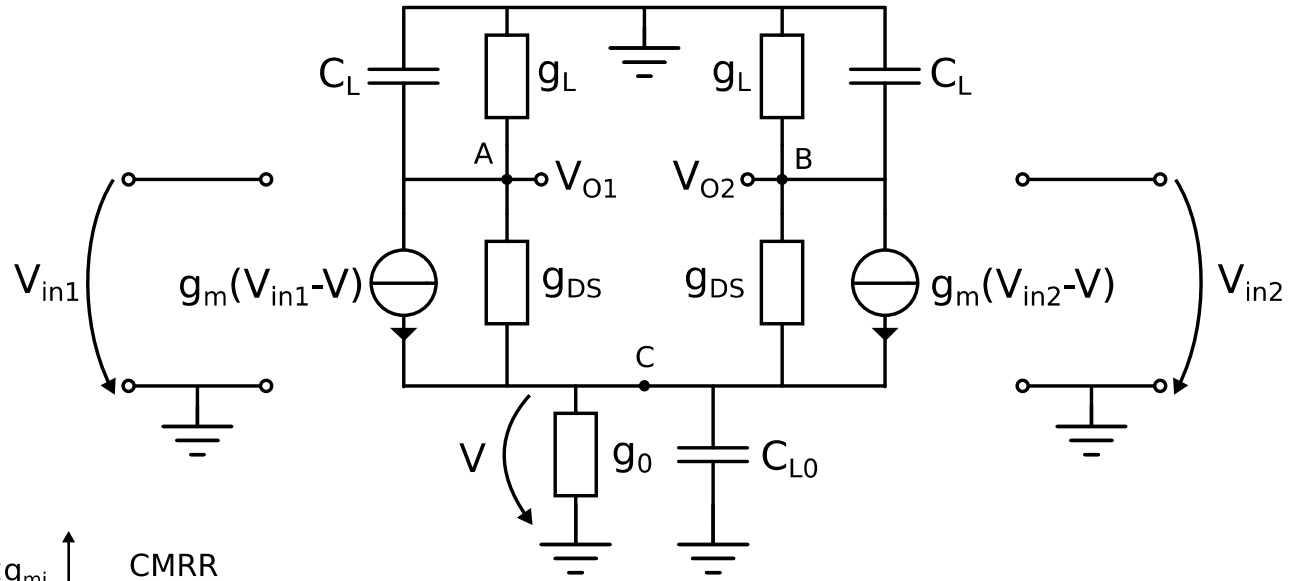
Assume single pole approximation

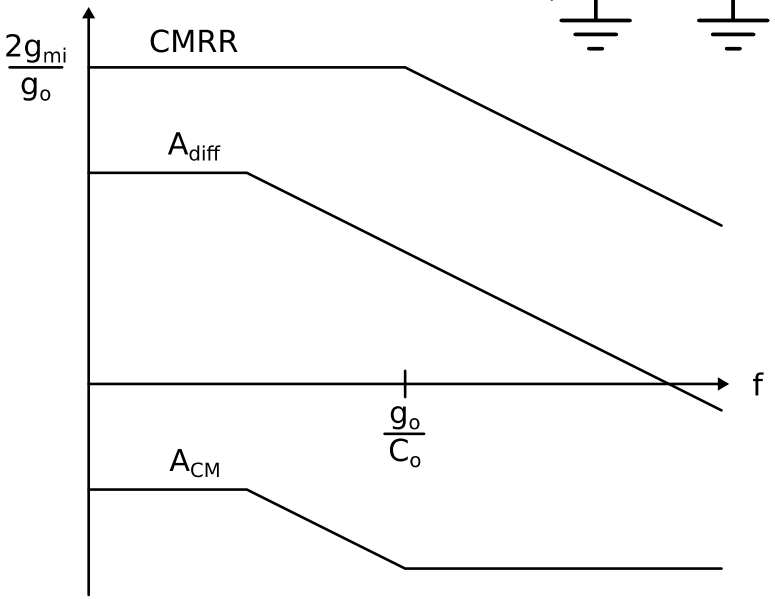
$$A_{diff}(s) = -\frac{g_m}{g_L + g_{DS} + sC_L}$$

$$A_{cm}(s) = -\frac{g_o + sC_o}{2(g_L + g_{DS} + sC_L)}$$

Common-mode rejection

$$CMRR = \frac{2g_m}{g_o + sC_o}$$





Common-mode rejection with current mirror loading

With finite current source impedance

$$A_{diff} = \frac{g_{m1}g_{m4}}{D}\left[2\left(g_{ds1}+g_{m1}\right)+g_o\left(1+\frac{g_{ds1}}{2g_{m4}}\right)\right]$$

$$A_{cm} = -\frac{g_{m1}g_{m4}}{D}\left[2\left(g_{ds1}+g_{m1}\right)+g_o\left(1+\frac{g_{ds1}}{2g_{m4}}\right)\right]$$

$$D = \left(g_{ds1}+g_{m1}\right)\left[g_{ds4}g_{ds1}+2g_{m4}\left(g_{ds4}+g_{ds1}\right)\right]+g_o\left(g_{ds1}+g_{m4}\right)\left(g_{ds4}+g_{d1}\right)$$

assume $g_m >> g_{DS}, g_o \Rightarrow$

$$A_{dm} = \frac{g_{m1}}{g_{ds4}+g_{ds1}}$$

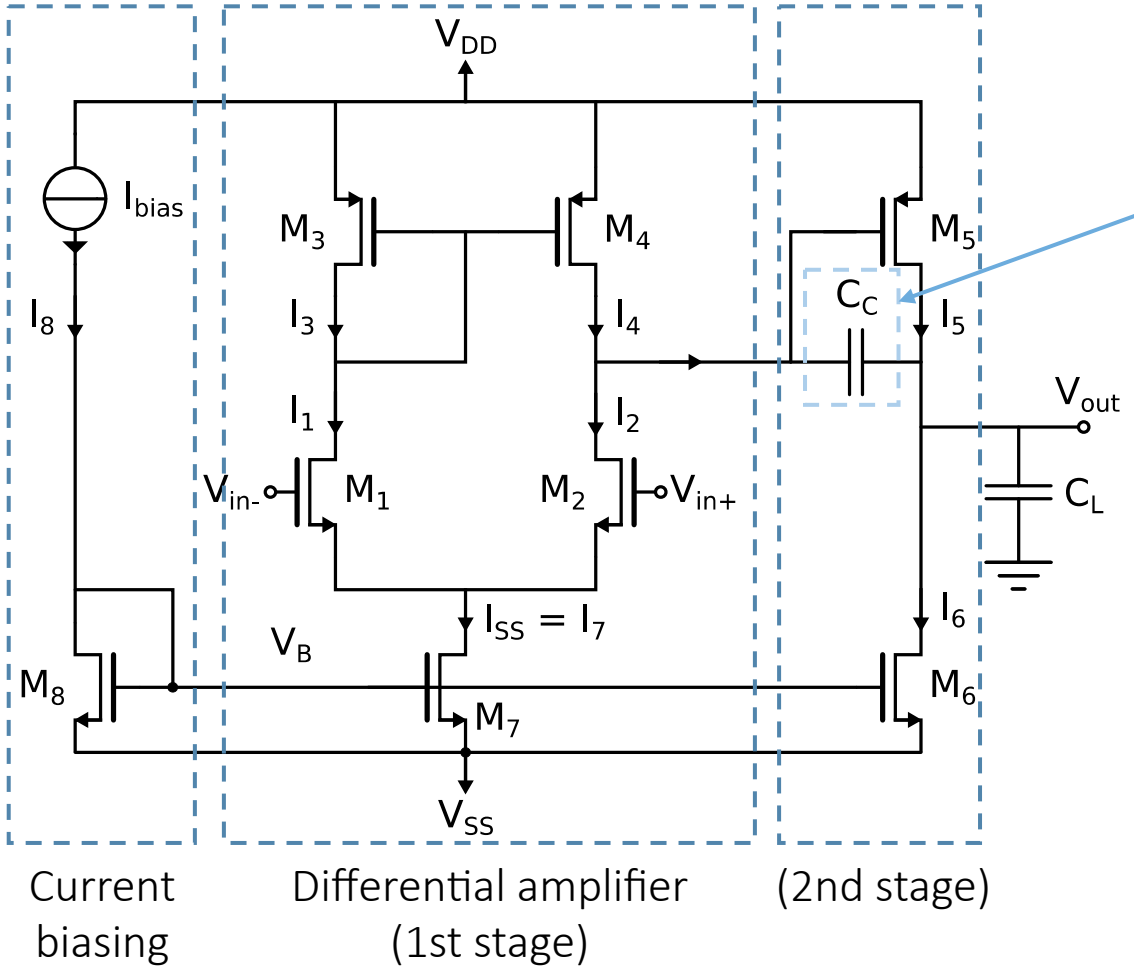
$$A_{cm} = \frac{-g_o g_{ds1}}{2g_{m4}\left(g_{ds4}+g_{ds1}\right)}$$

$$\Rightarrow \text{CMRR} = 2\frac{g_{m1}g_{m4}}{g_o g_{ds1}} \approx 120\text{dB}$$

$$\Rightarrow \text{CMRR increased with factor } \frac{g_{m4}}{g_{ds1}} \approx 100-1000$$

Current sources

Operational amplifier



Compensation

- 2 gain stages (80…120dB)
- Differential input stage
- Miller compensation
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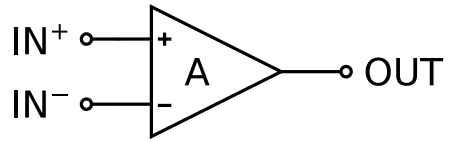
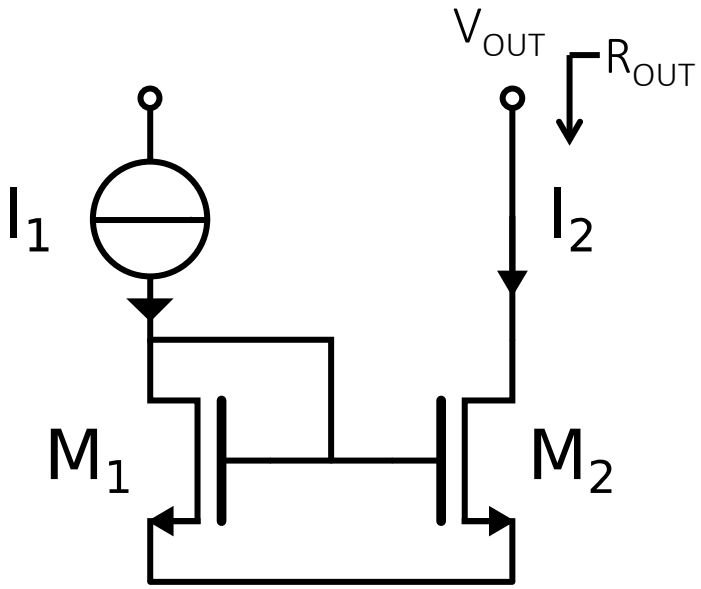
Symbol:



CMOS current mirror



Same gate voltage:

$$V_{GS1} = V_{GS2}$$

Transistors in saturation:

$$\left.\begin{aligned} I_1 &= k_1\left(V_{GS1} - V_T\right)^2 \\ I_2 &= k_2\left(V_{GS2} - V_T\right)^2 \end{aligned}\right\}$$

$$\Rightarrow k_i = \frac{\mu C_{OX}\left(\frac{W}{L}\right)_i}{2}$$

Same type of transistors (NMOS)
Different dimensions (W/L)

$$\frac{I_1}{I_2} = \frac{k_1}{k_2} = \frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_2}$$

Assume same length $L_1=L_2$

$$\Rightarrow \frac{I_1}{I_2} = \frac{W_1}{W_2}$$

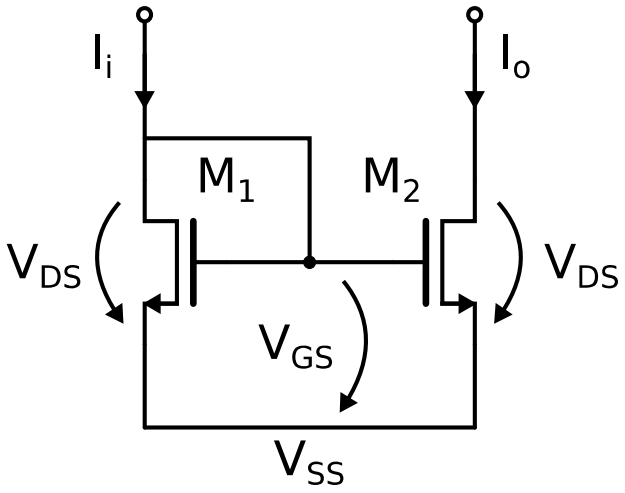
Inaccuracy due to channel length modulation when

$V_{DS1} \neq V_{DS2}$

Output impedance:

$$R_{OUT} = r_{DS2} = g_{DS2}^{-1}$$

Effect of channel length modulation



$$I_1 = k_1 (V_{GS1} - V_T)^2 (1 + \lambda V_{DS1})$$
$$I_2 = k_2 (V_{GS2} - V_T)^2 (1 + \lambda V_{DS2})$$

$$V_{GS1} = V_{GS2} \Rightarrow$$
$$\frac{I_1}{I_2} = \frac{k_1 (1 + \lambda V_{DS1})}{k_2 (1 + \lambda V_{DS2})}$$
$$\frac{I_1}{I_2} = \frac{\left(\frac{W}{L}\right)_1 (1 + \lambda V_{DS1})}{\left(\frac{W}{L}\right)_2 (1 + \lambda V_{DS2})}$$

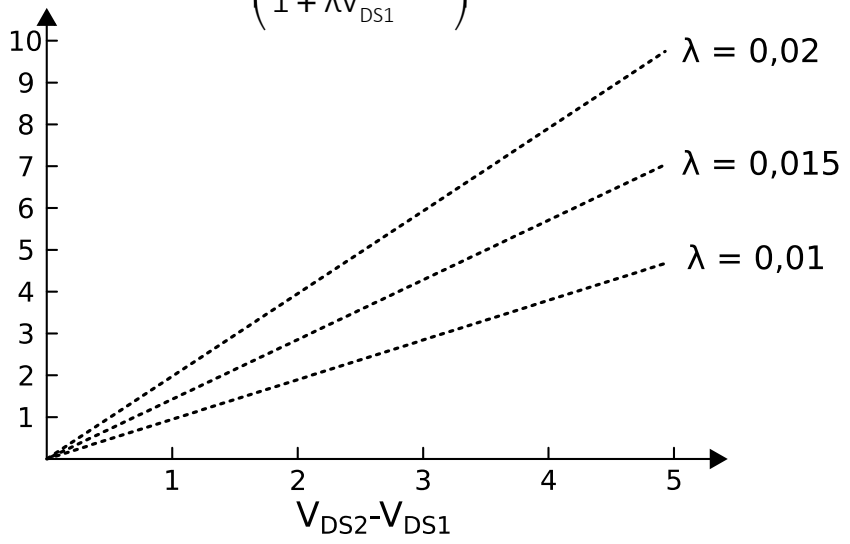
$$\lambda = \frac{I_D}{L V_E}, r_{out} \sim \frac{1}{\lambda}$$

$\Rightarrow$ big L $\Rightarrow$ effect of V_{DS} smaller

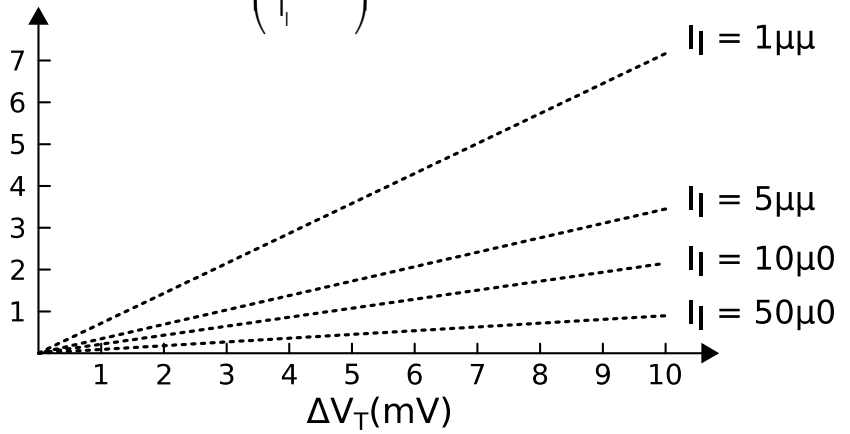
$$V_{DS1} = V_{DS2}$$

$$\Rightarrow \frac{I_1}{I_2} = \frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_2}$$

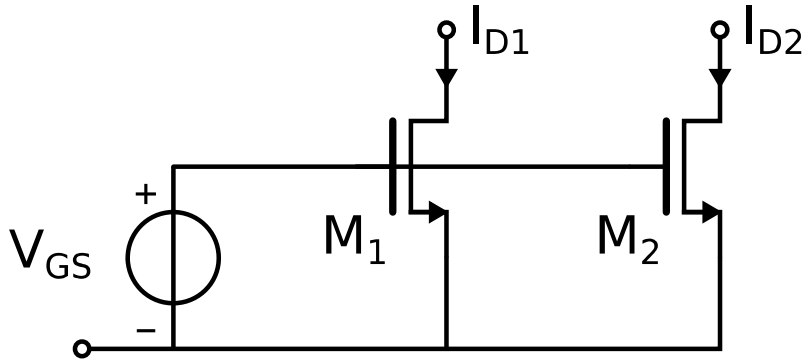
$$\text{RATIO ERROR} \left(\frac{1 + \lambda v_{DS2}}{1 + \lambda v_{DS1}} - 1 \right) 100\%$$



$$\text{RATIO ERROR} \left(\frac{i_O}{i_I} - 1 \right) 100\%$$



Matching of current mirror



M1 and M2 in saturation

$$I_{D1} = \frac{1}{2}\mu C_{OX}\left(\frac{W}{L}\right)_1 (V_{GS} - V_{T1})^2$$

$$I_{D2} = \frac{1}{2}\mu C_{OX}\left(\frac{W}{L}\right)_2 (V_{GS} - V_{T2})^2$$

Let's define:

$$\Delta I_D = I_{D1} - I_{D2} \quad , \quad I_D = \frac{1}{2}(I_{D1} + I_{D2})$$

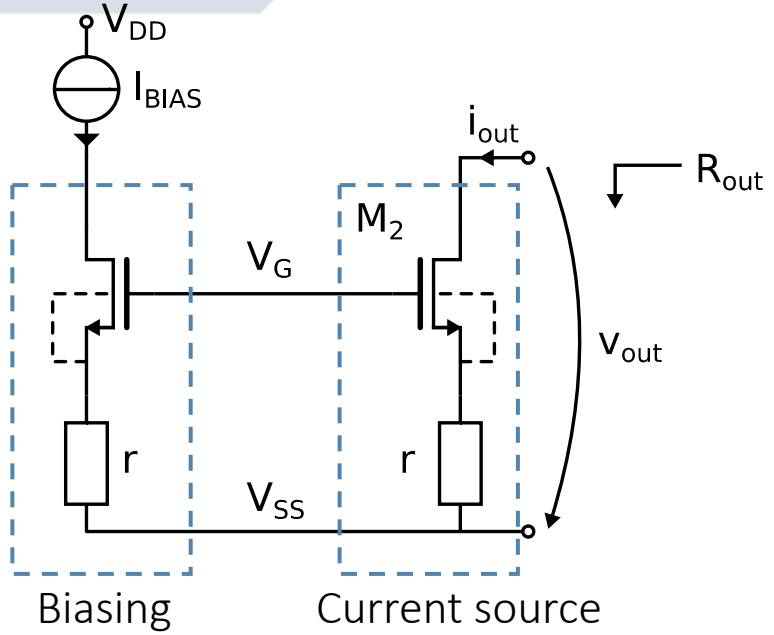
$$\Delta\left(\frac{W}{L}\right) = \left(\frac{W}{L}\right)_1 - \left(\frac{W}{L}\right)_2 \quad , \quad \frac{W}{L} = \frac{1}{2}\left(\left(\frac{W}{L}\right)_1 + \left(\frac{W}{L}\right)_2\right)$$

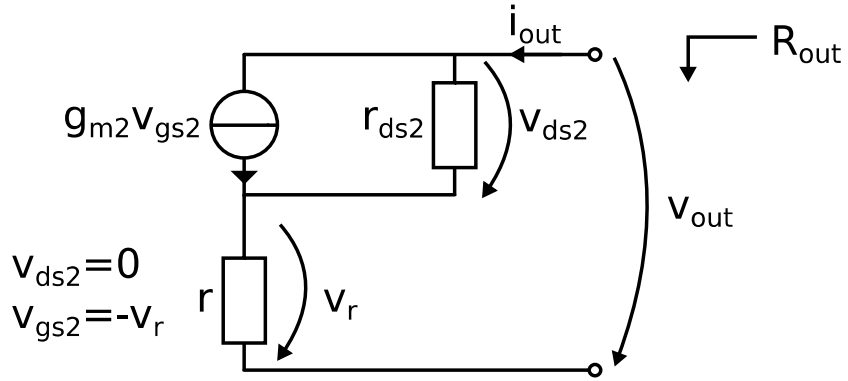
$$\Delta V_T = V_{T1} - V_{T2} \quad , \quad V_T = \frac{1}{2}(V_{T1} + V_{T2})$$

$$\Rightarrow \frac{\Delta I_D}{I_D} = \frac{\Delta\left(\frac{W}{L}\right)}{\frac{W}{L}} - 2\frac{\Delta V_T}{V_{GS} - V_T}$$

Matching improves, when V_{GS}-V_T increases!

Source degeneration





DC small signal circuit of current source

Voltage equation

$$V_{out} = V_{ds2} + V_r$$

Current equation

$$I_{out} = g_{m2}V_{gs2} + V_{ds2}\frac{1}{r_{ds2}} = -g_{m2}V_r + (V_{out} - V_r)\frac{1}{r_{ds2}}$$

$$= -\left(g_{m2} + \frac{1}{r_{ds2}}\right)V_r + V_{out}\frac{1}{r_{ds2}}$$

Voltage drop in r

$$V_r = I_{out}r$$

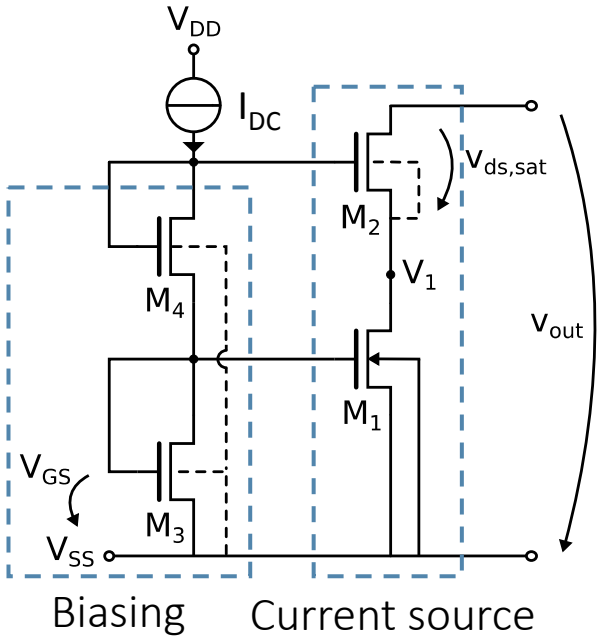
$$I_{out} = -\left(g_{m2} + \frac{1}{r_{ds2}}\right)rI_{out} + V_{out}\frac{1}{r_{ds2}}$$

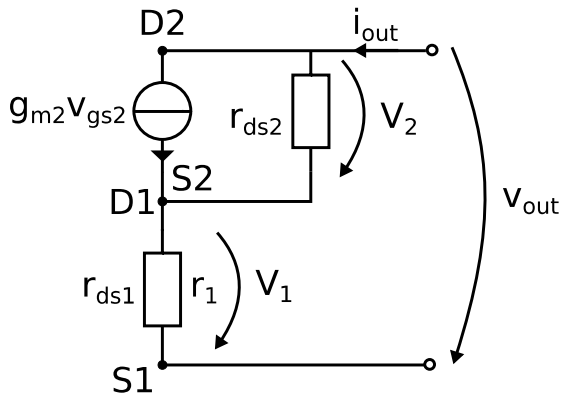
Solve r_{out}

$$\frac{V_{out}}{I_{out}} = r_{out} = r_{ds2} + r + g_{m2}r_{ds2}r$$

$$r_{out} \approx g_{m2}r_{ds2}r$$

Cascode Current Source





DC small signal circuit of current source

Output resistance:

$$r_{out} = \frac{v_{out}}{i_{out}}$$

Assume: $V_{GS1} = \text{constant} \Rightarrow v_{GS1} = 0$

$V_{G2} = \text{constant} \Rightarrow v_{GS2} = v_{S2}$

$V_{BS2} = 0$

Voltage equation at output

$$v_{out} = v_1 + v_2 \qquad v_2 = \left(i_{out} - g_{m2}v_{gs2}\right)\cdot r_{ds2} \qquad v_{GS2} = -v_1$$

$$v_{out} = v_1 + \left(i_{out} - g_{m2}v_{gs2}\right) r_{ds2} = v_1 + i_{out}r_{ds2} + g_{m2}r_{ds2}v_1$$

$$v_1 = i_{out}r_{ds1}$$

$$v_{out} = i_{out}r_{ds1} + i_{out}r_{ds2} + g_{m2}r_{ds2}r_{ds1}i_{out}$$

Solve r_{out}

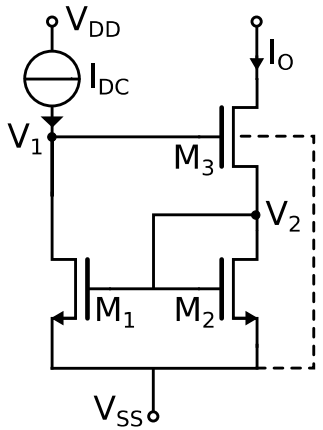
$$\Rightarrow r_{out} = \frac{v_{out}}{i_{out}} = r_{ds1} + r_{ds2} + g_{m2}r_{ds2}r_{ds1}$$

$$\boxed{r_{out} \approx g_{m2}r_{ds2}r_{ds1}} \quad ; \quad g_{m2}r_{ds2} >> 1$$

Wilson current source

Output voltage equation:

$$v_{out} = v_3 + v_2$$



Insert v_3 to v_{out}

$$v_3 = r_{ds3}\left(i_{out} - g_{m3}\left(v_1 - v_2\right)\right)$$

$$v_{out} = r_{ds3}\left(i_{out} - g_{m3}\left(v_1 - v_2\right)\right) + v_2$$

Insert v_1 to v_{out}

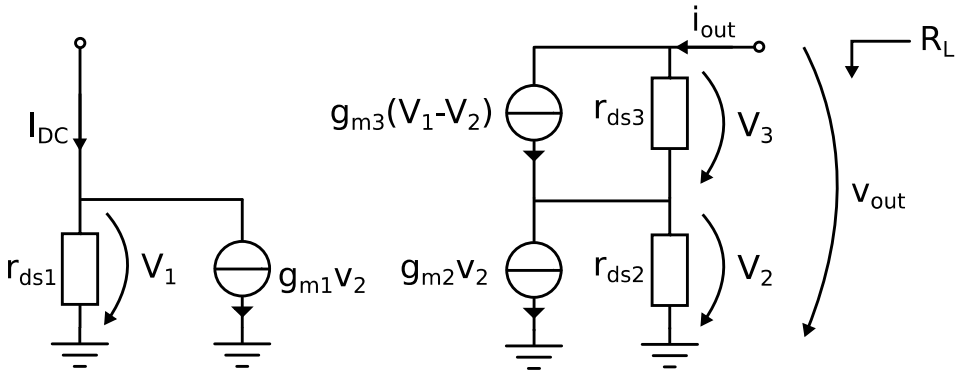
$$v_1 = -r_{ds1}g_{m1}v_2$$

$$v_{out} = r_{ds3}\left(i_{out} + g_{m3}\left(r_{ds1}g_{m1} + 1\right)v_2\right) + v_2$$

Insert v_2 to v_{out}

$$v_2 = \frac{\frac{1}{g_{m2}}r_{ds2}}{\frac{1}{g_{m2}} + r_{ds2}}i_{out} = \frac{r_{ds2}}{1 + g_{m2}r_{ds2}}i_{out}$$

$$v_{out} = r_{ds3}\left(i_{out} + g_{m3}\left(r_{ds1}g_{m1} + 1\right)\frac{r_{ds2}}{1 + g_{m2}r_{ds2}}i_{out}\right) + \frac{r_{ds2}}{1 + g_{m2}r_{ds2}}i_{out}$$



Solve R_{out}

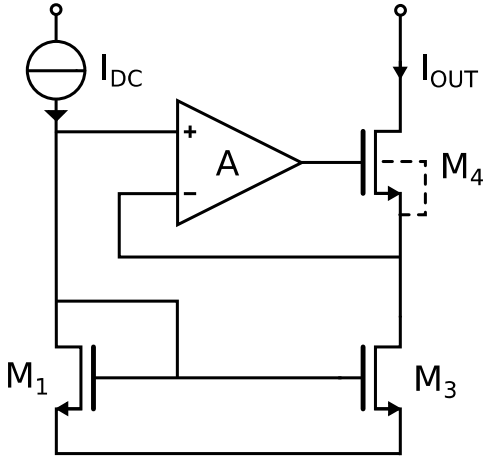
$$R_{out} = \frac{v_{out}}{i_{out}} = r_{ds3} + \frac{\left(r_{ds3}g_{m3}\left(r_{ds1}g_{m1} + 1\right) + 1\right)r_{ds2}}{1 + g_{m2}r_{ds2}}$$

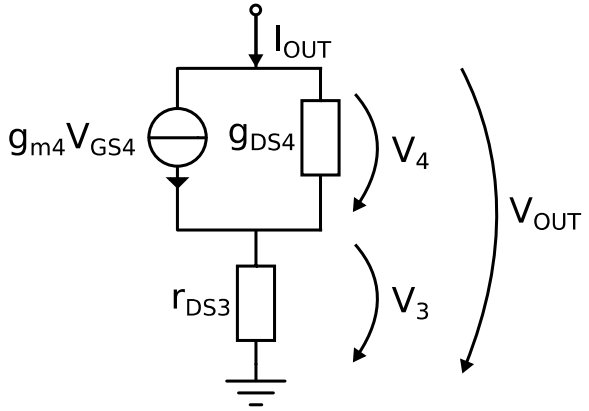
Assume: $g_{m1}r_{ds1} >> 1$

$$R_{out} \approx \left(g_{m1}r_{ds1}\right)\frac{g_{m3}}{g_{m2}}r_{ds3}$$

Increasing output impedance

Regulated cascode:





$$V_{OUT} = V_4 + V_3$$

$$V_3 = V_{S4} = I_{OUT} \cdot R_{DS3}$$

$$V_4 = \left(I_{OUT} - g_{m4} V_{GS4}\right) R_{DS4} = \left(I_{OUT} + g_{m4}\left(A+1\right) V_{S4}\right) R_{DS4}$$

$$V_{GS4} = -AV_{S4} - V_{S4} = -\left(A+1\right) V_{S4}$$

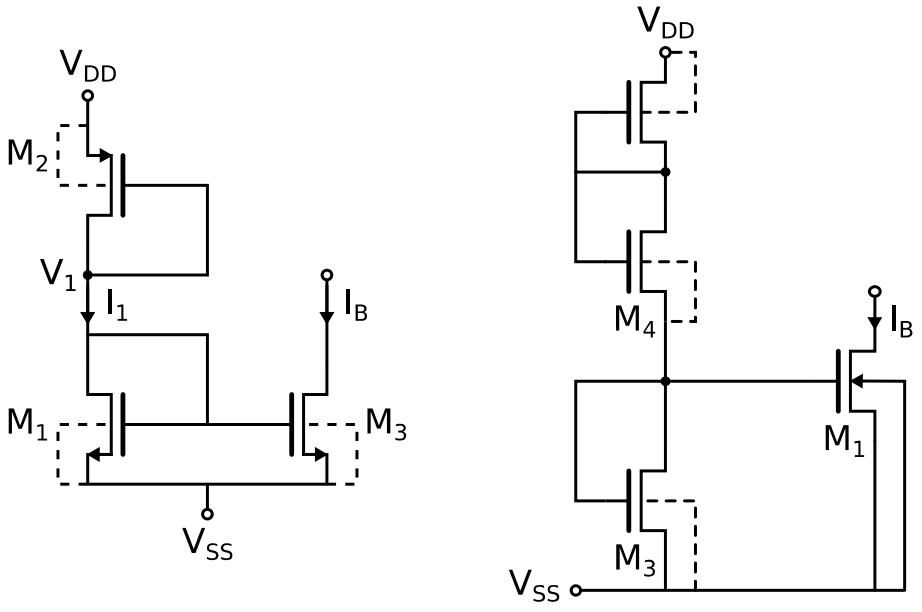
$$V_{G4} = A\left(V_b - V_{S4}\right) = -AV_{S4}$$

$$V_{OUT} = \left(I_{OUT} + g_{m4}\left(A+1\right) \cdot I_{OUT} \cdot R_{DS3}\right) R_{DS4} + I_{OUT} \cdot R_{DS3}$$

$$R_{OUT} = \frac{V_{OUT}}{I_{OUT}} = R_{DS3} + R_{DS4} + g_{m4}\left(A+1\right) R_{DS3} \cdot R_{DS4} \approx g_{m4}\left(A+1\right) R_{DS3} \cdot R_{DS4}$$

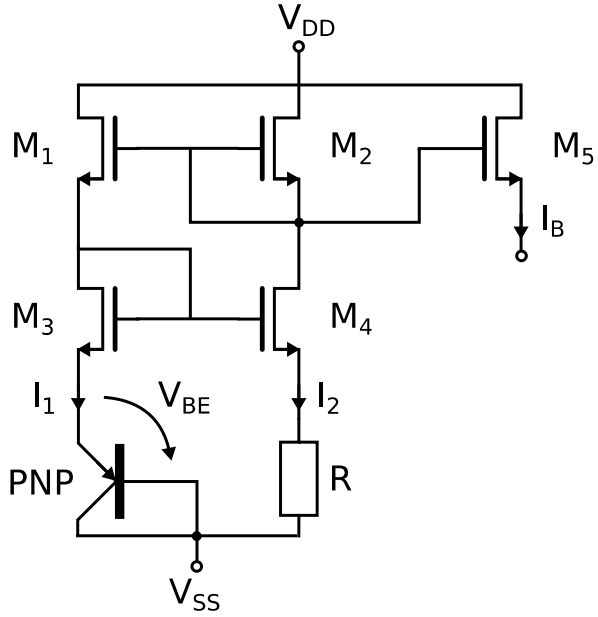
Generation of biasing current

Voltage divider:



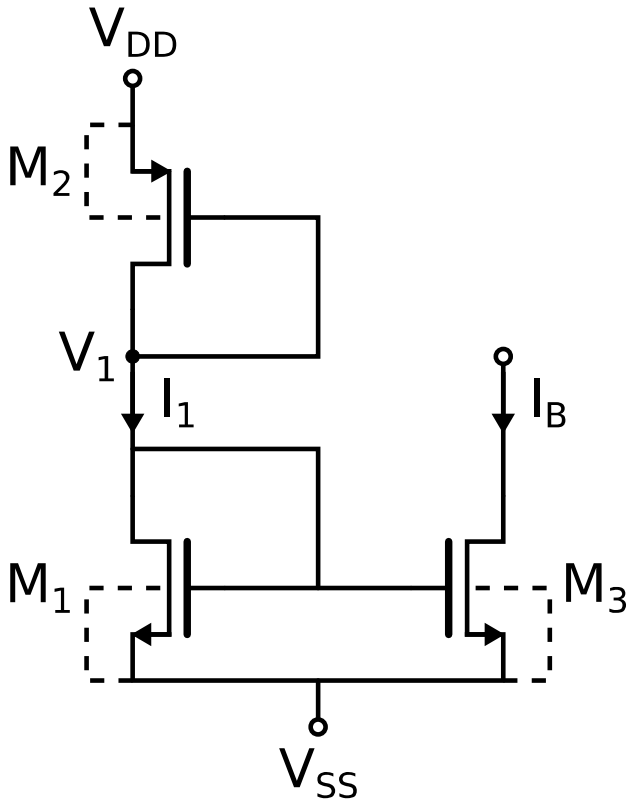
+ Simple
− Supply varies
− TEMP dependence
− Process dependence

PTAT current reference:



+ Supply independent
+ Low process dependence
+ Reduced TEMP coefficient
− More complex (BJT needed)

Voltage Biasing



Transistors in saturation:

$$I_1 = I_2$$

$$I_1 = k_1'\left(\frac{W}{L}\right)_1\left(V_{GS1} - V_{T1}\right)^2 \qquad ;k' = \frac{1}{2}\mu C_{OX}$$

$$I_2 = k_2'\left(\frac{W}{L}\right)_2\left(V_{GS2} - \left|V_{T2}\right|\right)^2$$

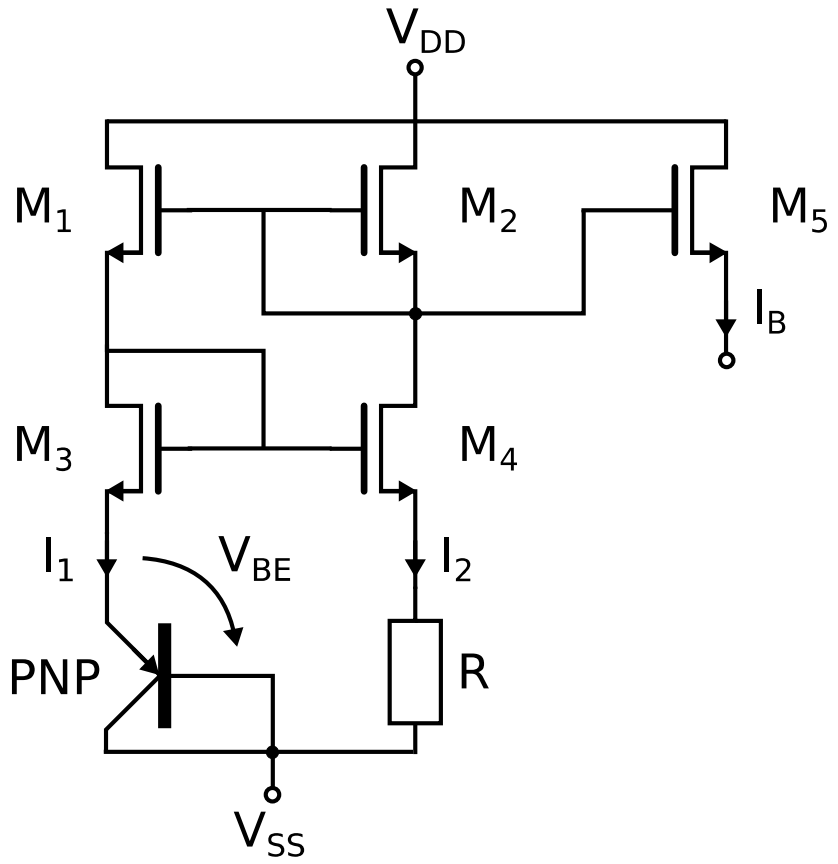
$$V_{GS1} = V_1 - V_{SS}$$

$$V_{GS2} = V_{DD} - V_1$$

Bias voltage:

$$\Rightarrow V_1 = \frac{\sqrt{\mu_p\left(\frac{W}{L}\right)_2}\left(V_{DD} - \left|V_{TP}\right|\right) + \sqrt{\mu_n\left(\frac{W}{L}\right)_1}\left(V_{SS} + V_{TN}\right)}{\sqrt{\mu_p\left(\frac{W}{L}\right)_2} + \sqrt{\mu_n\left(\frac{W}{L}\right)_1}} \qquad I_B = \frac{\left(\frac{W}{L}\right)_3}{\left(\frac{W}{L}\right)_1} I_1$$

PTAT current reference



Assume that transistors M_1 and M_2 are equal and M_3 and M_4 are equal

$$M_1 = M_2 \quad \text{and} \quad M_3 = M_4$$

Then $V_{GS1} = V_{GS2}$ and

$$\Rightarrow \quad I_1 = I_2$$

Thus the source voltages of M_3 and M_4 are equal

$$V_{S3} = V_{S4} \Rightarrow V_{BE} = I_2 R$$

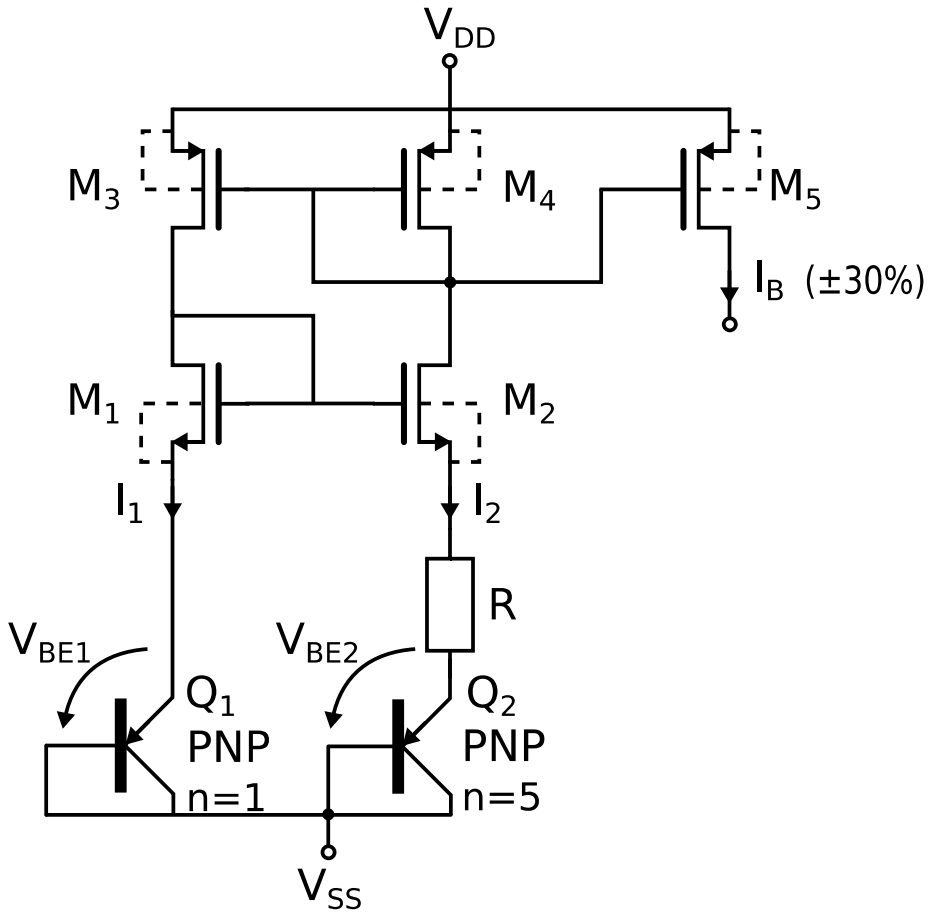
and

$$I_2 = \frac{V_{BE}}{R}$$

V_{BE} is less process and power supply dependent and depends on absolute temperature T.

(PTAT = proportional to absolute temperature)

Bandgap current reference



Assume equal transistors M_1 and M_2 and M_3 and M_4

$$M_1 = M_2 \quad \text{and} \quad M_3 = M_4$$

$$\text{then } V_{GS3} = V_{GS4}$$

$$\text{and} \Rightarrow \; I_1 = I_2 = I$$

Thus the source voltages of M_1 and M_2 are equal

$$V_{S1} = V_{S2}$$

$$\Rightarrow I_2 R = V_{BE1} - V_{BE2}$$

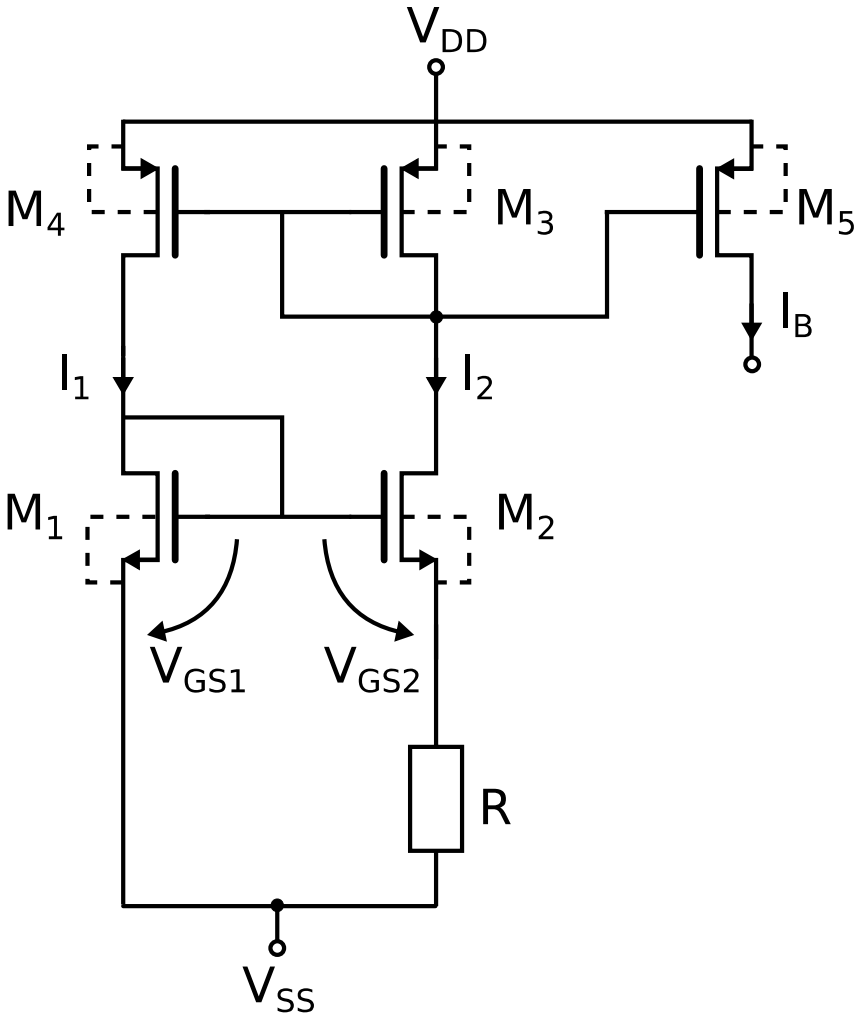
$$V_{BE1} = V_T \ln\left(\frac{I}{I_S}\right)$$

$$V_{BE2} = V_T \ln\left(\frac{I}{nI_S}\right)$$

n is the relative size of BJTs

$$\Rightarrow I_2 = \frac{V_T \ln(n)}{R}$$

CMOS current reference



Assume that M_3 and M_4 are equal and M_1 and M_2 are unequal

$$\text{i.e.} \left(\frac{W}{L}\right)_1 \neq \left(\frac{W}{L}\right)_2$$

$$\text{Then} I_1 = I_2$$

$$\text{However, } V_{GS1} \neq V_{GS2} \quad \text{if} \left(\frac{W}{L}\right)_2 > \left(\frac{W}{L}\right)_1 \Rightarrow V_{GS2} < V_{GS1}$$

A voltage difference V_{GS} is seen over resistor R

$$I_2 = \frac{\left(V_{GS1} - V_{GS2}\right)}{R}$$

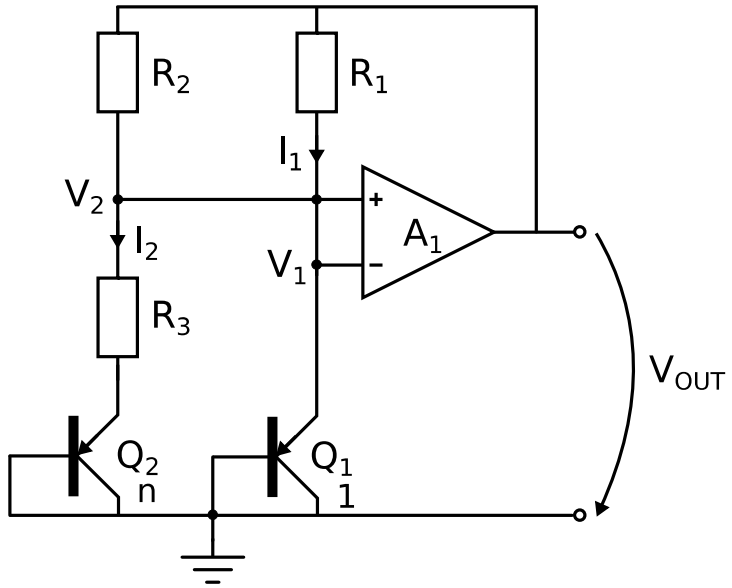
$$I_1 = k'\left(\frac{W}{L}\right)_1 \left(V_{GS1} - V_T\right)^2 \qquad k' = \frac{1}{2}\mu C_{OX}$$

$$I_2 = k'\left(\frac{W}{L}\right)_2 \left(V_{GS2} - V_T\right)^2$$

$$\Rightarrow I_2 = \frac{1}{R^2 k'}\left[\frac{1}{\sqrt{(W/L)_1}} - \frac{1}{\sqrt{(W/L)_2}}\right]^2$$

$$I_B = \frac{(W/L)_4}{(W/L)_3} I_2$$

Bandgap voltage reference



Voltage equation for the loop:

$$V_{BE1} = V_{BE2} + I_2R_3$$

$$\Delta V_{BE} = V_{BE1} - V_{BE2} = I_2R_3$$

From the BJT's current equations:

$$V_{BE1} - V_{BE2} = V_T \ln\frac{I_1}{I_{S1}} - V_T \ln\frac{I_2}{I_{S2}}$$

$$\Rightarrow \Delta V_{BE} = V_T \ln\frac{I_1 I_{S2}}{I_2 I_{S1}}$$

Voltage equation for R_1 and R_2

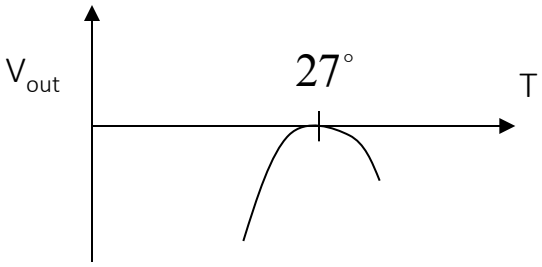
$$V_2 = V_1 \Rightarrow I_1R_1 = I_2R_2$$

$$\Rightarrow \frac{I_1}{I_2} = \frac{R_2}{R_1} \Rightarrow \Delta V_{BE} = V_T \ln\frac{R_2}{R_1}\cdot\frac{I_{S2}}{I_{S1}}$$

$$I_2 = \frac{\Delta V_{BE}}{R_3} = \frac{V_T}{R_3}\ln\frac{R_2}{R_1}\cdot\frac{I_{S2}}{I_{S1}} \qquad \frac{I_{S2}}{I_{S1}} = \frac{n}{1}$$

$$V_{OUT} = V_{BE1} + I_2R_2 = V_{BE1} + \frac{R_2}{R_3}V_T \ln\frac{R_2 I_{S2}}{R_1 I_{S1}}$$

$$V_{OUT} = V_{BE1} + KV_T$$



(1) $\frac{\partial V_{BE}}{\partial T} = -2\text{mV}/^\circ\text{C}$

(2) $V_T = \frac{kT}{q}$