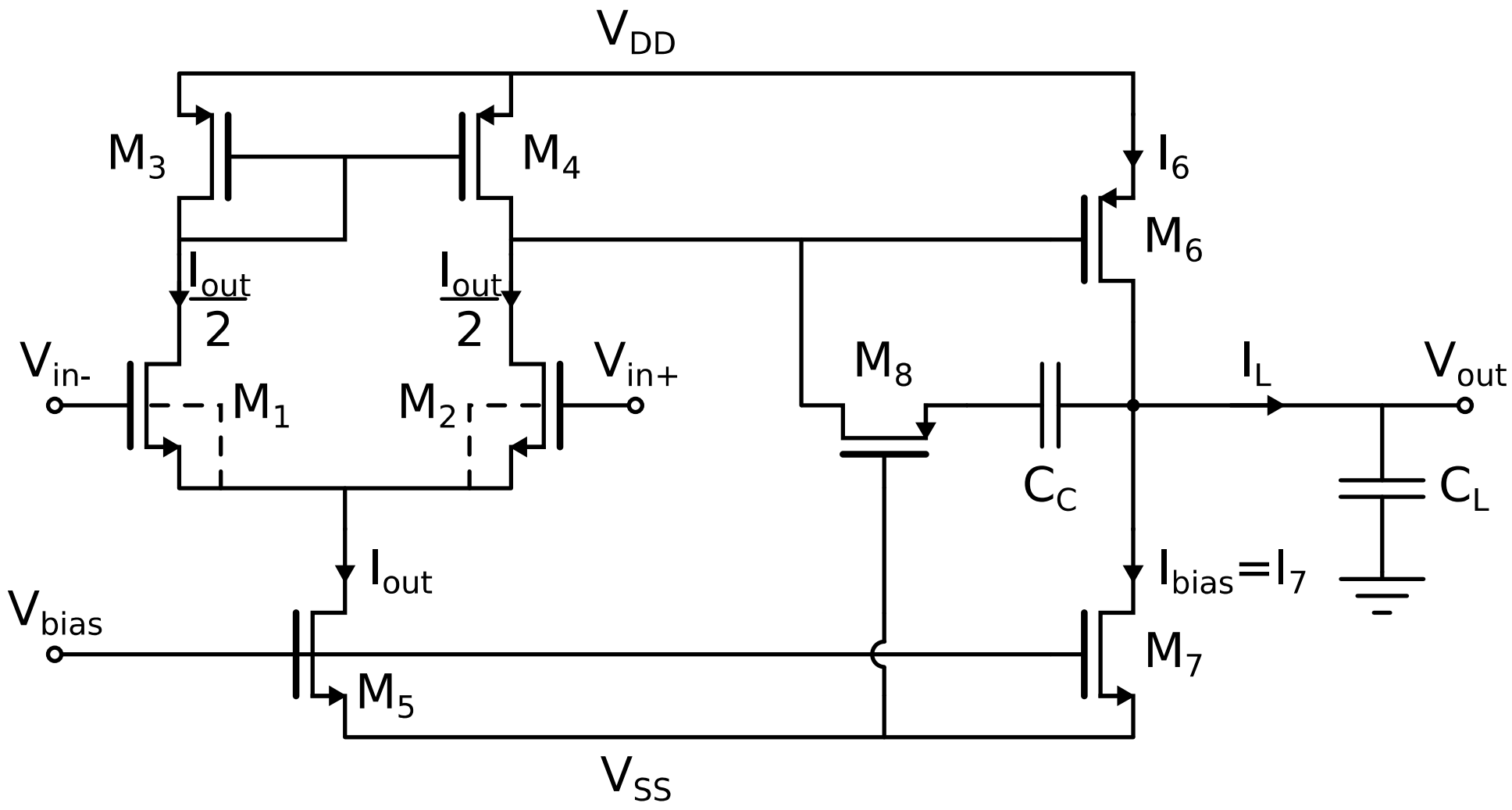
ELEC-E3510 Basics of IC Design

Example



CMOS op-amp with capacitive load

Amplifier specifications:

- DC-gain: $A_0 \geq 70dB$
- GBW: $f_0 \geq 2MHz$
- Slew-rate: $s_r \geq 4V/\mu s$
- CMRR: $\geq 80dB$
- Phase margin: $f_m \geq 60°$
- Load C_L: 10pF
- Supply voltage: $\pm 5V$

Transistor parameters:

- $K'_p = 12\mu A/V^2$
- $K' = \mu C_{OX}/2$
- $v_{Tn} = 1.2V$
- $v_{Tp} = -1V$
- $\lambda = 0.03V^{-1}$
- $L = 10\mu m$

Saturation mode:

$$I_D = K'\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

$$g_m = \sqrt{2K' I_D \frac{W}{L}}$$

Let us assume: $C_C = C_L = 10\text{pF}$

1) $\omega_0 = 2\pi f_0 = \frac{g_{m1}}{C_C}$

$\Rightarrow g_{m1} = 2\pi f_0 C_C = 2\pi \cdot 2 \cdot 10^6 \cdot 10 \cdot 10^{-12} = 126\frac{\mu A}{V}$

Let us select $C_C = C_L = 10\text{pF}$

2) Assume two pole transfer function

$$A(s) = \frac{A_0}{(s-s_{p1})(s-s_{p2})}$$

Now, if $|s_{p2}| = 2\omega_0$ then s_{p2} turns the phase 30° at GBW and phase margin is 60°

$\Rightarrow$ Let us select $|s_{p2}| = 3\omega_0 \Rightarrow$ PM$>$60°

$$s_{p2} = \frac{-g_{m6}C_C}{C_A(C_L+C_C)+C_LC_C} \approx -\frac{g_{m6}}{C_L}, \text{ assuming } C_A \prec\prec C_C, C_L$$

$$\Rightarrow |s_{p2}| = \frac{g_{m6}}{C_L} = \frac{3g_{m1}}{C_C} 3\omega_0$$

$C_L = C_C$

$$\omega_0 = \frac{g_{m1}}{C_C}$$

$$\Rightarrow g_{m6} = 3g_{m1}$$

On the other hand $g_{m1} = \omega_0 C_C = 2\pi \cdot 2 \cdot 10^6 \cdot 10 \cdot 10^{-12} = 126 \frac{\mu A}{V}$

$$\Rightarrow g_{m6} = 3\omega_0 C_C = 377.1 \frac{\mu A}{V}$$

3) Slew-rate determines the input stage biasing current:

$$s_R = \frac{I_0}{C_C}$$

$$\Rightarrow I_0 = s_R C_C \geq 4 \cdot 10^6 \cdot 10 \cdot 10^{-12} = 40\mu A$$

Because th output stage is biased with a current source, we must ensure that it doue not limit the settling speed:

$$s_{r0} = \frac{I_{b7}}{C_L}$$

Let us select $s_{r0} = 2.5 \cdot s_r = 10\text{V}/\mu\text{s}$

$$\Rightarrow I_{b7} = s_{r0} \cdot C_L = 2.5 \cdot I_0 = 2.5 \cdot 40\mu A$$

Larger I_{b7} reduces the size of the transistor in the output stage, on the other hand power consumption is increased and the output linear range is reduced!

4) DC-gain

$$A_0 = \frac{g_{m1}g_{m6}}{(g_{d2} + g_{d4})(g_{d6} + g_{d7})}$$

$$g_d = \lambda I_D$$

$$\Rightarrow g_{d2} = g_{d4} = \lambda \frac{I_0}{2}$$

$$g_{d6} = g_{d7} = \lambda I_{b7}$$

We obtain

$$A_0 = \frac{g_{m1}g_{m6}}{\lambda^2 * I_0 * 2\, I_{b7}} = \frac{125.7 \cdot 10^{-6} \cdot 377 \cdot 10^{-6}}{0.03 \cdot 40 \cdot 10^{-6} \cdot 2 \cdot 0.03 \cdot 100 \cdot 10^{-6}} \approx 6582$$

$$\Rightarrow A_0 = 76dB (\succ 70dB)$$

5) Offset minimisation

$$g_m = \sqrt{2\mu c_{OX} \frac{W}{L} I_D}$$

$$\frac{\left(\frac{W}{L}\right)_{3,4}}{\left(\frac{W}{L}\right)_6} = \frac{\frac{I_0}{2}}{I_{b7}} = \frac{1}{5}$$

On the other hand

$$\frac{g_{m4}}{g_{m6}} = \sqrt{\frac{\left(\frac{W}{L}\right)_4 \cdot \frac{I_0}{2}}{\left(\frac{W}{L}\right)_6 \cdot I_{b7}}} = \frac{\frac{I_0}{2}}{I_{b7}} = \frac{1}{5}$$

$$\Rightarrow g_{m4} = \frac{1}{5} \cdot g_{m6} = 75.4 \ \frac{\mu A}{V}$$

$$g_{m3} = g_{m4} = 75.4 \frac{\mu A}{V}$$

6) Compensation

Miller zero:

$$s_z = \frac{-1}{\left(R_C - \frac{1}{g_{m6}}\right) C_C}$$

a) $s_z \longrightarrow \infty$

$$\Rightarrow R_C = \frac{1}{g_{m6}} = 2.65k\Omega$$

b) $s_z = s_{p2}$

$$\Rightarrow R_C = \frac{1}{|s_{p2}|C_C} + \frac{1}{g_{m6}} \approx \frac{C_L}{g_{m6}C_C} + \frac{1}{g_{m6}} = \frac{2}{g_{m6}} = 5.3k\Omega$$

Let us select $R_C = 5.3k\Omega$

$$\frac{1}{R_C} = \left|\frac{\partial I_D}{\partial V_{DS}}\right| = \mu c_{OX}\left(\frac{W}{L}\right)_8 |V_{GS8} - V_T| = 2K_8(|V_{SS} - V_{b8}| - V_T)$$

$$I_D = \mu c_{OX}\frac{W}{L}(V_{GS8} - V_T)V_{DS} - \frac{1}{2}{V_{DS}}^2$$

7) CMRR

$$CMRR = \frac{2g_{m1}g_{m3}}{g_{d5}g_{d1}}$$

Assuming

$g_{d5} = \lambda I_0$

$g_{d1} = \lambda \frac{I_0}{2}$

$$\Rightarrow CMRR = \frac{2 \cdot g_{m1} \cdot g_{m3}}{\lambda I_0 \cdot \frac{1}{2}\lambda I_0} = \frac{4 \cdot g_{m1} \cdot g_{m3}}{(\lambda I_0)^2} \approx 26327$$

$$\Rightarrow CMRR \approx 88dB$$

8) Let us design the transistor dimensions.

The value of all g_m are known. Also I_0 and I_{b7} are known.

$$g_m = \sqrt{2\,K'\,\frac{W}{L} I_D}$$

$$\frac{W}{L} = \frac{{g_m}^2}{2KI_D}$$

$$\left(\frac{W}{L}\right)_{1,2} = \frac{{g_{m1}}^2}{2K_n'\frac{I_0}{2}} = \frac{(125.7 \cdot 10^{-6})^2}{2 \cdot 30 \cdot 10^{-6} \cdot \frac{1}{2} \cdot 40 \cdot 10^{-6}} = 13.16$$

$$\left(\frac{W}{L}\right)_{3,4} = \frac{{g_{m4}}^2}{2K_p'\frac{I_0}{2}} = 11.84$$

$$\left(\frac{W}{L}\right)_{6} = 5 \cdot \left(\frac{W}{L}\right)_{4} = 59.2$$

$\lambda = 0.03\frac{1}{V}$ corresponds to channel lenght of $L = 10\mu m$ and leads to enough high gain, thus let us select $L = 10\mu m$ and we obtain

W_1=W_2=130μm
W_3=W_4=120μm
W_6=600μm

Let us calculate the drain voltage V_{DS} of the compensation transistor M_8.

$$V_D = V_{DD} - |V_{GS3}|$$

$$I_{b3} = \frac{I_0}{2} = K_p' \left(\frac{W}{L}\right)_3 = \left(|V_{GS3}| - |V_{Tp}|\right)^2$$

$$\Rightarrow |V_{GS3}| = |V_{Tp}| + \sqrt{\frac{\frac{I_0}{2}}{K_p' \left(\frac{W}{L}\right)_3}} = 1.375V$$

$$\Rightarrow V_{b3} = V_{D8} = V_{DD} - |V_{GS3}| = 3.625\text{V}$$

Now use the linear region equation to calculate the equivalent resistor of M_8.

$$R_C = \frac{1}{2K_p' \left(\frac{W}{L}\right)_8 (V_{SS} + V_{D8} - V_T)}$$

$$\Rightarrow \left(\frac{W}{L}\right)_8 = \frac{1}{2K_p' (V_{SS} + V_{D8} - V_T) R_C} = 1.05$$

$$\Rightarrow W_8 = L_8 = 10\mu m$$