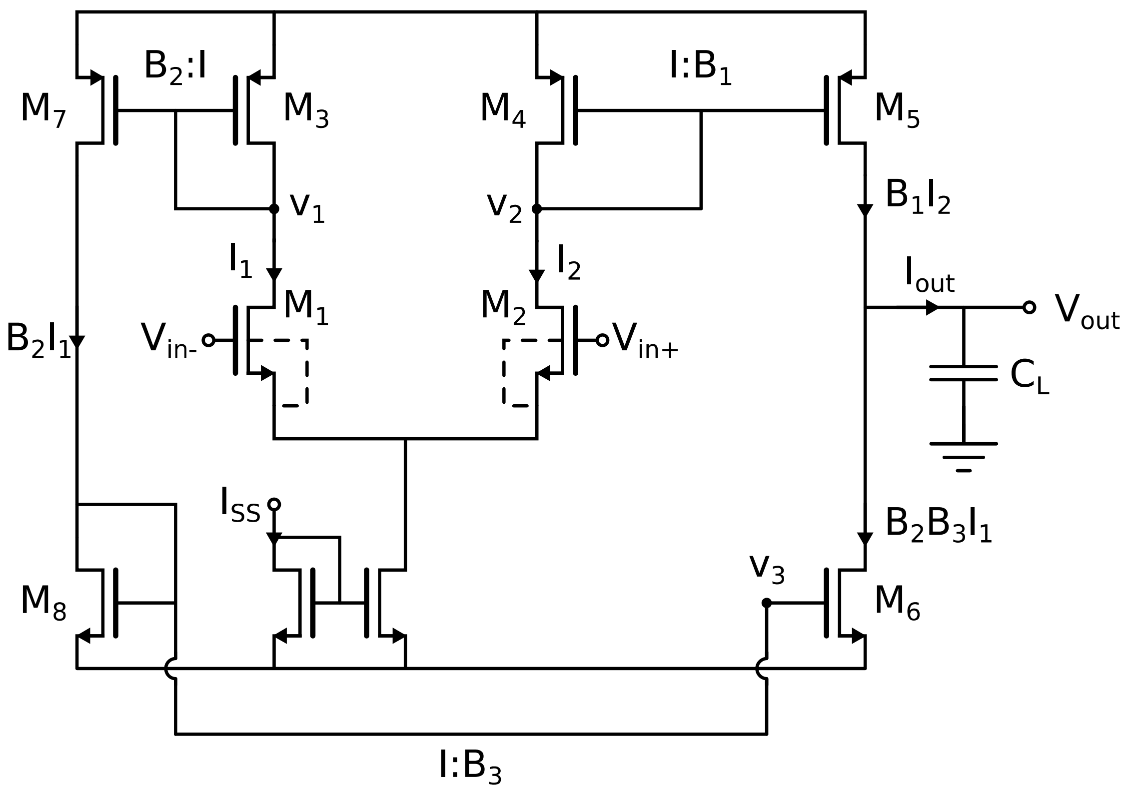
ELEC-E3510 Basics of IC Design

Lecture 5:
OTA Amplifiers

OTA – Operational Transconductance Amplifier



Symmetrical input stage:

$$M1 \equiv M2 \quad \text{and} \quad M3 \equiv M4$$

Current mirrors:

$$M4 \,\&\, M5 \Rightarrow I_5 = \frac{(W/L)_5}{(W/L)_4} \cdot I_4 = \frac{g_{m5}}{g_{m4}} \cdot I_4 = B_1 \cdot I_4$$

$$M3 \,\&\, M7 \Rightarrow I_7 = \frac{(W/L)_7}{(W/L)_3} \cdot I_3 = \frac{g_{m7}}{g_{m3}} \cdot I_3 = B_2 \cdot I_3$$

$$M8 \,\&\, M6 \Rightarrow I_6 = \frac{(W/L)_6}{(W/L)_8} \cdot I_8 = \frac{g_{m6}}{g_{m8}} \cdot I_8 = B_3 \cdot I_8$$

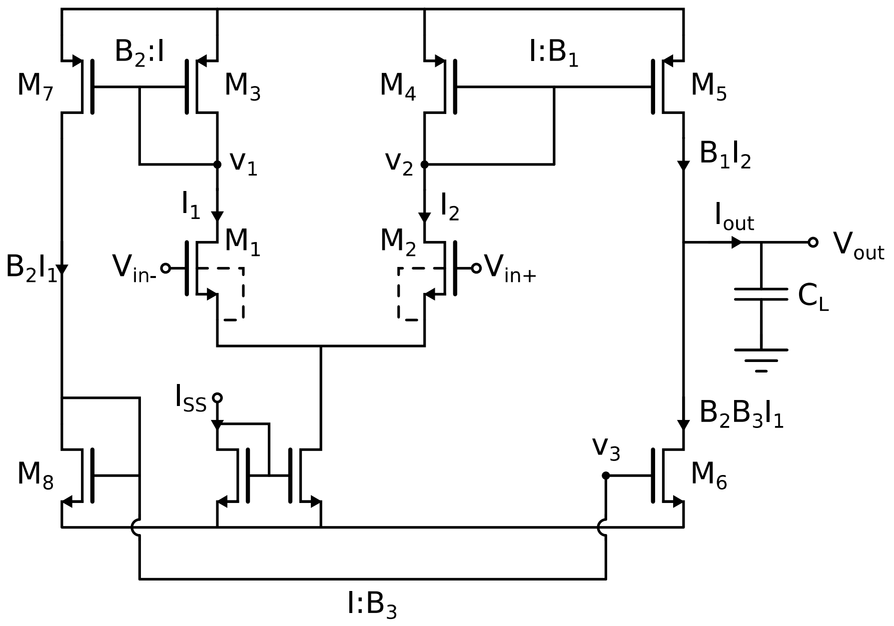
Required:

$$B_1 = B_2 \cdot B_3$$

$$\text{if } M5 \equiv M7 \quad \text{and} \quad M8 \equiv M6$$

$$\Rightarrow B_2 \equiv B_1 \quad \text{and} \quad B_3 = 1$$

OTA transconductance and gain



OTA transforms the input voltage difference to the output current:

$$I_1 - I_2 = g_{m1} \cdot \Delta V_{in}$$

$$I_5 = B_1 \cdot I_2$$

$$I_7 = B_2 \cdot I_3 = B_2 \cdot I_1$$

$$I_6 = B_3 \cdot I_8 = B_3 \cdot I_7 = B_2 \cdot B_3 \cdot I_1$$

$$I_{OUT} = I_5 - I_6 = B_1 \cdot I_2 - \underbrace{B_2 \cdot B_3}_{B_1} \cdot I_1 = B_1 \cdot (I_2 - I_1)$$

$$= -B_1 \cdot g_{m1} \cdot \Delta V_{in}$$

Transconductance of OTA:

$$\Rightarrow g_m = B_1 g_{m1}$$

Voltage gain is obtained by feeding the output current into output load resistor.

$$V_{OUT} = I_{OUT} \cdot R_{OUT}$$

$$= B_1 g_{m1} \cdot R_{OUT} \cdot \Delta V_{in}$$

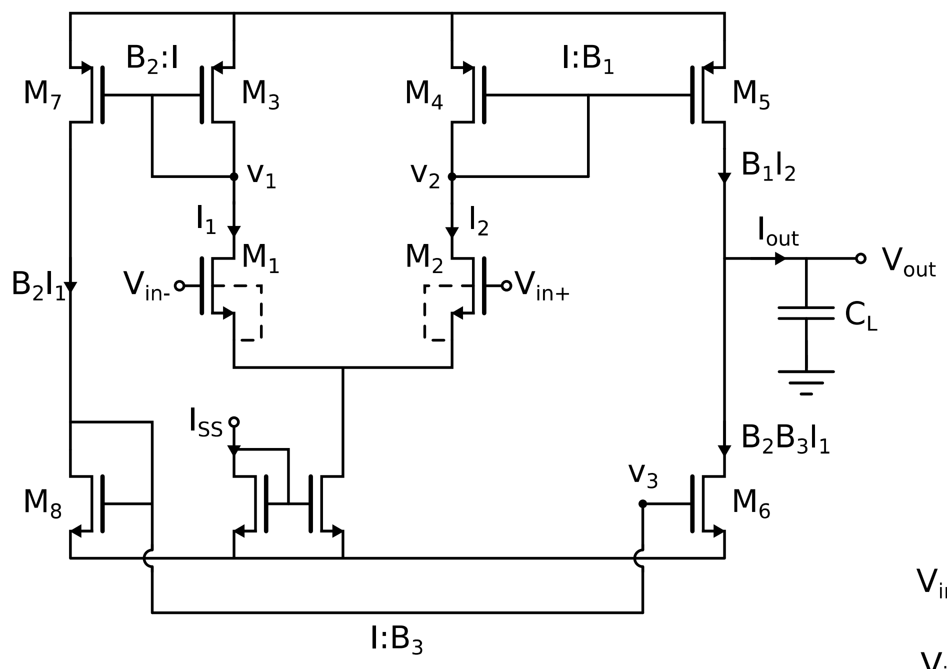
$$A = \frac{V_{OUT}}{\Delta V_{in}} = B_1 g_{m1} \cdot R_{OUT}$$

Without external load resistor:

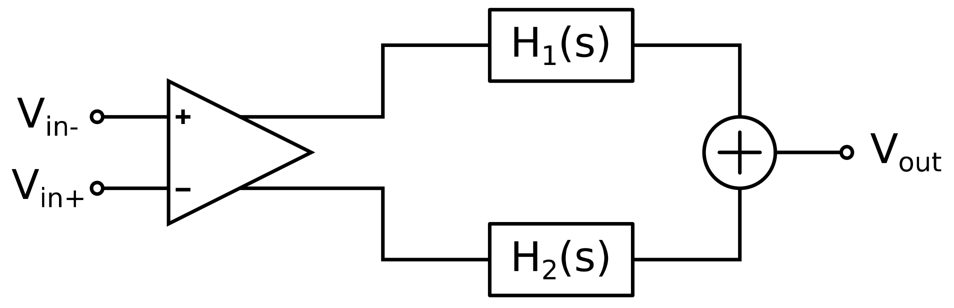
$$R_{OUT} = \frac{1}{g_{DS5} + g_{DS6}}$$

$$\Rightarrow A = \frac{B_1 g_{m1}}{g_{DS5} + g_{DS6}}$$

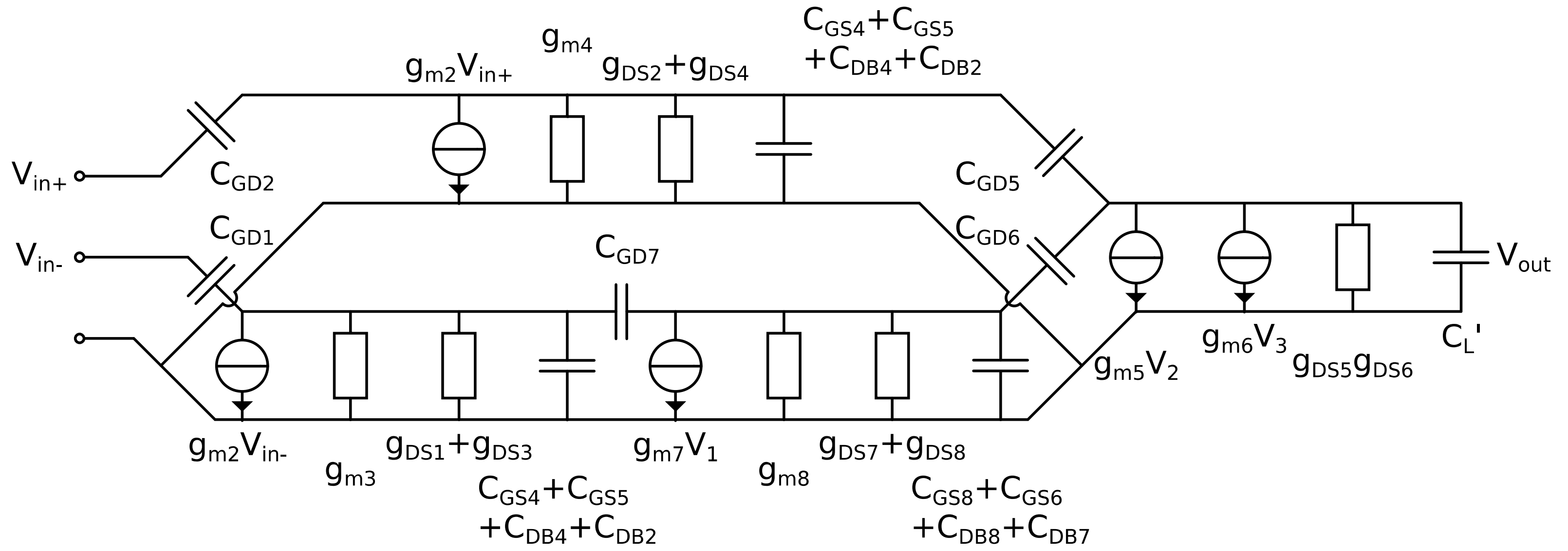
Small-signal analysis



Exclude Miller effect due to a small overlap capacitor



$$H(s) = H_1(s) + H_2(s)$$



$$V_{in}^{+} = \frac{1}{2}\Delta V_{in}$$

$$V_{in}^{-} = -\frac{1}{2}\Delta V_{in}$$

$$C_L' = C_L + C_{DB5} + C_{DB6}$$

Transferfunction of the two signal branches:

$$H_1(s)=\frac{\frac{1}{2}\frac{g_{m2}}{g_{m4}}\cdot\frac{g_{m5}}{g_{DS5}+g_{DS6}}}{\left(1+\frac{s}{p_1}\right)\left(1+\frac{s}{p_L}\right)}=\frac{\frac{1}{2}\frac{B_1 g_{m2}}{g_{DS5}+g_{DS6}}}{\left(1+\frac{s}{p_1}\right)\left(1+\frac{s}{p_L}\right)}$$

$$H_2(s)=\frac{\frac{1}{2}\frac{g_{m1}}{g_{m3}}\cdot\frac{g_{m7}}{g_{m8}}\cdot\frac{g_{m6}}{g_{DS5}+g_{DS6}}}{\left(1+\frac{s}{p_2}\right)\left(1+\frac{s}{p_3}\right)\left(1+\frac{s}{p_L}\right)}=\frac{\frac{1}{2}\frac{B_2\cdot B_3\cdot g_{m1}}{g_{DS5}+g_{DS6}}}{\left(1+\frac{s}{p_2}\right)\left(1+\frac{s}{p_3}\right)\left(1+\frac{s}{p_L}\right)}$$

Poles:

$$p_2=\frac{g_{m3}+g_{DS1}+g_{DS3}}{C_{GS3}+C_{GS7}+C_{DB1}+C_{DB3}}\approx\frac{g_{m3}}{C_{p2}}$$

$$p_1=\frac{g_{m4}+g_{DS2}+g_{DS4}}{C_{GS4}+C_{GS5}+C_{DB2}+C_{DB4}}\approx\frac{g_{m4}}{C_{p1}}$$

$$p_3=\frac{g_{m8}+g_{DS7}+g_{DS8}}{C_{GS8}+C_{GS6}+C_{DB7}+C_{DB8}}\approx\frac{g_{m8}}{C_{p3}}$$

$$p_L=\frac{g_{DS5}+g_{DS6}}{C_L'}$$

$$g_{DS5}+g_{DS6}<<g_{mi}$$

$$p_L<<p_1,p_2,p_3$$

Symmetrical design:

ass. $M_1=M_2,\ M_3=M_4,\ (M_7=M_5)(M_8=M_6)$

$$\Rightarrow g_{m3}=g_{m4},\ C_{p2}=C_{p1}$$

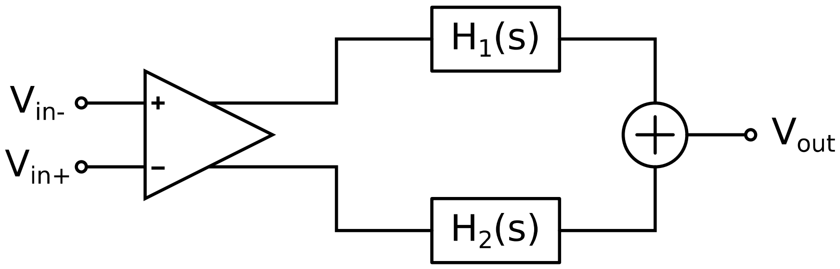
$$\Rightarrow p_1=p_2$$

$B_2=B_1:\quad B_3=1$

$$\Rightarrow p_1=p_2$$

Transferfunction of OTA:

Combine the two signal paths



$$H(s) = H_1(s) + H_2(s)$$

$$= \frac{\frac{1}{2}\frac{g_{m1}}{g_{DS5}+g_{DS6}}\left(B_1\left(1+\frac{s}{p_3}\right)+B_2B_3\right)}{\left(1+\frac{s}{p_1}\right)\left(1+\frac{s}{p_3}\right)\left(1+\frac{s}{p_L}\right)}$$

$$= \frac{\frac{B_1 g_{m1}}{g_{DS5}+g_{DS6}}\left(1+\frac{s}{2p_3}\right)}{\left(1+\frac{s}{p_1}\right)\left(1+\frac{s}{p_3}\right)\left(1+\frac{s}{p_L}\right)}$$

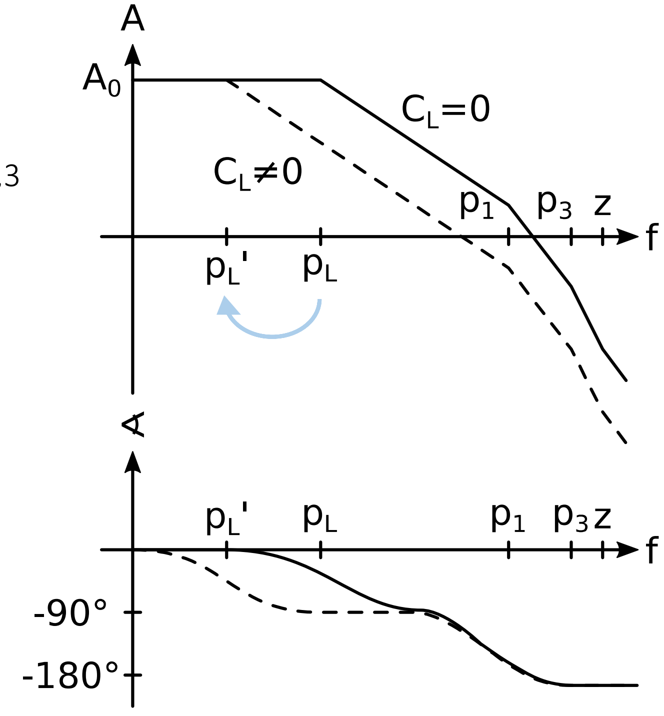
$$A_0 = \frac{\frac{g_{m1}}{g_{m4}}\cdot g_{m5}}{g_{DS5}+g_{DS6}}$$

$$A_0 = \frac{B_1 g_{m1}}{g_{DS5}+g_{DS6}} \qquad (100\ldots5000)$$

Compensation of OTA amplifier:

assume $g_{DS_1 i} << g_{m_1 i}$

$$\Rightarrow p_L = \frac{g_{DS5}+g_{DS6}}{C_L} << \frac{g_{mi}}{C_{pi}} = p_i \qquad i = 1,3$$



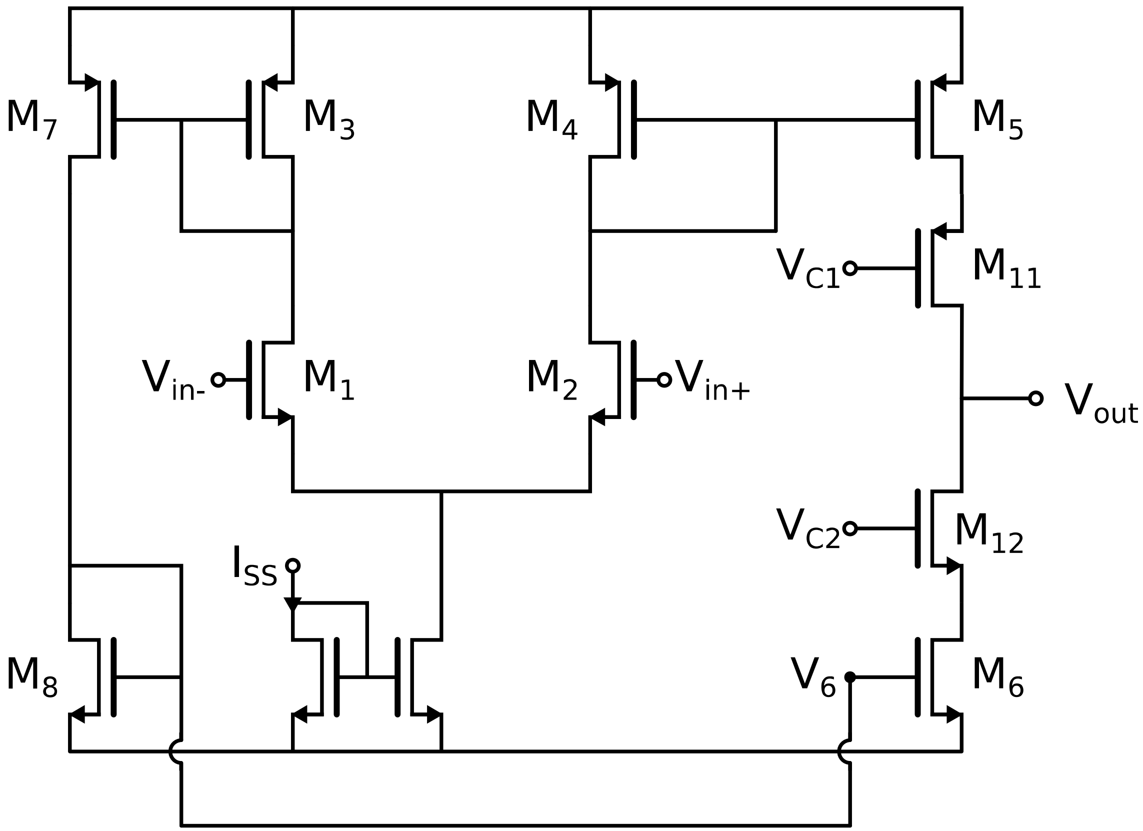
Output node is
a high impedance node!

$\rightarrow$ Compensation is
performed by increasing C_L

assume $A(s) \approx \dfrac{A_0}{\left(1+\frac{s}{p_L}\right)}$

$$\Rightarrow GBW = A_0 \cdot p_L = \frac{B_1 g_{m1}}{g_{DS5}+g_{DS6}} \cdot \frac{g_{DS5}+g_{DS6}}{C_L} = \frac{B_1 g_{m1}}{C_L} = \frac{g_m}{C_L}$$

Cascode OTA



OTA gain is

$$A = \frac{B_1 g_{m1}}{g_L} = \frac{B_1 g_{m1}}{g_{DS5} + g_{DS6}} = B_1 g_{m1}\left(R_{DS5} \,||\, R_{DS6}\right)$$

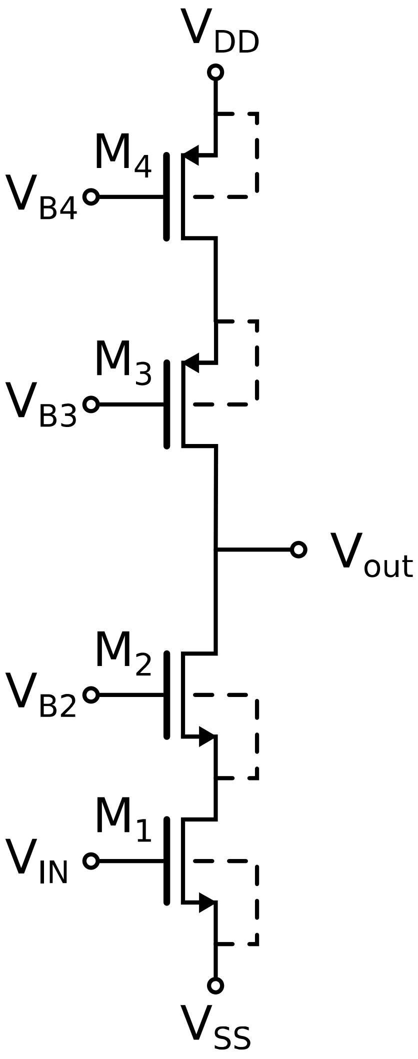
Larger output resistance gives higher voltage gain
⇒ use cascode transistors to increase the output impedance.

Replace M_5 and M_6 with cascode current sources.

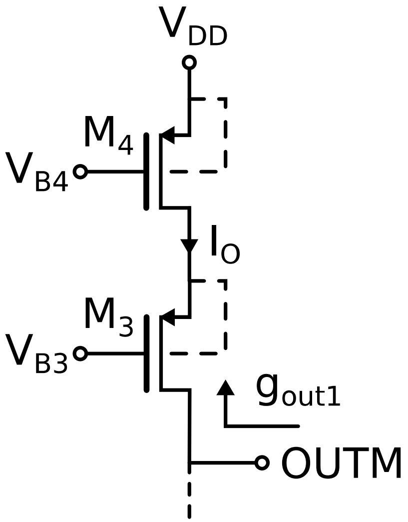
Cascode transistors increase the output impedance by the internal gain of the cascode transistor.

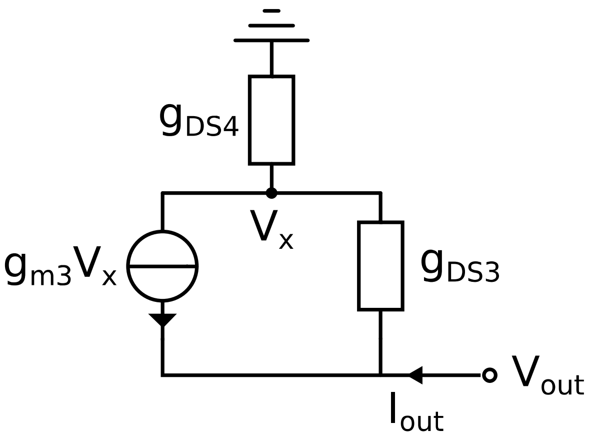
$$r_0 = \frac{1}{\frac{g_{DS5} g_{DS11}}{g_{m11}} + \frac{g_{DS6} g_{DS12}}{g_{m12}}}$$

Let's calculate the gain of a cascode amplifier. The input voltage is connected to the gate of transistor M_1 and the other transistors are biased with voltages V_{B2}, V_{B3} and V_{B4}. The difference to a simple current source loaded inverter is the addition of the cascode transistors M_2 and M_3.



Let's start the analysis with the cascode current source of M_3 and M_4 and calculate its small signal output conductance.





Writing the node equations we get

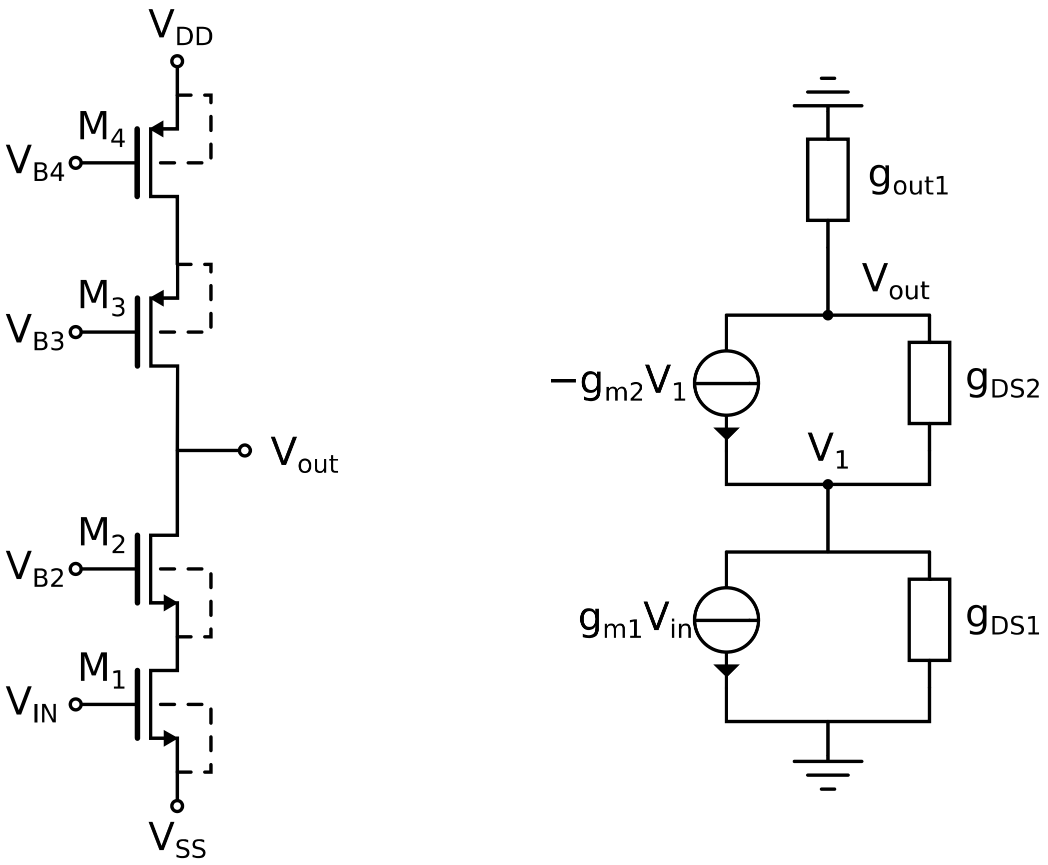
$$(g_{DS3} + g_{DS4})v_X - g_{DS3}v_{out} = -g_{m3}v_X$$

$$g_{DS3}v_{out} - g_{DS3}v_X = g_{m3}v_X + i_{out}$$

The resulting small signal output conductance is

$$g_{out1} = \frac{i_{out}}{v_{out}} = \frac{g_{DS3}g_{DS4}}{g_{DS3} + g_{DS4} + g_{m3}} \approx \frac{g_{DS3}}{g_{m3}} g_{DS4}$$

Now we can solve the rest of the small signal circuit and the resulting gain.



The node equations are

$$(g_{DS1} + g_{DS2})v_1 - g_{DS2}v_{out} = -g_{m1}v_{in} - g_{m2}v_1$$
$$(g_{out1} + g_{DS2})v_{out} - g_{DS2}v_1 = g_{m2}v_1$$

With some arranging we get

$$(g_{m2} + g_{DS1} + g_{DS2})v_1 - g_{DS2}v_{out} = -g_{m1}v_{in}$$

$$v_1 = \frac{g_{out1} + g_{DS2}}{g_{m2} + g_{DS2}} v_{out}$$

Inserting the value of v_1 to the first equation we get

$$(g_{m2} + g_{DS1} + g_{DS2}) \frac{g_{out1} + g_{DS2}}{g_{m2} + g_{DS2}} v_{out} - g_{DS2}v_{out} = -g_{m1}v_{in}$$

$$\frac{(g_{m2} + g_{DS1} + g_{DS2})g_{out1} + g_{DS1}g_{DS2}}{g_{m2} + g_{DS2}} v_{out} = -g_{m1}v_{in}$$

The transfer function after simplification ($g_m >> g_{DS}$) is

$$\frac{v_{out}}{v_{in}} = \frac{g_{m1}}{\frac{g_{DS2}}{g_{m2}} g_{DS1} + g_{out1}} = \frac{g_{m1}}{\frac{g_{DS2}}{g_{m2}} g_{DS1} + \frac{g_{DS3}}{g_{m3}} g_{DS4}}$$

The output conductance of the whole amplifier is very small due to the g_{DS}/g_m terms.

Cascode OTA

The gain of cascode OTA becomes:

$$A_0 = g_m \cdot R_L = \frac{g_m R_p R_N}{R_p + R_N} = \frac{B_1 g_{m1}}{\frac{g_{DS5} g_{DS11}}{g_{m11}} + \frac{g_{DS6} g_{DS12}}{g_{m12}}}$$

There is also a pole associated with a cascode transistor. Assuming $M_{11} = M_{12}$ (i.e. matched)

$$p_4 = \frac{g_{m11}}{C_{GS11}} \cong \frac{g_{m12}}{C_{GS12}} = p_5$$

However, as $p_4 = p_5$ => there is also a zero

$$z = \frac{1}{2}(p_4 + p_5)$$

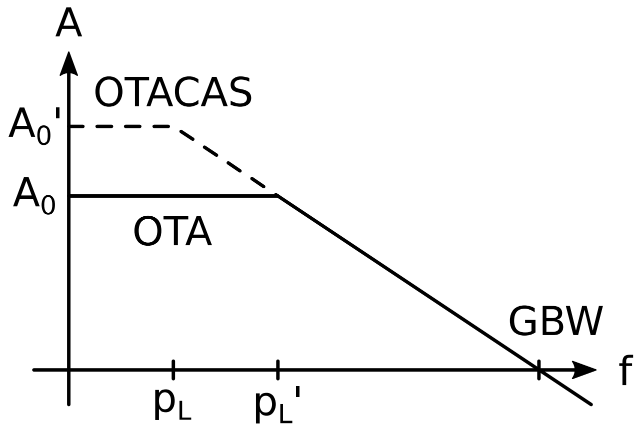
Which compensates one of the poles!

The dominant pole of the cascode OTA is

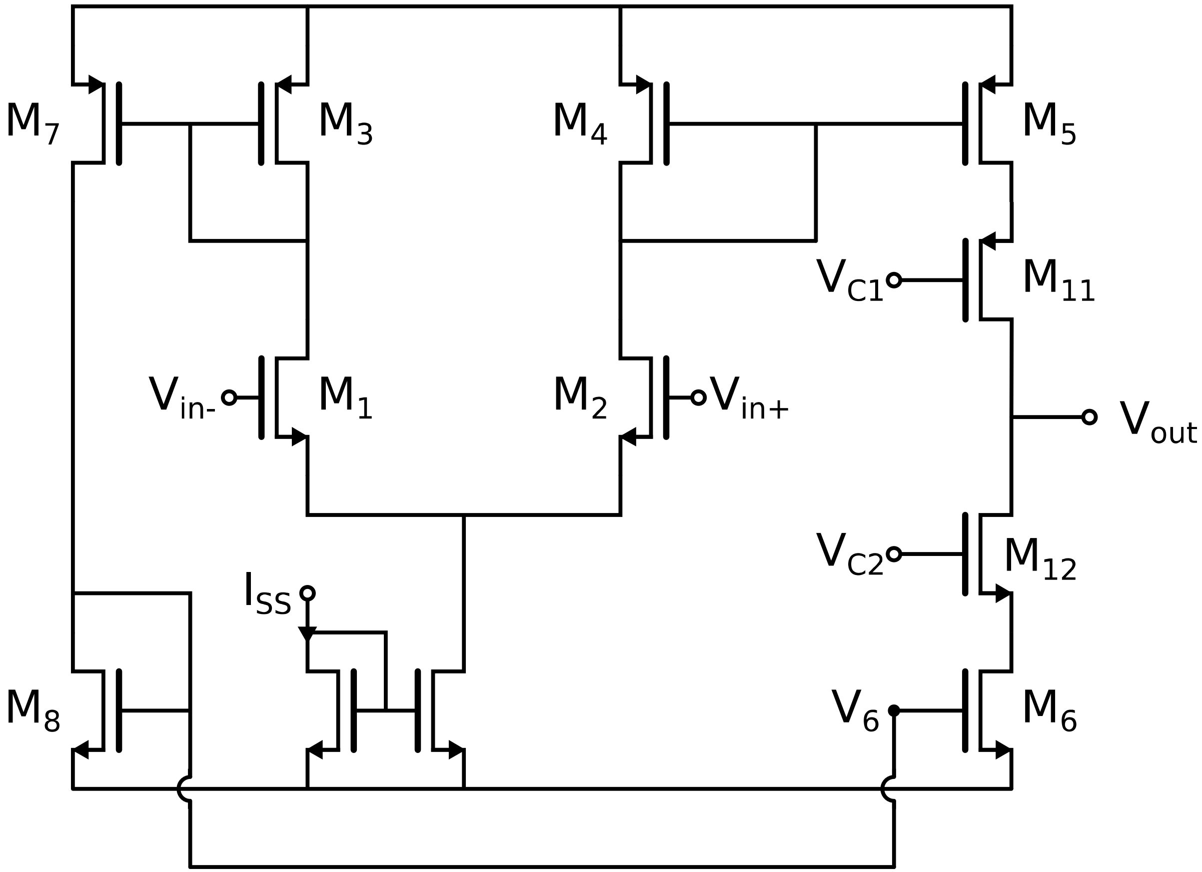
$$p_L = \frac{g_L}{C_L} = \frac{1}{R_L C_L} = \frac{\frac{g_{DS5} g_{DS11}}{g_{m11}} + \frac{g_{DS6} g_{DS12}}{g_{m12}}}{C_L}$$

$$A(s) \cong \frac{A_0}{1 + \frac{s}{p_L}}$$

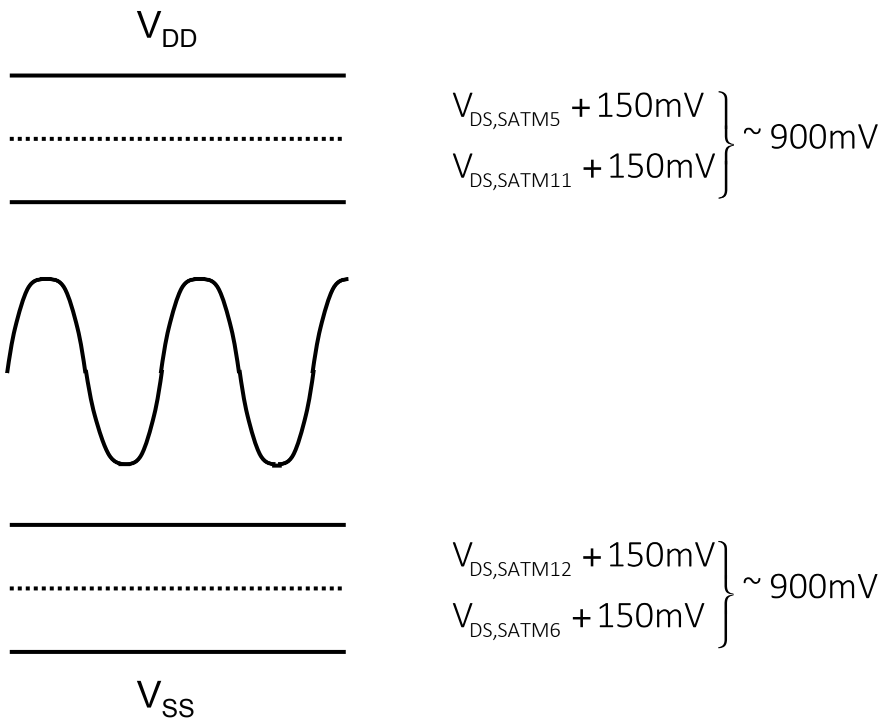
$$GBW = A_0 \cdot p_L = \frac{B_1 g_{m1}}{C_L}$$



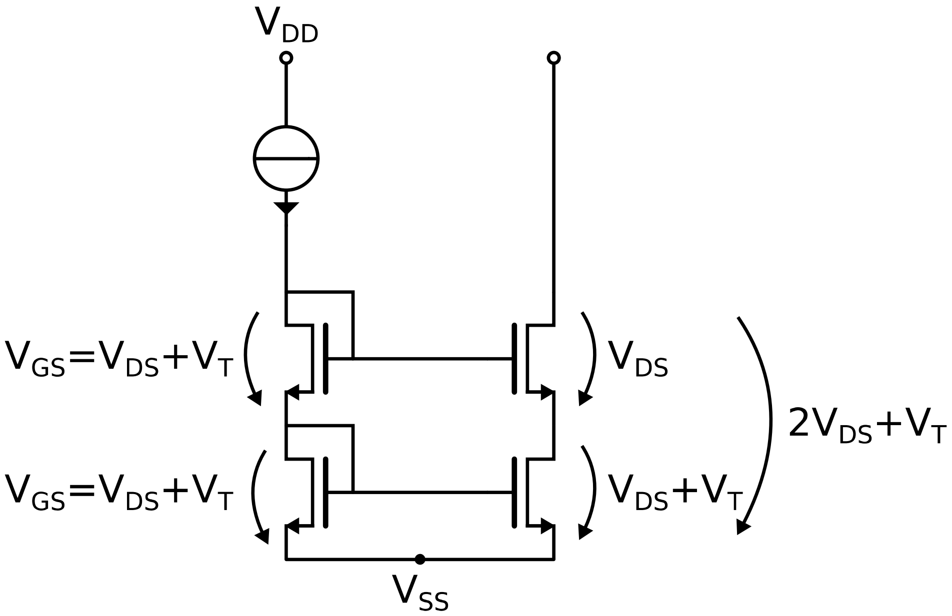
Output signal swing of cascode OTA



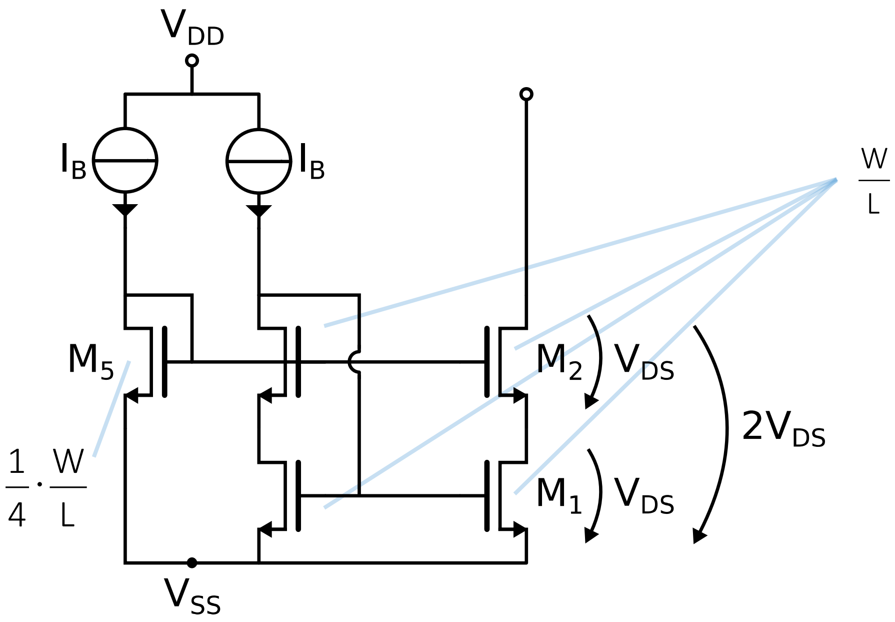
Cascode OTA has limited signal swing



Cascode biasing



Biasing for maximum output swing



$$\left(\frac{W}{L}\right)_5 = \frac{1}{4}\left(\frac{W}{L}\right)_{1,2}$$

$$\Rightarrow V_{DS5,SAT} = 2V_{DS1,SAT}$$

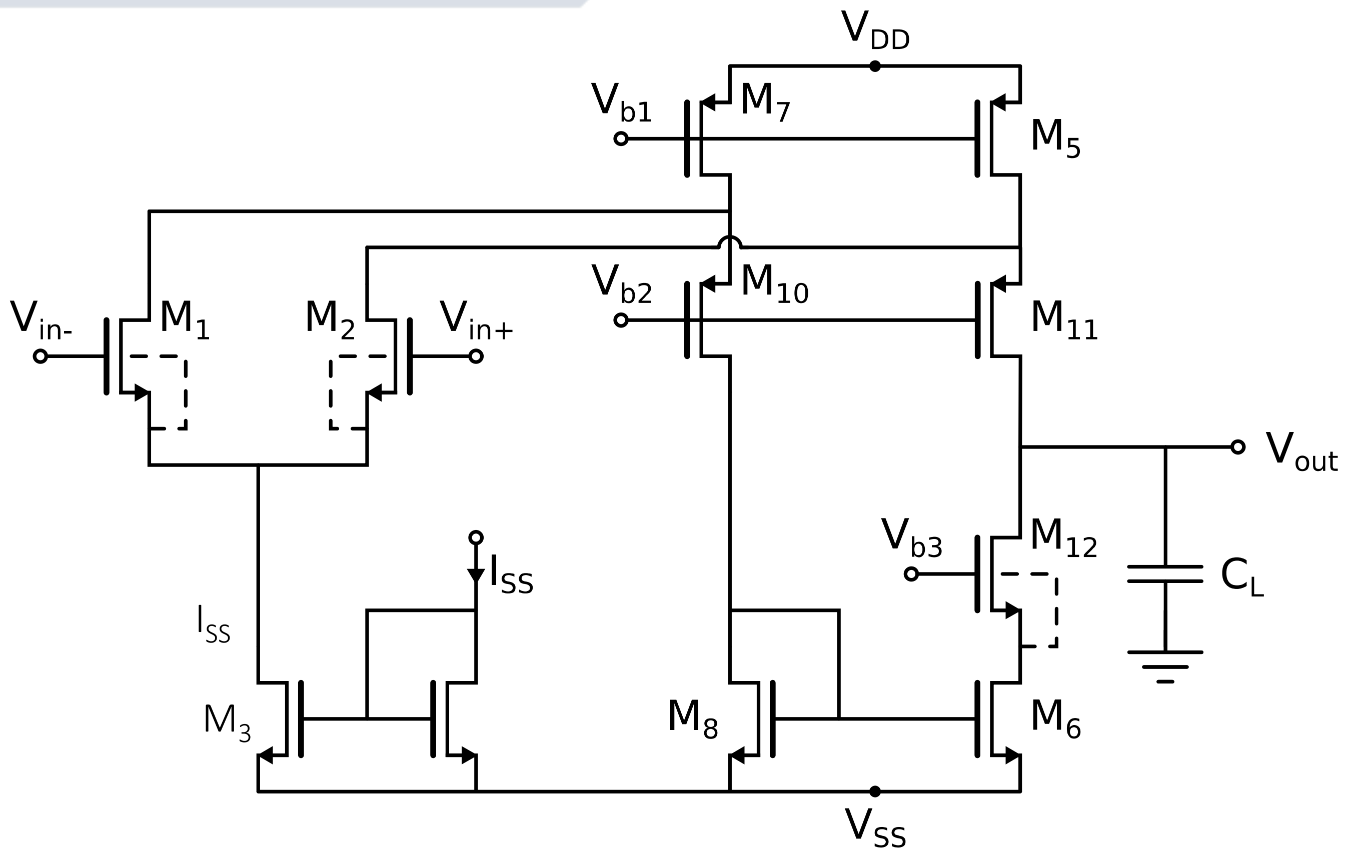
$$\Rightarrow V_{GS5} = V_{TN} + V_{DS5,SAT} = V_{TN} + 2V_{DS1,SAT}$$

$$H(s)=\frac{A_0\left(1+\frac{s}{z}\right)}{\left(1+\frac{s}{p_1}\right)\left(1+\frac{s}{p_2}\right)\left(1+\frac{s}{p_3}\right)\left(1+\frac{s}{p_L}\right)}$$

	OTA CAS	**2 Stage (Miller comp.)**
A_0	$\frac{B_1 g_{m1}}{\frac{g_{DS5}g_{DS11}}{g_{m11}}+\frac{g_{DS6}g_{DS12}}{g_{m12}}}$	$\frac{g_{m1}(g_{m8}+g_{m9})}{(g_{DS2}+g_{DS4})(g_{DS8}+g_{DS9})}$
p_1	$\frac{g_{m3}}{2C_{GS}+2C_{DB}}$	$\frac{g_{m3}}{2C_{GS}+2C_{DB}}$
p_2	$\frac{g_{m2}}{2C_{GS}+2C_{DB}}$	$\frac{(g_{DS2}+g_{DS4})(g_{DS8}+g_{DS9})}{(g_{m8}+g_{m9})C_C}=\frac{g_{m1}}{A_0 C_C}$
p_3	$\frac{g_{m11}}{C_{GS11}}$	$\frac{1}{R_z C_C}$

	OTA CAS	2 Stage (Miller comp.)
p_L	$\frac{\frac{g_{DS5}g_{DS11}}{g_{m11}} + \frac{g_{DS6}g_{DS12}}{g_{m12}}}{C_L}$	$\frac{(g_{m8}+g_{m9})C_C}{C_AC_L+(C_A+C_L)C_C} \approx \frac{g_{m8}+g_{m9}}{C_L}$
z	$\frac{1}{2p_3}$	
GBW	$\frac{B_1 g_{m1}}{C_L}$	$\frac{g_{m1}}{C_C}$
SR	$\frac{B_1 I_{SS}}{C_L}$	$\frac{I_{SS}}{C_C}$

Folded – cascode OTA



Typical biasing $I_{M3} = I_{M7} = I_{M5} = I_{SS}$
and $I_{M1} = I_{M2} = I_{M10} = I_{M11} = I_{M8} = I_{M6} = I_{SS}/2$

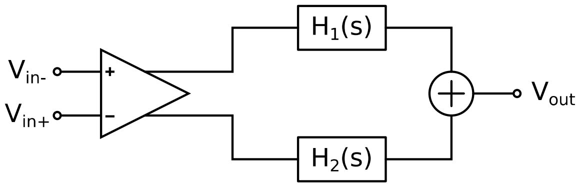
- Eliminates the diode connected load transistors of the input stage
  ⇒ one pole less
  ⇒ broader bandwidth possible
- No current mirror
  ⇒ no current gain
  ⇒ $g_m = g_{m1}$
- Larger parasitic capacitance at the source of M_{10} and M_{11}
  ⇒ cascode pole at lower frequencies

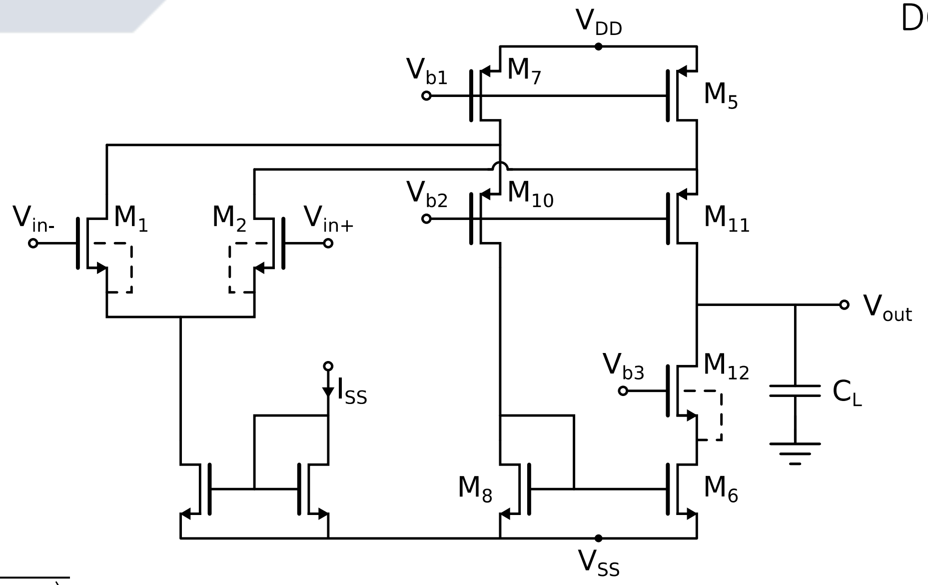
Input voltage divides the input stage biasing current I_{SS} between M1 and M2, on the other hand I_{M1} and I_{M2} defines how much biasing current of M7 and M5 goes to output stage through M10 and M11

$$I_{OUT} = I_{M1} – I_{M2}$$

Folded – cascode OTA transferfunction

Folded-cascode OTA transferfunction analysis:





$$H_1(s) = \frac{V_{OUT}}{V_{in}/2} = \frac{A_0}{\left(1+\frac{s}{p_1}\right)\left(1+\frac{s}{p_L}\right)}$$

$$H_2(s) = \frac{V_{OUT}}{V_{in}/2} = \frac{A_0}{\left(1+\frac{s}{p_1}\right)\left(1+\frac{s}{p_2}\right)\left(1+\frac{s}{p_3}\right)\left(1+\frac{s}{p_L}\right)}$$

$$H(s) = H_1(s) + H_2(s) = \frac{V_{OUT}}{V_{in}} = \frac{A_0\left(1+\frac{s}{z_2}\right)\left(1+\frac{s}{z_3}\right)}{\left(1+\frac{s}{p_1}\right)\left(1+\frac{s}{p_2}\right)\left(1+\frac{s}{p_3}\right)\left(1+\frac{s}{p_L}\right)}$$

DC-gain:

$$A_0 = \frac{g_{m1}}{\frac{g_{DS6}g_{DS12}}{g_{m12}} + \frac{(g_{DS2}+g_{DS5})g_{DS11}}{g_{m11}}}$$

Load pole: p_L is the dominant pole

$$p_L = \frac{g_L}{C_L} = -\frac{\frac{g_{DS6}g_{DS12}}{g_{m12}} + \frac{(g_{DS2}+g_{DS5})g_{DS11}}{g_{m11}}}{C_L}$$

Cascode-transistor M_{11}(= M_{10}) pole:

$$p_1 = \frac{-g_{m11}}{C_{GS11}+C_{DB2}+C_{DB5}+C_{DB11}}$$

Pole-zero pair of current mirror M_8 and M_6:

$$p_2 = \frac{-g_{m8}}{C_{GS8}+C_{GS6}+C_{DB8}+C_{DB10}} \qquad z_2 \cong p_2$$

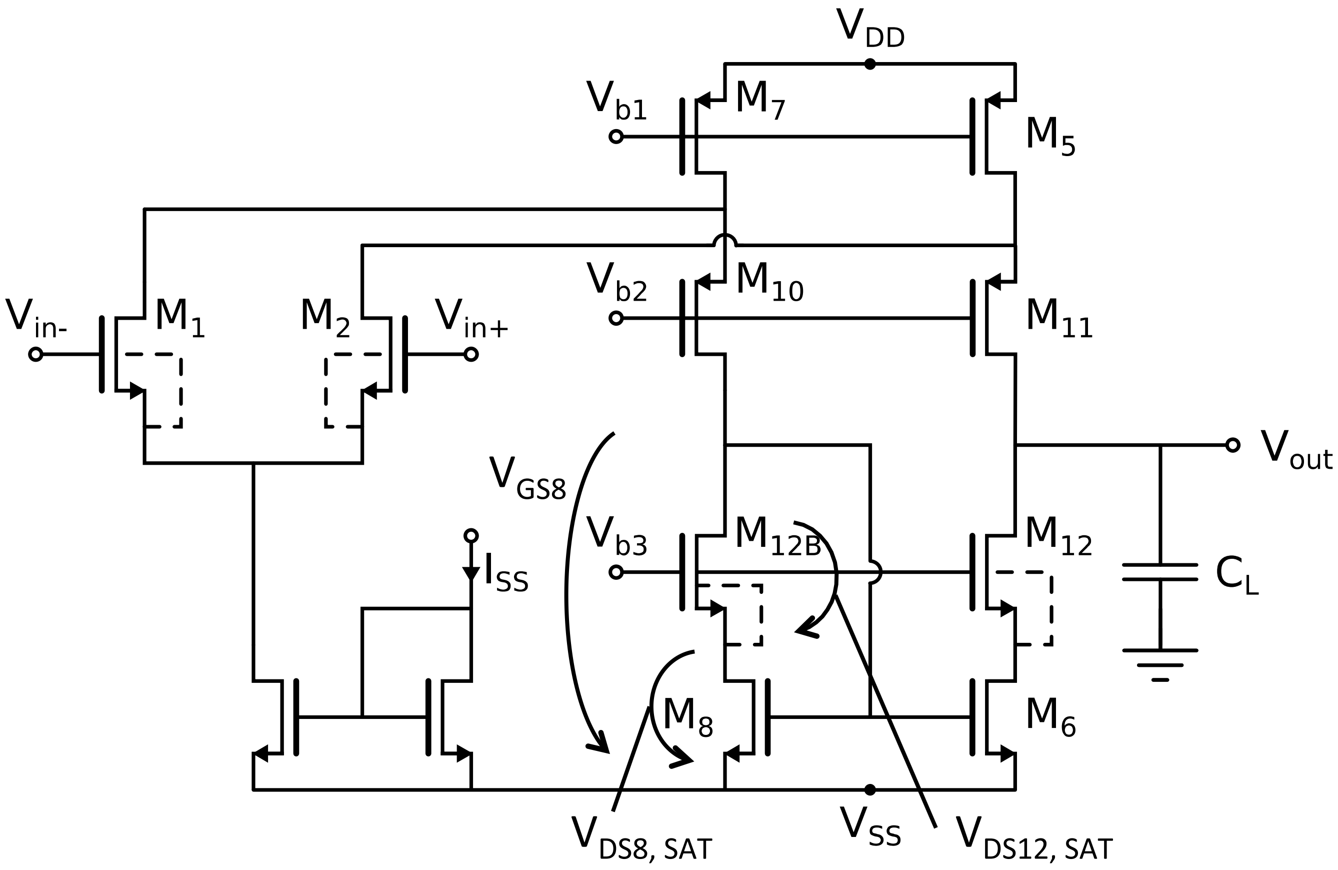
Pole-zero pair due to cascode device M_{12}:

$$P_3 = \frac{-g_{m12}}{C_{DB6}+C_{SB12}+C_{GS12}} \qquad z_3 \cong p_3$$

P_L is dominant pole $p_L << p_i \Rightarrow$ $\quad A(s) \approx \frac{A_0}{1+\frac{s}{p_L}}$

GBW is given by: $GBW = p_L \cdot A_0 = \frac{g_{m1}}{C_L}$

Modified folded – cascode OTA

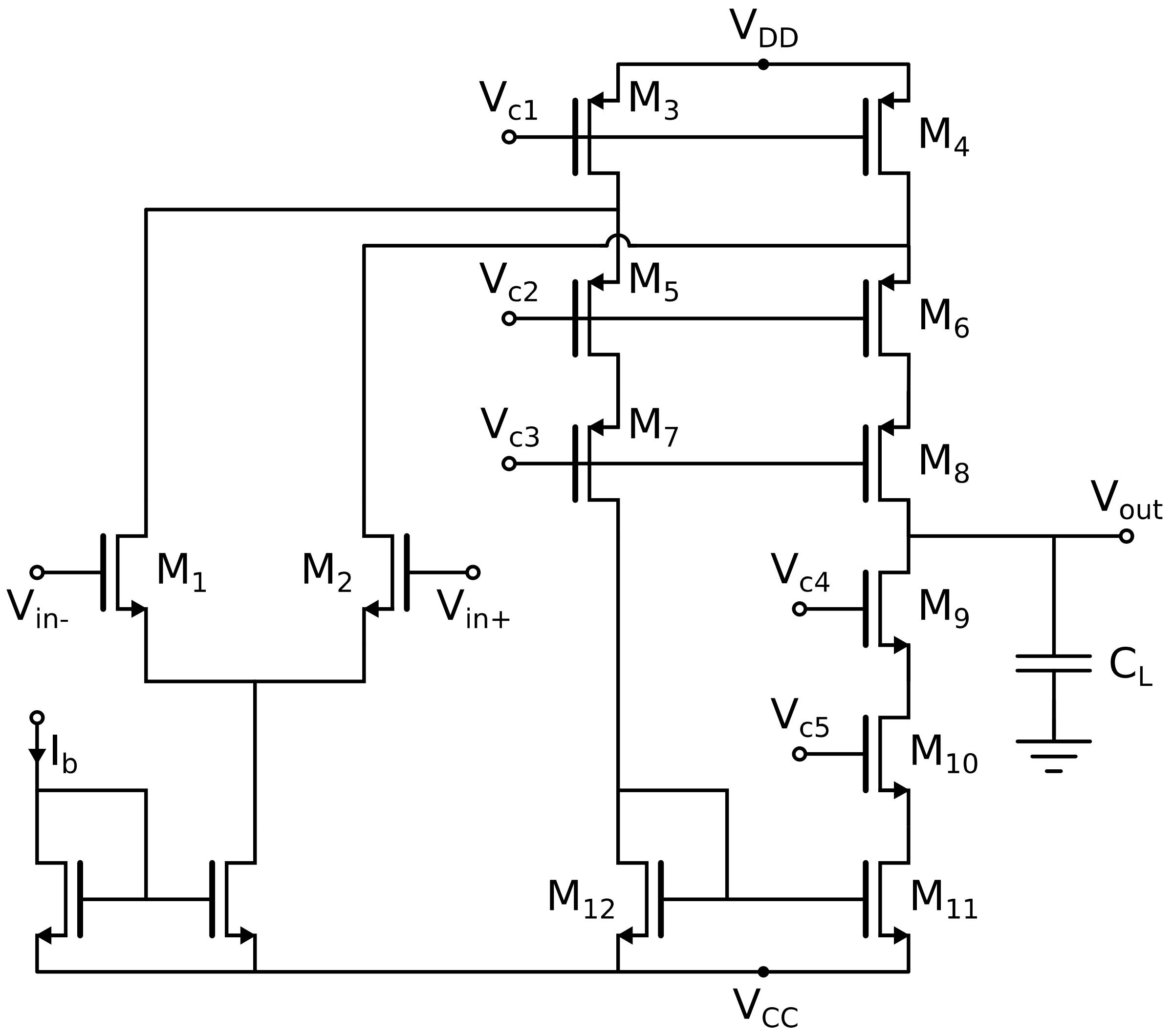


Ideally ZERO offset:

Cascode transistor M_{12B} added so that:

- $V_{DS8} \equiv V_{DS6}$
  $\Rightarrow I_{D,M8} \equiv I_{D,M6}$
- Channel length modulation eliminated
  $\Rightarrow$ systematic offset eliminated
  $\Rightarrow$ also PSRR improved
- DC operating point harder to design to keep M_8 in saturation
  $V_{GS8} > V_{DS12,SAT} + V_{DS8,SAT}$
  $V_{GS8} = V_{DS8,SAT} + V_{T8}$
  $V_{DS12,SAT} < V_{T8}$

Tripple – cascode FOTA



Second cascode transistor added to increase the output impedance and DC-gain:

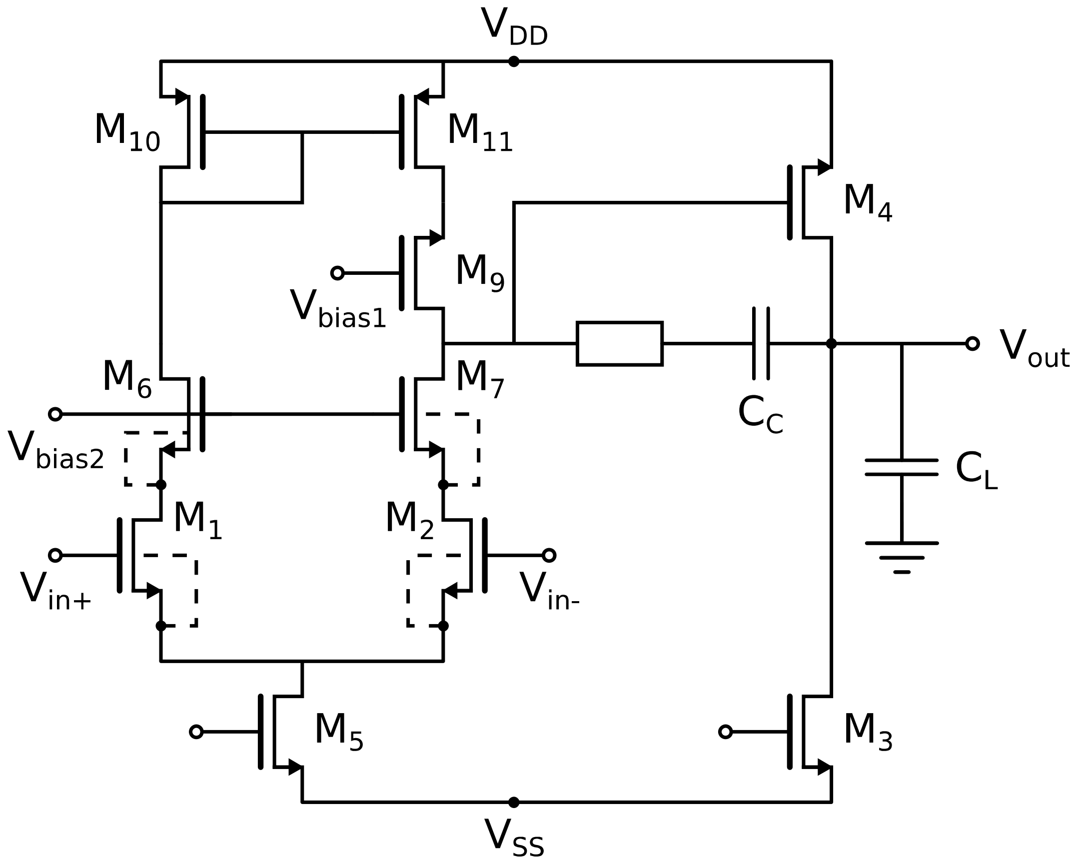
$$A = \frac{g_{m1}}{\frac{(g_{d4} + g_{d2})g_{d6} \cdot g_{d8}}{g_{m6} \cdot g_{m8}} + \frac{g_{d11} \cdot g_{d10} \cdot g_{d9}}{g_{m10} \cdot g_{m9}}}$$

$$\approx 10^6$$

$$= 120\text{dB}$$

- Reduced output swing due to three devices in series (all need to be in saturation for high gain)

Miller compensated amplifier with cascode input stage

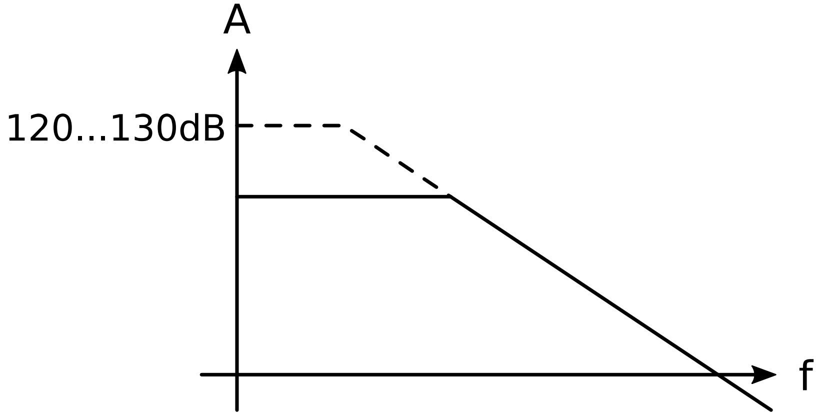


Cascode-transistors added to input gain stage to increase the output impedance and gain by gain of cascode transistor.

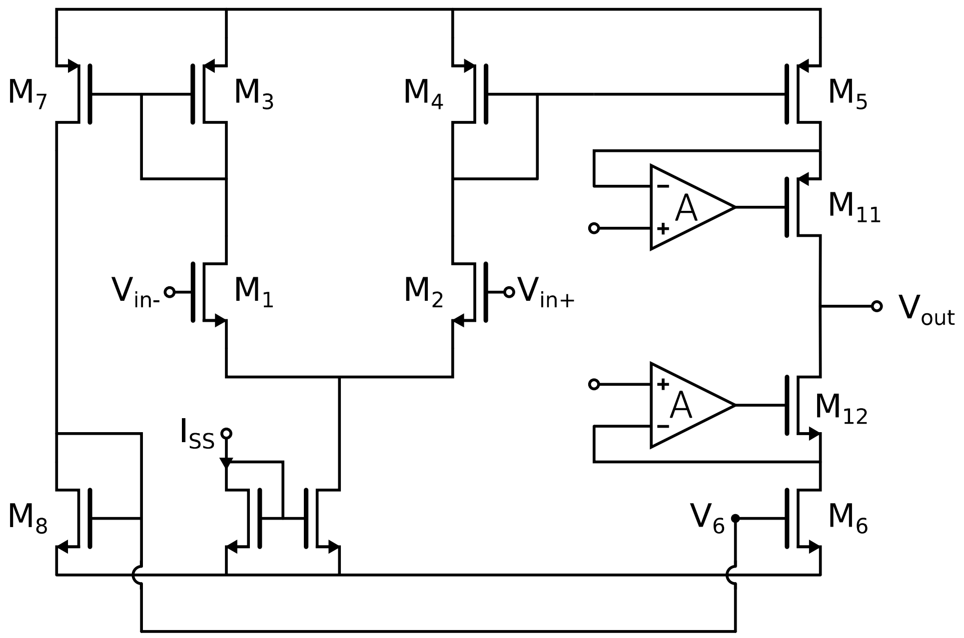
Cascode transistors do not limit linear signal range because only 10-20 mV signal swing needed at the output of the input stage.

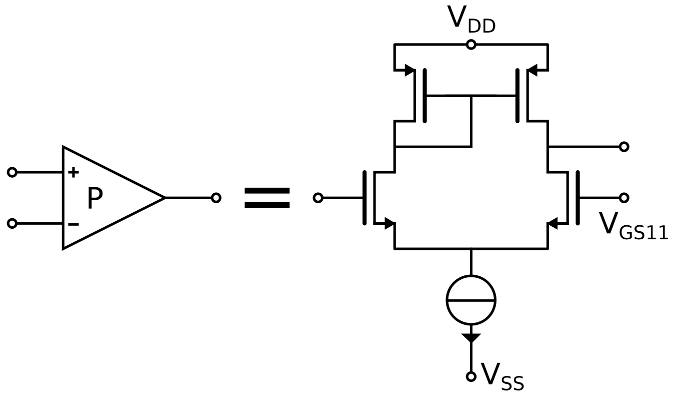
Gain increased by 30-50 dB and can be as high as 120…130 dB.

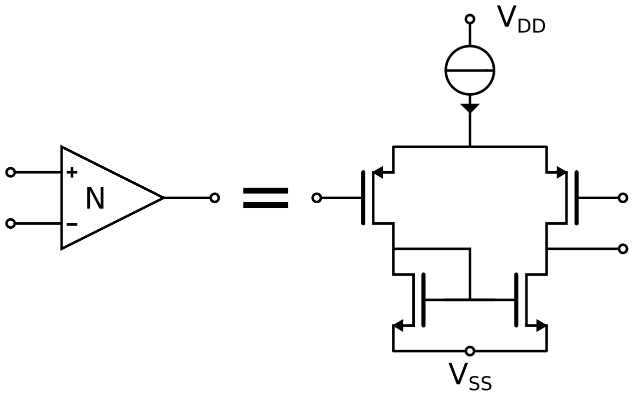
$$A_0 = \frac{g_{m1} g_{m4}}{\left(g_{DS3} + g_{DS4}\right)\left(\dfrac{g_{DS11} \cdot g_{DS9}}{g_{m9}} + \dfrac{g_{DS2} \cdot g_{DS7}}{g_{m7}}\right)}$$



Regulated cascode OTA







- Regulated cascode transistors increases the output impedance

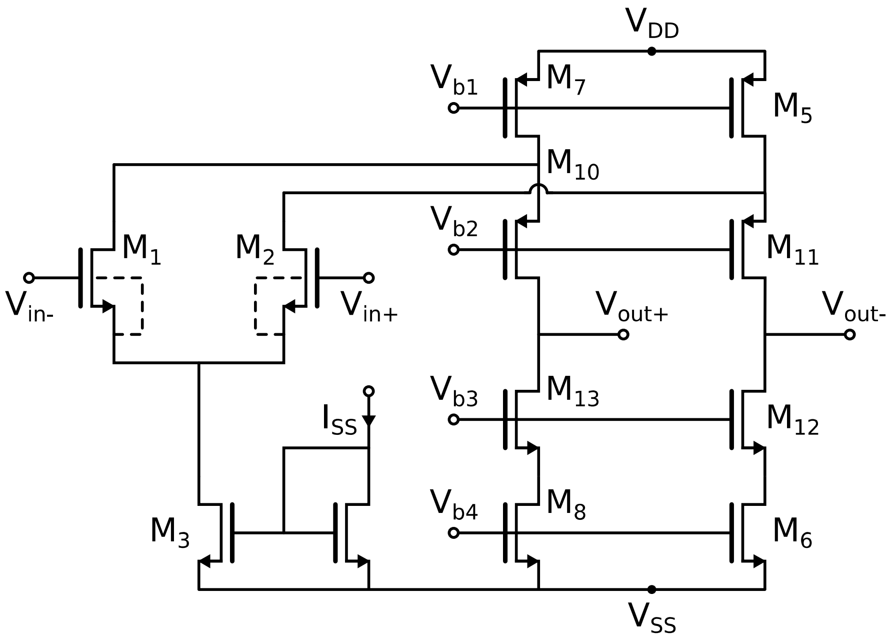
$$r_{OUT} = \frac{1}{\frac{g_{DS5}g_{DS11}}{Ag_{m11}} + \frac{g_{DS6}g_{DS12}}{Ag_{m12}}}$$

- Output impedance and gain are increased with the gain of A
- Settling is affected by regulation amplifiers, may cause ringing
- The gain of regulated cascode OTA:

$$A = Bg_{m1}V_{OUT}$$

$$= \frac{ABg_{m1}}{\frac{g_{DS5}g_{DS11}}{g_{m1}} + \frac{g_{DS6}g_{DS12}}{g_{m12}}}$$

Fully differential OTA



- No diode connection of M_8
  $\Rightarrow$ one zero-pole pair less
  $\Rightarrow$ faster settling
- Fully symmetrical
  $\Rightarrow$ very good PSRR

  Disturbances from power lines rejected.

Ideally a 2-pole transfer-function:

$$H(S) = \frac{A_0}{\left(1+\frac{S}{p_1}\right)\left(1+\frac{S}{p_2}\right)}$$

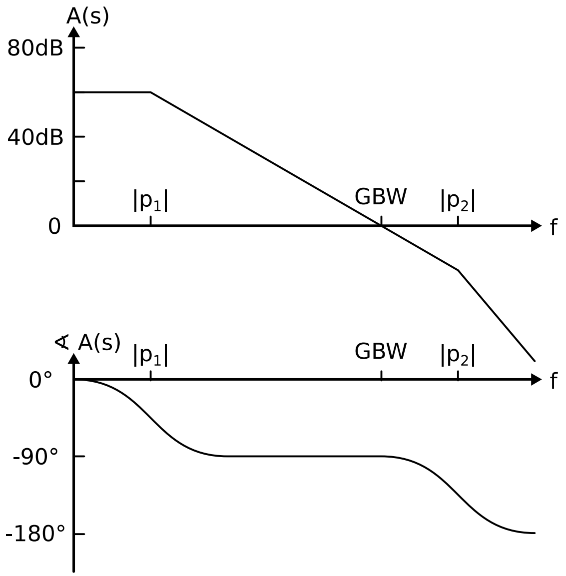
$$A_0 = \frac{g_{m1}}{\frac{g_{DS6}g_{DS12}}{g_{m12}} + \frac{\left(g_{DS2}+g_{DS5}\right)\, g_{DS11}}{g_{m11}}}$$

$$p_1 = -\frac{\frac{g_{DS6}g_{DS12}}{g_{m12}} + \frac{\left(g_{DS2}+g_{DS5}\right)\, g_{DS11}}{g_{m11}}}{C_L}$$

$$p_2 = \frac{-g_{m11}}{C_{GS11}+C_{DB2}+C_{DB5}+C_{DB11}}$$

$p_1 << p_2$ P_2 is a dominant pole

$$GBW = p_1 \cdot A_0 = \frac{g_{m1}}{C_L}$$



Needs a common-mode feedback to stabilize output DC-level (output can fluctuate freely).