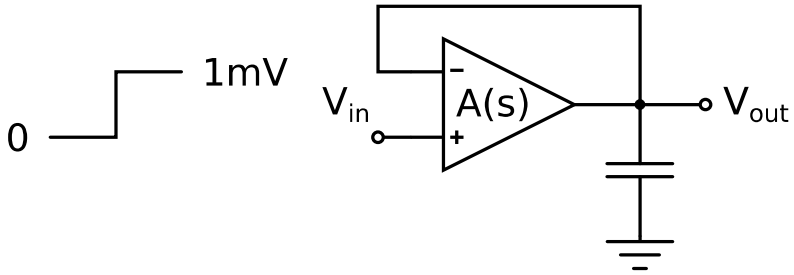
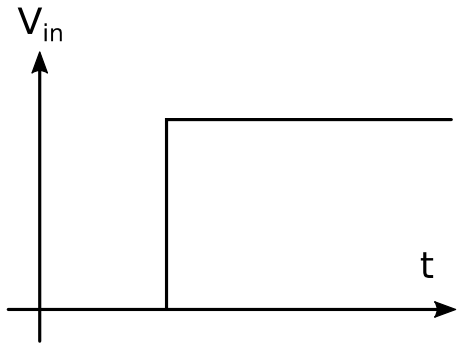
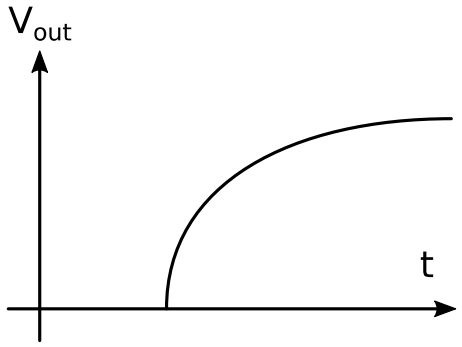
ELEC-E3510 Basics of IC Design

Lecture 7:
Comparators

Settling with small input step







Open loop gain:

$$A(s) = \frac{A_0}{1 - \frac{s}{s_{p_1}}} \qquad ,s >> s_{p_1} \Rightarrow A(s) = \frac{A_0}{\frac{s}{s_{p_1}}} = \frac{1}{\frac{s}{CBW}}$$

Closed loop gain:

$$H(s) = \frac{A(s)}{1 + \beta A(s)} = \frac{1}{1 + \frac{s}{GBW}}$$

Step response for closed loop amplifier:

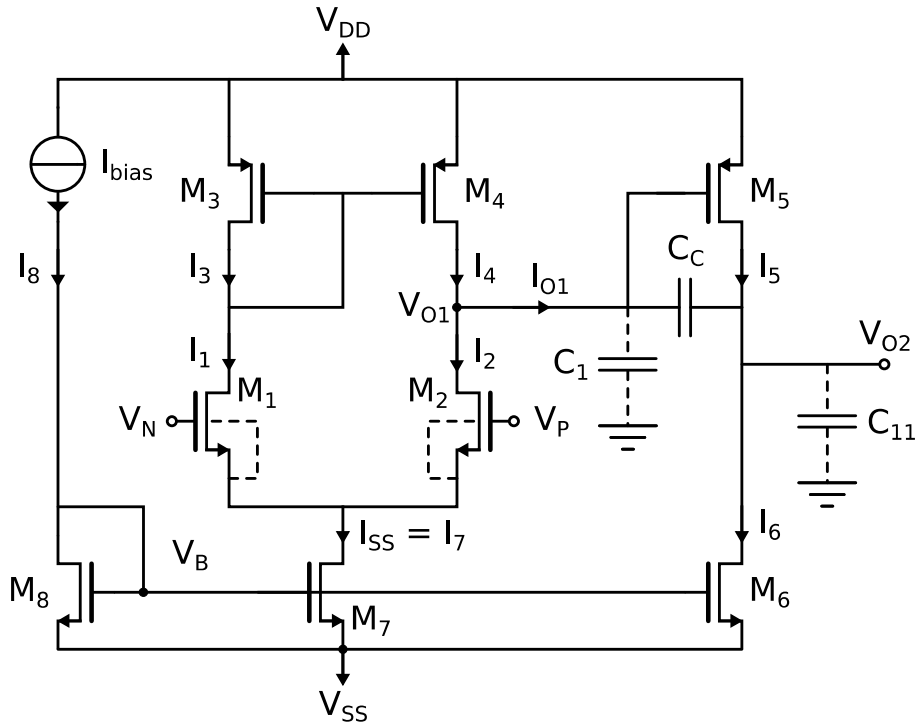
$$V_{out}(t) = V_{in}\left(1 - e^{-A_0 s_{p_1} t}\right) = V_{in}\left(1 - e^{-GBW t}\right)$$

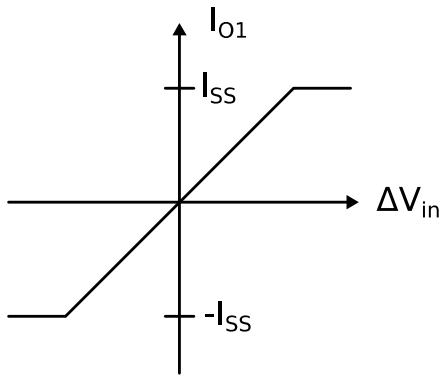
Settling is exponential with small input signal.
The time constant is determined by GBW:

$$GBW = \frac{g_{m1}}{C_C} \quad \text{for 2-stage amplifier}$$

$$GBW = \frac{g_{m1}}{C_L} \quad \text{for OTA-amplifier}$$

Settling with large input step





The maximum speed of change in input stage:

$$\frac{dV_{O1}}{dt} = \frac{I_{SS}}{C_1 + C_C} = SR = \text{slewrate}$$

The maximum speed of change in output stage:

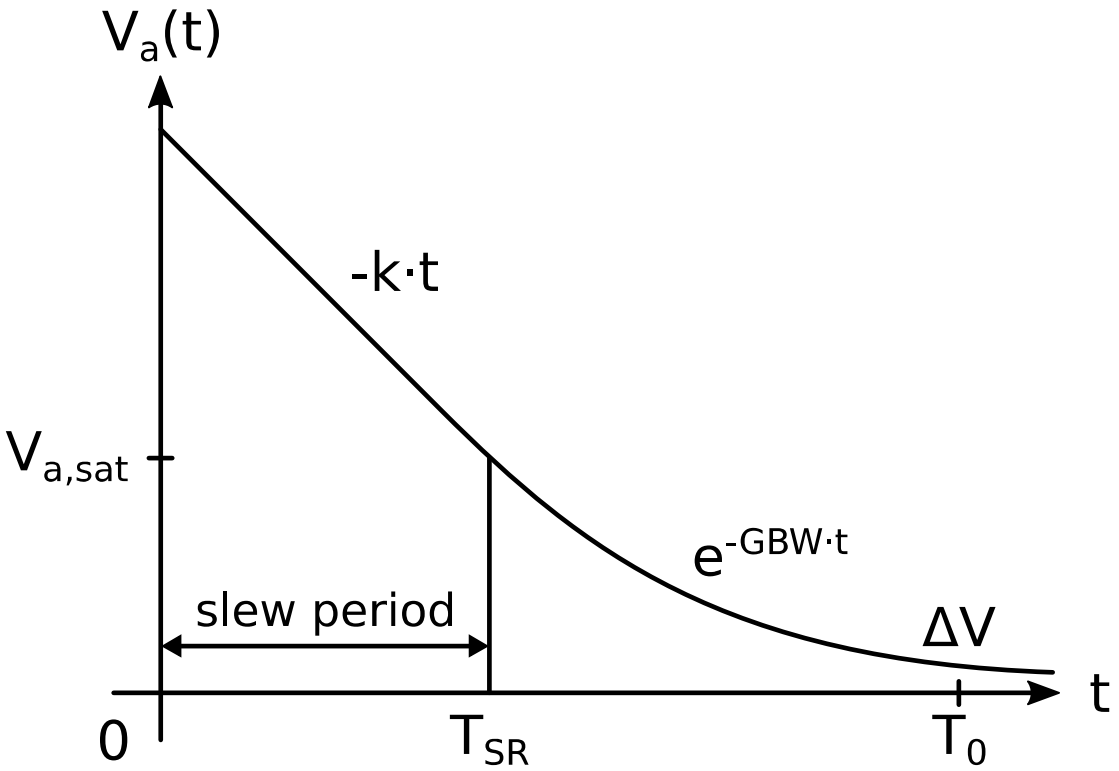
$$V_{O2}\downarrow \qquad \frac{dV_{O2}}{dt} = \frac{I_6}{C_{11}}; \qquad \text{down-step}$$

$$V_{O2}\uparrow \qquad \frac{dV_{02}}{dt} = \frac{I_5 - I_6}{C_{11}}; \qquad \text{up-step}$$

Symmetrical settling when input stage dominates:
Normally select

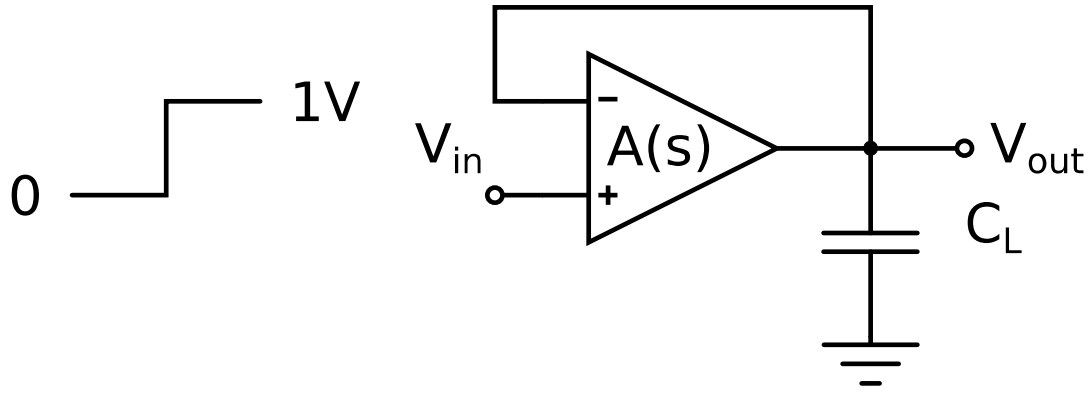
$$\frac{dV_{01}}{dt} = \frac{I_{SS}}{C_1 + C_C} < \frac{I_6}{C_{11}} = \frac{dV_{02}}{dt}$$

Closed loop system



In closed loop system

- With large input step, settling occurs first with slewing.
- After input voltage is smaller than $V_{a,sat}$ settling occurs with GBW.



Non-symmetry in the settling of input stage

Up-pulse:

$$I_{out}(t) = I_o + i\omega(t)$$

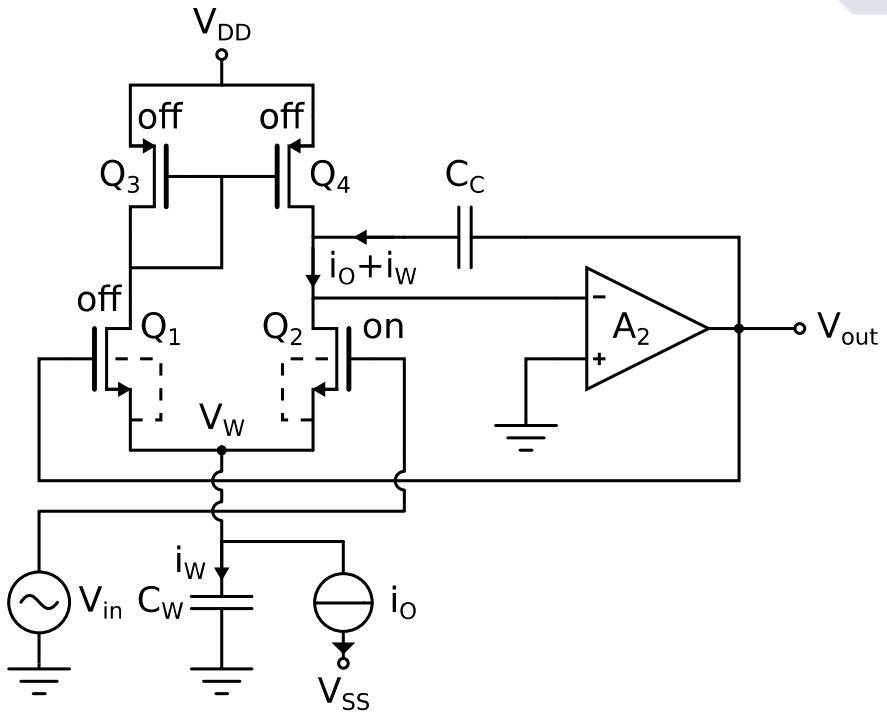
$$\frac{dV_{out}}{dt} = \frac{I_{out}(t)}{C_C}$$

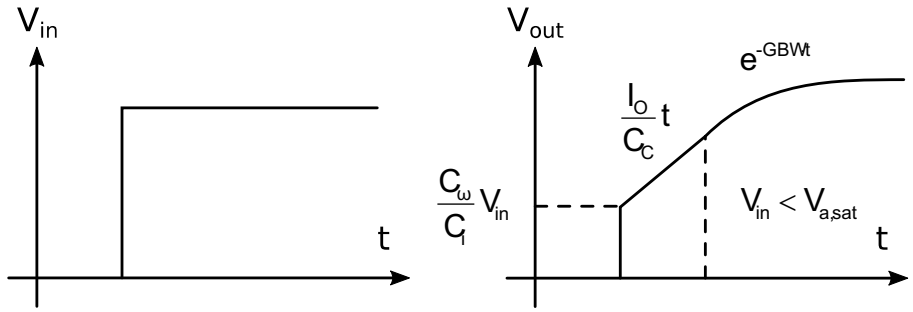
$$\Rightarrow i_\omega = C_\omega \frac{dV_{in}(t)}{dt}$$

$$V_{out}(t) = \frac{1}{C_C}\int_0^t (I_o + i\omega)dt$$

$$= \frac{I_o}{C_C}t + \frac{C_\omega}{C_C}\int_0^t \frac{dV_{in}}{dt}\cdot dt$$

$$= \frac{I_o}{C_C}t + \frac{C_\omega}{C_C}\cdot V_{in}$$





Down-pulse:

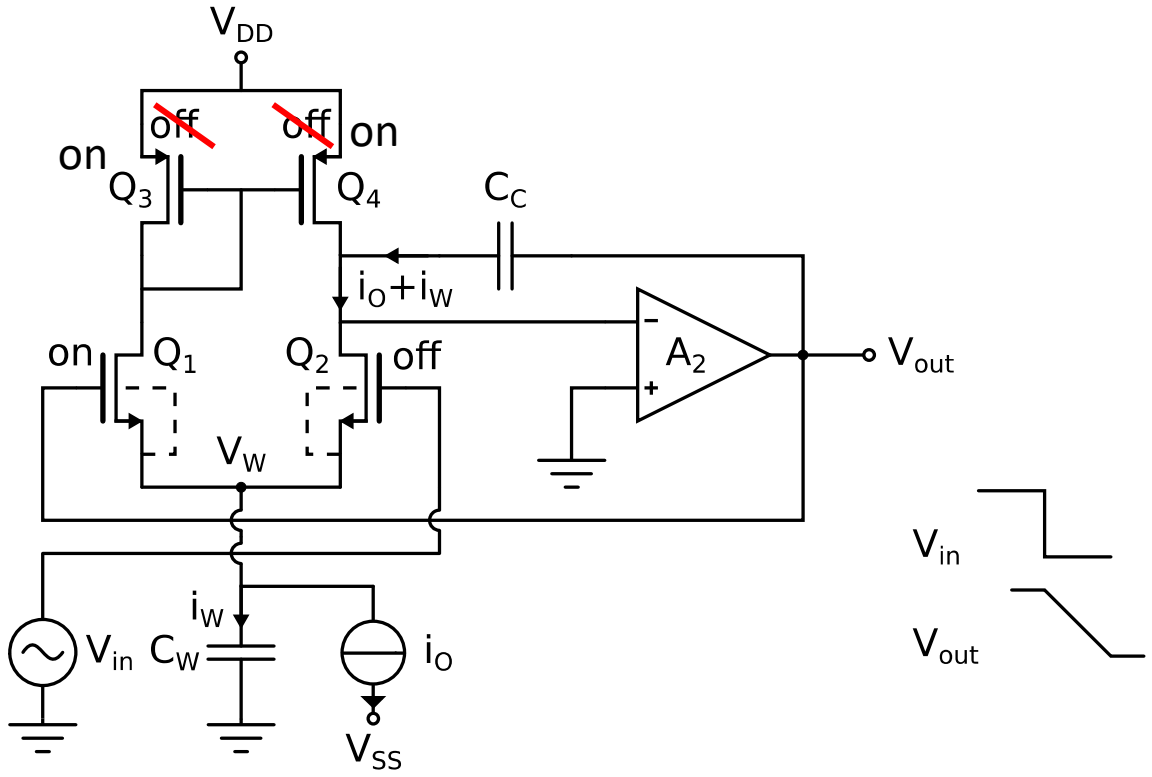
$$(1)\frac{dV_{OUT}}{dt} = -\frac{I_o - i_\omega}{C_C}$$

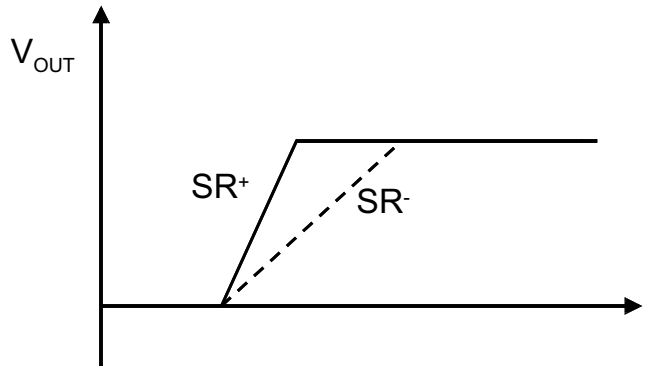
$$(2)\frac{dv_W}{dt} = \frac{dV_{OUT}}{dt} = -\frac{i_\omega}{C_\omega}$$

$$\Rightarrow i_\omega = \frac{C_\omega}{C_C + C_\omega}\cdot I_O$$

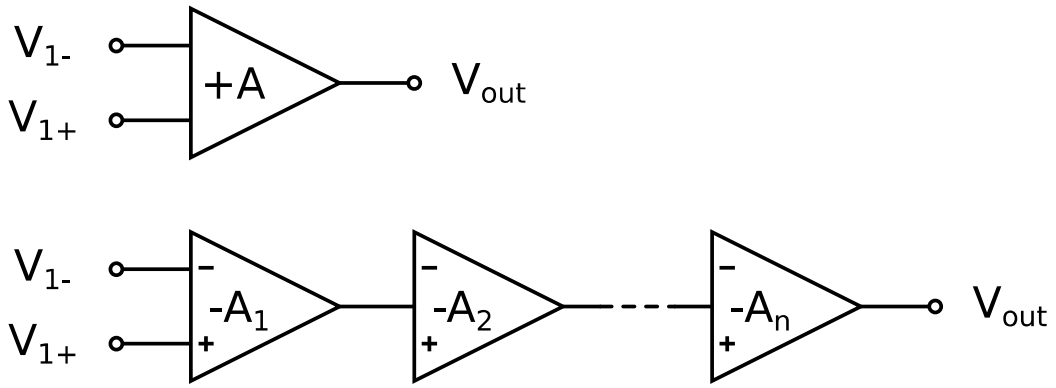
$$\Rightarrow \frac{dV_{out}}{dt} = -\frac{I_O}{C_C + C_\omega}$$

$$\Rightarrow SR^- = \frac{I_O}{C_C + C_\omega} < SR^+ = \frac{I_O}{C_C}$$





Comparator resolution



A	Res.
40dB	30mV
60dB	3mV
80dB	0,3mV
100dB	30µV

Resolution:

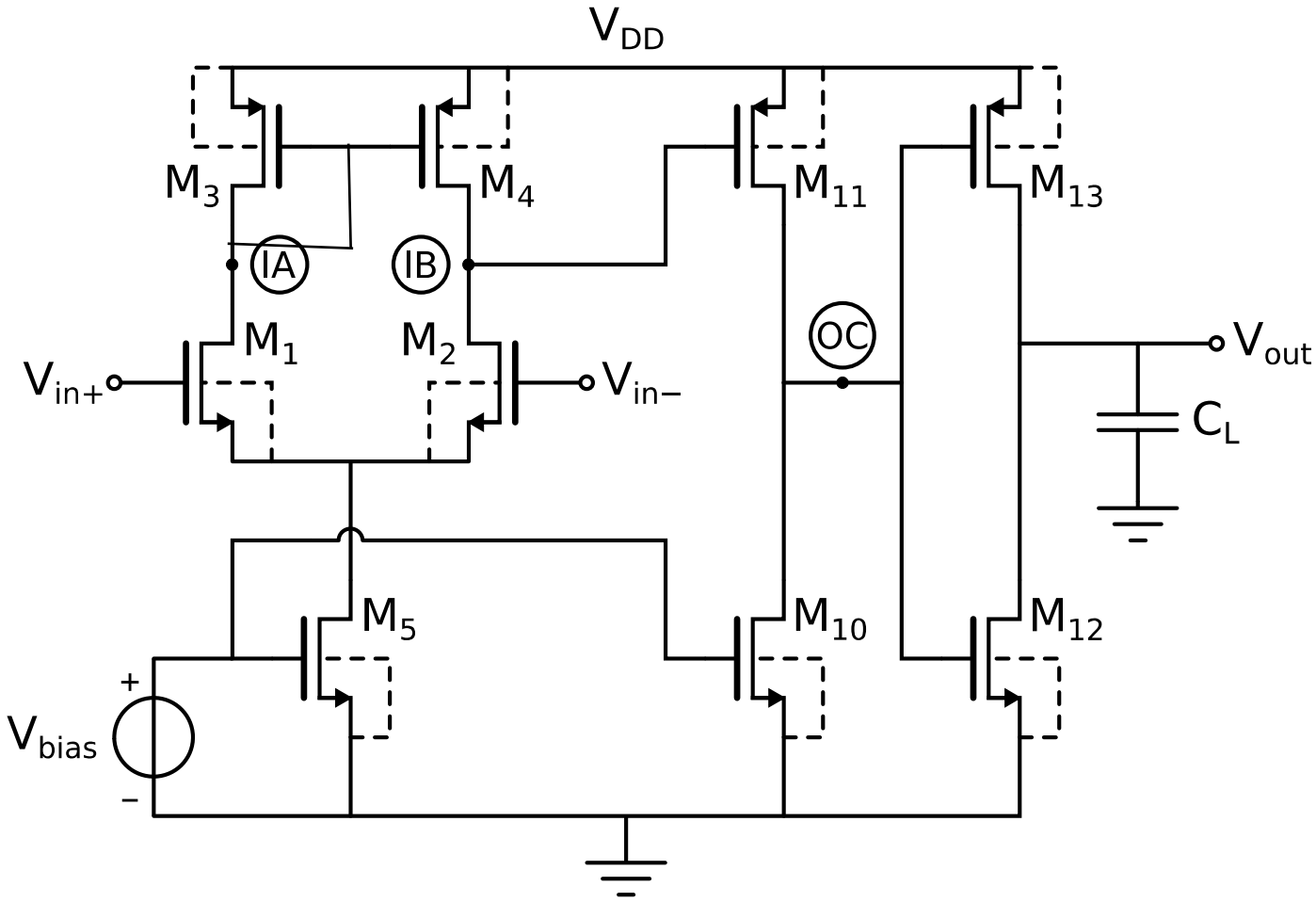
$$\Delta V_{in} = \frac{V_{OH} - V_{OL}}{A}$$

$V_{OH} - V_{OL} = 3V$
$A_i = 30...40dB$

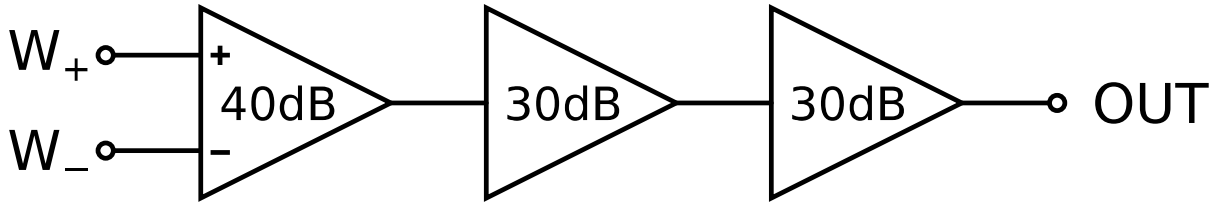
Resolution is limited by offsets and noise.

Example:
$V_{off2} = 10mV$

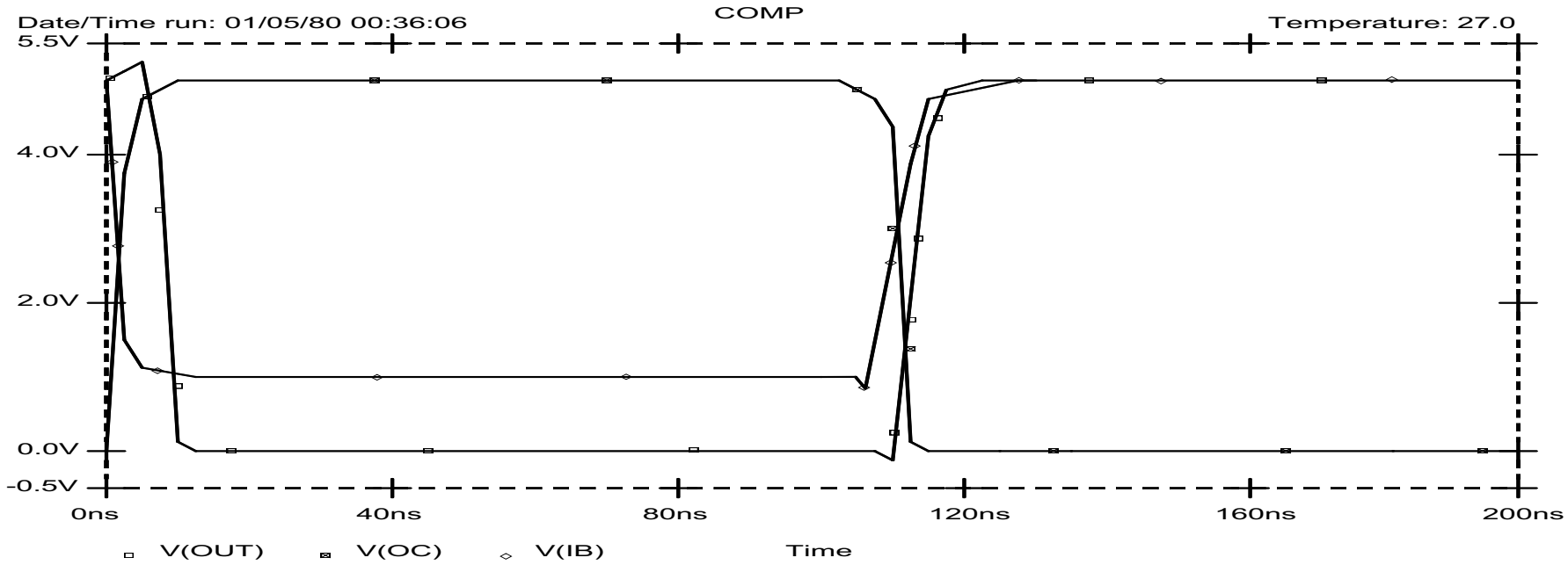
$$\Rightarrow \Delta V_{in} > \frac{V_{off2}}{A_1} = \frac{10mV}{100} = 0,1mV$$



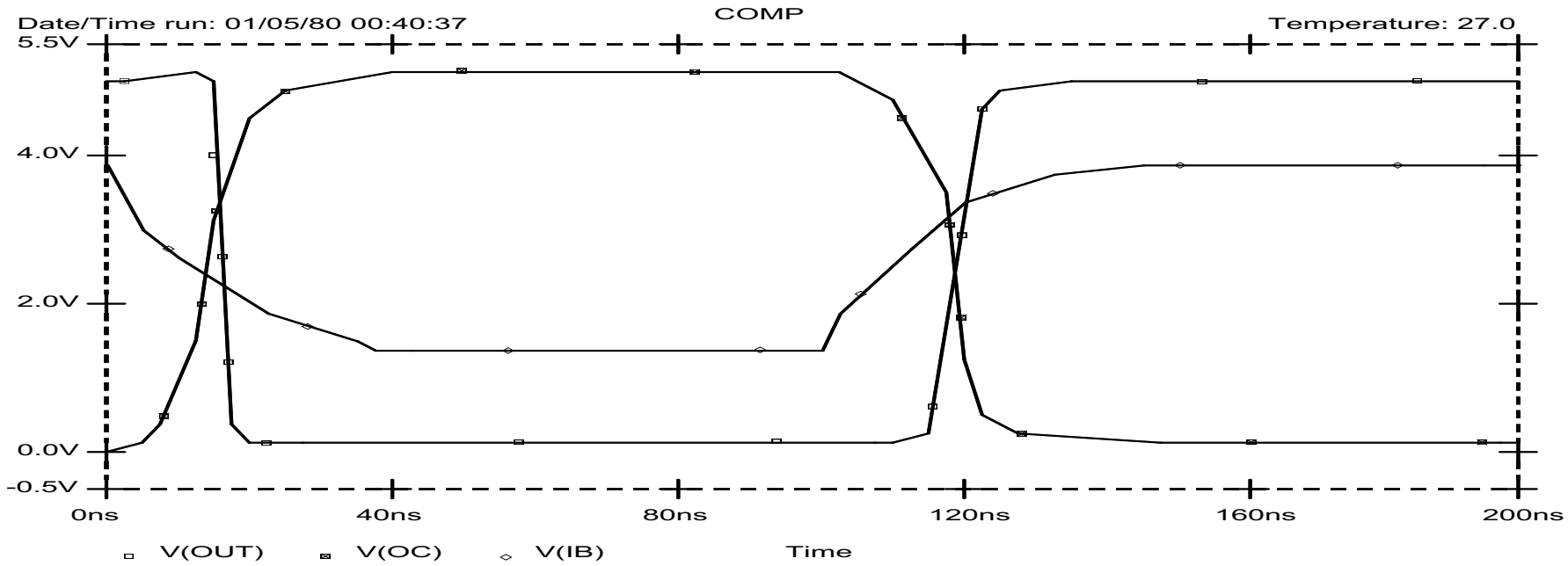
V_{bias} = 1.5V
C_L = 130.4fF



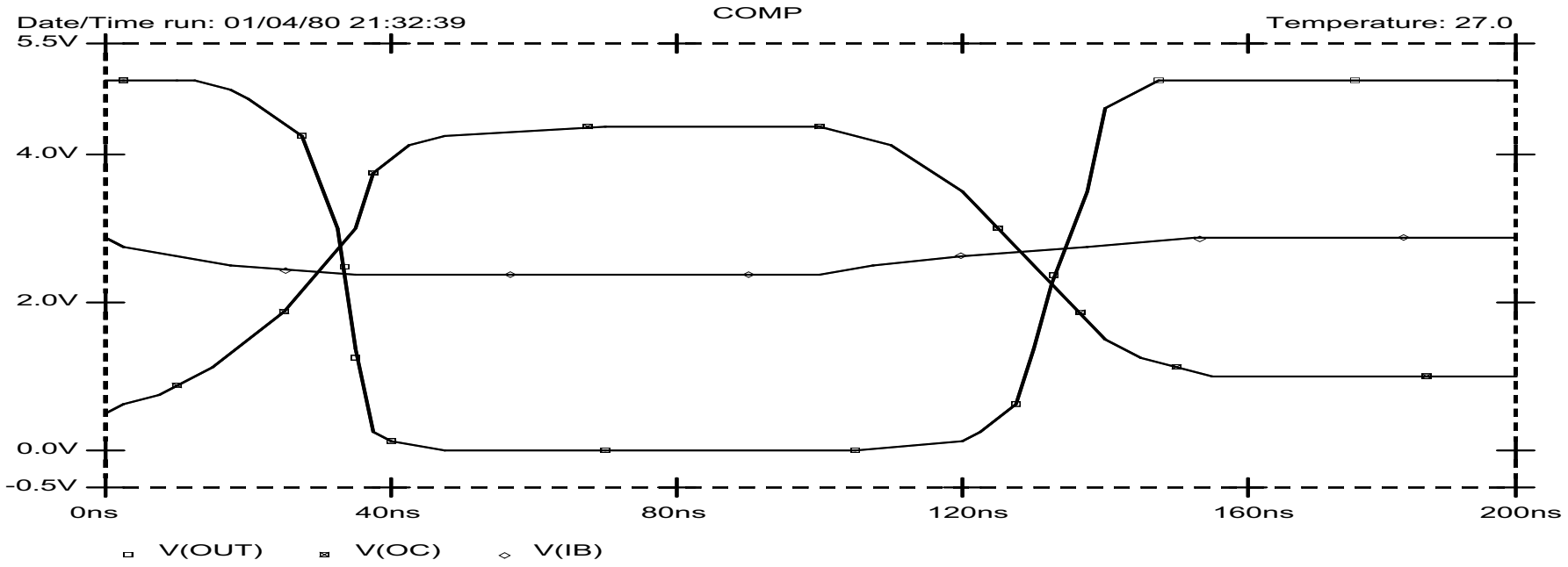
V_{in} = 1V



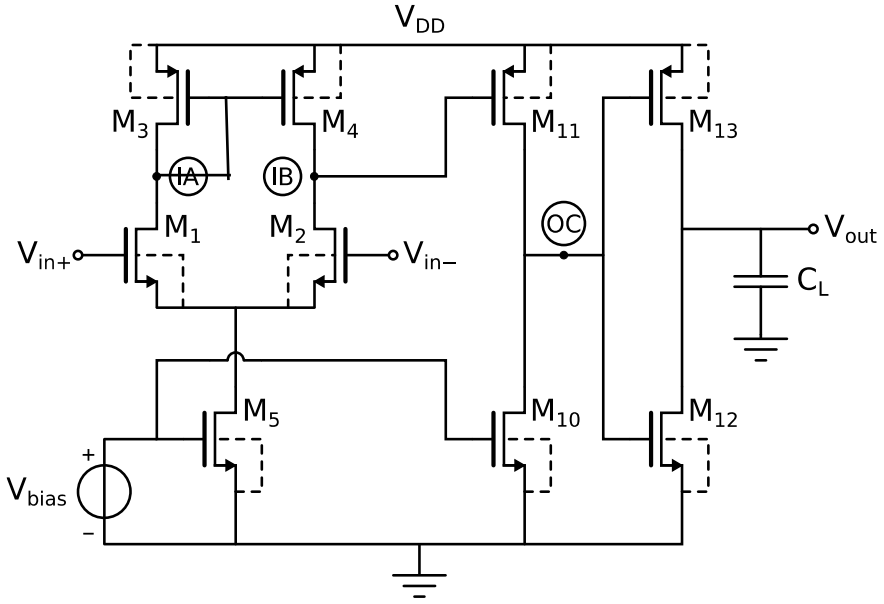
V_{in} = 100mV

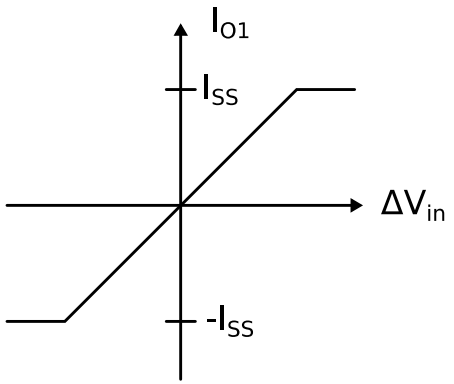


V_{in} = 10mV


COMP
Date/Time run: 01/04/80 21:32:39
Temperature: 27.0
5.5V
4.0V
2.0V
0.0V
-0.5V
0ns
40ns
80ns
120ns
160ns
200ns
V(OUT)
V(OC)
V(IB)

Speed of the comparator





- With large input signal the speed is limited by slewing behaviour, i.e. slewing current I_{SS}.

$$\frac{dV_{1B}}{dt} = \frac{I_{SS}}{C_{1B}}$$

- With small input signal the speed is limited by small signal behaviour, i.e. transconductance of the input transistors.
- With small input signal the charging of input stage load capacitor is slow, because of small available current $I_{out} = g_m * \Delta v_{in}$

$$\frac{dV_{1B}}{dt} = \frac{g_{m1}\Delta V_{in}}{C_{1B}}$$

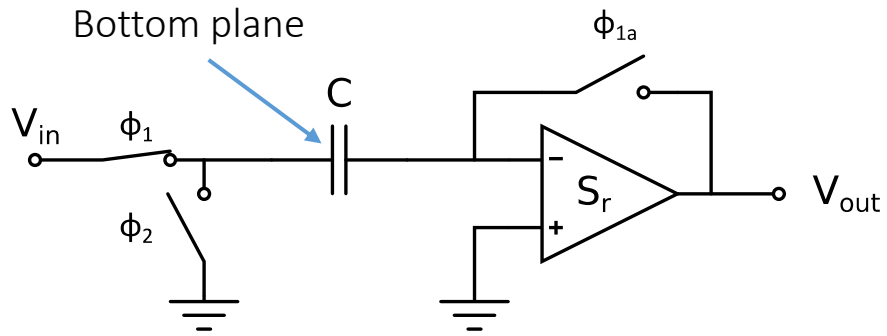
E.g. With 1mV input and transconductance of 1mS the output current is only 1µA, so a load capacitor of 1pF to be charged up to 1V, will take 1µs,

with 100µV input 10µs and

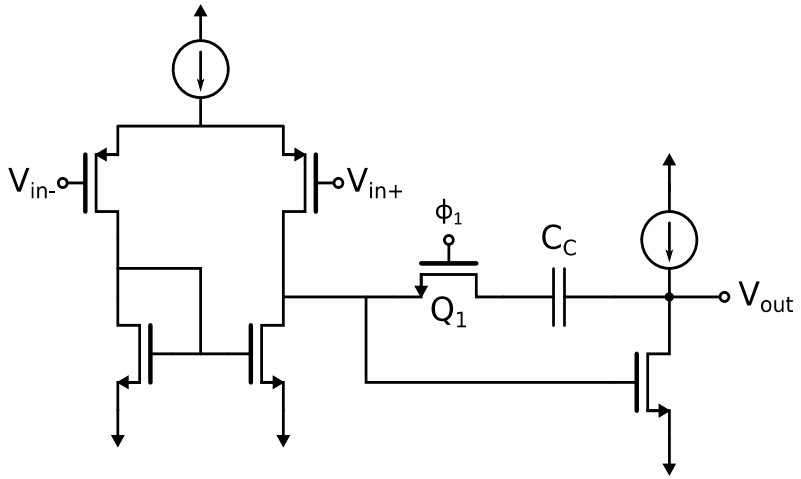
with 10µV input 100µs.

Autozeroing comparator

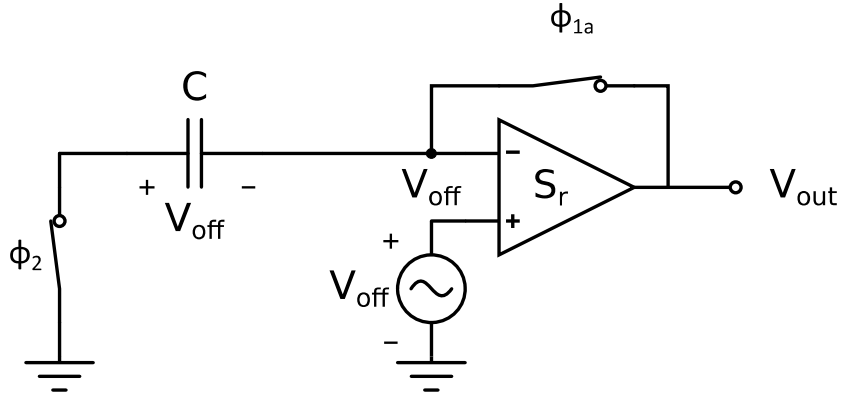
For higher resolution offset is compensated for by using autozeroing:



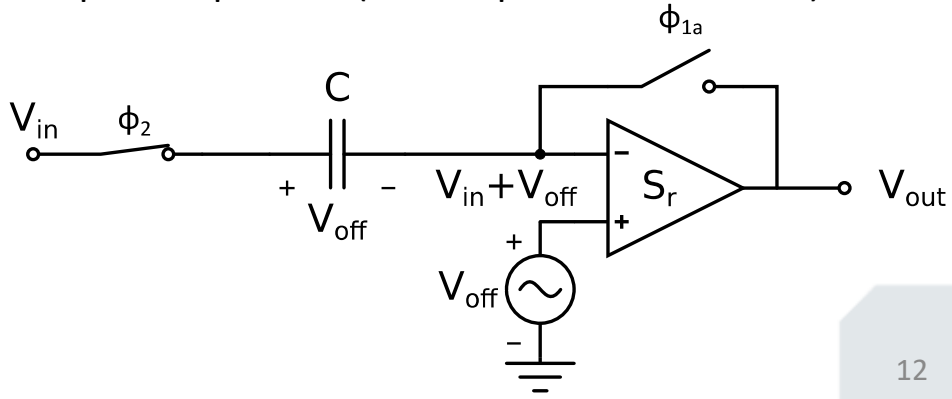
Amplifier is connected to unity-gain feedback mode to sample the offset by capacitor C
=> frequency compensation is needed



During ϕ_1: offset sampled to C, amplifier connected to unity-gain feedback mode

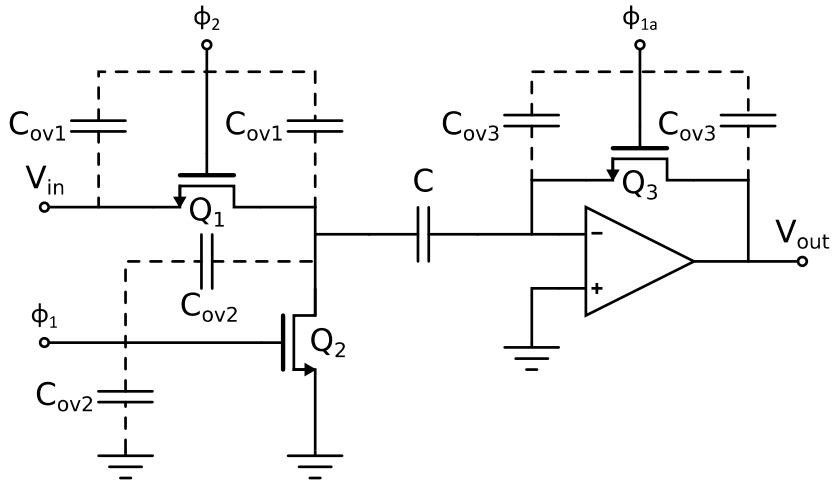


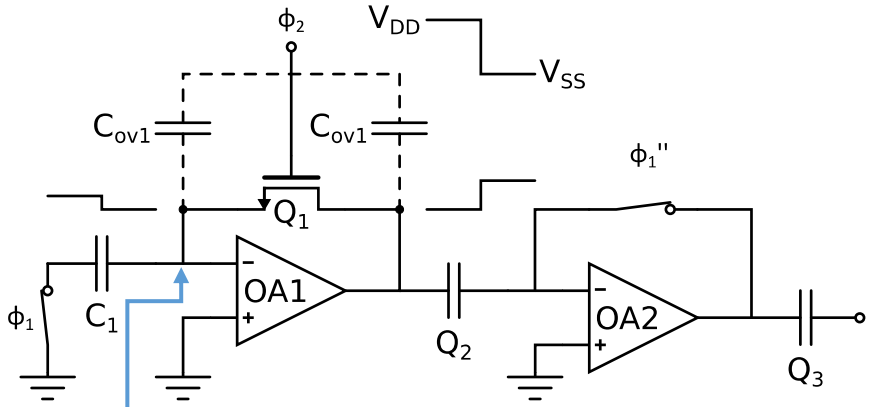
During ϕ_2: comparison of input, amplifier connected to open-loop mode (no compensation needed)



Autozeroing comparator

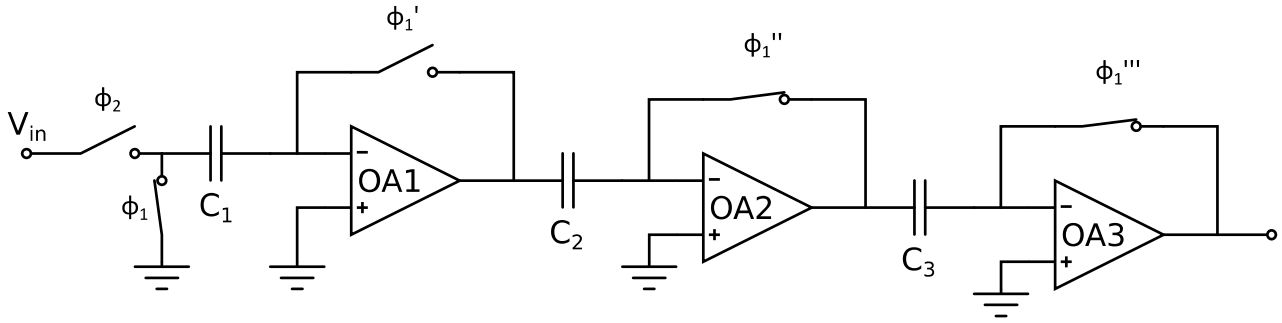
Charge injection in autozeroing comparator

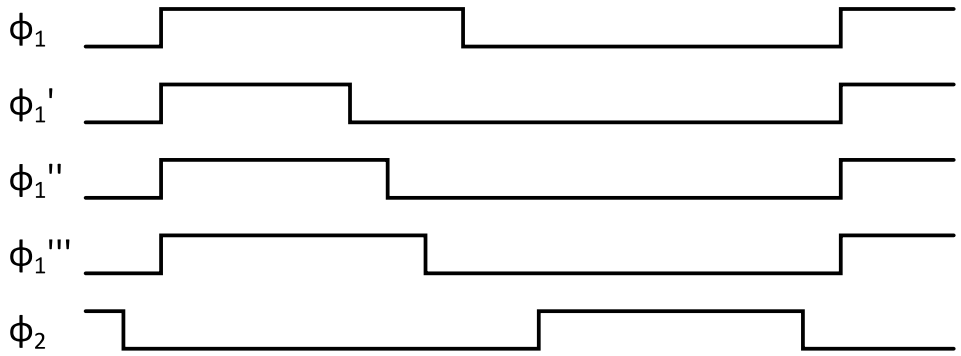




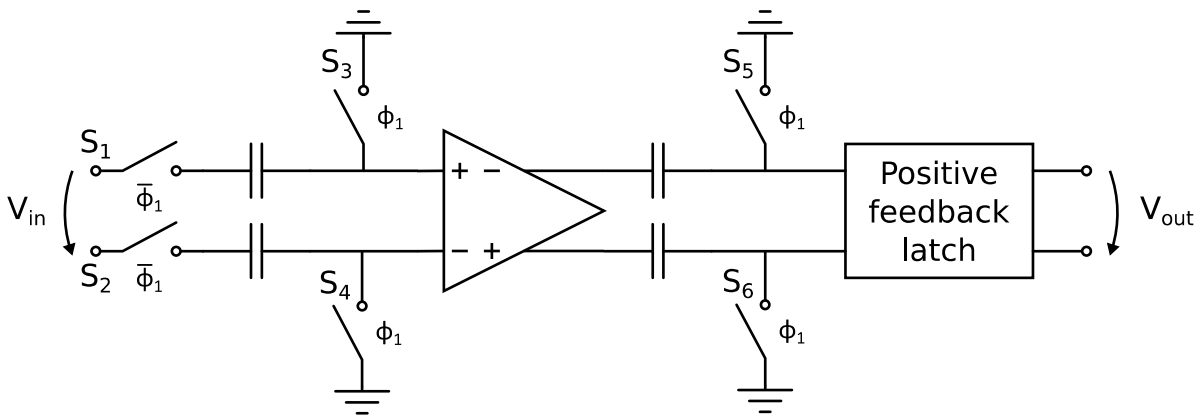
Negative charge injection

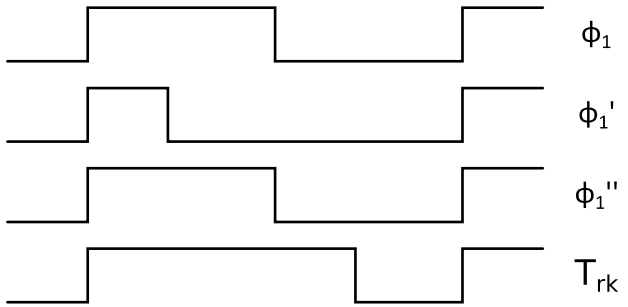
Charge injection elimination

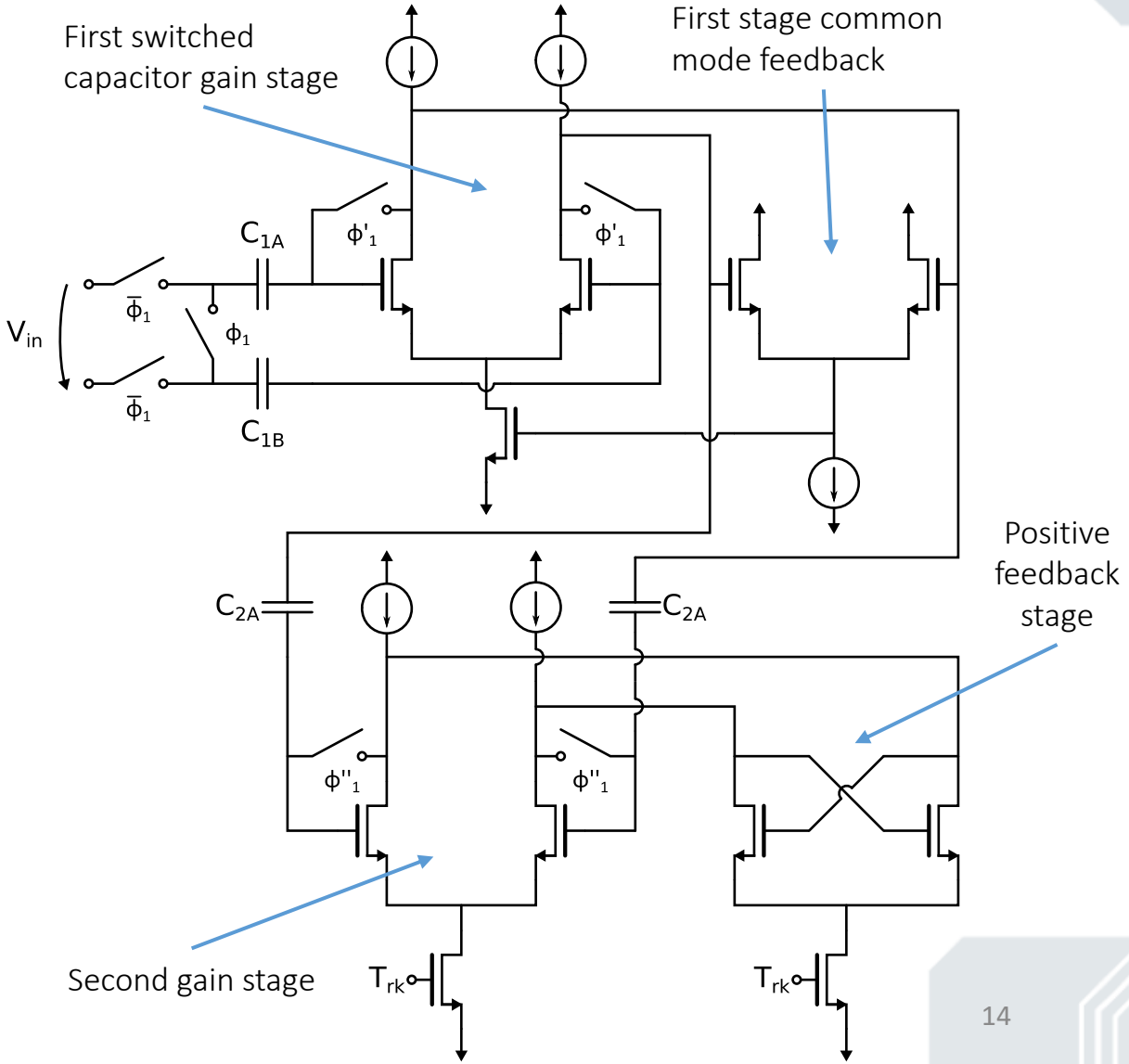




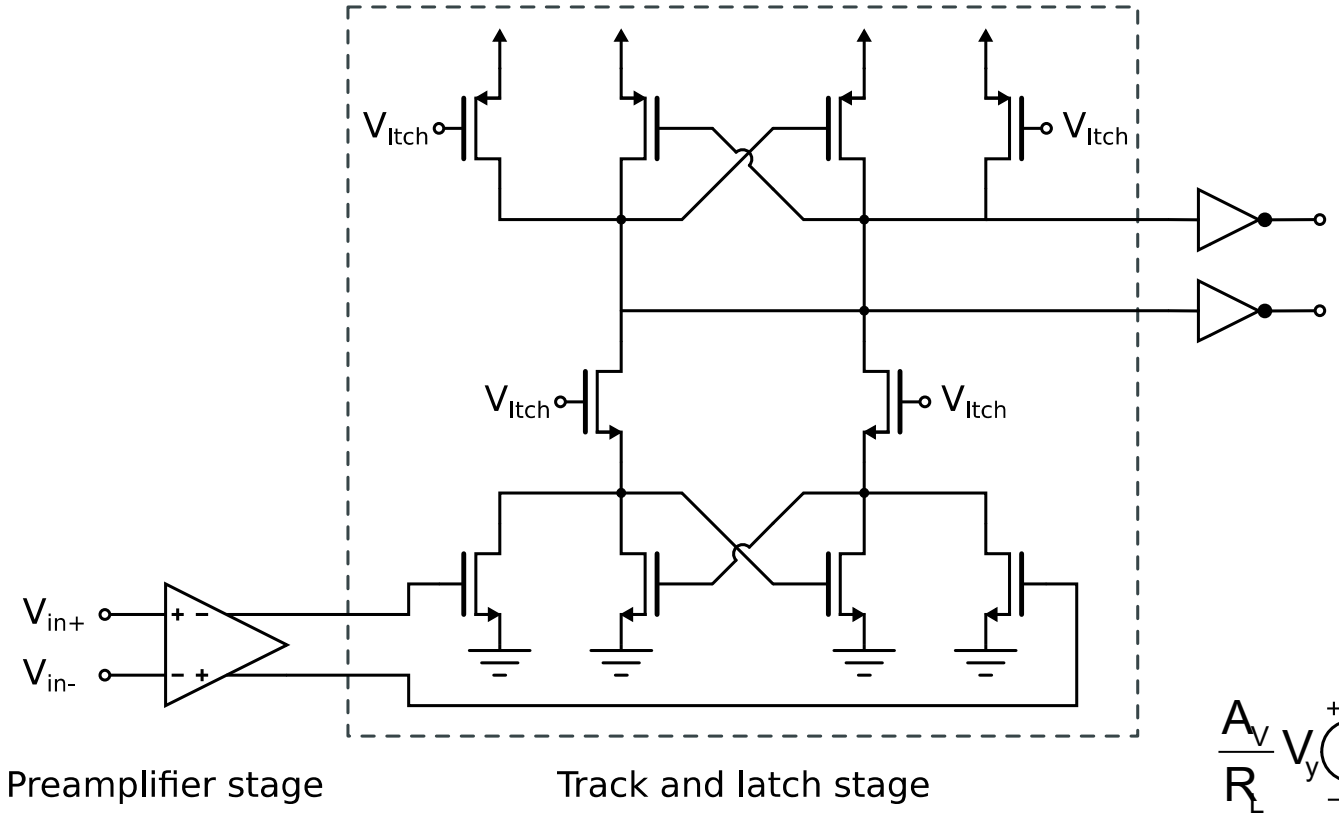
Autozeroed fully differential comparator with a positive feedback latch







Positive feedback latch



$$\tau_{ltch} = \frac{C_L}{g_m}; \qquad g_m = \frac{A_V}{R_L}$$

$$C_L = K_1 W L C_{OX}$$

$$g_m = K_2 \mu_n C_{OX} \frac{W}{L}(V_{GS} - V_{TH})$$

$$\Rightarrow \tau_{ltch} = \frac{K_1}{K_2} \frac{L^2}{\mu_n (V_{GS} - V_{TH})}$$