CIC Decimators and Interpolators

- An elegant application of multirate digital signal processing is in the design of the oversampling A/D converter
- In this type of converter, the analog signal is sampled at a rate much higher than the Nyquist rate, resulting in very closely sampled samples

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CIC Decimators and Interpolators

- As a consequence, the difference between the amplitudes of two consecutive samples is very small, permitting it to be represented in digital form using very few bits, usually one bit
- The sampling rate is then decreased by passing the digital signal through a factor-of-M decimator to lower the sampling rate from MF_T to F_T

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CIC Decimators and Interpolators

- The decimator is designed by cascading an anti-aliasing lowpass M-th band digital filter to reduce the bandwidth of the input digital signal to π/M with a factor-of-M down-sampler
- The simplest lowpass FIR filter that can be employed is the box-car filter (also called a running-sum filter) with a transfer function

$$H(z) = 1 + z^{-1} + z^{-1} + \ldots + z^{-(M-1)}$$

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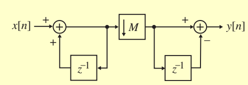
CIC Decimators and Interpolators

- A more convenient form of the box-car filter transfer function is given by

$$H(z) = \frac{1 - z^{-M}}{1 - z^{-1}}$$

- A multiplier-less realization of the factor-of-M decimator is shown below



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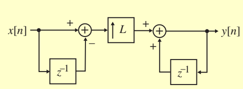
CIC Decimators and Interpolators

- The recursive running-sum filter can also be employed to design a computationally efficient interpolator
- A multiplier-less factor-of-L interpolator designed using a running-sum filter is shown below



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CIC Decimator

- Since the decimator based on a running-sum filter does not provide sufficient out-of-band attenuation, often a multistage decimator formed by a cascade of running-sum decimators, more commonly known as cascaded integrator comb (CIC) filters, is used in practice

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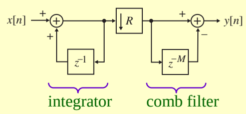
CIC Decimator

- The structure of a two-stage CIC decimator is shown below



- It can be seen that the first stage is an integrator and the last stage is a comb filter with a factor-of-R down-sampler in the middle

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CIC Decimator

- The structure shown is equivalent to a factor-of-R decimator with a length-RM running-sum decimation filter
- Further flexibility in the design of a CIC decimator is obtained by including K integrator sections before the K comb filters after the down-sampler as shown in the bext slide

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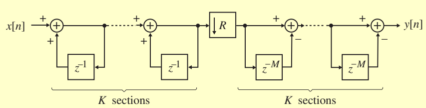
CIC Decimator



- The transfer function of the decimation filter is thus given by

$$H(z) = \left(\frac{1 - z^{-RM}}{1 - z^{-1}} \right)^{K}$$

- The parameters M and K can be adjusted for a given down-sampling factor R to yield the desired out-of-band attenuation

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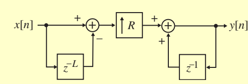
CIC Interpolator

- A two-stage CIC interpolator is obtained by interchanging the positions of the integrator and the comb filter of the two-stage CIC decimator and replacing the down-sampler with an up-sampler as shown below



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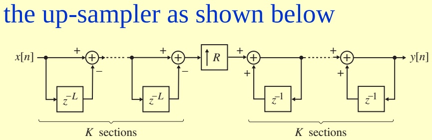
CIC Interpolator

- Additional flexibility in the design of a CIC interpolator is obtained by including K comb filters before and K integrators after the up-sampler as shown below



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FIR Decimation and Interpolation Filters

- The CIC decimators and interpolators are multiplier-less structures and thus computationally efficient in addition being easy to implement
- However, the wordlength of the adder in each integrator grows rapidly in the multistage implementation

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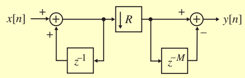
FIR Decimation and Interpolation Filters

- This problem can be avoided by realizing the running-sum filter in each stage as an FIR filter
- Consider the two-stage decimator shown below for $M = 1$



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FIR Decimation and Interpolation Filters

- The transfer function of the decimation filter is now given by

$$H(z) = \frac{1-z^{-R}}{1-z^{-1}} = 1 + z^{-1} + z^{-2} \ldots + z^{-(R-1)}$$

- If R is a power-of-2 integer, say $R = 2^J$, $H(z)$ can be rewritten in a factored form

$$H(z) = (1+z^{-1})(1+z^{-2})(1+z^{-4})\cdots(1+z^{-2^{J-1}})$$

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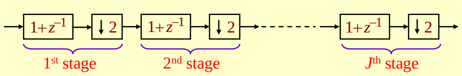
FIR Decimation and Interpolation Filters

- The above decomposition then leads to the cascaded structure shown below with a simple first-order FIR filter in each stage



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FIR Decimation and Interpolation Filters

- In the general case, when $M \neq 1$, each first-order FIR filter with a transfer function $1+z^{-1}$ is replaced with an M-th order FIR filter with a transfer function $(1+z^{-1})^M$
- The integer-valued coefficients of the decimation filter transfer functions can be expressed in the form $2^r \pm 1$, leading to an implementation of the multiplication operation using only shift-and-add operations

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FIR Decimation and Interpolation Filters

Example – We illustrate the implementation for $M = 5$

- The transfer function of the FIR decimation filter in each stage is then given by

$$H(z) = (1+z^{-1})^5$$
$$= 1 + 5z^{-1} + 10z^{-2} + 10z^{-3} + 5z^{-4} + z^{-5}$$
$$= \underbrace{(1+10z^{-2}+5z^{-4})}_{E_0(z^2)} + z^{-1}\underbrace{(5+10z^{-2}+z^{-4})}_{E_1(z^2)}$$

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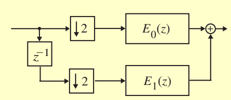
FIR Decimation and Interpolation Filters

- Thus $H(z) = E_0(z^2) + z^{-1}E_1(z^2)$
- A schematic representation of a single-stage factor-of-2 decimator based on the above polyphase decomposition is indicated below



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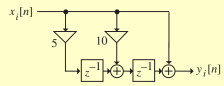
FIR Decimation and Interpolation Filters

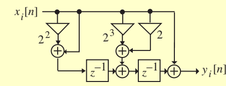
- A realization of $E_0(z)$ based on the second direct form FIR structure is shown below



- Now the multiplier coefficient of value 5 can be expressed as $4+1=2^2+1$ and the multiplier coefficient of value 10 can be expressed as $8+2=2^3+2$

FIR Decimation and Interpolation Filters

- Hence a multiplier-less realization of $E_0(z)$ is thus as shown below



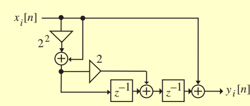
- The above realization requires 3 shift operations and 2 additions in addition to the 2 original adders

FIR Decimation and Interpolation Filters

- Further reductions in the number of shift and add operations is obtained by substructure sharing technique
- To this end, we observe that the shift-and-add operations 2^3+2 can be written as $2^3+2=2(2^2+1)$

FIR Decimation and Interpolation Filters

- The shift-and-add operations 2^2+1 in the expression $2(2^2+1)$ can be shared with the same at the input to the delay chain resulting in the final structure shown below



- The above realization requires 2 shift operations and 3 additions