Users Manual

RESISTIVITY OF SEMICONDUCTORS BY FOUR PROBE METHOD AT DIFFERENT TEMPERATURES

MOODY
INTERNATIONAL

UKAS
QUALITY
MANAGEMENT
014

ENERGY

← r

r_1 O r_1

r →

WORK REQUIRED TO FREE
OUTER SHELL ELECTRON
$E_\infty \sim 10\,eV$

AN UNFILLED SHELL

OUTER SHELL POSITION

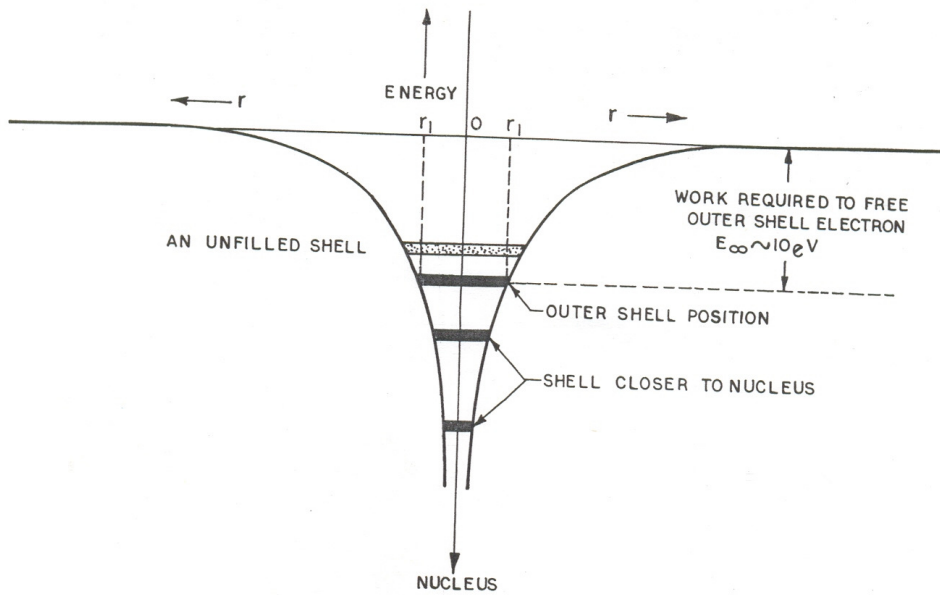SHELL CLOSER TO NUCLEUS

NUCLEUS
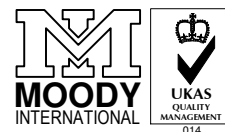
FIG. 1   POTENTIAL DISTRIBUTION AROUND AN INDIVIDUAL
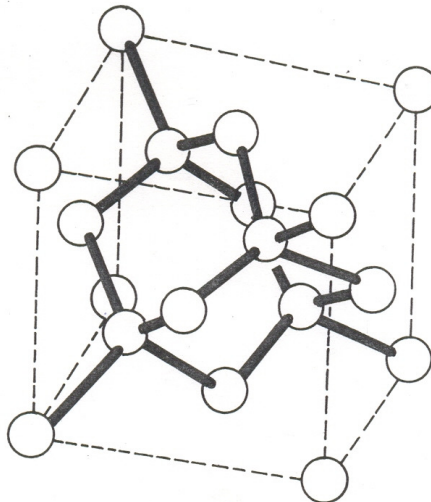ATOM

FIG. 2   STRUCTURE OF THE DIAMOND
LATTICE

INTRODUCTION

The properties of the bulk material used for the fabrication of transistors and other semiconductor devices are essential in determining the characteristics of the completed devices. Resistivity and lifetime (of minority carriers) measurements are generally made on germanium crystals to determine their suitability. The resistivity, in particular, must be measured accurately since its value is critical in many devices. The value of some transistor parameters, like the equivalent base resistance, are at least linearly related to the resistivity.

ELECTRONIC CONDUCTION IN SOLIDS

The electrical properties of semiconductors involve the motion of charged particles within them. Therefore, we must have an understanding of the forces which control the motion of these particles. It is of course, the physical structure of the solid which exerts their control. This topic is very large, and hence <u>only the high lights will be covered</u>. The reader is referred to many excellent sources which are listed at the end, for more details on specific aspects.

Atoms, of which a solid is composed, consist of positively charged nuclei with electron orbiting around them. The positive charge is compensated by negatively charged electrons, so that a complete atom is electrically neutral. Electrons are arranged in shells, and the closer they are to the nucleus the more strongly they are bound. If we take the particular case of silicon, a well known semiconductor, we find that it has 14 electrons which are accommodated in the shells as $(1S)^2$, $(2S)^2$, $(2P)^6$, $(3S)^2$, $(3P)^2$. Since the third shell is not even half filled, the 4 electrons are available for chemical binding giving silicon a valency of four. (Germanium also has a chemical valency of 4, but from the fourth shell). Fig. 1 shows an energy diagram of an individual atom.

Let us now concentrate our attention on solids, if we bring many atoms close to one another, interatomic forces become quite strong as electronic orbits begin to overlap. The outer shell electrons play an important role, because their orbits are the most disturbed. These electrons are no longer associated with a particular atom, the outer shell electron may make an orbit around one atom and continue about another. In this fashion, the outer shell or <u>valency electrons are continually traded among atoms and wander all over the solid</u>. <u>The continuous interchange of valence electrons between atoms holds the solid</u> <u>together</u>. This is the predominant type of bonding in silicon and germanium, and is called the valence bonding.
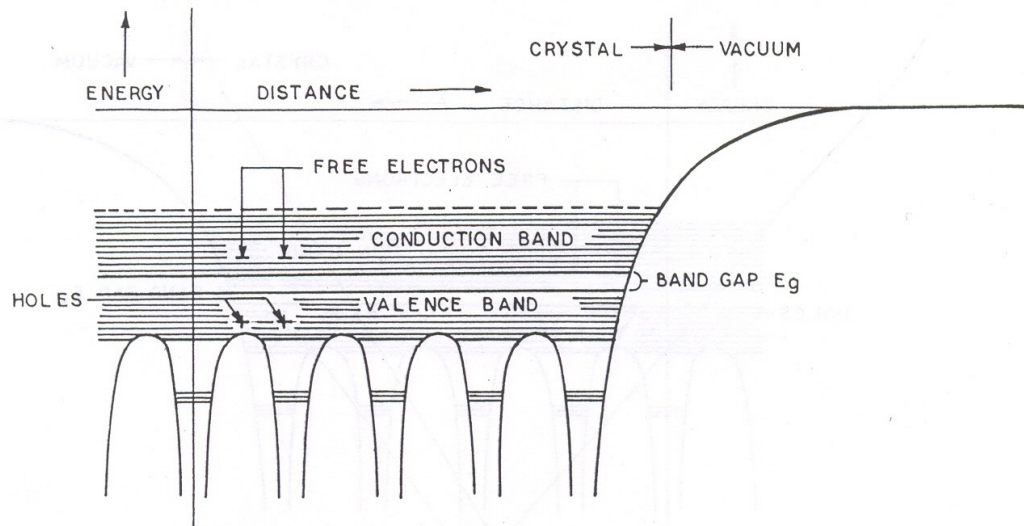
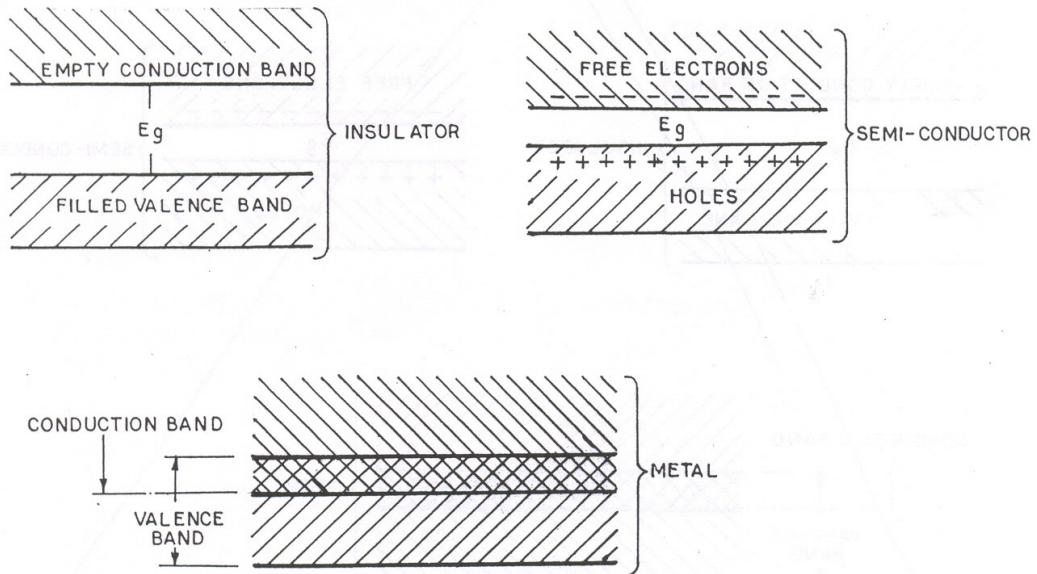FIG. 3   UNUSED SHELLS FORM THE CONDUCTION
BAND

FIG. 4   BAND STRUCTURES FOR INSULATORS, SEMICONDUCTOR
AND METALS

In solids, atoms are usually arranged in a regular way to achieve a dense packing and thereby form a crystal. The arrangement has very desirable characteristics, i.e. the transport of holes and free electrons is very smooth in these structures. When the arrangement is not crystalline complication arise. Here we will be concerned only with the properties of perfect crystals. Silicon and germanium (and carbon) crystallize with an identical crystal structure, the called diamond structure. Such a structure is shown in fig.

2 The arrangement of atoms in the illustration form a <u>Unit Cell</u>, and the crystal is made up of adjacent unit cells.

Fig. 3 shows a potential diagram of an array of atoms. An actual crystal is of course there dimensional. The most important difference between the potential plot of an isolated atom and one dimensional array is the splitting of energy levels. In fact, bringing N atoms together we find 'N' times as many levels throughout the crystal. The spreading of energy level depends on the degree of interaction, therefore, the inner orbits split into levels combined in a narrow energy than the outer ones.

As a result of the interaction between the tremendous number of atoms in crystal (10^{22} per cm^3), the energy level found in isolated atoms will be split and form bands of allowed energies which contain almost continuum of levels. Accordingly, electrons are located in energy bands in crystalline solid. The band which contains the valence electrons is called the <u>valence band</u>. The unoccupied energy levels also split up and form another band called the <u>conduction band</u>. The interaction between the unused shells is very large and they spread widely. Therefore, while there is a bandgap, E_g (or forbidden region) between the valence and conduction bands, splitting of higher orbit is so wide that they usually overlap.

The bands below the energy gap E_g are completely filled at absolute zero temperature and the conduction band is empty. This is a very important point and has direct consequences on the conduction properties, as we shall see soon. The fundamental theory is that <u>current conduction is not possible in empty and filled bands</u>. The reasons about the empty band is obvious since current is not possible without carriers. The reason about the filled band is as follows : though the valence electrons move about the crystal but they <u>can not be accelerated</u> because the acceleration means gain of energy and there are no higher energy levels available to which they could rise.

We can now readily see that the crystal band structure shown in Fig. 3 does not allow current conduction at T=0. <u>If we increase the temperature, however, thermal agitation increases and some valence electron will gain energy greater than E_g and jump into the conduction band</u>. <u>The electron in the conduction band is called a free electron, and its former place in the valence band is called a hole</u>. Electrons in

conduction band can gain energy when a field is applied, because there are many higher energy states available. The fact that electrons left the valence band leaves some empty energy levels, this allows conduction in the valence band as well. Electrons can now gain energy in the valence band also, and we observe a motion of holes in the direction of the field. Because of this we begin to speak of a <u>hole as a current carrying particles</u>.

According to the proceeding theory, an insulator must have a large bandgap, so that at room temperature the conduction band is practically empty and the valence band is practically filled and a semiconductors must have a narrower band gaps so that appreciable number of carriers are present in the valence and conduction bands at room temperature.

<u>In metals</u>, however, the valence and conduction bands overlap and application of an electric field can, therefore, accelerate a great sea of electrons. The non-existance of a bandgap make conduction in metal almost independent of temperature, as compared to semiconductors. Fig. 4 summarizes the above points.

The fact that electrons can be found in energy bands within a crystal and other conclusions mentioned so far can be shown by quantum mechanical calculations also which we shall not carry out here, but will use the results for quantitative analysis.

CONCENTRATION OF INTRINSIC CARRIERS

The concentration of intrinsic carriers i.e. the number of electrons in conduction band per unit volume is given by the expression :*

$$n = 2 \left(\frac{m_e \, k \, T}{2p \, h^2} \right)^{\frac{3}{2}} \exp{(\mu - E_g)} / kT \qquad (1)$$

and the concentration of holes in valence band is given by the expressions*

$$p = 2 \left(\frac{m_h \, k \, T}{2p \, h^2} \right)^{\frac{3}{2}} \exp{(- \mu / kT)} \qquad (2)$$

If we multiply together the expression for n and p to obtain equilibrium relation :

$$np = 4 \left(\frac{kT}{2p \, h^2} \right)^{3} (m_e \, m_h)^{3/2} \exp{(-E_g / kT)} \qquad (3)$$

This does not involve the Fermi level μ and is known as the expression of law of mass action.

Where m_e = Effective mass of an electron

                      m_h = Effective mass of a hole

                  k = Boltzamann's constant, μ = Fermi level

                  E_g = Bandgap, T = Temperature in K

In case of intrinsic (highly purified) crystals, the number of electrons is equal to the number of holes, because the thermal excitation of an electron leave behind a hole in the valence band. Thus, from(3) we have, letting the subscript i denote intrinsic

$$n_i = p_i = 2 \left(\frac{kT}{2p\, \hbar^2} \right)^{\frac{3}{2}} (m_e\, m_h)^{3/4} \exp(-E_g/2kT) \tag{4}$$

Thus, we see that the concentration of intrinsic carrier depend exponentially on $E_g/2kT$.

CONDUCTIVITY OF INTRINSIC SEMICONDUCTOR

The electrical conductivity will be the sum of the contributions of both electrons and holes :

$$\sigma = (n_i\, e\, \mu_e + p_i\, e\, \mu_h) \tag{5}$$

Where e is the electron charge. μ_e and μ_h are the average velocities acquired by the electrons and holes in a unit electric field and <u>known as mobilities</u>.

or $\sigma = e\, n_i\, (\mu_n + \mu_h)$ Since $n_i = p_i$

$$= (K)\, T^{3/2}\, (\mu_n + \mu_p).\ \exp \frac{-E_g}{2kT} \tag{6}$$

using Eq. 4 where K is a constant.

The factor $T^{3/2}$ and the mobilities change relatively slow with temperature compared with the exponential term, and hence the logarithm of resistivity ρ (=$1/\sigma$) varies linearly with 1/T. The width of the energy gap may be determined from the slope of the curve

Thus we have,

$$\text{Log}_e\, \rho = \frac{E_g}{2kT}\ -\ \log_e K \tag{7}$$

EXPERIMENTAL CONSIDERATIONS

1. High resistance or rectification appears fairly often in electrical contacts to semiconductors and in fact is one of the major problem.

2. In single crystal material the resistivity may vary smoothly from point to point. In fact this is generally the case. The question is the amount of this variation rather than any question of its presence. Often, however, it is conventionally stated that the resistivity is constant within some percentage and when the variation does in fact fall within this tolerance, it is ignored.

3. Soldered probe contacts may disturb the current flow shorting out part of the sample and add to the ambiguity in the measurement of the probe spacing. Soldering directly to the body of the sample can affect the sample properties by heating effect and by contamination unless care is taken. These problems can be avoided by using pressure contacts. The principal draw backs of this kind of contacts are that they may be noisy.

4. The current through the sample should not be large enough to cause heating. A further precaution is necessary to prevent 'injecting effect' from affecting the measured value of ρ Even good contacts, to germanium, for example, may inject. This is minimized by keeping the voltage drop at the contacts low. If the surface near the current contacts is rough (lapped surface) and the electric flow in the crystal is low, these injected carriers will recombine before reaching the measuring probes.

    Since ρ is independent of current, it is possible to determine whether or not any of these effects are interfering with the measuring of ρ at several values of I. It should be kept in mind that these points of experimental technique affect essentially all the measurements and not the resistivity measurements only.

FOUR PROBE METHOD

Many conventional methods for measuring resistivity are unsatisfactory for semiconductors because metal-semiconductor contacts are usually rectifying in nature. Also there is generally minority carrier injection by one of the current carrying contacts.
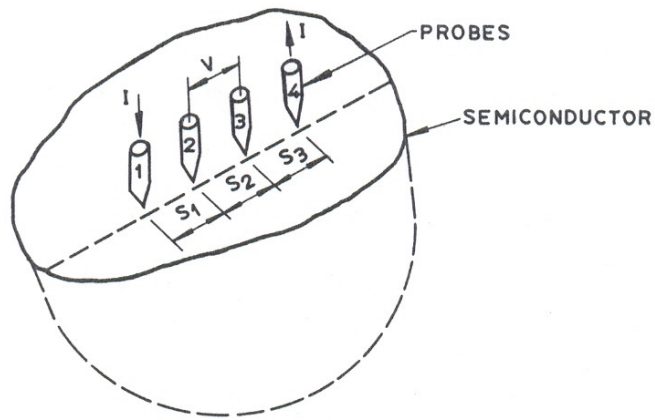
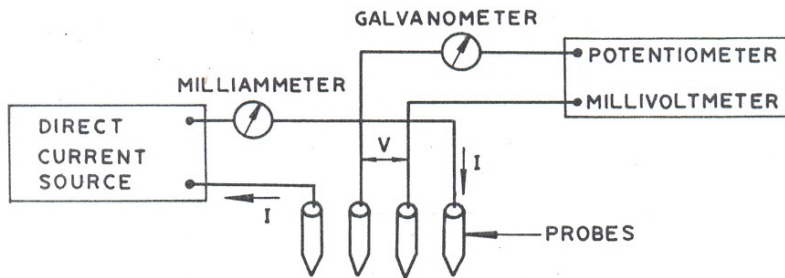FIG. 5 MODEL FOR THE FOUR PROBE RESISTIVITY
        MEASUREMENTS

FIG. 6 CIRCUIT USED FOR RESISTIVITY MEASUREMENTS

An excess concentration of minority carriers will affect the potential of other contacts and modulate the resistance of the material.

The method described here overcomes the difficulties mentioned above and also offers several other advantages. It permits measurements of resistivity in samples having a wide variety of shapes, including the resistivity of small volumes within bigger pieces of semiconductor. In this manner the resistivity of both sides of p-n junction can be determined with good accuracy before the material is cut into bars for making devices. This method of measurement is also applicable to silicon and other semiconductor materials.

The basic model for all these measurements is indicated in Fig. 5. Four sharp probes are placed on a flat surface of the material to be measured, current is passed through the two outer electrodes, and the floating potential is measured across the inner pair. If the flat surface on which the probes rest is adequately large and the crystal is big the semiconductor may be considered to be a semi-infinite volume. To prevent minority carrier injection and make good contacts, the surface on which the probes rest, maybe mechanically lapped.

The experimental circuit used for measurement is illustrated schematically in Fig. 6. A nominal value of probe spacing which has been found satisfactory is an equal distance of 2.0 mm between adjacent probes. This permit measurement with reasonable current of n-type or p-type semiconductor from 0.001 to 50 ohm. cm.

In order to use this four probe method in semiconductor crystals or slides it is necessary to assume that :

1.   The resistivity of the material is uniform in the area of measurement.

2.   If there is minority carrier injection into the semiconductor by the current - carrying electrodes most of the carriers recombine near the electrodes so that their effect on the conductivity is negligible. (This means that the measurements should be made on surface which have a high recombination rate, such as mechanical lapped surfaces).

3.   The surface on which the probes rest is flat with no surface leakage.

4.   The four probes used for resistivity measurements contact the surface at points that lie in a straight line.

5.   The diameter of the contact between the metallic probes and the semiconductor should be small compared to the distance between probes.

6. The boundary between the current-carrying electrodes and the bulk material is hemispherical and small in diameter.

7. The surfaces of the semiconductor crystal may be either conducting or non-conducting.

   (a) A conducting boundary is one on which a material of much lower resistivity than semiconductor (such as copper) has been plated.

   (b) A non-conducting boundary is produced when the surface of the crystal is in contact with an insulator.

CASE 1 - RESISTIVITY MEASUREMENTS ON A LARGE SAMPLE

One added boundary condition is required to treat this case namely, that the probes are far from any of the other surfaces of the sample and the sample can thus be considered a semi-infinite volume of uniform resistivity material. Fig. 5 shows the geometry of this case. Four probes are spaced S_1, S_2 and S_3 apart. Current I is passed through the outer probes (1 and 4) and the floating potential V is measured across the inner pair of probes 2 and 3.

The floating potential V_f a distance r from an electrode carrying a current I in a material of resistivity ρ_0 is given by

$$V_f = \frac{\rho_0\, I}{2\pi\, r}$$

In the model shown in Fig. 5 there are two current-carrying electrodes, numbered 1 and 4, and the floating potential V_f, at any Y point in the semiconductor is the difference between the potential induced by each of the electrodes, since they carry currents of equal magnitude but in opposite directions Thus :

$$V_f = \frac{\rho_0\, I}{2\pi} \left(\frac{1}{r_1} - \frac{1}{r_4} \right) \tag{9}$$

Where r_1 = distance from probe number 1.

r_4 = distance from probe number 4.

The floating potentials at probe 2, V_{f2}, and at probe 3, V_{f3} can be calculated from (9) by substituting the proper distances as follows :
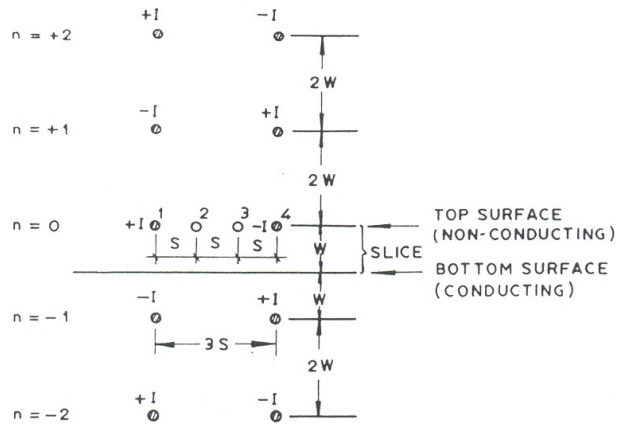
FIG.7 IMAGES FOR THE CASE OF THE RESISTIVITY PROBES
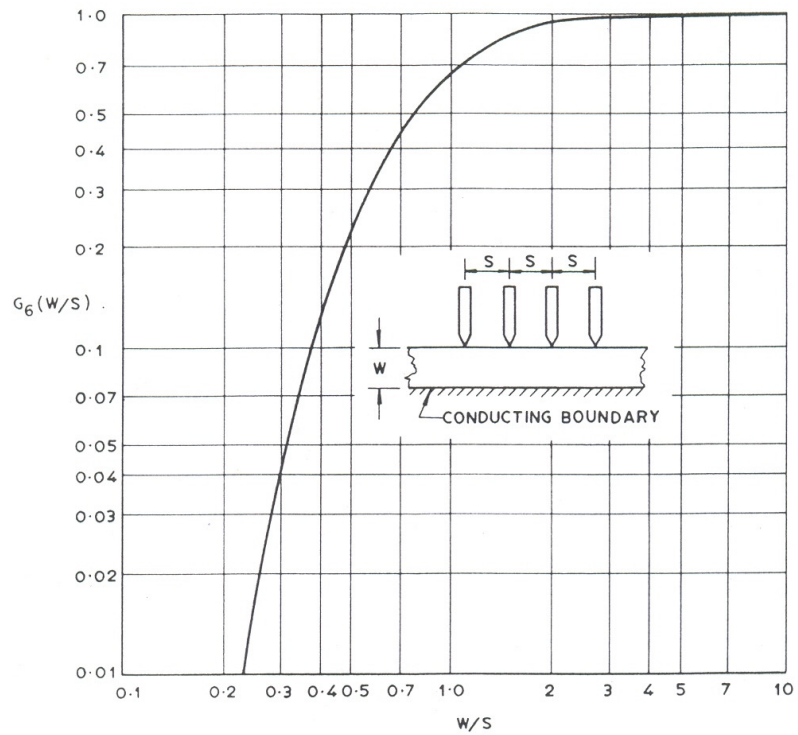ON A THIN SLICE WITH A CONDUCTING BOTTOM
SURFACE

FIG. 8 CORRECTION DIVISOR FOR PROBES ON A SLICE
WITH A CONDUCTING BOTTOM SURFACE

$$V_{f2} = \frac{\rho_0 I}{2\pi}\left(\frac{1}{S_1} - \frac{1}{S_2 + S_3}\right)$$

$$V_{f3} = \frac{\rho_0 I}{2\pi}\left(\frac{1}{S_1 + S_2} - \frac{1}{S_3}\right)$$

The potential difference V between probes 2 and 3 is then

$$V = V_{f2} - V_{f3} = \frac{r_{0i}}{2p}\left(\frac{1}{S_1} + \frac{1}{S_3} - \frac{1}{S_2 + S_3} - \frac{1}{S_1 + S_2}\right)$$

and the resistivity ρ_0 is computable as

$$r_0 = \frac{V}{I} - \frac{2p}{\left(\dfrac{1}{S_1} + \dfrac{1}{S_3} - \dfrac{1}{S_1 + S_2} - \dfrac{1}{S_2 + S_3}\right)} \tag{10}$$

When the point spacing equal, that is, $S_1 = S_2 = S_3 = S$ the above simplifies to :

$$\rho_0 = \frac{V}{I} \times 2\pi S \tag{11}$$

CASE 2- RESISTIVITY MEASUREMENTS ON A THIN SLICE-CONDUCTING BOTTOM SURFACE.

Two boundary conditions must be met in this case; the top surface of the slice must be a reflecting (non-conducting) surface and the bottom surface must be an absorbing (conducting) surface. Since the two boundaries are parallel, a solution by the method of images required for each current source an infinite series of images along a line normal to the places and passing through the current source.

The model for this case is shown in Fig. 7. The side surface of the slice are assumed to be far from the area of measurement and, therefore, only the effect of the bottom surface needs to be considered. In this analysis equal probe spacing S shall be assumed. The width of the slice is W. The array of images needed is indicated in Fig. 7. where the polarity and spacing of the first few images are as shown.

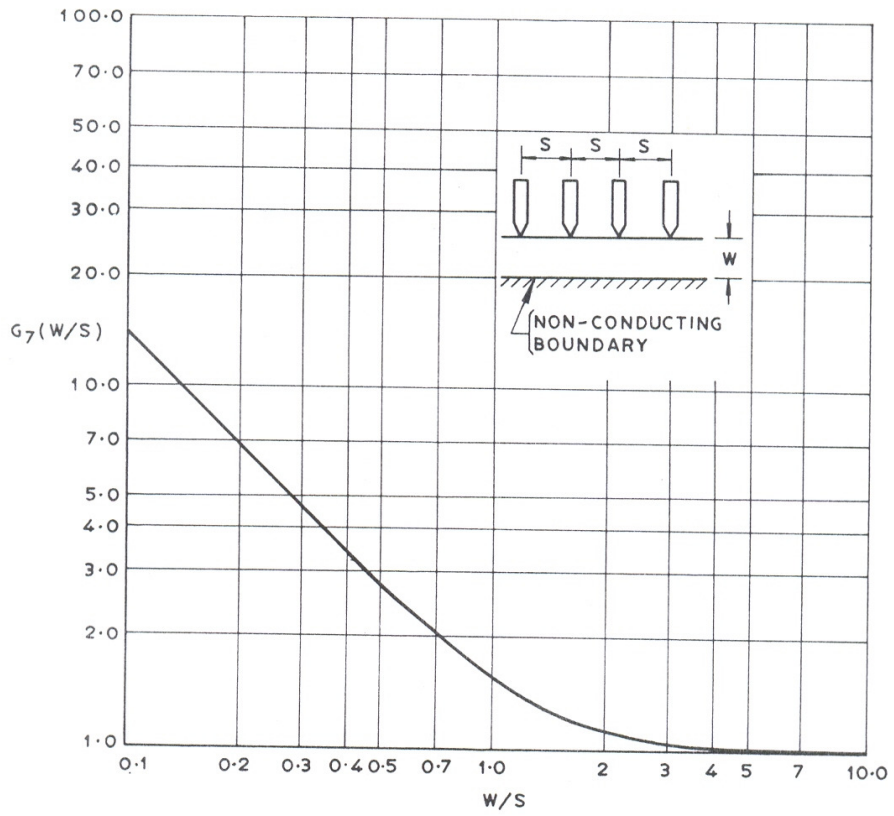The floating potential V_{f2} at electrodes 2 is

FIG.9 CORRECTION DIVISOR FOR PROBES ON A THIN
SLICE WITH A NONCONDUCTING BOTTOM SURFACE

$$V_{f2} = \frac{r\,I}{2p}\left[\sum_{n=-\infty}^{n=\infty}(-1)^n\frac{1}{\sqrt{S^2+(2nW)^2}} - \sum_{n=-\infty}^{n=\infty}(-1)^n\frac{1}{\sqrt{(2S)^2+(2nW)^2}}\right] \quad (12)$$

Likewise, the floating potential at electrode (3) can be obtained and

$$V = \frac{r\,I}{2p}\left[\frac{1}{S} + \sum_{n=1}^{n=\infty}(-1)^n\frac{4}{\sqrt{S^2+(2nW)^2}} - \sum_{n=1}^{n=\infty}(-1)^n\frac{4}{\sqrt{(2S)^2+(2nW)^2}}\right]$$

(13)

The resistivity then becomes

$$\rho = \frac{\rho_0}{G_6\,(W/S)}$$

(14)

Where resistivity ρ_0 is computable from (10, and 11) can be used if the point spacing are different, but approximately equal. The function $G_6\,(W/S)$ is computed from

$$G_6\left(\frac{W}{S}\right) = 1 + 4\frac{S}{W}\sum_{n=1}^{n=\infty}(-1)^n\left[\frac{1}{\sqrt{\left(\frac{S}{W}\right)^2+(2n)^2}} - \frac{1}{\sqrt{\left(2\frac{S}{W}\right)^2+(2n)^2}}\right]$$

(15)

which is tabulated in Table I and plotted in Fig. 8.

TABLE I

S. No.	W/S	G_6 (W/S)	G_7 (W/S)
1	0.100	0.0000019	13.863
2	0.141	0.00018	9.704
3	0.200	0.00342	6.931
4	0.33	0.0604	4.159
5	0.500	0.228	2.780
6	1.000	0.683	1.504
7	1.414	0.848	1.223
8	2.000	0.933	1.094
9	3.333	0.9838	1.0228
10	5.000	0.9948	1.0070
11	10.000	0.9993	1.00045
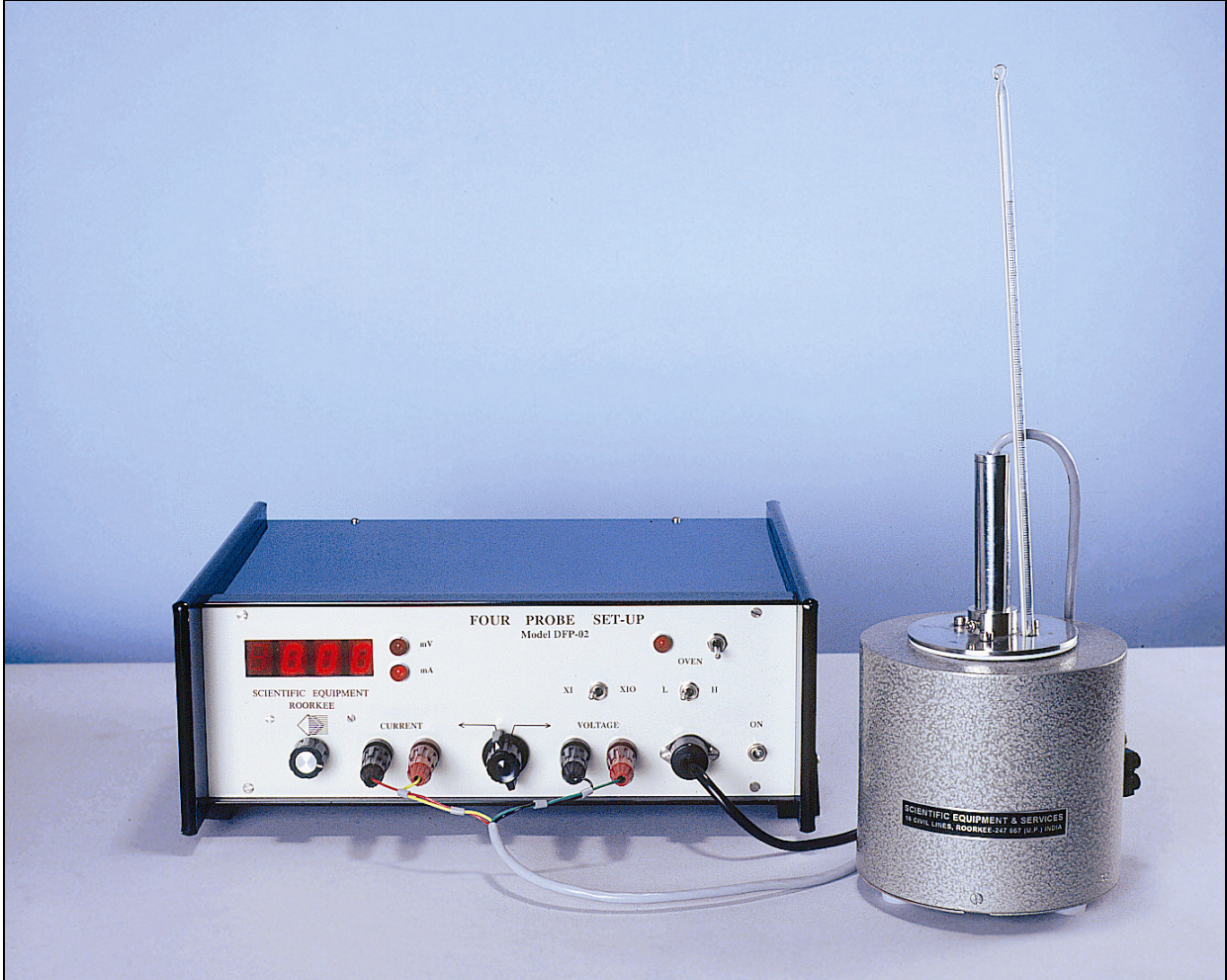
CASE 3 RESISTIVITY MEASUREMENTS ON A THIN SLICE-NON-CONDUCTING BOTTOM SURFACE.

The model for these measurements is like the case 2, except that the bottom surface of the slice is nonconducting. This means that all the images of Fig. 7 have the same charge as the current source. Thus all the images on a row have equal charges and Eq. 13 describes the potential difference across the inner pair of probes, if $(-1)^n$ is removed from the equation. Then,

$$\rho = \frac{\rho_0}{G_7(W/S)} \tag{16}$$

Where,

$$G_7(W/S) = 1 + 4\frac{S}{W}\sum_{n=1}^{n=\infty}\left[\frac{1}{\sqrt{\left(\frac{S}{W}\right)^2 + (n)^2}} - \frac{1}{\sqrt{\left(2\frac{S}{W}\right)^2 + (2n)^2}}\right] \tag{17}$$

This function $G_7(W/S)$ is tabulated in Table I. and plotted in Fig. 9. For smaller values of W/S the function $G_7(W/S)$ approaches the case for an infinitely thin slice, or

$$G_7\left(\frac{W}{S}\right) = \frac{2S}{W}\log_e 2 \tag{18}$$

BRIEF DESCRIPTION OF THE APPARATUS REQUIRED

1. **Probes Arrangement** : It has four individually spring loaded probes, coated with Zn at the tips. The probes are colinear and equally spaced. The Zn coating & individual spring ensure good electrical contacts with the sample. The probes are mounted in a teflon bush which ensure a good electrical insulation between the probe. A teflon spacer near the tips is also provided to keep the probes at equal distance. The whole arrangement is mounted on a suitable stand and leads are provided for current and voltage measurements.

2. **Sample** : Ge or Si crystal in the form of a chip/slice

3. **Oven** : It is a small oven for the variation of temperature of the crystal from room temperature to about 200 °C.

4. Four Probes Set-up : (Measuring Unit) - It has three subunits all enclosed in one cabinet.

(i) Multirange Digital Voltmeter

In this unit intersil 3½ digit single chip A/D converter ICL 7107 has been used. It has high accuracy, auto zero to less than 10 µV, zero drift-less than 1 µV/°C, input bias current of 10 pA and roll over error of less than one count. Since the use of internal reference causes the degradation in performance due to internal heating, an external reference has been used.

SPECIFICATION

Range : X 1 (0 - 200.0 mV) & X 10 (0 - 2.000 V)

Resolution : 100 µV *at* X 1 *range*

Accuracy : ± 0.1% *of reading* ± 1 *digit*

Impedance : 10 *M ohm*

Display : 3½ *digit, 7 segment, LED (12.5 mm height) with auto polarity and decimal indication.*

Overload Indicator : Sign of 1 *on the left and blanking of other digits.*

(ii) Constant Current Generator

It is a IC regulated current generator to provide a constant current to the outer probes irrespective of the changing resistance of the sample due to change in temperatures.

The basic scheme is to use the feedback principle to limit the load current of the supply to preset maximum value. Variations in the current are achieved by a potentiometer included for that purpose. The supply is a highly regulated and practically ripple free d.c. source. The current is measured by the digital panel meter.

SPECIFICATION

Open circuit voltage : 18 V

Current range : 0 - 20 mA

Resolution : 10 µA

Accuracy : ± 0.25% *of the reading* ±1 *digit*

Load regulation : 0.03% *for* 0 *to full load*

Line regulation : 0.05% *for* 10% *changes*

(iii) Oven Power Supply

Suitable voltage for the oven is obtained through a step down transformer with a provision for low and high rates of heating. A glowing LED indicates, when the oven power supply is 'ON'.

EXPERIMENTAL PROCEDURES

1. Put the sample on the base plate of the four probe arrangement. Unscrew the pipe holding the four probes and let the four probes rest in the middle of the sample. Apply a very gentle pressure on the probes and tighten the pipe in this position. Check the continuity between the probes for proper electrical contacts.

   CAUTION : The Ge crystal is very brittle. Therefore, use only the minimum pressure required for proper electrical contacts.

2. Connect the outer pair of probes (red/black) leads to the constant current power supply and the inner pair (yellow/green leads) to the probe voltage terminals.

3. Place the four probe arrangement in the oven and fix the thermometer in the oven through the hole provided.

4. Switch on the ac mains of Four Probe Set-up and put the digital panel meter in the current measuring mode through the selector switch. In this position LED facing mA would glow. Adjust the current to a desired value (Say 5 mA).

5. Now put the digital panel meter in voltage measuring mode. In this position LED facing mV would glow and the meter would read the voltage between the probes.

6. Connect the oven power supply. Rate of heating may be selected with the help of a switch - Low or High as desired. Switch on the power to the Oven. The glowing LED indicates the power to the oven is 'ON'.

OBSERVATION & TABULATION

Current (I) =   mA (Constant)

.No.	Temperature(°C)	Voltage (volts)	Temperature (T in K)	ρ (ohm. cm.)	T^{-1} x 10^3	$Log_{10}\,\rho$

Distance between probes (S)   =   mm

Thickness of the crystal (W)   =   mm

CALCULATION

From Eq. (11)

$$\rho_0 = \frac{V}{I} \times 2\pi S$$

Since the thickness of the crystal is small compared to the probe distance a correction factor for it has to be applied. Further the bottom surface is non-conducting in the present case, Eq. (17) will be applied.

$$\rho = \frac{\rho_0}{G_7(W/S)}$$

The function G_7 (W/S) may be obtained from Table-I or Fig. 9 for the appropriate value of (W/S). Thus ρ may be calculated for various temperature.

Plot a graph for $Log_{10}\rho$ vs. T^{-1} X 10^{-3}

Using Eq. (7) $Log_e\rho = \dfrac{E_g}{2kT} - log_e K$

the slope of the curve is given by $\dfrac{\log_e \rho}{\dfrac{1}{T}} = \dfrac{E_g}{2k}$ (19)

Thus E_g may be obtained from the slope of the graph. Note that $\log_e = 2.3026$ $\log_{10}$ and the Eq. (7) is applicable only in the intrinsic region of the semiconductor. A typical graph is shown in Fig. 10.

QUESTIONS

1. What is the advantage of Four Probe method over the other conventional methods.

2. Can we use an ordinary millivoltmeter instead of electronic millivoltmeter or potentiometer to measure the inner probe voltage. why?

3. Explain the behaviour of the $\log_{10}\rho$ vs. 1/T curve.

4. Why a semiconductor behaves as an insulator at zero degree kelvin.

MATERIALS GIVEN HERE IS BASED ON

1. Introduction of Solid State Physics, by C. Kittel IVth edition.

2. Fundamental of Semiconductor Devices by J. Lindmayer and C.Y. Wriegley, 1071 East West Press.

3. 'Resistivity Measurements on Germanium for Transistor' by L.B. Valdes, Proceedings of the IRE, Vol. 42, p. 420 (1954).

4. Hand Book of Semiconductor Electronics, by L.P. Hunter (ed.) McGraw Hill Book Co,Inc. NY (1962).

5. 'Electrons and Holes', W. Shockley, D van Nostrand NY 1950.

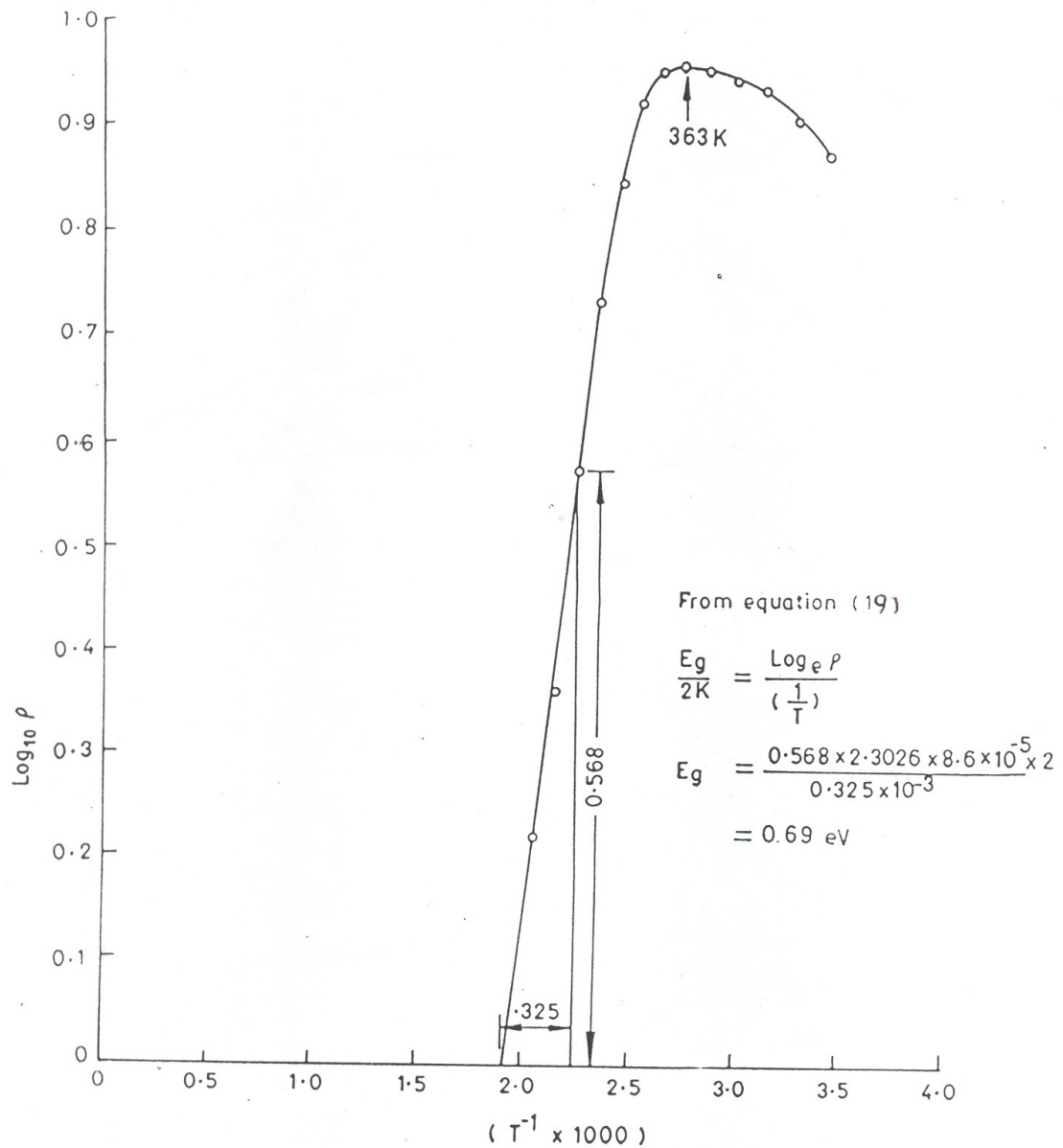6. 'Experiments in Modern Physics', by A.C. Melissions, Academic Press NY 1966.

FIG.10 THE RESISTIVITY OF A GERMANIUM CRYSTAL AS A FUNCTION OF INVERSE TEMPERATURE. FOR THIS SAMPLE T < 363°K, CONDUCTION IS DUE MAINLY TO THE IMPURITY CARRIERS (EXTRINSIC REGION), FOR T > 363, CONDUCTION IS DUE TO ELECTRONS TRANSFERRED TO THE CONDUCTION BAND (AND THE CORRESPONDING HOLES CREATED IN THE VALENCE BAND). THIS IS THE INTRINSIC REGION.

TEST RESULTS

EXPERIMENT: Measurement of Resistivity of si chip Four Probe Method # 227

Sample: Silicon Chip (n-Type)
Thickness (W): $0.50 \pm 2\%$ cm
Probe distance (S): $0.200 \pm 2\%$ cm (fixed)

OBSERVATION

S.No.	Current (I)	Voltage (V)	V/I
1.	0.500 mA	15.4 mV	30.80
2.	1.000 mA	30.8 mV	30.80
3.	1.500 mA	46.3 mV	30.87
4.	1.986 mA	61.2 mV	30.82
			Mean Value = 30.82

$$\text{Resistivity } \rho_0 = \frac{V}{I} \times 2\pi S$$
$$= 30.82 \times 2 \times 3.14 \times 0.2$$
$$= 38.71 \text{ ohm. cm}$$

Correction factor for thin films - non-conducting bottom surface

$$*G_7\left(\frac{W}{S}\right) = G_7\left(\frac{0.050}{0.2}\right) = G_7(0.25) = \textbf{5.89*}$$

$$\text{Corrected } \rho = \frac{\rho_0}{G_7\left(\frac{W}{S}\right)} = \frac{38.71}{5.89} = 6.57 \text{ ohm. cm.}$$

Result

Value of ρ specified by the manufacturers = 6 ± 1 ohm. cm
* Please refer to the booklet provides with the instrument
Sources of Error

1. The above formula of ρ is valid for semi-infinite /very large surface in compression with the probe distance.
2. Variation of doping in the sample

Passed for dispatch: Yes

Dated: 10/12/2008

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P.S.: The surface of Si Crystal get easily oxidized, therefore it is to be cleaned every time the experiment is to be performed. Put a small amount of emery powder and a drop of water on clean glass surface and rub it gently for 1 minute.