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Basic Semiconductor Physics and Technology

The majority of power electronic circuits utilise power semiconductor switching devices which *ideally* present infinite resistance when off, zero resistance when on, and switch instantaneously between those two states. It is necessary for the power electronics engineer to have a general appreciation of the semiconductor physics aspects applicable to power switching devices so as to be able to understand the vocabulary and the non-ideal device electrical phenomena. To this end, it is only necessary to attempt a qualitative description of switching devices and the relation between their geometry, material parameters, and physical operating mechanisms.

Typical power switching devices such as diodes, thyristors, and transistors are based on a monocrystalline group IV silicon semiconductor structure or a group IV polytype, silicon carbide. These semiconductor materials are distinguished by having a specific electrical conductivity, σ, somewhere between that of good conductors (>10^{20} free electron density) and that of good insulators (<10^{3} free electron density). Silicon is less expensive, more widely used, and a more versatile processing material than silicon carbide, thus the electrical and processing properties of silicon are considered first, in more detail.

In pure silicon at equilibrium, the number of *electrons* is equal to the number of *holes*. The silicon is called *intrinsic* and the electrons are considered as negative charge-carriers. Holes and electrons both contribute to conduction, although holes have less mobility due to the covalent bonding. Electron-hole pairs are continually being *generated* by thermal ionization and in order to preserve equilibrium previously generated pairs *recombine.* The intrinsic carrier concentrations n_i are equal, small (1.4×10^{10} /cc), and highly dependent on temperature. In order to fabricate a power-switching device, it is necessary to increase greatly the free hole or electron population. This is achieved by deliberately doping the silicon, by adding specific impurities called *dopants.* The doped silicon is subsequently called *extrinsic* and as the concentration of dopant N_c increases, the resistivity ρ decreases.

Silicon doped with group V elements, such as As, Sb or P, will be rich in electrons compared to holes. Four of the five valence electrons of the group V

dopant will take part in the covalent bonding with the neighbouring silicon atom, while the fifth electron is only weakly attached and is relatively 'free'. The semiconductor is called *n-type* because of its free negative charge-carriers. A group V dopant is called a *donor,* having donated an electron for conduction. The resultant electron impurity concentration is denoted by N_D - the donor concentration.

If silicon is doped with atoms from group III, such as B, Al, Ga or In, which have three valence electrons, the covalent bonds in the silicon involving the dopant will have one covalent-bonded electron missing. The impurity atom can accept an electron because of the available thermal energy. The dopant is thus called an *acceptor*, which is ionised with a net positive charge. Silicon doped with acceptors is rich in holes and is therefore called *p-type.* The resultant hole impurity concentration is denoted by N_A - the acceptor concentration.

Electrons in n-type silicon and holes in p-type are called *majority carriers,* while holes in n-type and electrons in p-type are called *minority carriers.* The carrier concentration equilibrium can be significantly changed by irradiation by photons, the application of an electric field or by heat. Such carrier injection mechanisms create *excess carriers.*

If n-type silicon is irradiated by photons with enough energy to ionise the valence electrons, electron-hole pairs are generated. There is already an abundance of majority electrons in the n-type silicon, thus the photon-generated excess minority holes are of more relative and detectable importance. If the light source is removed, the time constant associated with recombination, or decay of excess minority carriers, is called the *minority carrier hole lifetime,* τ_h. For a p-type silicon, exposed to light, excess minority electrons are generated and after the source is removed, decay at a rate called the *minority carrier electron lifetime,* τ_e. The minority carrier lifetime is often called the *recombination lifetime.*

A difficulty faced by manufacturers of high-voltage, large-area semiconductor devices is that of obtaining uniformity of n-type phosphorus doping throughout the usual high-resistivity silicon starting material. Normal crystal-growing and doping techniques give no better than ±10 per cent fluctuation around the wanted resistivity at the required low concentration levels (<10^{14} /cc). Final device electrical properties will therefore vary widely in all lattice directions. Tolerances better than ±1 per cent in resistivity and homogeneous distribution of phosphorus can be attained by neutron radiation, commonly called *neutron transmutation doping,* NTD. The neutron irradiation flux transmutes silicon atoms first into a silicon isotope with a short 2.62-hour half-lifetime, which then decays into phosphorus. Subsequent annealing removes any crystal damage caused by the irradiation. Neutrons can penetrate over 100mm into silicon, thus large silicon crystals can be processed using the NTD technique.

1.1 Processes forming pn junctions

A pn junction is the location in a semiconductor where the impurity changes from p to n while the monocrystalline lattice continues undisturbed. A bipolar diode is thus created, which forms the basis of any bipolar semiconductor device.

The donor-acceptor impurities junction is formed by any one of a number of process techniques, namely alloying, diffusion, epitaxy, ion implantation or the metallization for ohmic contacts.

1.1.1 The alloyed junction

At the desired region on an n-type wafer, a small amount of p-type impurity is deposited. The wafer is then heated in an inert atmosphere and a thin film of melt forms on the interface. On gradual cooling, a continuous crystalline structure results, having a step or abrupt pn junction as shown in figure 1.1. This junction-forming process is rarely employed to form a power pn junction.

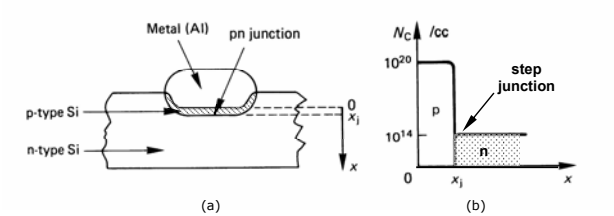

Figure 1.1. *n-Si to Al metal alloy junction: (a) cross-section where x_j is the junction depth below the metal-semiconductor boundary and (b) impurity profile of the formed step junction.*

1.1.2 The diffused junction

An n-type silicon substrate is heated to about 1000°C in a diffusion furnace. A p-type impurity is entered in a mixed vapour compound form. This compound breaks down as a result of the high temperature, and is slowly diffused into the substrate. The maximum impurity concentration occurs at the surface, tailing off towards the inside. The doping profile is mathematically defined and is varied by controlling the vapour mixture concentration, the furnace temperature, and time of diffusion. If the source concentration is continuously replenished, thus maintained constant, the doping profile is given by a complementary error function, erfc. If natural depletion of dopant occurs, then the profile is an exponential function, which gives a Gaussian diffusion distribution. The actual areas of diffusion are selected by a surface-blocking mask of silicon dioxide, as illustrated in figure 1.2.

The diffusion process is the only junction forming technique that is not applicable to silicon carbide wafer processing.

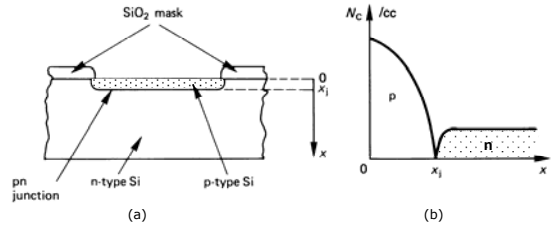

Figure 1.2. *Diffused pn junction: (a) cross-section where x_j is the junction depth below the silicon surface and (b) impurity concentration profile.*

1.1.3 The epitaxy junction

A pre-cleaned, polished, almost perfect silicon crystal surface acts as a substrate for subsequent deposition. The pre-doped silicon is heated to about 1150°C in a quartz reactor. A hydrogen gas flow carrying a compound of silicon such as $SiCl_4$ or SiH_4 is passed over the hot substrate surface, and silicon atoms are deposited, growing a new continuous lattice. If phosphine (PH_3) or diborane (B_2H_6) is included in the silicon compound gas flow, a layer of the required type and resistivity occurs. Up to 100µm of doped silicon can be grown on substrates for power devices at a rate of about 1 µm/min at 1200°C. A very low crystalline fault rate is essential if uniform electrical properties are to be attained.

1.1.4 The ion-implanted junction

Ion impurities (B, P or As) are accelerated in a vacuum at high keV energies at the pre-doped silicon substrate, which is at room temperature. The ions penetrate the lattice to less than a few microns, typically 1µm at about ½MeV. The resultant doping profile is Gaussian, with the smaller ion like boron, penetrating deeper. In so doing, the lattice is disrupted and subsequent annealing at elevated temperatures of about 700°C restores the uniform lattice structure, without activating the implanted atoms. Boron requires higher annealing temperatures which may cause undesired diffusion of the dopant. Ion implantation is the most accurate and controllable doping process, giving excellent doping level uniformity and production repeatability.

1.1.5 The ohmic-contact junction

An ohmic contact is a resistive connection which is voltage independent. Aluminium is commonly evaporated in a vacuum at near room temperature, onto the wafer surface to form a metallised electrical contact. Deposit rates of ½ µm/minute are typical. If the silicon is n-type, a pn Schottky junction is formed, which is undesirable as an ohmic contact. This junction forming aspect is

discussed at the end of section 3.1.4. Ohmic metal contact to p-type semiconductors with a large bandgap, like silicon carbide, is technically difficult.

1.2 The oxidation and masking process

An extremely useful and convenient process employed during device fabrication is the formation of silicon dioxide (silica) $Si0_2$ on the silicon wafer surface.

Wafers of silicon placed in a furnace for three to four hours at 1000-1200°C containing oxygen gas form a surface oxide layer of $Si0_2$ usually less than 1μm thick. The oxide penetration into the silicon is about 40% of its thickness. Wet oxidation, with water added, is about 20 times faster than dry oxidation but the oxide quality is lower. The wafer is effectively encapsulated by silica glass, which will prevent penetration by normal impurity atoms, except gallium atoms. Selective diffusions are made in the silicon by opening windows through the oxide by selective etching with HF following a photo-resist lithography masking process.

The excellent electrical-insulating properties of $Si0_2$ may be utilised for surface junction passivation. Silicon dioxide has an amorphous structure with a very high resistivity and a dielectric constant of 3.85, which make it a useful insulator. Silicon dioxide is used extensively as an insulating barrier between the gate metal and channel of insulated gate semiconductor switching devices.

1.3 Polysilicon deposition

Polycrystaline silicon is used as the gate electrode in metal oxide devices and for metallization. The deposition method involves the pyrolysis of silane $SiH_{4\,(g)} \rightarrow Si_{\,(s)} + 2H_{2\,(g)}$ and at 600°C and normal pressure, deposits about 20nm/minute. The polysilicon is heavily doped to reduce the resistivity using phosphine or diborane *in situ* or by ion implantation. Diffusion is used at higher temperatures in order to attain the lowest resistivities.

1.4 Lifetime control

Two basic processes have been developed to reduce the lifetime of carriers in power devices.

- Thermal diffusion of gold or platinum or
- Bombardment of the silicon with high-energy particles such as electrons and protons.

The diffusion of gold or platinum occurs more rapidly than the diffusion of group III and V dopants, hence the precious metal is diffused at 800 to 900°C, just prior to metallization, which is performed at a lower temperature. The higher the precious metal diffusion temperature the higher the solubility and the lower the carrier lifetime. Disadvantages of precious metal diffusion include:

- devices cannot be tested prior to or immediately after impurity diffusion and
- small temperature changes cause a wide variation in device characteristics.

In high-resistivity silicon used to fabricate power devices, irradiation bombardment causes defects composed of complexes of vacancies with impurity atoms of oxygen and of two adjacent vacancy sites in the lattice. The advantages of the use of irradiation in order to reduce carrier lifetime in power devices are:

- irradiation is performed at room temperature, after fabrication;
- irradiation can be accurately controlled hence a tighter distribution of electrical characteristics results;
- overdose annealing can be performed at only 400°C; and
- it is a clean, non-contaminating process.

Much attention has been focussed on proton irradiation, which has high costs and long processing scan times, but offers the most accurate and precise form of lifetime control. The electrical consequences of lifetime control are an improvement in switching speed at the expense of increased leakage and on-state voltage.

1.5 Silicon Carbide

Wide bandgap semiconductors (GaN, SiC, diamond, etc.) have better high voltage and temperature characteristics than silicon devices. However, because silicon carbide, SiC, sublimes at high temperature, ≈1800ºC, processing is more difficult than for silicon (which melts at a lower temperature of 1415°C). The similar chemistry properties of silicon and silicon carbide (both in group IV) means that many of the existing processes for silicon can be applied to silicon carbide, but with some refinement and higher processing temperatures. The exception is thermal diffusion which is not effective if a good SiC surface morphology is to be retained.

The SiC crystal boules are grown by seeded sublimation using the physical vapour transport (PVT) method. Alternatively, chemical vapour deposition (CVD) can be used, where SiH_4, C_3H_8, and H_2 are typically injected into the chamber. This process is mainly used for producing SiC epitaxial growth. A hot walled CVD reactor can deposit 100μm at a rate of 1 to 5 μm/hour at 1200ºC to 1500ºC. Crystal defects (micropipes, stack faults, etc.) occur at a rate of less than 1 per cm^2. Proprietary defect healing technology can significantly decrease the defect rate. The main single crystal polytypes for power switching device fabrication are 4H-SiC and 6H-SiC (this lattice structure terminology is based on the Ramsdell notation).

Nitrogen for n-type and aluminium or boron for p-type can be used in epitaxial growth and ion implantation. Substrates usually have an n or p epitaxial drift layer. Typical n-type epitaxy (50μm) can be thicker than a p-type layer (10μm), and the n-type epitaxy has a thin 1μm n-type buffer or fieldstop.

Ion implantation is shallow, typically less than 1μm, and requires high temperature and 30 to 300keV. Subsequent annealing is at 1650ºC. The lower the

temperature, the longer the annealing time. Contact metallization can use nickel on highly n-doped SiC, which is annealed at 1150ºC for a few minutes. A nickel and titanium Schottky metal combination is suitable for p^+ region metallization. $Si0_2$ is an electrical-insulator that can be grown on both Si and SiC. Oxide growth for SiC is slower than that on silicon and involves nitridation of nitric oxide, N_20, at 1300ºC. Because of the physical and chemical stability of silicon carbide, acid wet etching is ineffective and dry reactive ion etching tends to be used for etching.

1.6 Si and SiC physical and electrical properties compared

The processing of silicon is a mature, cost efficient technology, with 12-inch wafers and submicron resolution common within the microelectronics industry. So-called wide bandgap semiconductors like silicon carbide offer promising high voltage and temperature power switching device possibilities as material quality and process yields improve. Figure 1.3 shows and allows comparison of the key physical and electrical properties of the main semiconductor materials applicable to power switching device fabrication.

The higher

- the energy bandgap, E_g, the higher the possible operating temperature before intrinsic conduction mechanisms produce adverse effects;
- the avalanche breakdown electric field, ξ_b, the higher the possible rated voltage;
- the thermal conductivity, σ_T, the more readily heat dissipated can be removed; and
- the saturation electron drift velocity, v_{sat}, and the electron mobility, μ_n, the faster possible switching speeds.

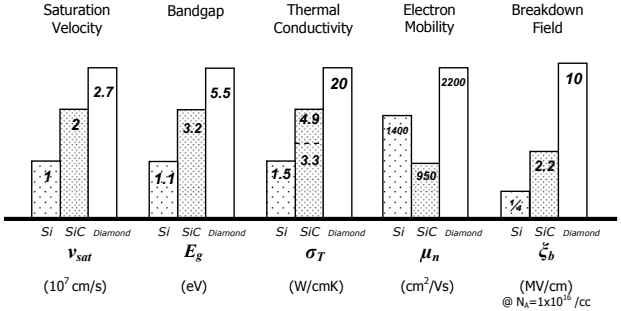

Figure 1.3. *Key electrical and thermal characteristics of group IV monocrystalline silicon and diamond and polytype 4H-silicon carbide, at room temperature.*

Although the attributes of wide bandgap materials are evident, processing is more difficult and some of the parameters vary significantly with a wide operating temperature range. SiC performance figures are slightly better than those for GaN, except, importantly, GaN has better carrier mobility. GaN growth is complicated by the fact that Nitrogen tends to revert to the gaseous state, and therefore only thin layers are usually grown on sapphire or SiC substrates. Lattice-substrate boundary mismatch occurs because of the significant difference in molecule sizes and packing. Such a boundary imperfection may prove problematic with power devices where principle current flow is usual vertically through the structure, hence through the imperfect lattice boundary.

Some of the physical and electrical parameters and their values in figure 1.3 will be explained and used in subsequent chapters. Other useful substrate data is given in table 1.1.

Table 1.1. Other useful substrate material data

			Si	SiC	Diamond
relative dielectric constant	ε_r		11.8	9.7	5.8
maximum operating temperature	T_{max}	°C	300	1240	1100
melting temperature	T_{melt}	°C	1415	sublime >1800	phase change

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