2

The pn Junction

The diode is the simplest bipolar semiconductor device. It comprises p-type and n-type semiconductor materials brought together, usually after diffusion, to form a (step or abrupt) junction as shown in figure 2.la.

A *depletion layer*, or alternatively a *space charge layer*, scl, is built up at the junction as a result of diffusion caused by the large carrier concentration gradients. The holes diffuse from the p-side into the n-side while electrons diffuse from the n-side to the p-side, as shown in figure 2.lb. The n-side, losing electrons, is charged positively because of the net donor charge left behind, while the p-side conversely becomes negatively charged. An electric potential barrier, ξ, builds up, creating a drift current which opposes the diffusion flow, both of which balance at thermo-dynamic equilibrium as shown in figure 2.lc. There are no free carriers in the scl.

The zero external bias, built-in, junction potential or scl potential is given by

$$\Phi = \frac{kT_j}{q} \ell n \frac{N_A N_D}{n_i^2} \qquad \text{(V)} \qquad (2.1)$$

where q is the electron charge, 1.6 x 10^{-19} C
k is Boltzmann's constant, 1.38 x 10^{-23} J/K
T_j is the junction temperature, K.
Thus $\varphi = kT_j/q = 0.0259$ eV at room temperature, 300 K.

One important feature of the pn junction is that current (holes) flows freely in the p to n direction when forward-biased, that is, the p-region is biased positive with respect to the n-region. Only a small leakage current flows in the reverse voltage bias case. This asymmetry makes the pn junction diode useful as a rectifier, exhibiting static voltage-current characteristics as illustrated in figure 2.2.

2.1 The pn junction under forward bias (steady-state)

If the p-region is externally positively-biased with respect to the n-region as shown in figure 2.3b, the scl narrows and current flows freely. The emf positive potential supplies holes to the p-region, while the negative emf potential provides electrons to the n-region. The carriers both combine, but are continuously replenished from the emf source. A large emf source current flows through the diode, which is termed *forward-biased*.

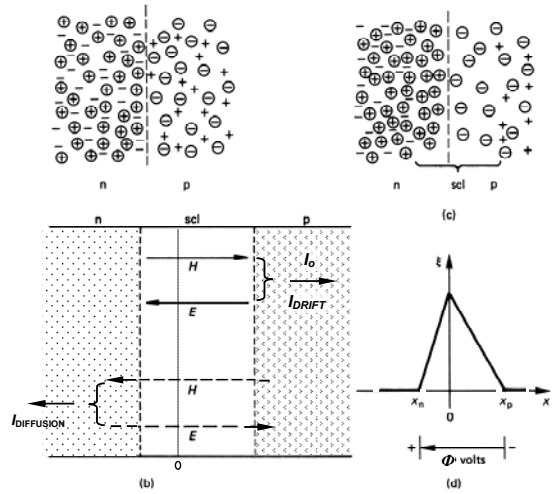


Figure 2.1. *The step junction. (a) The junction if carriers did not diffuse: ⊕ ionised donors, ⊖ ionised acceptors, + holes and - electrons; (b) electron and hole movements: ---- diffusion flows, ——— drift flows; (c) equilibrium distribution of ionised impurities and free carriers; and (d) scl electric field and voltage.*

2.2 The pn junction under reverse bias (steady-state)

If a bias voltage is applied across the p and n regions as shown in figure 2.3c, with the p-terminal negative with respect to the n-terminal, then the scl widens. This is because electrons in the n-region are attracted to the positive external emf source while holes in the p-region are attracted to the negative emf potential. As the scl widens, the peak electric field ξ_m at the junction increases as shown in figure 2.3d.

The only current that flows is the small *leakage current* which is due to carriers generated in the scl or minority carriers which diffuse to the junction and are collected. The junction is termed *reverse-biased.*

Increasing applied reverse bias eventually leads to junction reverse voltage breakdown, V_b, as shown in figure 2.2, and the diode current is controlled by the external circuit. Breakdown is due to one of three phenomena, depending on the doping levels of the regions and, most importantly, on the concentration of the lower doped side of the junction.

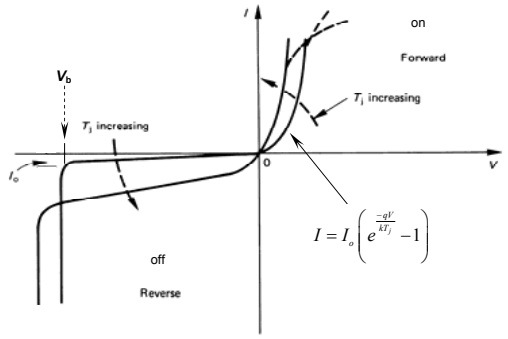


Figure 2.2. *Typical I-V static characteristics of a silicon pn junction diode, and the effects of junction temperature, T_j.*

2.2.1 Punch-through voltage

The reverse voltage extends the scl to at least one of the ohmic contacts and the device presents a short circuit to that voltage in excess of the *punch-through* voltage, V_{PT}. Punch-through tends to occur at low temperatures with devices which employ a low concentration region (usually the n-side), as is usual with high-voltage devices. The punch-through voltage for silicon can be approximated by

$$V_{PT} = 7.67\times10^{-16} N_c W_c^2 \qquad \text{(V)} \qquad (2.2)$$

where N_c is the concentration in /cc of the lighter doped region and
W_c is the width of that region in μm.

2.2.2 Avalanche breakdown

Avalanche breakdown or *multiplication breakdown*, is the most common mode of breakdown and occurs when the peak electric field, ξ_m, in the scl at the junction exceeds a certain level which is dependent on the doping level of the lighter doped

region. Minority carriers associated with the leakage current are accelerated to kinetic energies high enough for them to ionise silicon atoms on collision, thereby creating a new hole-electron pair. These are accelerated in opposite directions, because of the high electric field strength, colliding and ionising repeatedly - hence the term avalanche, impact ionisation or carrier multiplication. If the lighter doped silicon region has a concentration of

$$10^{13} < N_c < 5\times10^{14} \qquad (\text{/cc})$$

then the avalanche voltage may be approximated by

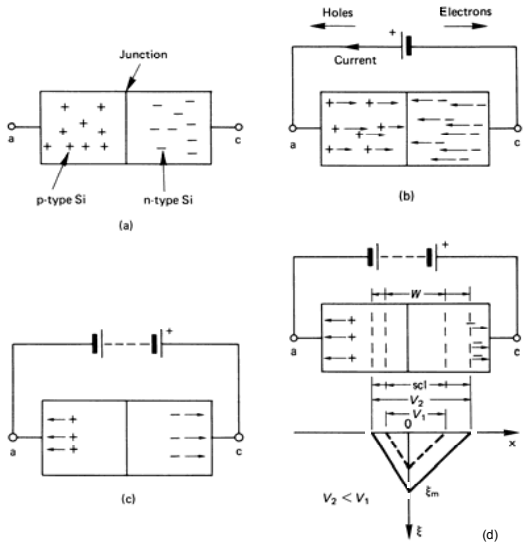
$$V_b = 5.34 \times 10^{13}\, N_c^{-3/4} \qquad \text{(V)} \qquad (2.3)$$

The peak electric field at the junction will be

$$\xi_b = 3.91 \times 10^{5}\, N_c^{1/8} \qquad \text{(V/m)} \qquad (2.4)$$

and the width of the scl, mainly in the lighter doped region, at breakdown is given by

$$W = 2\, V_b / \xi_b \qquad (2.5)$$



Figur ity
c
voltage; (c) with reverse applied voltage; and (d) electric field and scl change with increased reverse applied voltage.

2.2.3 Zener breakdown

Field or Zener breakdown occurs with heavily doped junction regions and at usually less than 5V reverse bias. It occurs when the scl is too narrow for avalanche yet the electric field grows very large and electrons tunnel directly from the valence band on the p-side to the conduction band on the n-side. This reverse current is called the *Zener effect.*

These three modes of reverse voltage breakdown are not necessarily destructive provided the current is uniformly distributed. If the current density in a particular area is too high, a local hot spot may occur, leading to device thermal destruction.

2.3 Thermal effects

The pn junction current, I, shown in figure 2.2, is related to the scl voltage, V, according to

$$I(V) = I_o[e^{-qV/kT_j} - 1] \quad \text{(A)} \qquad (2.6)$$

where I_o, is the reverse leakage current in amps.
The forward conduction voltage decreases with increased junction temperature, T_j. That is, the on-state voltage has a negative temperature coefficient. In practical silicon pn diodes, at low currents, the temperature coefficient is typically -2.4 mV/K, becoming less negative with increased current. At higher currents, the coefficient becomes positive because of the reduced carrier mobility at higher temperatures, which causes non-scl regions to increase in resistance. The effects of the change in temperature coefficient at higher currents, in practical devices, are shown dotted in figure 2.2. Neglecting the exponential silicon bad gap temperature dependence, the temperature effects at high current, on the diffusion constant component of the leakage current I_o in equation (2.6), called the saturation current, is given by

$$I_o(T) = I_o(25°C)\left(\frac{T}{300}\right)^{1.8} \qquad (2.7)$$

Silicon carbide diodes have a higher temperature coefficient, typically +8mV/K.

The avalanche voltage increases with temperature, as does the reverse leakage current. The effects of temperature on the reverse bias characteristics are shown in figure 2.2. In the case of silicon carbide, increased temperature decreases the avalanche voltage and increases the leakage current.

The silicon temperature coefficient for avalanche is positive since the mean distance between collisions is reduced because of the increased thermal energy, which increases the vibrational amplitude. Higher electric fields are necessary for the carriers to gain sufficient kinetic energy for ionisation.

Equation (2.6) also indicates that the reverse bias current increases with increased junction temperature. This positive temperature coefficient does not generally result in thermal instability with silicon devices, provided sufficient heat sinking is employed on smaller devices.

2.4 Models for the junction diode

Semiconductor device models are used extensively for power electronic circuit simulation. A basic piecewise-linear model is applicable to simple manual calculations, where the terminal I-V characteristics are empirically modelled based on ideal circuit elements. A more complex and accurate model is required for computer transient analysis simulation. Such accurate models are based on the semiconductor physics of the device. Many power switching semiconductor device manufacturers provide values for the model parameters suitable for circuit simulation in the packages PSpice and SABER.

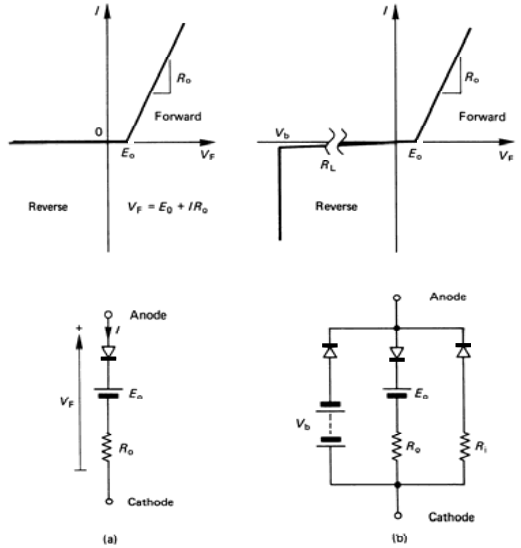


Figure 2.4. *Piecewise-linear approximations of junction diode characteristics: (a) ideal diode with an offset voltage and resistance to account for slope in the forward characteristic and (b) model including reverse bias characteristics.*

2.4.1 Piecewise-linear junction diode model

The pn junction diode is a unilateral device that, to a good approximation, conducts current in only one direction. Figure 2.4a shows a *piecewise-linear* (pwl) model of the diode that is suitable for static modelling in power electronic circuits. It includes a perfect diode, an on-state voltage source E_o, and a series resistor of value R_o to account for the slope in the actual forward characteristic. The forward *I-V* characteristic at a given temperature is given by

$$V_F(I_F) = E_0 + I_F R_0 \quad \text{for } V_F > E_0 \qquad \text{(V)} \qquad (2.8)$$

The model in figure 2.4a does not incorporate the static reverse characteristics of leakage and avalanche. These are shown in figure 2.4b, where V_b from equation (2.3) models the avalanche limit and $R_i(=V_b/I_o)$ gives linear leakage current properties for a given junction temperature. The three diode components are assumed perfect.

The model given by equation (2.8) is adequate for calculation of static balancing requirements of parallel and series connected diodes and thyristors, as considered in section 10.1 and the associated problems, 10.4, 10.5, and 10.9 to 10.12.

Example 2.1: ***Using the pwl junction diode model***

An approximation to the forward characteristic of the diode shown in figure 2.4a, is given by $V_F = 1.0 + 0.01 I_F$. For a constant current of 45A for ⅔ of a cycle, calculate the diode

- ***i.*** on-state voltage;
- ***ii.*** mean power loss; and
- ***iii.*** rms current.

Solution

i. The on-state voltage at 45A is given by

$$V_F(i_F) = 1.0 + i_F\ 0.01 = 1.0 + 45 \times 0.01 = 1.45\text{V}$$

ii. If the on-state duty cycle is δ=⅔, the average power loss is

$$\bar{P} = \delta \times V_F \times I_F = \tfrac{2}{3} \times 1.45\text{V} \times 45\text{A} = 43.2\text{W}$$

iii. The diode rms current is given by

$$I_{rms} = \sqrt{\delta} \times I_{dc} = \sqrt{\tfrac{2}{3}} \times 45\text{A} = 36.7\text{A}$$

♣

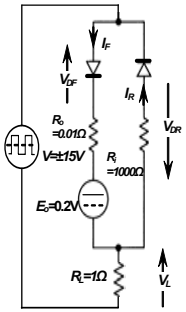
Example 2.2: ***Static diode model***

A Schottky diode is used to half-wave rectify a square wave ±15V source in series with a 1Ω resistor. If the diode model shown in figure 2.4b is modelled by R_o = 0.01 Ω, E_o = 0.2V, R_i = 1000Ω, and V_b = 30V, then determine:

- ***i.*** the diode model forward and reverse bias operating point equations for the series circuit
- ***ii.*** the load current and diode voltage

- ***iii.*** the rectifier losses (neglecting any recovery effects) and the load power dissipation
- ***iv.*** Estimate the power dissipated in the load if the source is ac with the same fundamental component as the square wave.
- ***v.*** What is the non-fundamental power dissipated with the square wave source.

Solution



i. When the diode is *forward biased*

$$i_F = \frac{1}{R_o}\left(v_{DF} - E_o\right) \quad \text{for} \quad v_{DF} \geq 0.2\text{V}$$

Kirchhoff's voltage law for the series circuit gives

$$V_s = i_F R_L + v_{DF}$$

Eliminating the diode voltage v_{DF} gives series circuit current

$$i_F = \frac{V_s - E_o}{R_o + R_L} \quad \text{for} \quad V_s \geq E_o$$

$$i_F = 0 \quad \text{for} \quad 0 < V_s < E_o$$

The diode voltage is therefore given by

$$v_{DF} = \frac{V_s R_o + E_o R_L}{R_o + R_L} = E_o + i_F R_o \quad \text{for } i > 0$$

When the diode is *reversed biased*, below the reverse breakdown voltage V_b

$$i_R = \frac{1}{R_i} v_{DR} \quad \text{for} \quad v_{DR} < V_b$$

$$V_s = i_R R_L + v_{DR}$$

Eliminating the diode voltage v_D gives series circuit current

$$i_R = \frac{V_s}{R_i + R_L}$$

The diode voltage is thus given by

$$v_{DR} = \frac{V_s R_i}{R_i + R_L} = i_R R_i$$

ii. The circuit voltages and current are, when the diode is forward biased,

$$i_F = \frac{15\text{V} - 0.2\text{V}}{0.01\Omega + 1\Omega} = 14.65\text{A}$$

$$V_{D_F} = 0.2\text{V} + 14.65\text{A} \times 0.01\Omega = 0.35\text{V}$$

If $R_L >> R_o$, the diode current equation can be simplified using R_o=0.

When the diode is reverse biased

$$i_R = \frac{15\text{V}}{1000\Omega + 1\Omega} = 15.0\text{mA}$$

$$V_{D_R} = 15\text{mA} \times 1000\Omega = 15.0\text{V}$$

If $R_i >> R_L$ the diode current and voltage equations can be simplified using R_L=0.

iii. The rectifier losses are, when forward biased,

$$P_{D_F} = v_{D_F} \times i_F$$
$$= 0.35\text{V} \times 14.65\text{A} = 5.127\text{W}$$

and when reverse biased

$$P_{D_R} = v_{D_R} \times i_R$$
$$= 15\text{V} \times 15\text{mA} = 0.225\text{W}$$

Total diode losses are therefore ½(5.127 + 0.225) = 2.68W.
The power from the square wave supply is

$$½ \times (15\text{V} \times 14.65\text{A} + 15\text{V} \times 15\text{mA}) = 110\text{W}$$

with 110 – 2.68 = 107.32W dissipated in the 1Ω resistor load.

iv. The magnitude of the fundamental of a square wave is 4/π times the square wave magnitude, that is, 15V×4/π = 19.1V peak.
The forward biased diode does not conduct until the supply voltage exceeds 0.2V. This is a small percentage of the sine wave, hence can be neglected in the loss estimate. The forward current flow is approximately

$$i_F = \frac{19.1\text{V} - 0.2\text{V}}{1\Omega + 0.01\Omega} \times \sin \omega t = 18.7 \times \sin \omega t$$

The rms of a sine is 1/√2 its magnitude and 1/√2 again for a half wave rectified sine. That is

$$i_{Frms} = \frac{18.7\text{A}}{\sqrt{2}\sqrt{2}} = 9.35\text{A rms}$$

The reverse leakage current is given by

$$i_R = \frac{19.1\text{V}}{1000\Omega + 1\Omega} \times \sin \omega t = 0.019 \times \sin \omega t$$

which gives an rms current of

$$i_{Rrms} = \frac{19\text{mA}}{\sqrt{2}\sqrt{2}} = 9.5\text{mA rms}$$

The power dissipated in the 1Ω load resistor is

$$P_L = \left(i_{F_{rms}}^2 + i_{R_{rms}}^2\right) \times R_L$$
$$= \left(9.35^2 + 0.0095^2\right) \times 1\Omega = 87.42\text{W} + 90\mu\text{W} = 87.42\text{W}$$

Clearly, the reverse leakage current related component is negligible.

v. With the square wave, from part iii., 107.32W are dissipated in the load but from part ii., only 87.42W are dissipated for a sine wave with the same fundamental magnitude. The 19.9W difference is power produced by the harmonics of the fundamental (3rd, 5th, …). For a resistive heating load this power produces useful heating, but in a motor the harmonic power would produce unwanted torque pulsations and motor heating.

♣

2.4.2 Semiconductor physics based junction diode model

The charge-carrier diode model shown in figure 2.5 is necessary for transient circuit analysis involving diodes. The pn junction diode is assumed to have an abrupt or step junction. The model components are voltage dependant current sources, I_n and I_b, voltage dependant capacitance C_t and C_j, and series access resistance R_s.

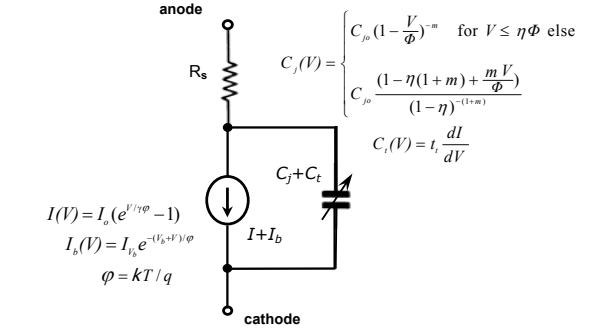


Figure 2.5. *PSpice transient analysis circuit model of the pn junction diode.*

The ideal diode current I is given by equation (2.6). The diode current I_b models reverse voltage breakdown, where the breakdown voltage V_b is assumed due to avalanche and is given by equation (2.3). The voltage dependant transit capacitance, C_t, which is dominant under forward bias, is related to the minority carrier lifetime t_t. The voltage dependant scl (depletion layer) capacitance C_j, which is dominant under reverse bias, involves the zero bias junction potential voltage Φ, given by equation (2.1) and the zero bias junction capacitance C_{jo}. In the case of the silicon carbide Schottky diode, $C_j >> C_t$. The scl capacitance, $C_j(V)$ can be evaluated from the pn diode structure and doping profile, as follows.

2.4.2i - Determination of C_{jo}

Poisson's equation, in conjunction with Gauss's law, for the one dimensional step junction shown in figure 2.6, give

$$\frac{d^2V}{dx^2} = -\frac{d\xi}{dx} = \frac{qN_D}{\varepsilon_s} = -\frac{qN_A}{\varepsilon_s} \qquad (2.9)$$

The dielectric permittivity $\varepsilon_s = \varepsilon_r \varepsilon_o$ comprises the free space permittivity $\varepsilon_o = 8.854\text{x}10^{-12}$ F/m and the relative permittivity $\varepsilon_r = 11.8$ for silicon and 9.7 for SiC.

$$\frac{d\xi(x)}{dx} = \begin{cases} \frac{q}{\varepsilon_s} N_D & \text{for} \quad -x_n < x < 0 \\ -\frac{q}{\varepsilon_s} N_A & \text{for} \quad 0 < x < x_p \end{cases} \tag{2.10}$$

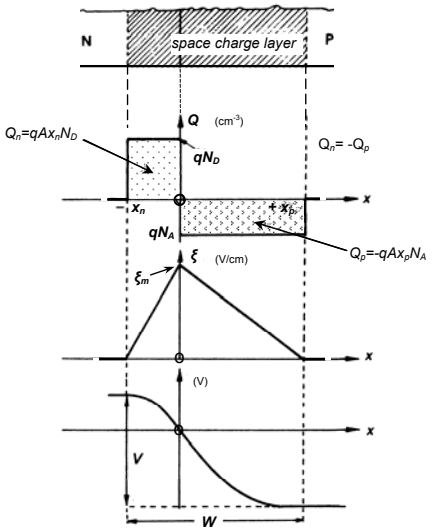


Figure 2.6. *The charge Q, electric field ξ, and voltage potential V, in the space charge layer of a step pn junction.*

Integrating both parts of equation (2.10) over the shown bounds, gives $\xi(x)$:

$$\frac{dV(x)}{dx} = \xi(x) = \begin{cases} \frac{q}{\varepsilon_s} N_D x + \xi_m & \text{for} \quad -x_n < x < 0 \\ -\frac{q}{\varepsilon_s} N_A x + \xi_m & \text{for} \quad 0 < x < x_p \end{cases} \tag{2.11}$$

where the maximium field intensity (at $x = 0$) is $\xi_m = \frac{q}{\varepsilon_s} N_D x_n = \frac{q}{\varepsilon_s} N_A x_p$

The piece-wise parabolic voltage potential across the scl shown in figure 2.6, is given by integration of the electric field, that is

$$\begin{aligned} V &= \int_{-x_n}^{0} \left(\frac{q}{\varepsilon_s} N_D x + \xi_m\right) dx \; + \; \int_{0}^{x_p} \left(-\frac{q}{\varepsilon_s} N_A x + \xi_m\right) dx \\ &= \tfrac{1}{2} \xi_m W \end{aligned} \tag{2.12}$$

Since the charges each side of the metallurgical junction must balance, equation (2.12) can be rearranged to give the scl width.

$$W = \sqrt{\left[\frac{2\varepsilon_s V}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)\right]} \tag{2.13}$$

From equation (2.1), a zero bias voltage Φ exists without the presence of any external voltage. Therefore, to incorporate non-equilibrium conditions, the electrostatic barrier potential becomes Φ-V, where V is the externally applied reverse bias voltage. Consequently the expression for the scl width becomes:

$$W = \sqrt{\left[\frac{2\varepsilon_s (\boldsymbol{\Phi} - \boldsymbol{V})}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)\right]} \tag{2.14}$$

The scl width voltage dependence can be expressed in terms of the zero bias scl width, W_0

$$\begin{aligned} W(\boldsymbol{V}) &= \sqrt{\left[\frac{2\varepsilon_s \boldsymbol{\Phi}}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)\right]} \sqrt{1 - \frac{\boldsymbol{V}}{\boldsymbol{\Phi}}} \\ &= W_0 \sqrt{1 - \frac{\boldsymbol{V}}{\boldsymbol{\Phi}}} \end{aligned} \tag{2.15}$$

$$\begin{aligned} x_{n0} &= \frac{W_0}{1 + N_D / N_A} \qquad & x_{p0} &= \frac{W_0}{1 + N_A / N_D} \\ x_n(V) &= x_{n0} \sqrt{1 - \frac{\boldsymbol{V}}{\boldsymbol{\Phi}}} \qquad & x_p(V) &= x_{p0} \sqrt{1 - \frac{\boldsymbol{V}}{\boldsymbol{\Phi}}} \end{aligned} \tag{2.16}$$

The magnitude of the voltage dependant charge on each side of the junction is

$$\begin{aligned} |Q(V)| &= q A \frac{N_D N_A}{N_D + N_A} W = A\left[2q\varepsilon_s \boldsymbol{\Phi} \frac{N_D N_A}{N_D + N_A}\right]^{\frac{1}{2}} \sqrt{1 - \frac{\boldsymbol{V}}{\boldsymbol{\Phi}}} \\ &= Q_0 \sqrt{1 - \frac{\boldsymbol{V}}{\boldsymbol{\Phi}}} \end{aligned} \tag{2.17}$$

The junction capacitance is given by differentiation of equation (2.17) with respect to Φ-V

$$C_j = \left|\frac{dQ}{d(\boldsymbol{\Phi} - V)}\right| = \varepsilon_s A \left[\frac{q}{2\varepsilon_s (\boldsymbol{\Phi} - \boldsymbol{V})} \frac{N_D N_A}{N_D + N_A}\right]^{\frac{1}{2}} = \frac{\varepsilon_s A}{W} \tag{2.18}$$

Equation (2.18) can be rearranged to give the PSpice capacitance form, in terms of the zero bias junction capacitance C_{jo}.

$$C_j(V) = \frac{C_{jo}}{\left(1 - \frac{V}{\Phi}\right)^{\frac{1}{2}}} \qquad \text{where } C_{jo} = \varepsilon_s A \left[\frac{q}{2\varepsilon_s \Phi} \frac{N_D N_A}{N_D + N_A}\right]^{\frac{1}{2}} \qquad (2.19)$$

The electric field at the metallurgical junction, from equation (2.12) is given by

$$\xi_j(V) = \xi_0 \sqrt{1 - \frac{V}{\Phi}} \quad \text{where} \quad \xi_0 = 2\Phi / W_0 \qquad (2.20)$$

2.4.2ii - One-sided pn diode equations

When $N_A >> N_D$, which is the usual case in high voltage pn diodes, equations (2.12) to (2.20) are approximated by the following one-sided diode equations.

$$W_0 = \sqrt{\left[\frac{2\varepsilon_s \Phi}{q N_D}\right]} \approx x_{no} \quad \text{and} \quad x_{po} \approx 0$$

$$Q_0 = A\sqrt{2q\varepsilon_s \Phi N_D} \qquad (2.21)$$

$$C_{jo} = \varepsilon_s A \sqrt{\frac{q N_D}{2\varepsilon_s \Phi}}$$

These equations show that the scl penetrates mostly into the n-side, (hence the name one-sided), which supports most of the voltage.

Example 2.3: ***Space charge layer parameter values***

A 10μm thick p-type $2\text{x}10^{16}$ /cc silicon epitaxial layer is grown on an n^--type $1\text{x}10^{14}$ /cc silicon substrate, of area 1 cm^2, to form an abrupt pn junction.

Calculate the following PSpice parameter values, at room temperature:

- ***i.*** zero bias junction potential, Φ;
- ***ii.*** zero bias scl width, maximum electric field, charge, and junction capacitance, W_0, ξ_0, Q_0, C_{jo}; and
- ***iii.*** avalanche breakdown voltage, V_b.

If the substrate is 150μm thick, for a 1000V reverse bias, calculate:

- ***iv.*** scl width and penetration depth each side of the junction, W, x_n, x_p;
- ***v.*** charge each side of the junction, maximum electric field, and the capacitance, Q, ξ_0, C_j.

Solution

i. From equation (2.1), the zero bias built-in voltage is

$$\Phi = \frac{kT_j}{q} \ln \frac{N_A N_D}{n_i^2} = 0.0259 \ln \frac{2\times10^{16} \times 1\times10^{14}}{2.25\times10^{20}}$$
$$= 0.0259 \ln(8.89\times10^{0}) = 0.534\text{V}$$

ii. From equations (2.15), (2.20), (2.17), and (2.19)

$$W_0 = \sqrt{\left[\frac{2\Phi\,\varepsilon_s}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)\right]}$$

$$W_0 = \sqrt{\left[\frac{2\times0.53\times11.8\times8.85\times10^{-12}}{1.6\times10^{-19}}\left\{\frac{1}{2\times10^{22}} + \frac{1}{1\times10^{20}}\right\}\right]} = 2.65\,\mu\text{m}$$

$$\xi_0 = 2\ \Phi / W = 2\times0.534/2.65\mu\text{m}$$
$$\xi_0 = 0.40\ \text{MV/m}$$

$$Q_0 = A\left[2q\varepsilon_s \Phi \frac{N_D N_A}{N_D + N_A}\right]^{\frac{1}{2}}$$

$$Q_0 = 1\times10^{-4}\sqrt{2\times0.53\times1.6\times10^{-19}\times11.8\times8.85\times10^{-12}\ \frac{2\times10^{42}}{2.01\times10^{22}}} = 4.21\ \text{nC}$$

$$C_{jo} = A\left[\frac{q\varepsilon_s}{2\Phi} \frac{N_D N_A}{N_D + N_A}\right]^{\frac{1}{2}}$$

$$C_{jo} = 1\times10^{-4}\left[\frac{1.6\times10^{-19}\times11.8\times8.85\times10^{-12}}{2\times0.53} \frac{2\times10^{42}}{2.01\times10^{22}}\right]^{\frac{1}{2}} = 3.95\times10^{-9}\,\text{F} = 3.95\ \text{nF}$$

iii. From equation (2.2), the estimated punch-through voltage is

$$V_{PT} = 7.67\times10^{-16} N_c W_c^2 = 7.67\times10^{-16}\times10^{14}\times(150)^2 = 1727\text{V}$$

That is, punch through occurs when the reverse bias is greater than the operating voltage, 1000V. If the diode is to breakdown due to avalanche then the avalanche breakdown voltage given by V_b (equation (2.3)) must be less than V_{PT}, 1727V.

$$V_b = 5.34\times10^{13}\ N_c^{-2/7} = 5.34\times10^{13}\times(1\times10^{14})^{-2/7} = 1689\text{V}$$

iv. From equation (2.15) the scl width at -1000V reverse bias is

$$W = W_0\sqrt{1 - \frac{V}{\Phi}} = 2.65\mu\sqrt{1 + \frac{1000}{0.533}}$$
$$= 114.6\mu\text{m}$$

From equation (2.16) the scl penetration into each side of the junction at -1000V is

$$x_n = \frac{W}{1+N_D/N_A} = \frac{114.6}{1+0.005} \qquad x_p = \frac{W}{1+N_A/N_D} = \frac{114.6}{1+200}$$

$$x_n = 114.0\mu\text{m} \qquad x_p = 0.57\mu\text{m}$$

Note that when $N_A >> N_D$, $x_n \approx W$, thus the lower the relative concentration, the deeper the scl penetration and the higher the portion of V supported in N_D. The junction scl can under these circumstances be analysed based on simplified equations – called one-sided junction equations.

v. The charge magnitude each side of the junction, shown in figure 2.6, is given by equation (2.17). The electric field at the junction is given by equation (2.20), while the junction capacitance at -1000V is given by equation (2.19):

$$Q_j = Q_0\sqrt{1-\frac{V}{\Phi}} = 4.21\text{n}\sqrt{1+\frac{1000}{0.533}}$$

$$= 182{\cdot}4\,\text{nC}$$

$$\xi_j = \xi_0\sqrt{1-\frac{V}{\Phi}} = 0.40\text{M}\sqrt{1+\frac{1000}{0.533}}$$

$$\xi_j = 17.5\,\text{MV/m} \qquad \left(< \xi_b = 25\text{MV/m}\right)$$

$$C_j = C_{jo}\left(1-\frac{V}{\Phi}\right)^{-\frac{1}{2}} = 3.95\text{n}\left(1+\frac{1000}{0.533}\right)^{-\frac{1}{2}}$$

$$= 91\text{pF}$$

♣

Reading list

See chapter 1 reading list.

Fraser, D. A., *The Physics of Semiconductor Devices*, OUP, 1977.

Wolf, H. F., *Semiconductors*, John Wiley-Interscience, New York, 1977.

Yang, E. S., *Fundamentals of Semiconductor Devices*, McGraw-Hill, 1978.

Problems

2.1. A silicon diode is to have a breakdown voltage of 1000 V. If breakdown is due to the avalanche mechanism calculate
   i. the concentration of the n^- region
   ii. the width of the n^- region
   iii. the maximum electric field
   iv. the expected punch-through voltage based on parts i. and ii.
   [2×10^{14}/cc, 83µm, $2.4\text{x}10^5$ V/cm, 1057 V]

2.2. What is the punch-through voltage for a silicon step junction with an n^- doping level of $5\text{x}10^{13}$ /cc and a width of 20µm? Calculate the doping level and scl width for a similarly voltage rated silicon avalanche diode assuming equations (2.3) and (2.5) are valid.
   [15.3 V, $5.27\text{x}10^{16}$/cc, 0.63µm]

2.3. An abrupt silicon pn junction consists of a p-type region containing 10^{16} cm^{-3} acceptors and an n-type region containing $5\text{x}10^{14}$ cm^{-3} donors. Calculate
   i. the built-in potential of this p-n junction.
   ii. the total width of the scl region if the applied voltage V_a equals 0, 0.5 and -100 V.
   iii. maximum electric field in the scl region at 0, 0.5 and -100 V.
   iv. the potential across the scl region in the n-type semiconductor at 0, 0.5 and -100 V.

2.4. Consider an abrupt pn diode with $N_A = 10^{18}$ cm^{-3} and $N_D = 10^{16}$ cm^{-3}. Calculate the junction capacitance at zero bias if the diode area is 10^{-4} cm^2. Repeat the problem while treating the diode as a one-sided diode and calculate the relative error.

2.5. Repeat example 2.1 using the single-sided diode equations in equation (2.21), where $N_A >> N_D$. Calculate the percentage error in using the assumptions.

2.6. A silicon pn diode with $N_A = 10^{18}$ cm^3 has a capacitance of 10^{-7} F/cm^2 at an applied reverse voltage of 1V. Calculate the donor density N_D.

2.7. A silicon pn diode has a maximum electric field magnitude of 10^7 V/cm and a scl width of 200µm. The acceptor concentration is 100 times the donor density. Calculate each doping density.

2.8. Repeat example 2.1 for the equivalent 4H silicon carbide junction diode having the same electrical operating conditions. Use the silicon carbide data given below.

See problems 10.4, 10.5, and 10.9 to 10.12.
Useful *SI* data for silicon and silicon carbide:
$q = -1.6\text{x}10^{-19}$ C $\xi_0 = 8.85\text{x}10^{-12}$ F/m $\xi_{r\text{Si}} = 11.8$ $\xi_{r\text{SiC}} = 9.7$ $kT/q = 0.0259$ eV at 300ºC
$n_{i\text{Si}} = 1.5\text{x}10^{16}$ m^{-3} $n_{i\text{SiC}} = 2.5\text{x}10^{-3}$ m^{-3}