# 7

# Driving Transistors and Thyristors

The thyristor, being a multiple bipolar junction device, is essentially a current-controlled device. As illustrated in figure 7.la, a current must be supplied between the gate and cathode terminals to produce anode current flow, provided the anode is forward biased. The magnitude of gate drive current determines the delay time and the anode current rise time. In gate commutated thyristors, a negative gate current must be produced, the magnitude determining the turn-off delay time and anode current fall time.

The power MOSFET and IGBT are voltage controlled devices and are fundamentally different to bipolar devices. With the n-channel enhancement-mode power MOSFET and IGBT, a positive voltage must be applied between the gate and source terminals to produce a drain current, if the drain is positively biased with respect to the source, as shown in figure 7.lb. Generally the MOSFET and IGBT are easier to drive than the bipolar thyristor, and only a few basic considerations are required for MOSFET and IGBT gate circuit implementation.
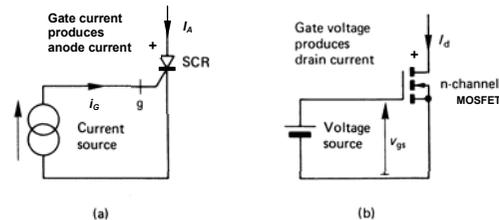


Figure 7.1. *Transistor and thyristor drive requirements:*
*(a) current drive for the bipolar junction thyristor and (b) voltage drive for the MOSFET and IGBT.*

**7.1        Application of the power MOSFET and IGBT**

The MOSFET gate is isolated electrically from the source by a layer of silicon dioxide. Theoretically no current flows into the gate when a dc voltage is applied to it. In practice, gate current is required to charge device capacitances and a small leakage current of the order of nano-amps does flow in order to maintain the gate voltage.

When no voltage is applied between the gate and source terminals, the drain-to-source impedance is very high and only a small leakage current of less than a milli-amp flows in the drain, until the applied voltage exceeds the drain-to-source avalanche voltage, $V_{DSS}$.

When a positive gate voltage is applied, an electric field is produced which modulates the drain-to-source resistance. When a gate voltage exceeds the threshold voltage level the channel resistance reduces to a low resistance and drain current flows. The maximum drain current depends on the gate voltage magnitude, assuming that the impedance of the external drain circuit is not current-limiting.

Turnoff - reducing the drain current to the leakage level - is achieved by reducing the gate voltage to below the gate threshold voltage level. The drain switching speeds are essentially determined by that speed at which the gate voltage can reach a level above the threshold voltage (for turn-on) or below the threshold voltage (for turn-off). Although the gate-to-source capacitance is an important parameter, the gate-to-drain capacitance is more significant because of the Miller effect, as considered in section 4.4.2. During switching the dynamic gate-to-drain capacitance can be effectively much larger than the gate-to-source capacitance. The Miller capacitance typically requires more charge for switching than the gate-to-source capacitance.

*7.1.1        Gate drive circuits*

The n-channel enhancement-mode power MOSFET (or IGBT) with a low threshold voltage interfaces easily with logic level integrated circuits. This allows low-power digital logic circuits to control directly high-power levels. Figure 7.2 shows a series of ttl and cmos circuits driving power MOSFETs, each circuit offering different levels of switching speed and performance.

When driving a MOSFET directly from a cmos gate output, as shown in figure 7.2a, only modest rise and fall times can be expected because of the limited source and sink current available from a cmos gate. Figure 7.3a illustrates the output configuration of a typical cmos output stage, which consists of a series-connected p and n-channel MOSFET with the gates connected together. The cmos totem pole output stage is driven by a common signal, hence the name complementary mos - cmos - and when the input is high the n-channel device is on and the p-channel off, while when the input is low, the p-channel turns on and the n-channel turns off. However, cmos has a limited current output capability as shown in the source-to-sink output characteristics in figure 7.3b and c. The cmos gate output has to drive as a load the power MOSFET capacitive

gate. In this configuration, the turn-on current is supplied from the p-channel fet, which has the poorer characteristics of the cmos pair. The turn-off current is sunk by the n-channel fet. Table 7.1 shows cmos typical current source and sink capabilities, switching speeds, and output impedance. It will be seen that the best performance, by far, is achieved from the 4049 and 4050 buffers.
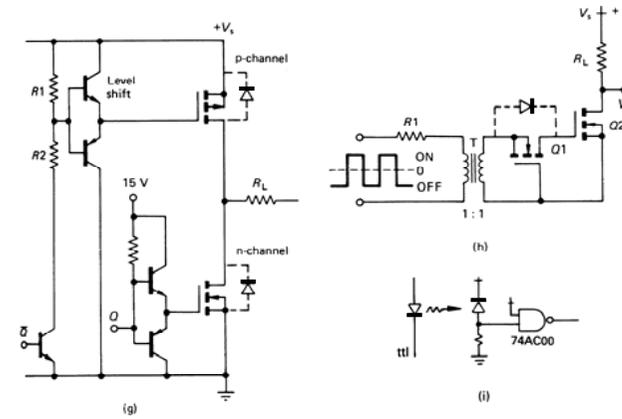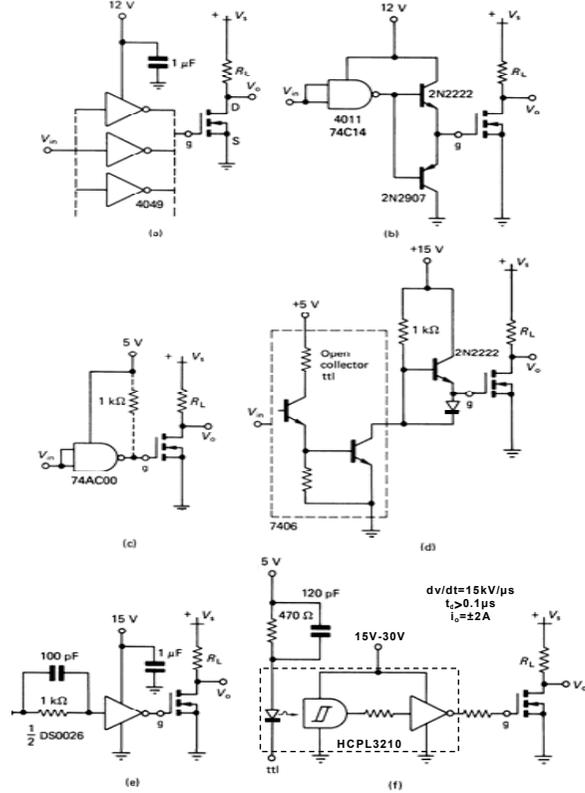
Figure 7.2.  *Gate drive circuits for the MOSFET and IGBT:*
*(a) driven from cmos; (b) driven from cmos and an emitter follower;*
*(c) driven from ttl with pull-up resistor which increases sourcing capability;*
*(d) driven from open collector ttl with an external current source;*
*(e) driven from a high-current cmos clock driver; (f) opto-isolated driver circuit;*
*(g) drive circuits for a totem pole connected p and n-channel MOSFET leg;*
*(h) driven from a pulse transformer; and (i) fibre optic translation stage.*

If shorter delays and faster drain rise and fall times are required there are several ways to obtain them. The simplest is to parallel a number of identical cmos inputs and outputs as shown dotted in figure 7.2a. The additional current capability, with the six parallel connected gates of the 4049, will significantly improve MOSFET switching performance.

In figure 7.2b the gate drive current is the output current of the cmos gate multiplied by the gain $\beta$ of the bipolar transistors. No bipolar saturation times are incurred since the transistors are operating as emitter followers, which cannot saturate. The operating frequency is no longer restricted by the cmos output current limitations.

MOSFETs can also be driven directly from ttl gates. Table 7.2 shows ttl typical current source and sink capabilities and switching speeds. Low supply voltage, typically 5V, and high internal sourcing impedance characteristics, restrict MOSFET switch-on speed and gate voltage level. The ttl sink capability is significantly higher than source capability, hence a pull-up resistor as shown in figure 7.2c enables the sinking

capability to be exploited at turn-on, as well as at turn off. A limitation of using ttl for driving MOSFETs is that the gate voltage is restricted to less than 5V, hence if the drain current is not to be restricted, low gate threshold voltage trench gate MOSFETs and IGBTs are used. An open collector ttl drive technique as shown in figure 7.2d overcomes the gate voltage limitation as well as improving the current source limit.
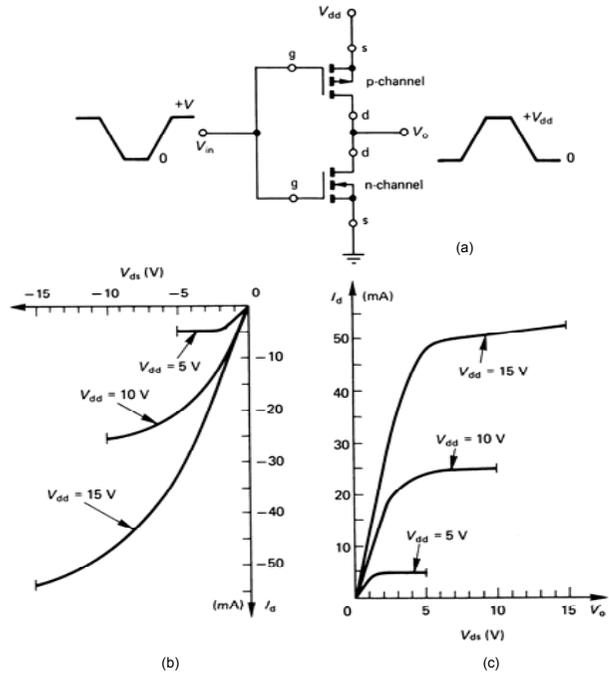


Figure 7.3. CMOS inverter output: (a) output cmos totem pole; (b) p-channel drain sourcing; and (b) n-channel drain sinking, both at 25°C.

Table 7.1  Driving mosfets from cmos (buffered)

| Logic conditions | Standard buffered outputs at logic supply voltage ($V_{dd}$) of | | | 4049/4050 drivers at logic supply voltage ($V_{dd}$) of | | |
|---|---|---|---|---|---|---|
| | 5 V | 10 V | 15 V | 5 V | 10 V | 15 V |
| **Logic zero** | | | | | | |
| Approximate sink current $I_{OL}$ (mA) for $V_{OL} \leq 1.5$ V | 1.5 | 3.5 | 4.0 | 20 | 40 | 40 |
| **Logic one** | | | | | | |
| Minimum source current $I_{OH}$ (mA) for $V_{OH}$ | −0.51 ≥4.6 V | −1.3 ≥9.5 V | −3.4 ≥13.5 V | −1.25 ≥2.5 V | −1.25 ≥9.5 V | −3.75 ≥13.5 V |
| **Typical switching times (ns) of logic drive signals:** | | | | | | |
| Rise | 100 | 50 | 40 | 100 | 50 | 40 |
| Fall | 100 | 50 | 40 | 40 | 20 | 15 |
| $R_{ds(on)}$ (ohms) (calculated) Source  Typ. | 1.7k | 500 | 430 | | | |
| Source  Max. | 12.5k | 2.5k | – | | | |
| Sink  Typ. | 500 | 420 | 190 | | | |
| Sink  Max. | 2k | 1k | – | | | |

Table 7.2 Driving mosfets from TTL

| Logic conditions | Logic type | | | | | | | | Open collector 74, 30 V |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| | 74 | 74AC | 74L | 74LS | 74S | 74ALS | 74HC | DS0026 | |
| **Logic zero** Min. sink current $I_{OL}$ for $V_{OL}$ = 0.4 V (mA) | 16 | 24 | 3.6 | 8 | 20 | 18 | 4 | 1.5A | 40 |
| **Logic one** Max. source current $I_{OH}$ for $V_{OH}$ = 2.4 V (mA) | −0.4 | −24 | −0.2 | −0.4 | −1.0 | −0.4 | −4 | −1.5A | 22 |
| Typical gate propagation delay (ns) | 10 | 7 | 50 | 12 | 4 | 4 | 10 | 15 | 12 |
| $V_{IL}$ max. (V) | 0.8 | 1.35 | 0.7 | 0.8 | 0.8 | 0.8 | 0.9 | — | 0.8 |
| $V_{IH}$ min. (V) | 2.0 | 3.15 | 2.0 | 2.0 | 2.0 | 2.0 | 3.15 | — | 2.0 |

Very fast switching speeds are attained with the capacitive driver shown in figure 7.2e. Such drivers can both source and sink typically 1.5 A in tens of nanoseconds. An isolated gate-to-source drive version is shown in figure 7.2f, where a floating 15 V rail is used and the gate control signal is optically transmitted with high *dv/dt* capability. The driver incorporates high current output, with modest propagation delays.

Drive circuits for p-channel MOSFETs may be complicated by the reference signal voltage level, as shown in the series n and p-channel totem pole in figure 7.2g. This figure illustrates how the p-channel drive may be derived by means of a level shifter. The emitter follower, pnp transistor used for turn-on must have a breakdown voltage rating in excess of the totem pole rail voltage. Above 300 V the pnp transistor can be replaced by a diode as shown in figure 7.2d, or a low current high voltage MOSFET. Restricted charging of the translation MOSFET output capacitance can lead to increased delay times. The resistor divider, *R1-R2,* ensures that the p-channel gate voltage limit is not exceeded. In order to increase gate drive capability *R2* can be decreased provided a 15 V Zener is used across the p-channel MOSFET gate to source. The low-voltage npn transistor in the p-channel driver stage is used for fast turn-off, shorting the p-channel source to its gate.

A simple method of driving an n-channel MOSFET, with its source not referenced to ground, is shown in figure 7.2h. Electrical (galvanic) isolation is achieved by means of a pulse transformer. The internal parasitic diode in Q1 provides the path for the n-channel MOSFET gate to charge. When the pulse transformer saturates, Q1 blocks any discharge of the gate until turn-off, when a negative transformer pulse turns on Q1, thereby discharging the n-channel gate charge.

An alternative translation method using a fibre optic stage is shown in figure 7.2i. The temperature-independent, high threshold characteristics of 74AC technology is used for a simple detector comparator. A Schmitt input (hysteresis) gate improves noise immunity. Translation from ttl levels can be achieved with Zener diode bias circuits.

From the circuits in figure 7.2 it is seen that there are two basic types of gate drives.

- Low-side
- High-side

Essentially a low-side driver is one where the control signal and the power device gate are at almost the same potential. The lower switches in bridge legs usually use a low-side driver, while the upper switches require high-side drivers which translate the control signal to a different potential. The gate drive circuits 7.2a to 7.2e are basic low-side gate drive circuits. The high-side drivers in figures 7.2f to 7.2i translate the control signal to the gate level.

Although the gate drive circuits in figures 7.2a to 7.2i translate the control signal to the device gate, these circuits do not address two important gate drive issues.

- The derivation of the gate drive supply, particularly for floating gate drives as encountered in inverters.
- The derivation of negative gate bias at turn-off for better immunity to false turn-on due to noise and induced Miller charging effects.

**7.1.1i -** *Negative gate drive*

The gate drive circuits shown in figure 7.2 only clamp the gate to near zero volts during the off period.

The lower bridge leg switch in figure 7.4 uses ±15V gate voltage. The complementary buffers drive the gate-source of the shown device in an H-bridge configuration. The buffers require an isolated 15V dc supply. Practically a negative gate bias of -5V is sufficient for noise immunity while any voltage in excess of this unnecessarily increases turn-on delay and increases gate power requirements. Manufacturers are continually improving power device properties and characteristics. Gate threshold voltage levels are constantly being decreased, and coupled with the fact that the threshold voltage decreases with temperature, negative voltage gate drive is necessary for high noise immunity to prevent false turn-on with high power devices.
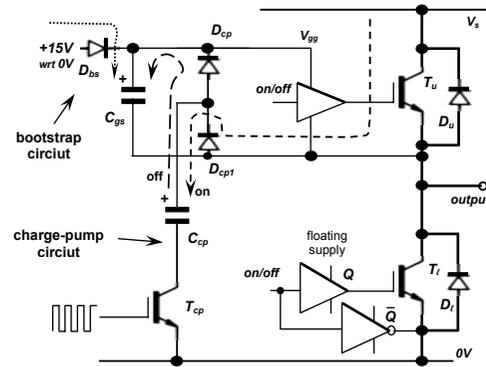


Figure 7.4. *Typical IGBT bridge leg showing ±15V gate drive on the leg lower switch and charge pump plus boot strap gate supply circuits for the leg upper switch.*

**7.1.1ii -** *Floating power supplies*

There are three basic methods for deriving floating power supplies for gate drives.
- A low inter-winding capacitance, high-frequency transformer
- A capacitive coupled charge pump
- A diode bootstrap

The upper bridge leg switch $T_u$ in figure 7.4 uses both a diode bootstrap via $D_{bs}$ and capacitor charge pumping via $C_{cp}$, in order to derive gate power.

*1 - capacitive coupled charge pump*

By switching $T_{cp}$ at high frequency the low capacitance capacitor $C_{cp}$ is successively charged through $D_{cp1}$ and discharged through $D_{cp}$. Discharge through $D_{cp}$ involves charging $C_{gs}$, the gate voltage supply capacitor. The shown charge and discharge paths both rely on either the upper switch $T_u$ or diode $D_u$ being in a conducting state.

*2 - diode bootstrap*

When the lower switch $T_\ell$ or diode $D_\ell$ conduct, diode $D_{bs}$ allows the upper gate supply capacitor $C_{gs}$ to charge from a 15V supply which is referenced to the 0V rail. When the upper switch or diode conduct, the bootstrap diode is reverse bias and supports $V_s$. Start-up is a problem since the gate of the upper switch $T_u$ is in a high impedance state while its supply is being charged after the lower switch is turned on. For this reason, the boot strap is usually used in conjunction with a capacitor charge pump.

The only foolproof method to ensure gate power at all times, particularly at start-up and during prolong on-state periods, is to use a high-frequency transformer approach.

**7.1.2    Gate drive design**

The effective gate to source capacitance, $C_{in}$, can be calculated from

$$C_{in} \triangleq \delta Q_g / \delta V_{gs} \qquad (7.1)$$

The initial slope of the charge in figure 7.5a, 740 pF, is due to the gate source capacitance charging below the gate threshold level. The next section between $Q_{g1}$ and $Q_{g2}$ in figure 7.5c is due to the Miller effect. The horizontal charge portion is due to the very high drain-source depletion field capacitance as the drain falls below the gate voltage level.

The drain switching times, similar to those derived in 4.4.2, can be calculated from the charge transfer characteristics in figure 7.5, using the following equations.

(i)     From figure 7.5c

$$t_{d\,on} = \frac{Q_{g1}}{V_{g1}} R_g \; \ell n \left( \frac{V_{gg}}{V_{gg} - V_{g1}} \right) \qquad (s) \qquad (7.2)$$

$$t_r = \frac{Q_{g2} - Q_{g1}}{V_{g2} - V_{g1}} R_g \; \ell n \left( \frac{V_{gg} - V_{g1}}{V_{gg} - V_{g2}} \right) \qquad (s) \qquad (7.3)$$

(ii)    From figure 7.5d

$$t_{d\,off} = \frac{Q_{g2} - Q_{g2}}{V_{g2} - V_{g2}} R_g \; \ell n \; \frac{V_{gg}}{V_{g2}} \qquad (s) \qquad (7.4)$$

$$t_f = \frac{Q_{g2} - Q_{g1}}{V_{g2} - V_{g1}} R_g \; \ell n \; \frac{V_{g2}}{V_{g1}} \qquad (s) \qquad (7.5)$$

where $R_g$ is the gate equivalent resistance and $V_{g1} = V_{TH}$.
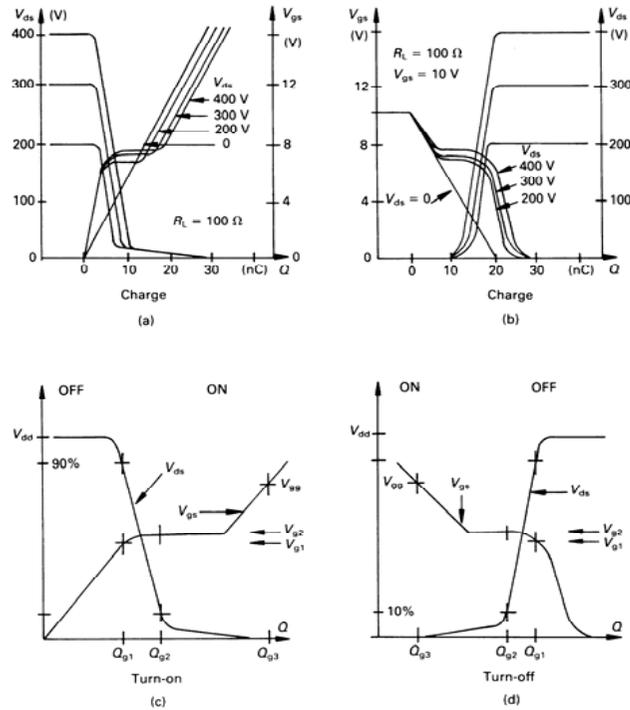
Figure 7.5. *Typical MOSFET charge transfer characteristics at:*
*(a) turn-on; (b) turn-off; (c) turn-on showing switching parameters; and*
*(d) turn-off showing switching parameters.*

The energy required for switching is given by

$$W = \tfrac{1}{2}Q_{g3}V_{gg} \qquad \text{(J)} \qquad\qquad (7.6)$$

which will be dependent on the drain current and voltage. The gate drive power requirements are given by

$$P = Q_{gs}\,V_{g3}\,f_s \qquad \text{(W)} \qquad\qquad (7.7)$$

Obviously the faster the switching speed requirement, the higher and faster the gate drive current delivery necessary.

If only 15 mA is available for gate drive then, based on figure 7.5, switching occurs in about 1 μs. This level of performance could be expected with circuit 7.2a, and longer switching for the circuit in figure 7.2c. By employing the gate drive in figure 7.2c, the gate voltage is limited to 5 V, hence the MOSFET represented by figure 7.5 could not be switched.

The circuits in figures 7.2b and 7.2d are capable of delivering about 100 mA, which yields switching speeds of the order of 150 ns, with only 50 mW of drive power dissipation at 100 kHz. The drive circuit in figure 7.2e is capable of delivering ± 1.5 A. Hence the device characterised by figure 7.5 can be switched in only 10 ns.

Switching times deteriorate slightly if reverse gate-to-source biasing is used for higher noise immunity in the off-state. Analysis of the increase in turn-on delay as a result of the use of negative gate drive is presented in Appendix 4.1.

**Example 7.1:**    *MOSFET input capacitance and switching times*
A MOSFET switching a resistive load has the following circuit parameters:

$$R_g = 47\Omega, \qquad R_L = 100\Omega$$
$$V_{gg} = 10 \text{ V}, \qquad V_{ds} = 400 \text{ V}$$

Based on the charge transfer characteristics in figure 7.5, calculate the gate input capacitance and switching times for MOSFET turn-on and turn-off.

*Solution*
The charge transfer characteristics shown in figure 7.5 are valid for 100 Ω resistive load and a 0-10 V gate voltage. A 400 V drain switching characteristic is shown.
At turn-on, from figure 7.5a and using equations (7.2) and (7.3)

(i)    $C_{in} = C_{gs} = Q_{g1}/V_{g1} = 4.4$ nC/6V = 740 pF
     $t_{d\,on} = 740$ pF × 47Ω $\ell n$ (10V/10V-6V) = 31.9 ns

(ii)    $C_{in} = (Q_{g2} - Q_{g1})/(V_{g2} - V_{g1}) = 5.6$ nC/1.5V = 3.7 nF
     $t_r = 3.7$ nF × 47Ω $\ell n$ 5.6/2.5 = 141.3 ns

At turn-off, from figure 7.5b and using equations (7.4) and (7.5)

(i)    $C_{in} = (Q_{g3} - Q_{g2})/(V_{gg} - V_{g2}) = 7.5$ nC/2.5V = 3 nF
     $t_{d\,off} = 3$ nF × 47Ω $\ell n$ 10V/7.5V = 40 ns

(ii)    $C_{in} = (Q_{g2} - Q_{g1})/(V_{g2} - V_{g1}) = 7.5$ nC/0.9V = 8.3 nF
     $t_f = 8.33$ nF × 47Ω $\ell n$ 7.5/6.6 = 50 ns

An underestimate of the fall time results if figure 7.5a is used for all calculations $(C_{in} = 3.7$ nF and $t_f = 39.1$ ns).

♣

## 7.2    Application of the Thyristor

The basic gate requirements to trigger a thyristor into the conduction state are that the current supplied to the gate is

- of adequate amplitude and sufficiently short rise time
- of sufficient duration.

The gate conditions are subject to the anode being forward-biased with respect to the cathode. Figure 7.6 illustrates a typical thyristor gate current waveform for turn-on.
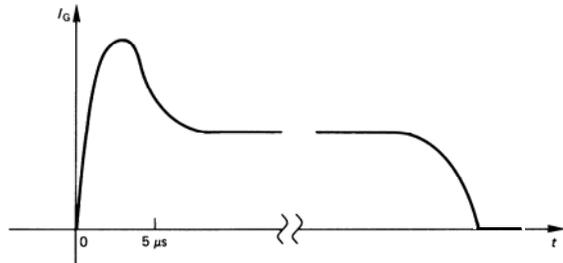


Figure 7.6.  *Ideal thyristor gate current waveform for turn-on.*

The initial high and rapid current quickly turns on the device so as to increase the anode initial *di/dt* capability. After a few microseconds the gate current can be decreased to a value in excess of the minimum gate requirement. After the thyristor has latched on, the gate drive may be removed in order to reduce gate power consumption, namely the losses. In some inductive load applications, where the load current lags, a continuous train of gate pulses is usually applied to ensure turn-on.
Gate drives can be divided broadly into two types, either electrically isolated or non-isolated. To obtain electrical isolation usually involves the use of a pulse-transformer or an opto-coupler but above a few kilovolts fibre-optic techniques are applicable.
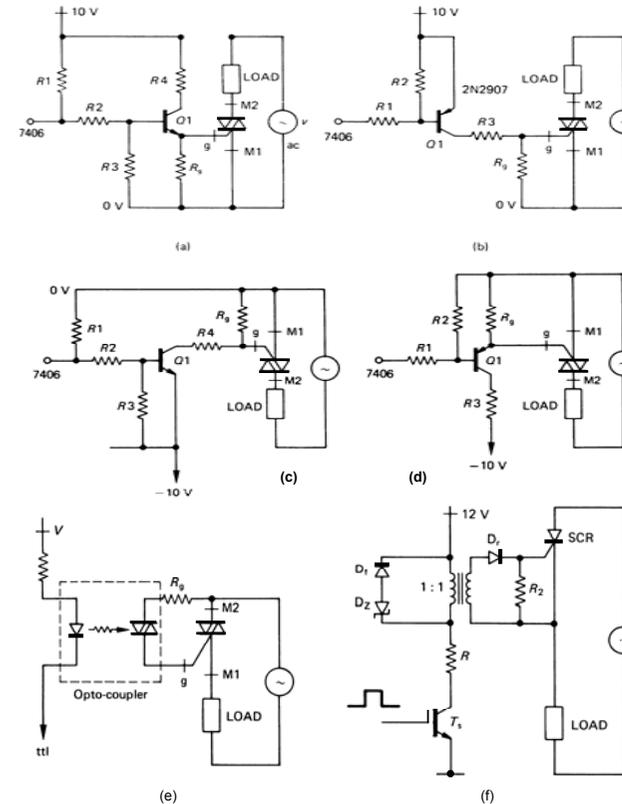
Figure 7.7.  *Integrated circuit compatible triac gate drive circuits:*
*(a) high level ttl activation;(b) low level ttl activation using an interfacing pnp transistor; (c) negative gate drive interface with high ttl output for triac activation;(d) negative gate drive interface with low ttl level for triac turn-on;*
*(e) a triac opto-coupler isolated gate drive used to gate-drive a higher power triac and (f) a pulse transformer drive isolated gate drive for a thyristor.*

### 7.2.1 Thyristor gate drive circuits

Only low-power thyristors with amplifying gates can be triggered directly from ttl or cmos. Usually a power interface stage is employed to convert ttl current sink and source levels of a few milliamps up to the required gate power levels.

Figure 7.7a and b shows two power interface circuits for triggering a triac. The triac could equally be another thyristor device. An important safety default feature of both these circuits is that no active device exists between the gate and Ml. During the off-state the gate is clamped by the resistor $R_g$ to a voltage well below the minimum voltage level for turn-on.

Bidirectional gate current can bring the triac into conduction. Figure 7.7c and d show how negative gate turn-on current can be derived.

If electrical isolation between the control circuitry and the thyristor circuit is required, a simple triac opto-coupler can be employed as shown in figure 7.7e. The photo-triac is optically turned on which allows bidirectional main triac gate current to flow, the magnitude of which is controlled by the resistor $R_g$. If the main device is an scr, an opto-coupled scr can be used for isolation and uni-direction gate triggering current.

When suitable voltage rails are not available or isolation is required, a pulse transformer drive circuit can be employed as shown in figure 7.7f. The diode/Zener diode series combination across the pulse transformer primary provides a path for primary magnetising current decay at turn-off and prevents saturation. The resistor $R$ limits the secondary current into the scr gate. This resistor can be placed in the pulse transformer primary or secondary by transforming the resistance in the turns ratio squared. If $R$ is in the primary circuit and transformer saturation inadvertently occurs, the resistor $R$ limits the current and protects the switching transistor $T_s$. The transformer secondary resistor $R_2$ is employed to decrease the gate to cathode impedance, thereby improving $dv/dt$ capability, while the gate diode $D_r$ prevents possible reverse gate voltage breakdown after $T_s$ is turned off and the output voltage reverses during core reset. The transformer duty cycle must satisfy $t_{off} V_z \geq t_{on} V_s$, neglecting $R$.

### 7.2.2 Thyristor gate drive design

In order to design a gate interface circuit, both the logic and thyristor gate requirements must be specified.

Consider interfacing a typical ttl-compatible microprocessor peripheral which offers the following specification

$$I_{OH} = 0.3\text{mA} \ @ \ V_{OH} = 2.4\text{V}$$
$$I_{OL} = 1.8\text{mA} \ @ \ V_{OL} = 0.4\text{V}$$
$$V_{cc} = 5\text{V}$$
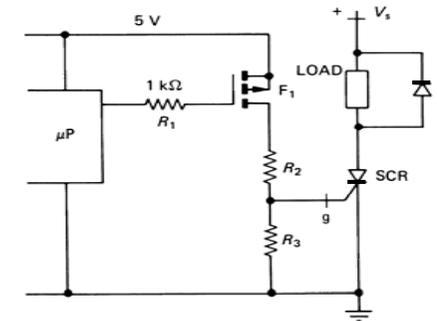
Figure 7.8. *Interfacing a microprocessor to a power thyristor.*

These specifications are inadequate for turning on a power thyristor or an optical interfacing device. If the power thyristor gate, worst case requirements are

$$I_{GT} = 75 \text{ mA}, V_{GT} = 3 \text{ V} \ @ \ -65°C$$

then a power interfacing circuit is necessary. Figure 7.8 shows an interfacing circuit utilising a p-channel MOSFET with the following characteristics

$$C_{gs} = 400 \text{ pf}$$
$$V_{TH} = 3.0\text{V}$$
$$R_{ds(on)} = 10 \text{ ohms}$$
$$I_d = 0.5\text{A}$$

The resistor $R_l$ limits the MOSFET $C_{gs}$ capacitance-charging current and also specifies the MOSFET turn-on time. If the charging current is to be limited to 1.8 mA when $V_{OL} = 0.4$ V, then

$$R_1 = (V_{cc} - V_{OL})/I_{OL} \quad \text{(ohms)}$$
$$= (5\text{V} - 0.4\text{V})/1.8\text{mA} = 2.7 \text{ kilohms}$$

A smaller resistance could be used but this would not preserve the microprocessor low-voltage output level integrity if it were being used as input to ttl logic. The MOSFET will not turn on until $C_{gs}$ has charged to 3 V or, with a 5 V rail, approximately one $R$-$C$ time constant. That is

$$t_{delay} = R_l C_{gs} \quad \text{(s)}$$
$$= 2.7 \text{ kilohms} \times 400 \text{ pF} = 1 \text{ μs}$$

The MOSFET must provide the thyristor gate current and the current through resistor $R_3$ when the gate is at 3 V.

The maximum value of resistor $R_2$ is when $R_3 = \infty$ and is given by

$$R_2 = \frac{V_{cc} - V_{GT} - I_{GT} \times R_{ds(on)}}{I_{GT}}$$

$$= \frac{5V - 3V - 75\text{ mA} \times 10\Omega}{75\text{ mA}} = 16.6 \text{ ohms}$$

Use $R_2 = 10$ ohms.

The resistor $R_3$ provides a low cathode-to-cathode impedance in the off-state, thus improving scr noise immunity. When $V_{GT} = 3$ V

$$I_d = \frac{V_{cc} - V_{GT}}{R_{ds(on)} + R_2} \qquad \text{(A)}$$

$$= \frac{5V - 3V}{10\Omega + 10\Omega} = 100\text{ mA}$$

of which 75 mA must flow into the gate, while 25 mA can flow through $R_3$. That is

$$R_3 = V_{GT} / (I_d - I_{GT}) \qquad \text{(ohms)}$$

$$= 3\text{ V}/25\text{ mA} = 120 \text{ ohms}$$

After turn-on the gate voltage will be about 1 V, hence the MOSFET current will be 200 mA. Assuming 100 per cent on-state duty cycle, the $I^2R$ power loss in the MOSFET and resistor $R_2$ will each be 0.4 W. A 1 W power dissipation 10 ohm resistor should be used for $R_2$.

**Example 7.2:** *A light dimmer*

A diac with a breakdown voltage of ±30 V is used in a light dimming circuit as shown in figure 7.9. If $R$ is variable from 1 kΩ to 22 kΩ and $C = 47$ nF, what are the maximum and minimum firing delays? What is the controllable output power range with a 10Ω load resistor?
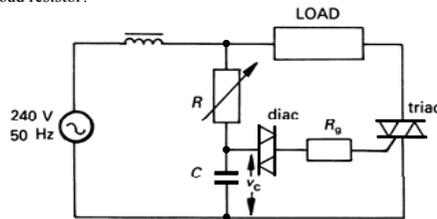


Figure 7.9. *Light dimmer*.

**Solution**

The capacitor voltage $v_c$ is given by

$$v_c = \frac{-j/\omega C}{R - j/\omega C} \times 240\angle 0°$$

$$= \frac{1}{1 + j\omega CR} \times 240\angle 0°$$

i. For $R = 1$ kΩ
$v_c = 237.36 \angle -8.4°$
that is, $v_c = 335.8 \sin(\omega t - 8.4°)$
The diac conducts when $v_c = 30$V, that is
minimum delay $= \omega t = 8.4° + \sin^{-1}(30\text{V}/335.8\text{V}) = 13.5°$

ii. For $R = 22$ kΩ
$v_c = 70.6 \angle -72.8°$
that is, $v_c = 99.8.8 \sin(\omega t - 72.8°)$
The diac conducts when $v_c = 30$V, that is
minimum delay $= \omega t = 72.8° + \sin^{-1}(30\text{V}/99.8\text{V}) = 92°$

From equation (12.14), the output power for a resistive load is given by

$$P_o = \frac{V_{rms}^2}{R} = \frac{V^2}{R}\left\{1 - \frac{2\alpha - \sin 2\alpha}{2\pi}\right\} \qquad \text{(W)}$$

Minimum power at $\alpha = 92°$ (1.6 rad) is $P_o = \frac{240^2}{10\Omega} \times \left\{1 - \frac{2\times 92° - \sin 2\times 92°}{2\pi}\right\} = 2862\text{W}$

Maximum power at $\alpha = 13\frac{1}{2}°$ (0.24 rad) is $P_o = \frac{240^2}{10\Omega} \times \left\{1 - \frac{2\times 13\frac{1}{2}° - \sin 2\times 13\frac{1}{2}°}{2\pi}\right\} = 5536\text{W}$

♣

**7.3 Drive design for GTO thyristors**

The gate turn-off thyristor is not only turned on from the gate but, as its name implies, is turned off from its gate with negative gate current. Basic GTO thyristor gate current requirements are very similar to those for the power bipolar transistor (now virtually obsolete) when reverse base current is used for fast turn-off.

Figure 7.10 shows a gate drive circuit for a GTO thyristor which is similar to that historically used for power bipolar junction transistor base drives. The inductor $L$, in figure 7.10, is the key turn-off component since it controls the *di/dt* of the reverse gate current. The smaller the value of $L$, the larger is the reverse *di/dt* and the shorter the turn-off time. But with a shorter turn-off time the turn-off gain decreases, eventually to unity. That is, if the GTO thyristor is switched off rapidly, the reverse gate current must be of the same magnitude as the anode current to be extinguished. A slowly applied

reverse gate current *di/dt* can produce a turn-off gain of over 20 but at the expense of increased turn-off switching losses. For the GTO thyristor $L$ is finite to get a turn-off gain of more than one, while to achieve unity gain turn-off for the GCT, $L$ is minimised. The GTO thyristor cathode-to-gate breakdown voltage rating $V_{RGM}$ specifies the maximum negative rail voltage level. A level of 15-20V is common, and for supply rail simplicity a $\pm$ 15 V rail may be selected.

Resistor $R_4$ limits the base current of $T_t$. If an open collector ttl driver is employed, the current through $R_4$ is given by

$$I_{OL} = (V_{cc} - V_{beT_t} - V_{Db} - V_{OL})/R_4 \qquad \text{(A)}$$
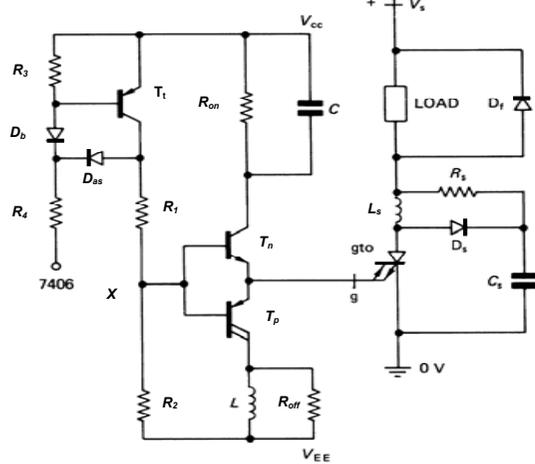


Figure 7.10. *Gate drive circuit and anode snubber circuits for a GTO thyristor.*

For open collector 74 ttl series, $I_{OL} = 40$ mA when $V_{OL}$ - 0.5 V and therefore $R_4$ can be specified. The resistor $R_3$ speeds up turn-off of $T_t$. It is as large as possible to ensure that minimal base current is diverted from $T_t$. Diodes $D_b$ and $D_{as}$ form a Baker's clamp, preventing $T_t$ from saturating thereby minimising its turn-off delay time.

The two driver transistor $T_n$ and $T_p$ should
- have high gains
- be fast switching
- have collector voltage ratings in excess of $V_{cc} + V_{EE}$.

The GTO thyristor gate turn-on current is determined by resistor $R_{on}$, which is specified by

$$R_{on} = \frac{V_{cc} - V_{ceT_n} - V_{GC}}{I_G} \qquad \text{(Ohms)}$$

The power rating of $R_{on}$ is given by

$$P_{R_{on}} = \delta(V_{cc} - V_{ceT_n} - V_{GC})I_G \qquad \text{(W)}$$

where $\delta$ is the maximum on-state duty cycle. The capacitor $C_{on}$, in parallel with $R_{on}$, provides a short current boost at turn-on, thereby speeding up turn-on, increasing turn-on initial *di/dt* capability, and reducing turn-on losses.

The series resistors $R_1$ and $R_2$ bias the bases of the totem pole level shift driver and, for an on-condition, the potential of point X in figure 7.10 is given by

$$V_X = V_{beT_n} + V_{GC} \qquad \text{(V)}$$

The total current flow through $R_1$ is made up of the transistor $T_n$ base current and that current flowing through $R_2$, that is

$$I_{R1} = \frac{I_G}{\beta_{T_n}} + \frac{V_X + V_{EE}}{R_2} \qquad \text{(A)}$$

from which

$$R_1 = (V_{cc} - V_X)/I_{R1} \qquad \text{(ohms)}$$

The power rating of $R_1$ is

$$P_{R_1} = \delta(V_{cc} - V_X)I_{R_1} \qquad \text{(W)}$$

For fast turn-off, if the reverse gate current at turn-off is to be of the same magnitude as the maximum anode current, then $R_2$ must allow sufficient base current to drive $T_p$. That is

$$R_2 = \frac{V_X + V_{beT_p}}{I_c / \beta\beta_p} \qquad \text{(ohms)}$$

Once the gate-to-cathode junction of the GTO has recovered, the reverse gate current falls to the leakage level. The power rating of $R_2$ can be low at lower switching frequencies.

The small inductor $L$ in the turn-off circuit is of the order of microhenrys and it limits the rate of rise of reverse gate current, while $R_{off}$ damps any inductor current oscillation. The turn-on and turn-off BJT circuits can be replaced by a suitable n-channel MOSFET circuit in high power GTO and GCT applications. In high power IGCT applications, MOSFET and rail decoupling electrolytic capacitors are extensively parallel connected. Typically 21 capacitors and 42 MOSFETs are parallel connected to provide a low impedance path for anode current extraction from the GCT gate. The gate inductance (including the GCT internal package inductance) is minimised, whence $L$ is zero.

**Table 7.3 Gate drive isolation technique summary**

| Technique | data transfer | power transfer | comments |
|---|---|---|---|
| Transformer | direct signal coupling | direct magnetic transfer | duty cycle limited corona breakdown limit |
| optocoupler | slow, with capacitive effects | n/a | voltage and *dv/dt* limit |
| fibre optics | fast, virtually no voltage limit | n/a | best signal transmission at MV and HV |
| charge couple | n/a | requires switching | induced effects between ground level and gate level, LV application |
| bootstrap | n/a | requires switching | |

**Reading list**

International Rectifier, *HEXFET Data Book,*
        HDB-5, 1987.

Peter, J. M., *The Power Transistor in its Environment,*
        Thomson-CSF, Sescosem, 1978.

Siliconix Inc., *Mospower Design Catalog,*
         January 1983.

Graffiam, D. R. *et al., SCR Manual,*
        General Electric Company, 6th Edition, 1979.

**Problems**

7.1.     Calculate suitable resistor values for the triac gate drive circuit in figure 7.7a, assuming a minimum gate current requirement of 50 mA and the gain of Q1 is 50 at 50 mA.

7.2.     Repeat problem 7.1 for the circuits in figures
    - 7.7b
    - 7.7c
    - 7.7d.