ELEC-E3540 Digital Microelectronics II L

Brief Modelsim tutorial

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February 2016

1   Brief Modelsim tutorial

1.1   Introduction

This tutorial will give you a quick introduction to Mentor Graphics' Modelsim HDL simulator. You will learn how to start the software, create a new work library, compile your VHDL files and testbench, and run a simulation.

In order to access the Modelsim software, you must be connected to VSPACE server. The instructions to setup the connection can be found from MyCourses.

1.2   Creating the directory tree

After you have successfully connected to VSPACE, create a directory tree for this course, in order to keep your files in order. Open a terminal, and use commands `mkdir` and `cd` to create and move through directories, respectively. The directory tree should look like this:

- **ELEC-E3540** *(course directory)*

    - **exercise1** *(exercise directory)*
        * **vhdl** *(save VHDL files here)*
        * **simulations** *(run simulations here)*
    - **exercise2**
    - **exercise3**
    - ...

1.3   Starting the software

Follow these steps to start the Modelsim software.

1. Open a terminal and navigate to the **simulations** directory.

2. Set the required environment variables by writing to the console: `use advms_15.3`

3. Start the Modelsim software by typing: `qhsim`
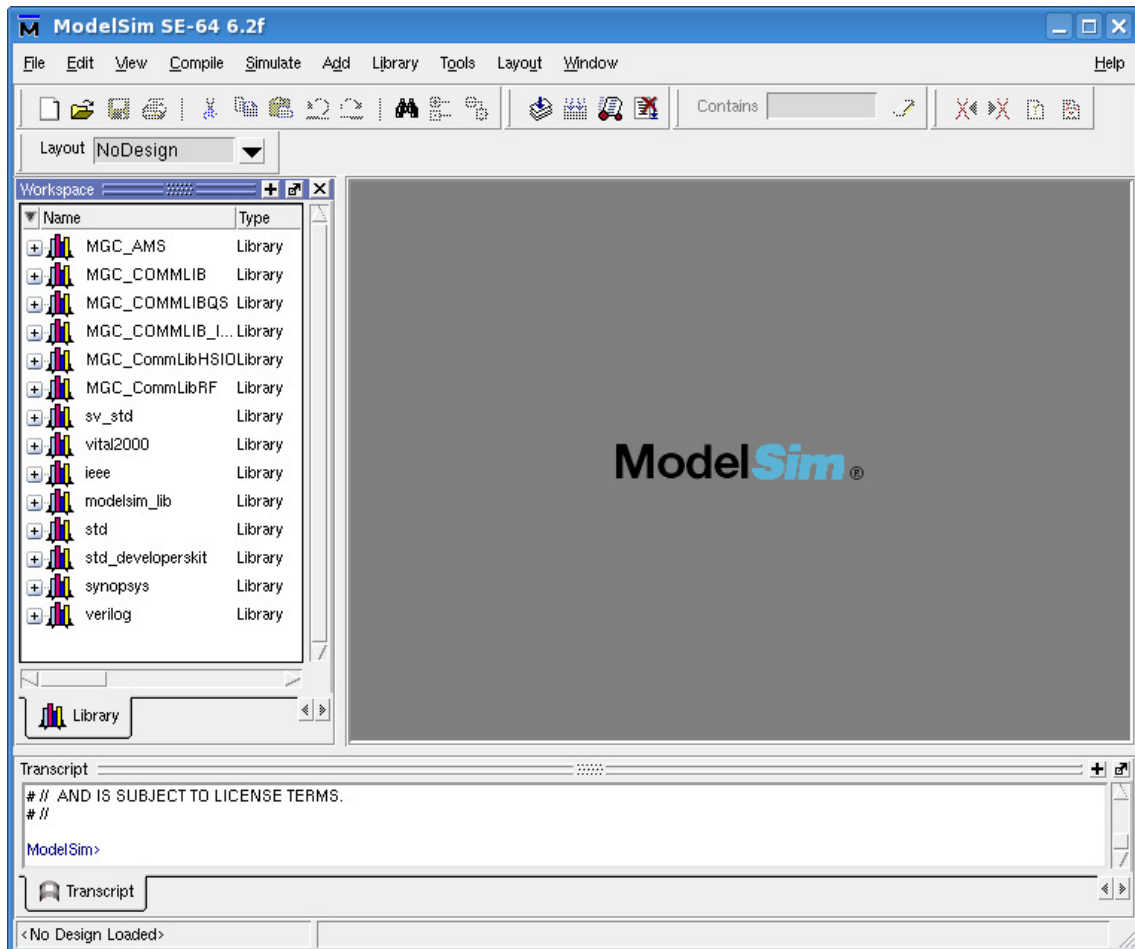
4. The GUI window appears (Figure 1.1).

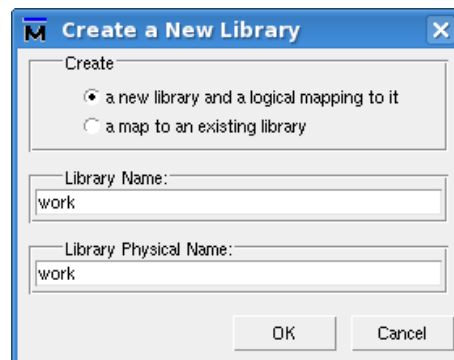Figure 1.1: Modelsim GUI window.

Figure 1.2: Create a New Library window.

1.4   Creating a new library

In this section, we will create a new library. The work library is used to store all compiled design files.

1. Select **File −> New −> Library...** to open the window shown in Figure 1.2.
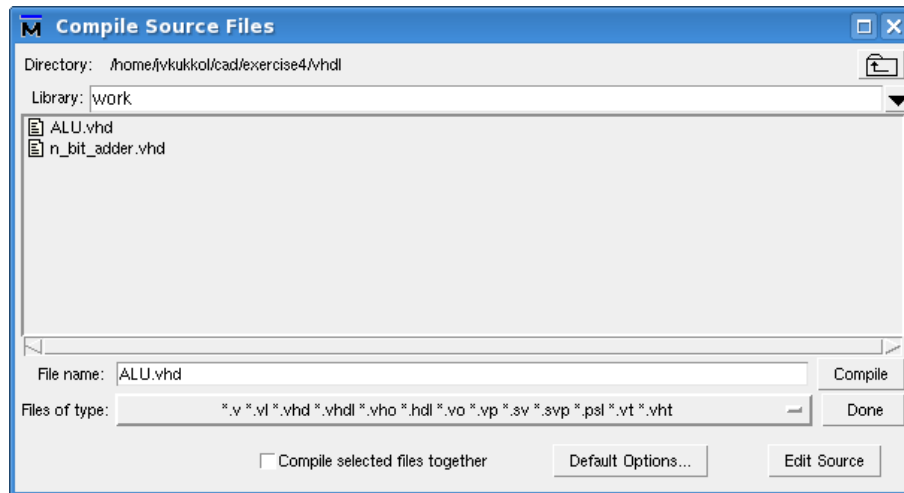
Figure 1.3: Compile Source Files window.

2. Verify that "a new library and a logical mapping to it" is selected.

3. Type "work" in the Library Name and Library Physical Name text fields. Do *not* choose a different name here!

4. Click OK. The work library appears in the Library tab.

1.5 Compiling VHDL files

Perform the following steps to compile the VHDL files that you have written.

1. Open the "Compile Source Files" window (Figure 1.3) with the **Compile −>
   Compile...** pull-down menu item.

2. Navigate to the directory location where your VHDL files are stored.

3. Select all VHDL files that you want to compile, and press the Compile button.
   Check the console for possible errors. All successfully compiled files will appear
   in the work library.

4. Then, click the Done button to close the "Compile Source Files" window.

1.6 Running a simulation

1.6.1 Initialization

1. First, expand the work library with a click on the "+" icon in the Library tab.

2. Then, double-click on your testbench tree item. New tabs appear in the main
   window.

Figure 1.4: Simulate toolbar.

3. If something goes wrong during initialization, error messages will appear in the console.

4. From the Objects tab, select the signals you wish to plot, right click and choose **Add to −> Wave −> Selected Signals** from the pop-up menu.

1.6.2 Change radix notation (if needed)

The default radix notation for plotted signals is Symbolic. However, you might use decimal numbers in your simulations. Therefore, the radix notation of the signals might need to be changed, so that you will be able to better visualize the simulation results.

If you wish to change the radix notation for a signal to decimal, right-click on the signal item in the Wave tab, and choose **Radix −> Decimal** from the pop-up menu.

1.6.3 Execute the simulation

To execute the simulation, first enter the desired advance time (for example 10 us, but this can vary greatly according to your testbench) in the Simulate toolbar (Figure 1.4). Then press the Run button on the same toolbar, to advance the simulation by the entered amount. Check the console for possible errors.

If everything works correctly, you should see some waveforms appearing in the Wave tab. Note that there are several zoom buttons available, if needed (e.g. zoom in/out, zoom to full simulation length).