Exercise problems of Topic 2

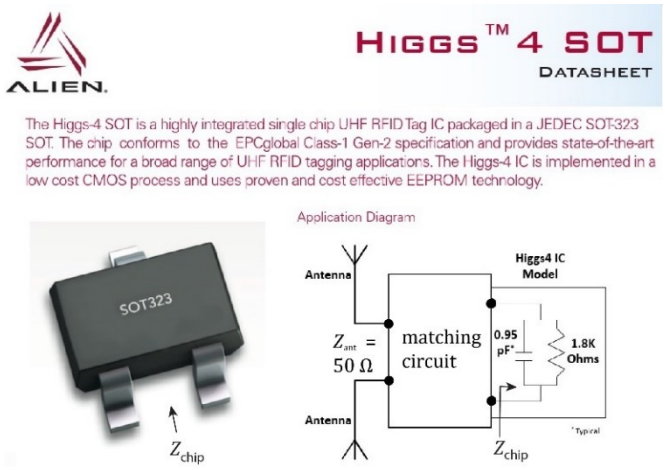
Write your answers clearly, so that the answer proceeds logically and includes necessary intermediate steps and enough explanations. Your answer should be understandable without oral explanations, too. See further instructions for systematic problem solving in MyCourses.

The exercise problem answers are to be returned during a pre-booked appointment on Mondays. The minimum is to return at least one answer per week. If you cannot meet this, you lose a chance to earn those points also later. It is good to note that average of two returned answers per week would be optimal to complete the course with flat speed.

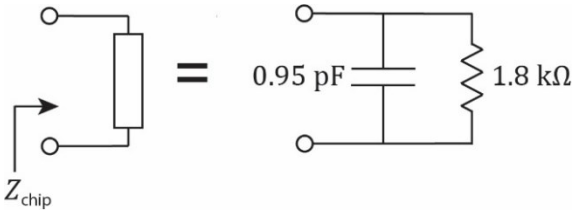
Topic 2 consists of **four (4)** problems. Be prepared to explain and justify your answer to the teacher. The purpose of this returning method is to enhance your learning through two-way communication and constructive feedback. The teacher will grade your answer in the scale of 0-3 points.

Exercise problem 2.1.

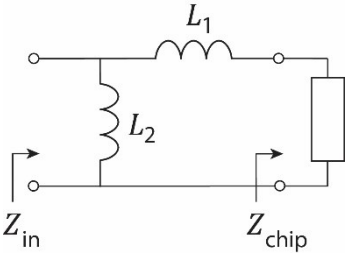
The Higgs-4 IC is a popular chip used in RFID applications at 0.84 – 0.96 GHz. Its input impedance is inherently capacitive due to a rectifier diode in its input. The input impedance is modelled with a 0.95-pF capacitor and 1.8-kΩ resistor in parallel configuration, see the equivalent circuit of the impedance below. The chip is attached through a matching circuit to a 50-Ω antenna. The matching circuit is needed for matching the impedances of the chip and the antenna.



Perform the following operations with the Smith chart graphically. Write all the intermediate phases and explanations to your answers. Attach the Smith charts together with your answers.

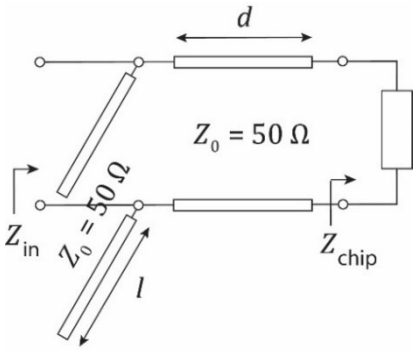


a. Match the chip impedance Z_{chip} to 50 Ω using an L-section inductor-inductor matching circuit at the centre frequency of the chip 0.90 GHz – i.e., calculate the inductor values L_1 and L_2 (in nH order of magnitude) so that the input impedance Z_{in} is 50 Ω. (*Pozar Chapter 5.1, also find a short video on lumped-element matching in MyCourses)*



b. part on the next page!

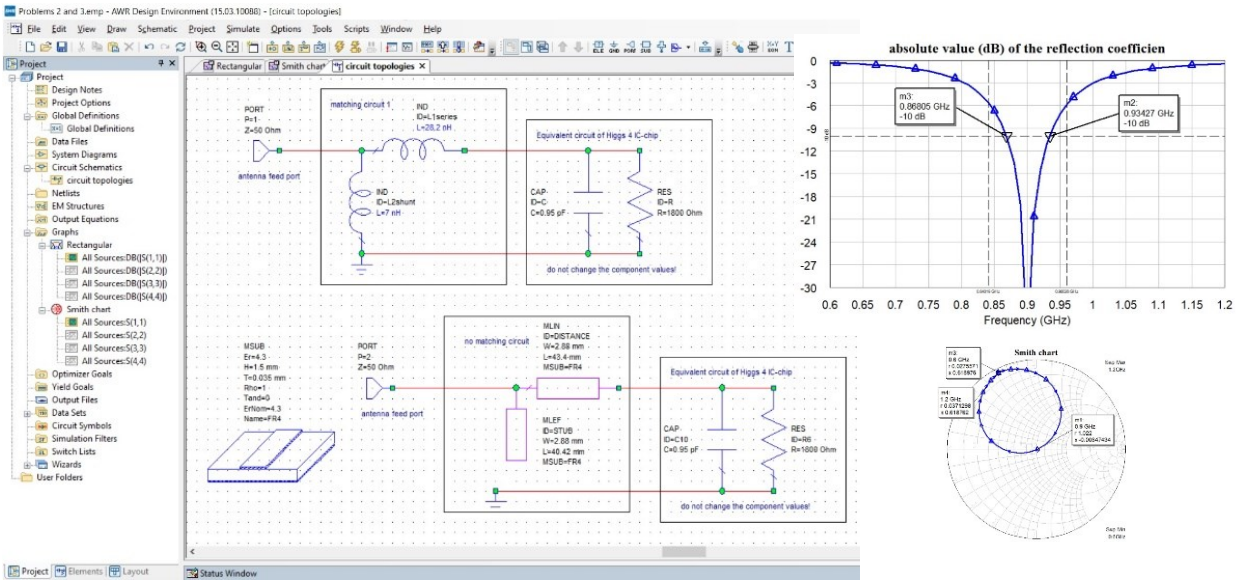
b. Match the chip impedance to 50 Ω at 0.90 GHz using an open parallel stub so that **the length *l* of the stub is minimized** – i.e., calculate the lengths d and l in *wavelengths* so that the input impedance Z_{in} is 50 Ω. (*Pozar Chapter 5.2)*



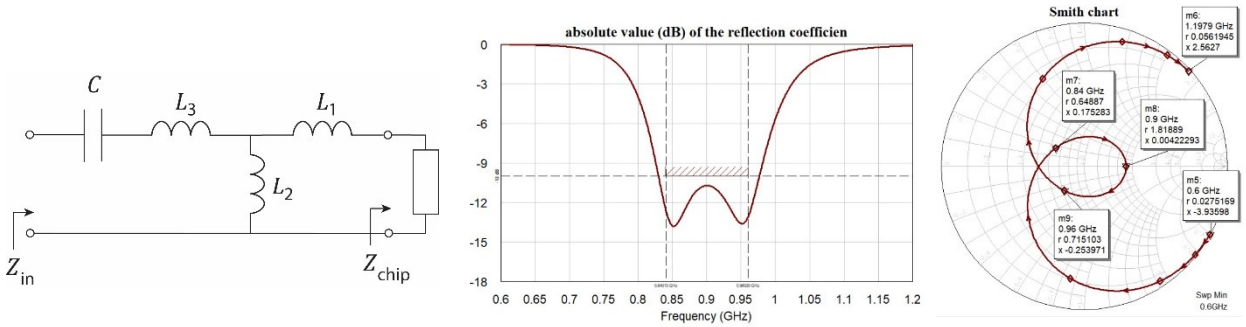
Exercise problem 2.2. The following two problems will be done with AWRDE circuit simulator. Return your answer, for instance, delivering copy-paste figures from AWRDE, see example figures below, and including written observations, explanations, and interpretation of the results.

Simulate the matching circuits of Problem 2.1 using your component values / lengths of transmission lines.

- Model the input impedance of the RFID chip with ideal resistor R = 1.8 kΩ (component "RES" in AWRDE) and capacitor C = 0.95 pF (component "CAP") in parallel.
- Implement the matching circuit of 2.1 a. with ideal inductors (component "IND").
- Implement the matching circuit of 2.1 b. on a 1.5-mm thick FR-4 substrate for which the relative permittivity ε_r = 4.3, loss tangent tan δ = 0.020 and the thickness of the metal t = 35 µm. It is recommended to use the TXLine calculator of AWRDE. Use component "MSUB" for defining the substrate in AWRDE. The microstrip line component is "MLIN" and open-ended microstrip line is "MLEF".
- Plot the absolute value of the reflection coefficient $|S(1,1)|$ (in dB scale) to the Cartesian coordinate system in 0.6 – 1.2 GHz. The reflection coefficient is measured in the input of the matching circuit.
- Plot the reflection coefficients $S(1,1)$ on the Smith chart in 0.60 – 1.2 GHz.
- If needed, tune the component values (L_1, L_2) / lengths (d, l) of the transmission lines so that Z_{in} is "fully matched" at 0.90 GHz – i.e., the circuit resonates at 0.90 GHz.



Exercise problem 2.3. Use the AWRDE circuit simulator and match the chip impedance Z_{chip} with a *dual-resonant* matching circuitry shown in the figure below. The centre frequency is 0.90 GHz and use $|\Gamma_{\text{m}}| = -10$ dB as the matching criterion. As there are no direct design formulas available for the dual-resonant matching circuit design, tune the component values using "Tuner" functionality so that the matching level is at least -10 dB over the entire operation band of the RFID chip – i.e., at 0.84 – 0.96 GHz. Written observations, explanations, and interpretation of the results are also asked in this problem.



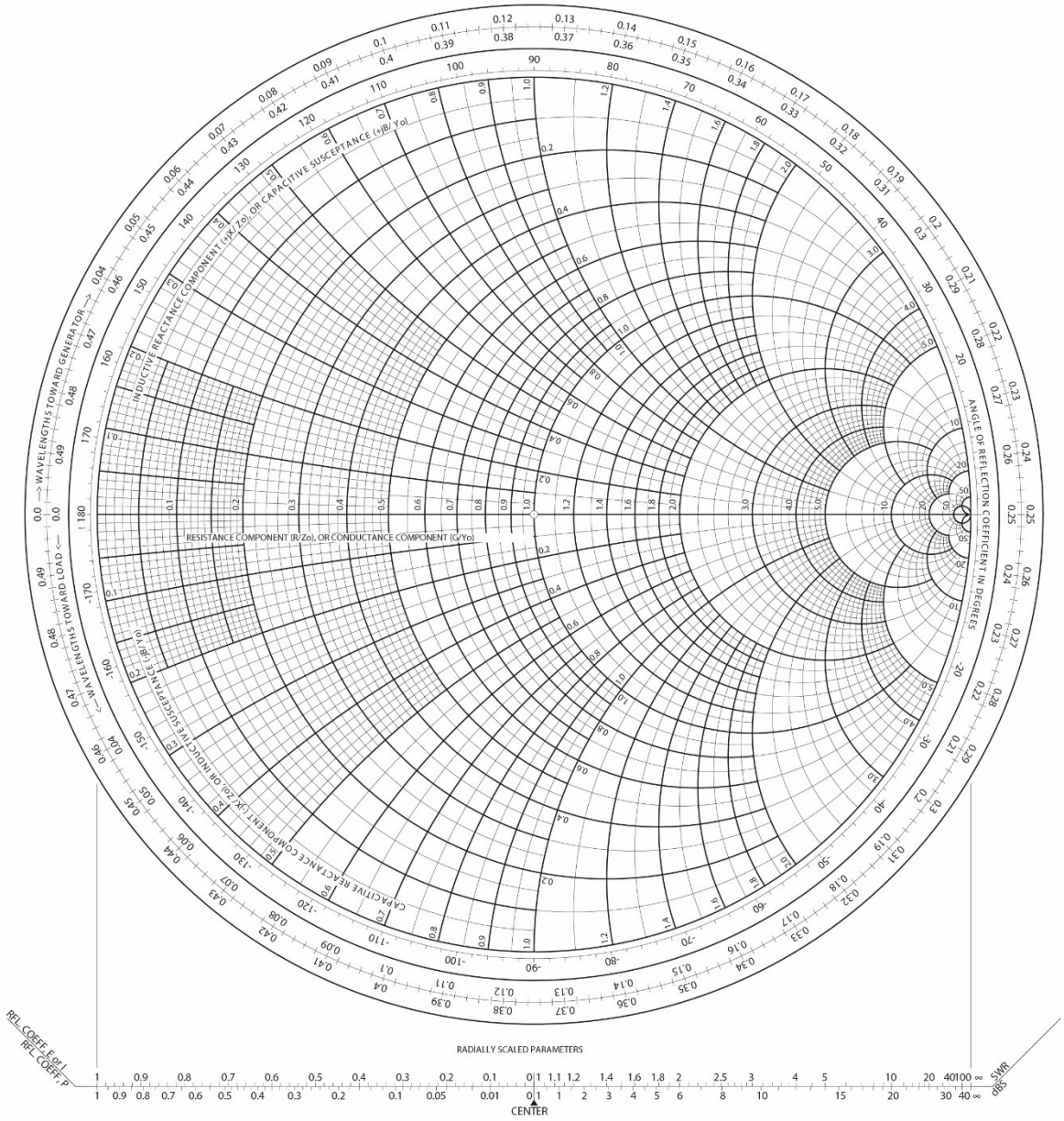
Earn **one extra point** by designing a **triple-resonant** matching circuitry. Add a shunt parallel LC resonator between the feed port and capacitor *C*.

Exercise problem 2.4. This problem deals with the *Bode-Fano criterion*, Pozar Chapter 5.9.

a. Calculate the maximum bandwidth (in MHz) of the impedance of the RFID chip (resistor R = 1.8 kΩ and a capacitor C = 0.95 pF in parallel). The maximum allowed reflection coefficient is $|\Gamma_{\text{m}}| = -10$ dB.

b. What is the percentage fraction that can be achieved with 1) the single-resonant matching circuit (Prob. 2.1 a.) and 2) dual-resonant matching circuit (Prob. 2.3) compared to the maximum bandwidth given by the Bode-Fano criterion (part a. of this problem)?

c. Explain using your own words, what the purpose of the Bode-Fano criterion is – i.e., what for do we need the Bode-Fano criterion?


WAVELENGTHS TOWARD GENERATOR
WAVELENGTHS TOWARD LOAD
ANGLE OF REFLECTION COEFFICIENT IN DEGREES
INDUCTIVE REACTANCE COMPONENT (+jX/Zo) OR CAPACITIVE SUSCEPTANCE (+jB/Yo)
RESISTANCE COMPONENT (R/Zo), OR CONDUCTANCE COMPONENT (G/Yo)
CAPACITIVE REACTANCE COMPONENT (-jX/Zo) OR INDUCTIVE SUSCEPTANCE (-jB/Yo)

RADIALLY SCALED PARAMETERS
REFL COEFF. E or I
REFL COEFF. P
SWR
SRP
CENTER