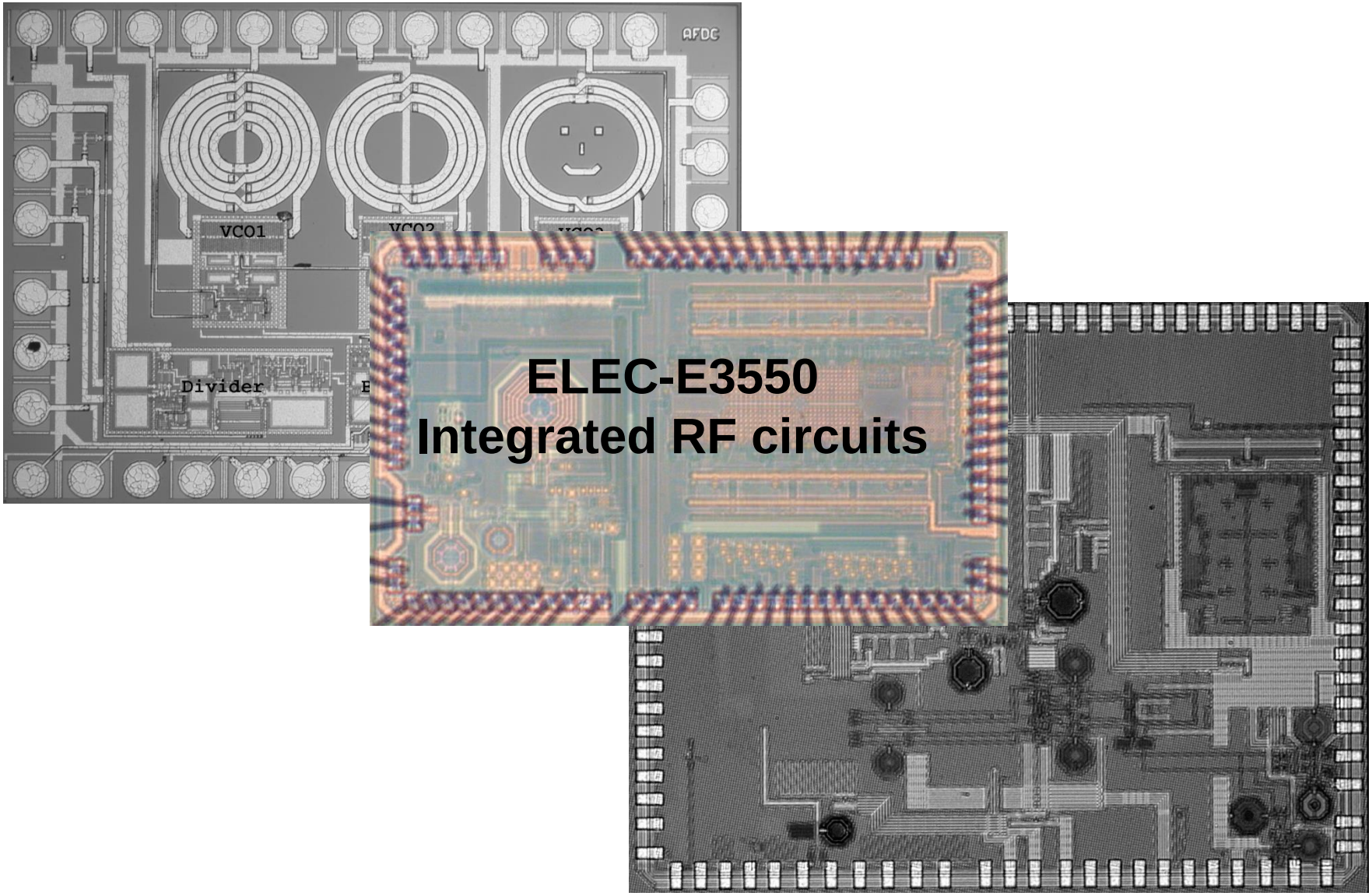


ELEC-E3550
Integrated RF circuits

Aalto University
School of Electrical
Engineering

Department of Micro and Nanosciences
Kari Stadius, Saeed Naghavi, Kimi Jokiniemi

Integrated RF circuits
Spring 2023

RF IC Technologies and Devices

Brief review on RF IC technologies

- MOS technology
- Passive devices
- Bonding
- Self-learning assignment 2

Exercises & Homework

- CAD exercise
- Homeworks

RF IC Technologies

Gallium Arsenide

- MESFET
- HEMT
- HBT

GaAs technologies have no or poor p-type FETs → no complementary devices → no good digital logic

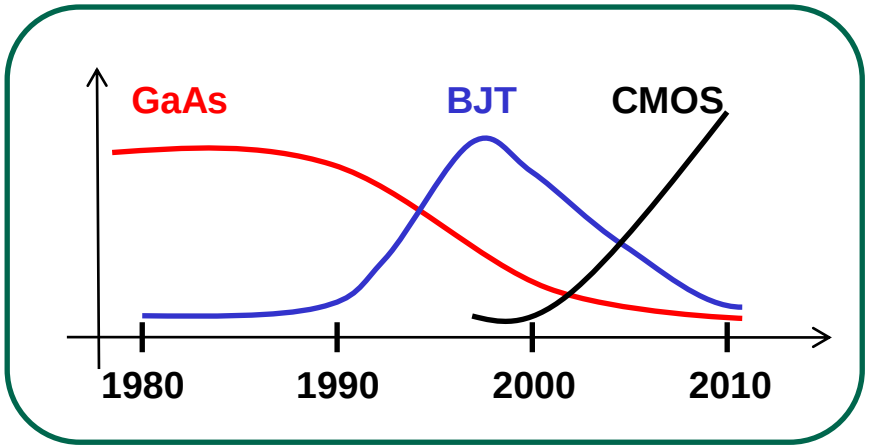
Silicon / SiGe

- BJT
- BiCMOS
- CMOS

Technologies for very high speed or power

- InP
- GaN
- SiC

RF IC designing has and will change …

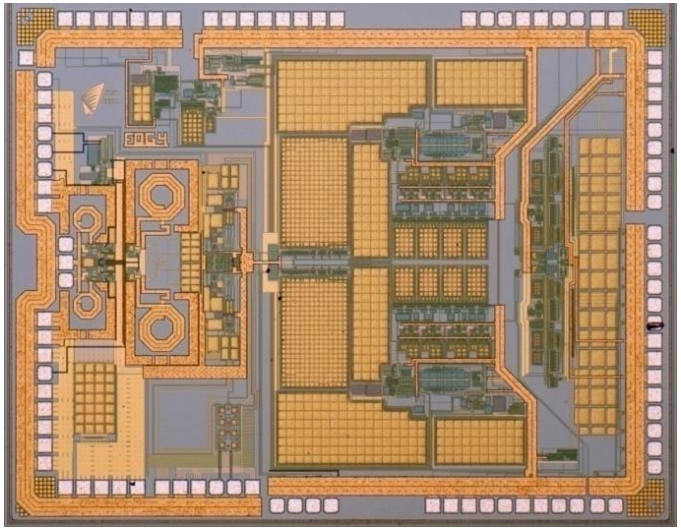


Trends:

- Technology
  - GaAs → Si BJT → BiCMOS → bulk CMOS → FD-SOI & Finfet CMOS
- Design complexity
  - Circuit → Block → RX-TX-SX → multi-system, SOC, SDR
- Design paradigm:
  - RF engineering → RF IC design → Multi-mode design
- Designers
  - Spesialists → in-house groups → fabless & foundry groups

Typical RF CMOS Process

- Gate lenght: 65 nm → 40 nm → **28 nm** → 14 nm → 10 nm → 7…5 ... 3 nm
- Typical device f_t 100-300 GHz
- 6-10 metal layers (copper or aluminium)
- NMOS & PMOS devices
  - 2-3 threshold voltage (V_T) levels
  - Specific RF devices = RF model & layout
  - Core devices simpler (model & layout)

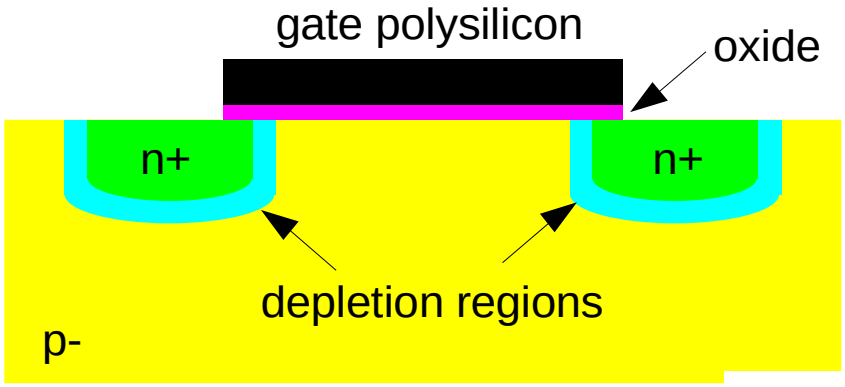


- Passive devices with RF model
  - Inductors and transformers
  - Capacitors (MIM)
  - Varactors (MOS & pn)
  - Resistors (poly-silicon, 2-3 different R_{sq})

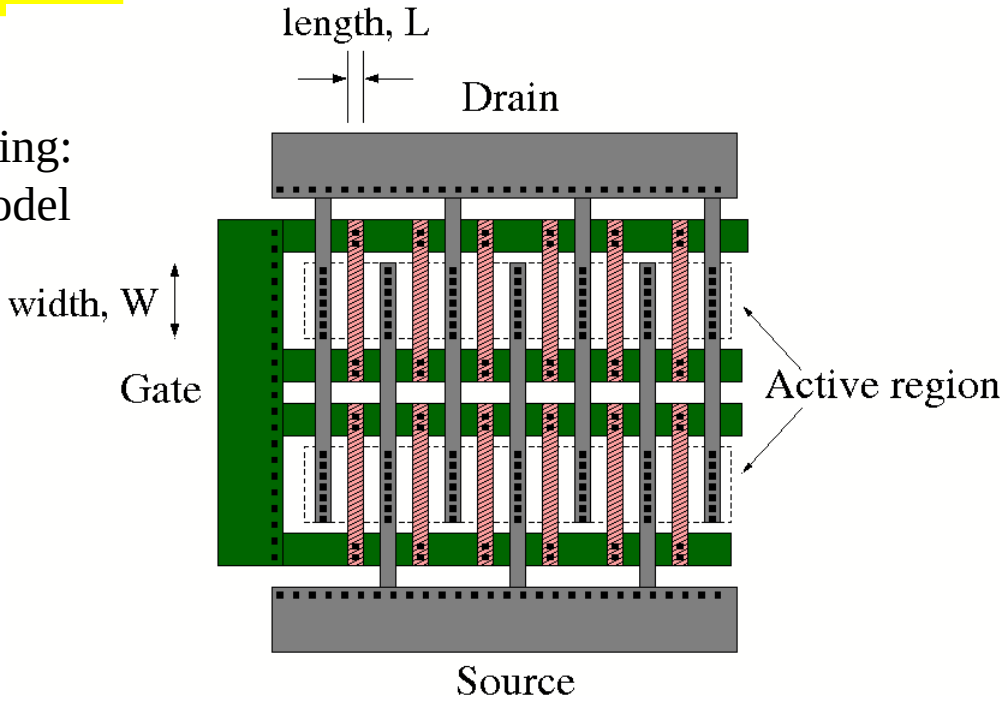
- Digital cell libraries (VHDL → compiler)

Modern CMOS technology is very versatile and good for RF ICs. Critical practical challenge is the quality (and availability) of device **MODELS.**

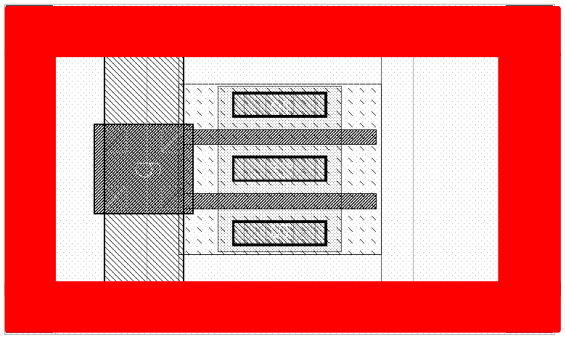
NMOS Device



At RF, multi-finger layout is used to keep the gate resistance reasonable

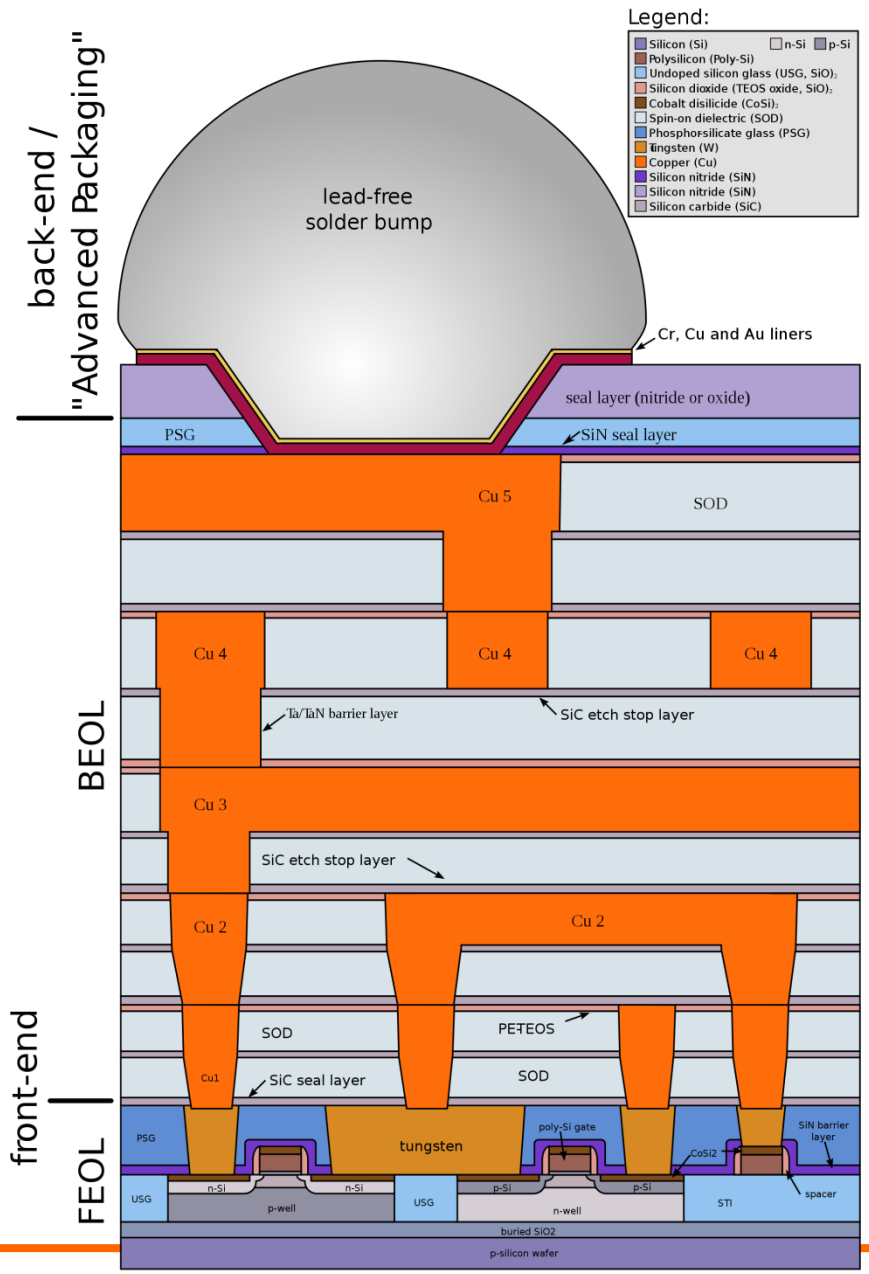


At RF, each device has its own guard ring: minimize coupling, accurate device model

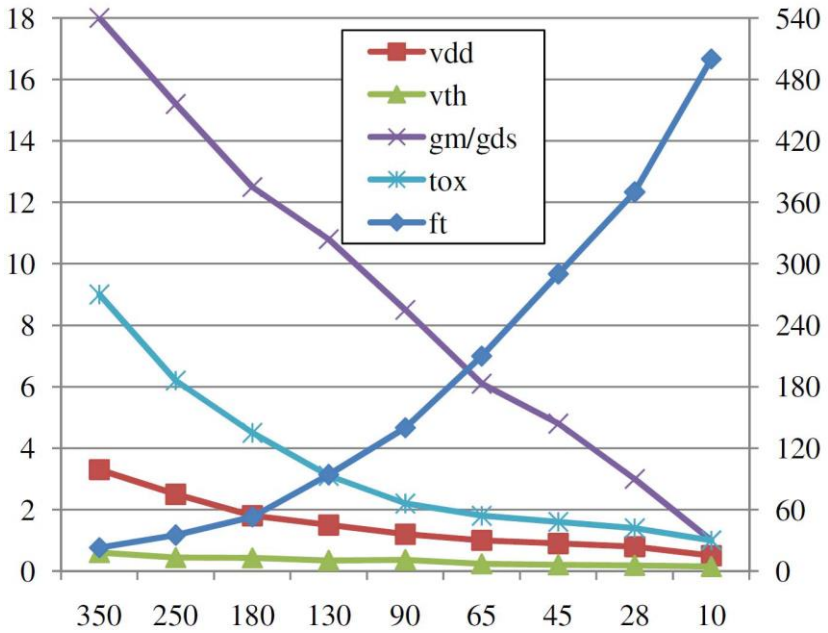


Red is p+ ring for gnd

CMOS Cross-Section



CMOS Scaling: Analog performance is declining

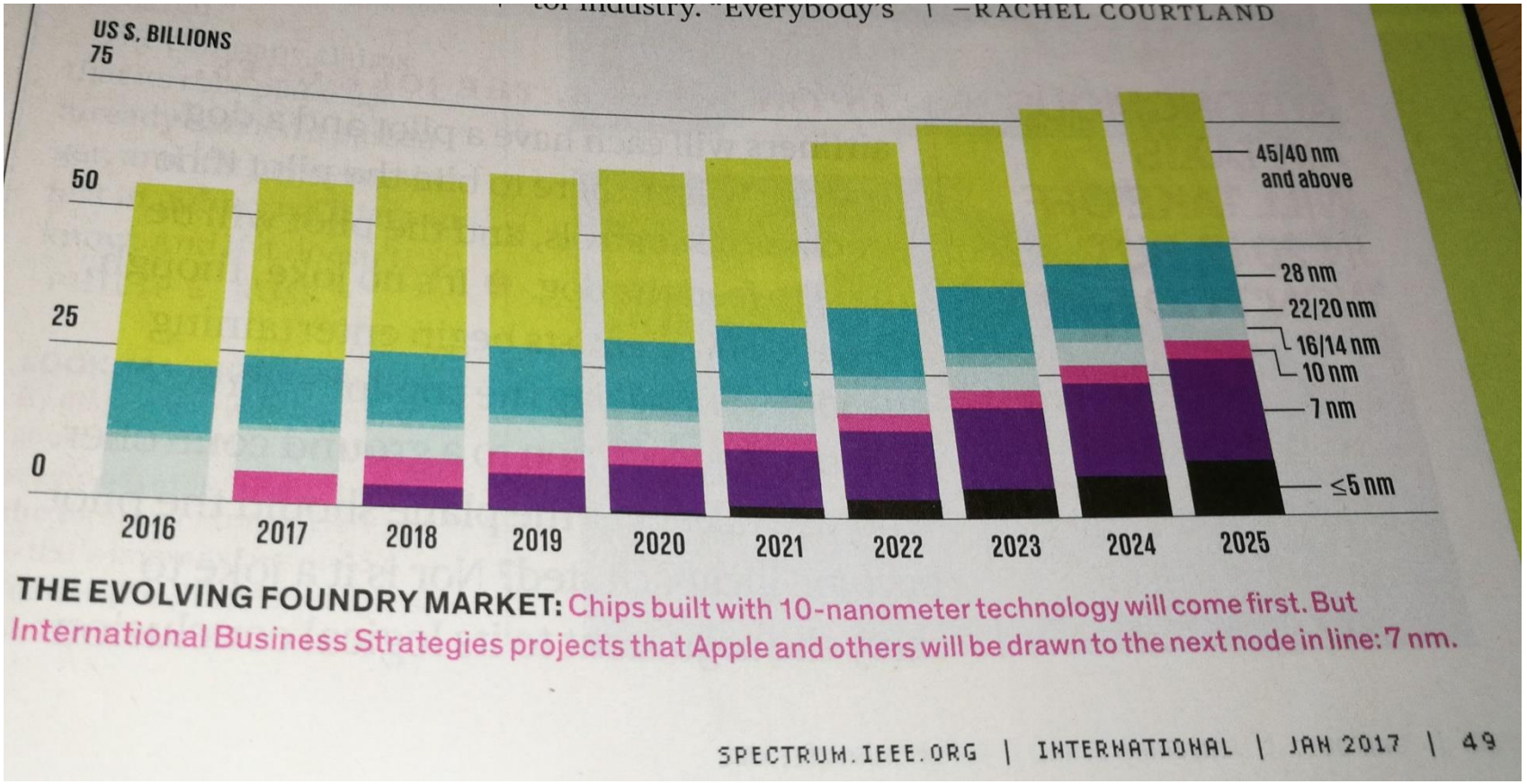


CMOS evolution has resulted in

- increased integration density
- higher speed
- low supply voltage → low power
- reduced signal headroom
- declined analog performance
  - Intrinsic gain gm/gds declines
  - Output impedance is low

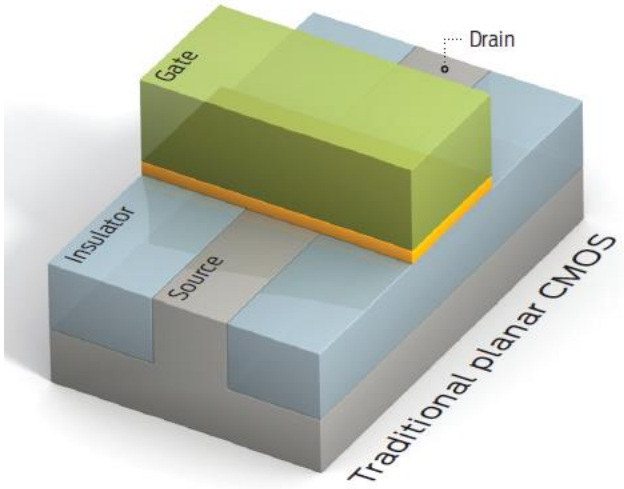
  = good switch, poor amplifier

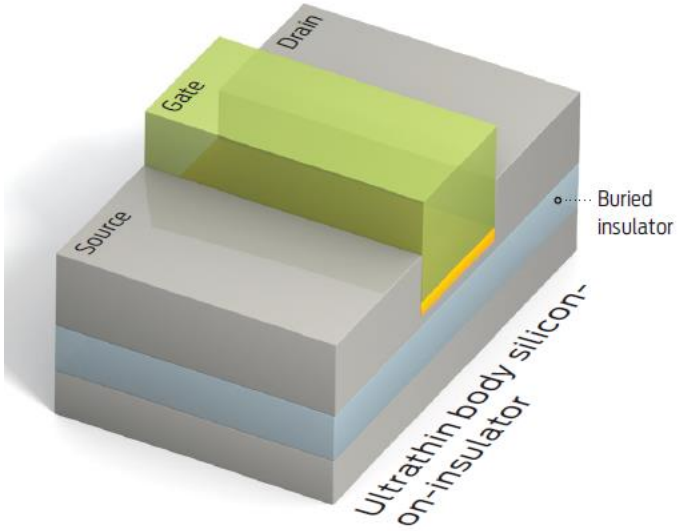
Moore's law has hold well

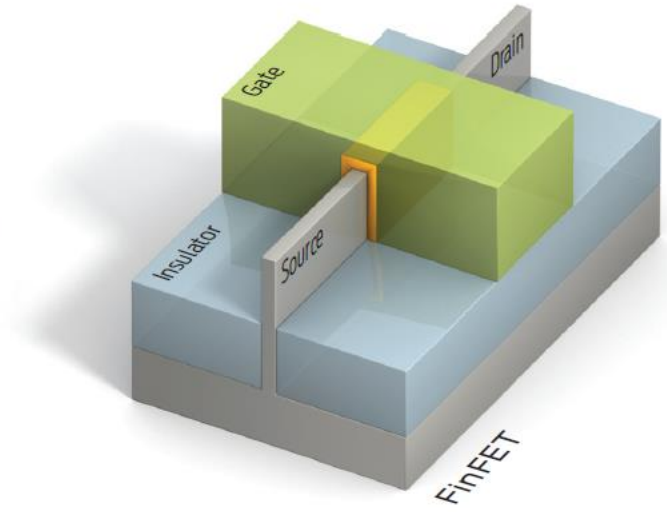


THE EVOLVING FOUNDRY MARKET: Chips built with 10-nanometer technology will come first. But International Business Strategies projects that Apple and others will be drawn to the next node in line: 7 nm.

CMOS Transistor Structures







Ahmed, K.; Schuegraf, K.; "Transistor wars," *IEEE Spectrum*, vol. 48, no.11, pp.50-66, Nov 2011

FD-SOI and FinFET Technologies

A video on FD-SOI by ST Microelectronics
https://www.youtube.com/watch?v=uvV7jcpQ7UY

A video on FinFET by ThresholdSystems
https://www.youtube.com/watch?v=c-3p8moNXfI&t=0s

Passive Devices in RF CMOS process

1. Resistor
2. Inductor
3. Transmission line
4. Capacitor
5. MOS varactor
6. SC network

7. Bonding pad
8. Wire bonding
9. Flip-chip (BGA)

Quality Factor Q

Quality factor Q is a metric to describe the losses of reactive component BUT, it is also used in filter design to define the steepness of your filter → A risk to a confusion.

- Q=10, low-quality passive such as on-chip coil
- Q=100, already close to ideal in most cases
- Q>1000, losses play role only in special cases

Quality Factor Q

The most general definition of the Q-factor is based on the ratio of stored energy to dissipated energy per cycle:

$$Q = \frac{E_{store}}{E_{diss} / \omega}$$

For an ideal inductor with a series resistor R, we have

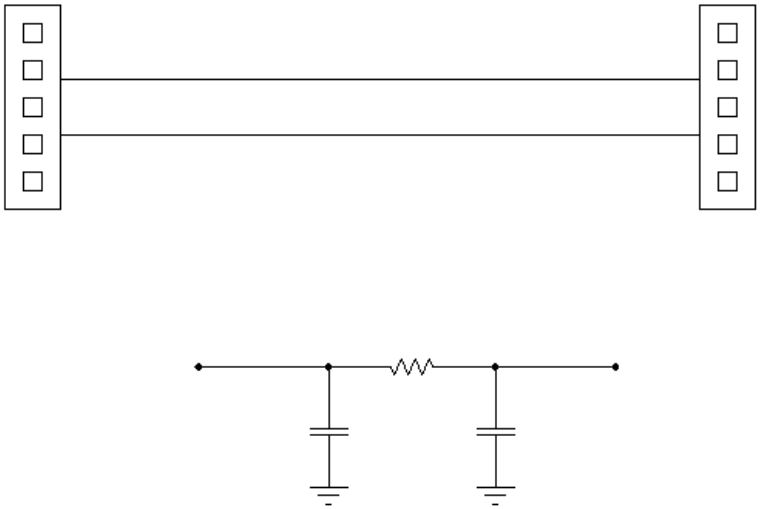
$$Q = \omega \frac{\frac{1}{2} L i^2}{\frac{1}{2} R i^2} = \frac{\omega L}{R}$$

Alternative definition is based on 3-dB bandwidth of a resonator / filter

$$Q_{3dB} = \frac{\omega_0}{\Delta \omega_{3dB}}$$

Now, consider an ideal (lossless) LC-bandpass filter: Q is infinite, Q_{3dB} is real.

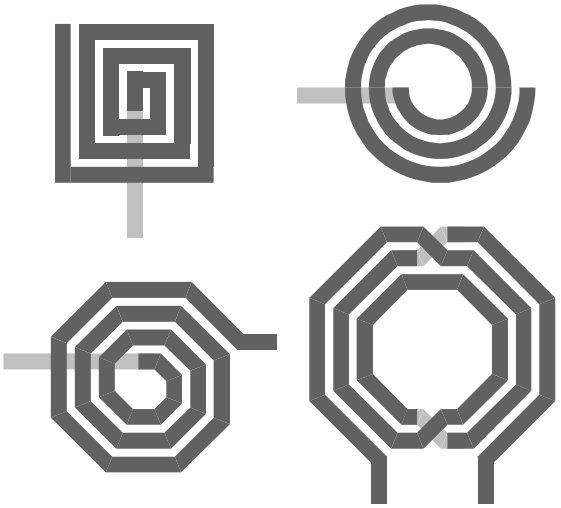
Integrated Resistor

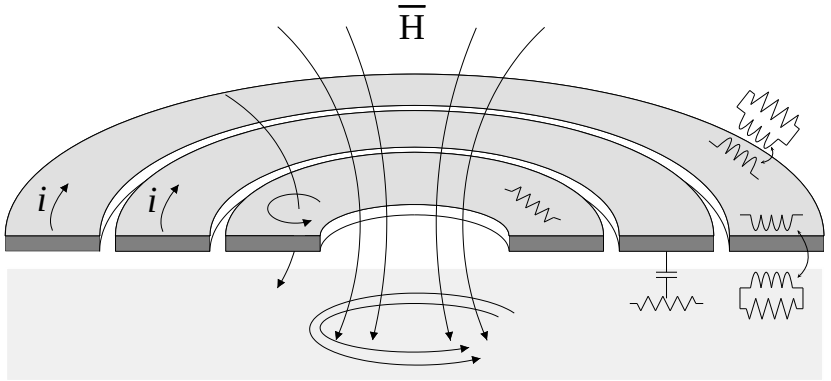


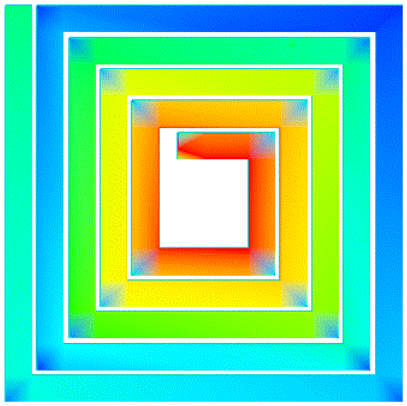
- Typical material is un-silicided polysilicon
- Sheet resistance typ. 100-300 Ω
- Quite small parasitic capacitance, OK for RF ICs
- Process variation significant, typ. 20-50 %
- “well”-type silicon resistors not good for RF; High Cpar

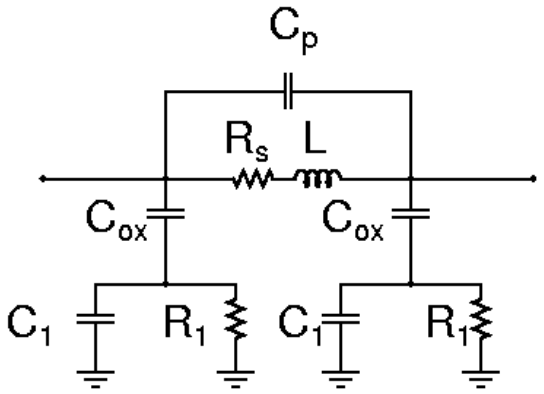
Monolithic Inductor

Very important for RF ICs → Self-learning assignment



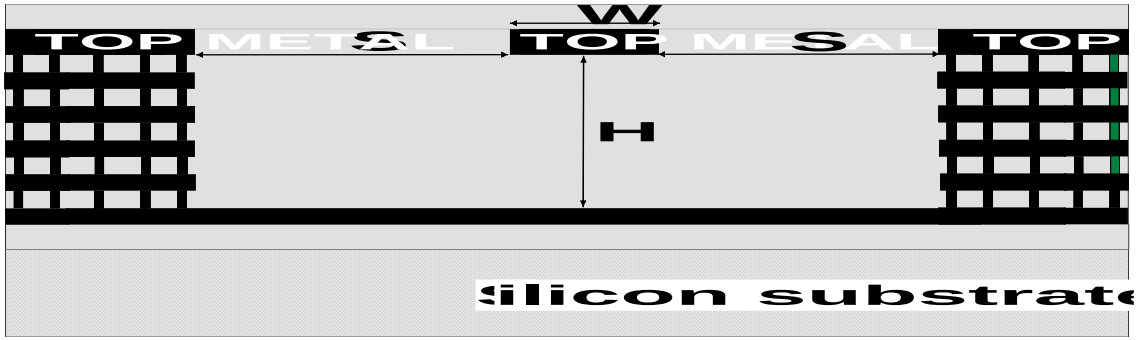




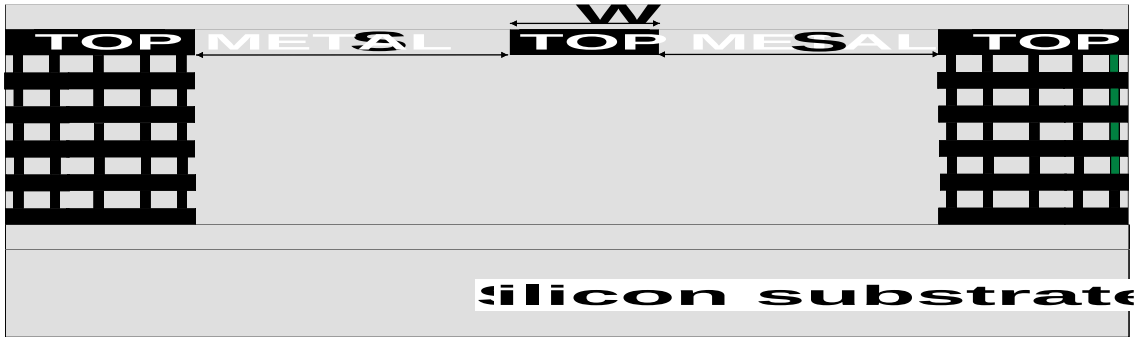


Integrated Transmission Line

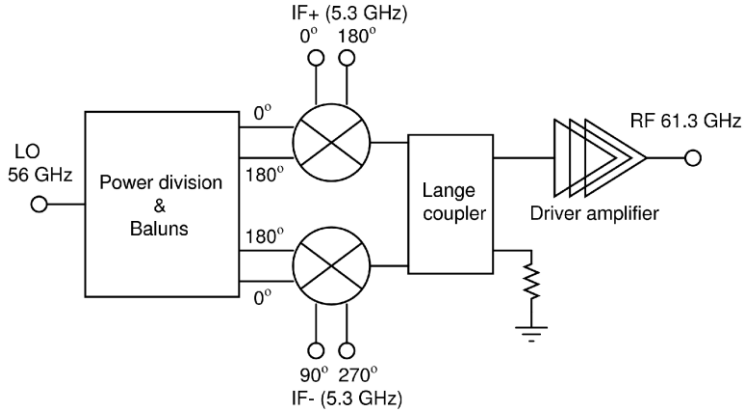
Microstrip line $h << s$

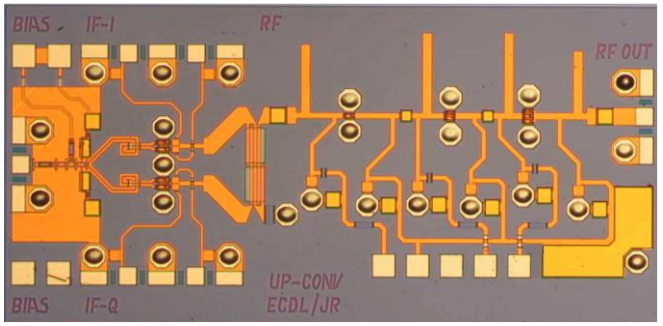


Coplanar waveguide (CPW)



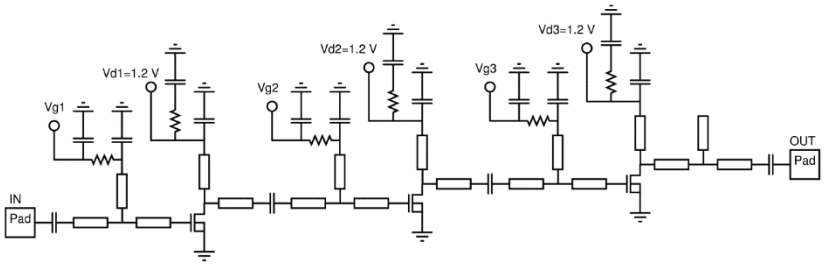
Examples of Transmission Line Circuits

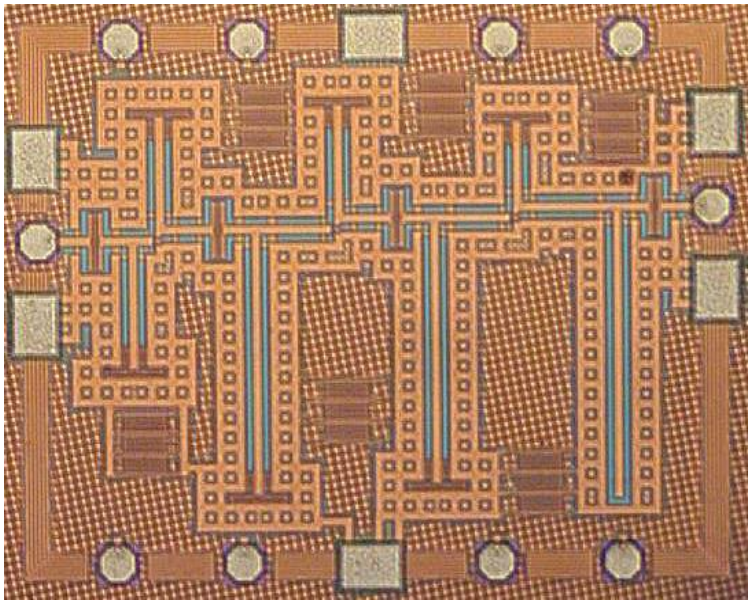




@ Jan Riska

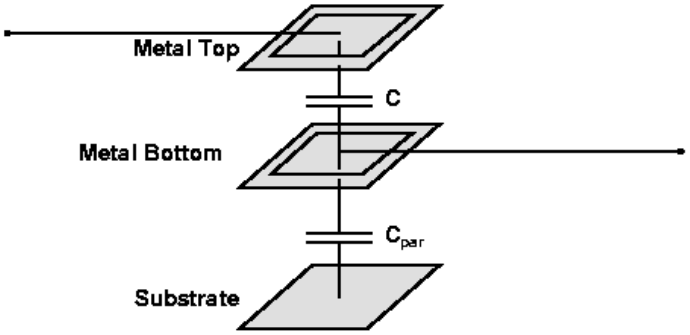
A 60-GHz three stage amplifier

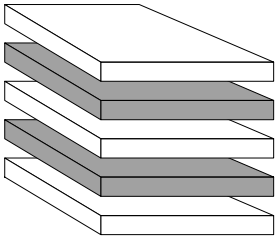


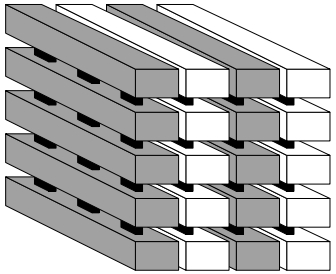


@ Mikko Varonen

Integrated Capacitors





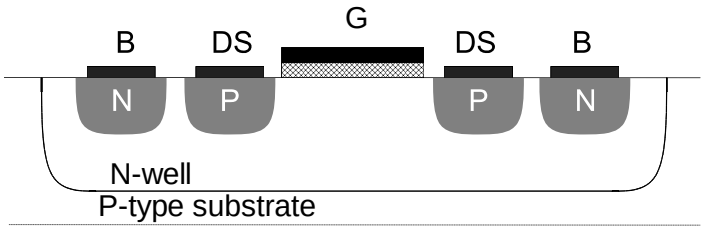


Metal-insulator-metal (MIM) Sandwich MIM Lateral flux

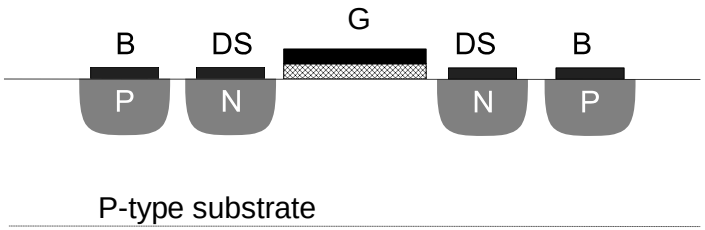
- Main issues are capacitance density and C/Cpar
- Quality factors are high; take care of interconnections
- In sub-100nm technologies lateral flux caps are better
- Process variation significant, typ. 10-30 %

MOS varactors

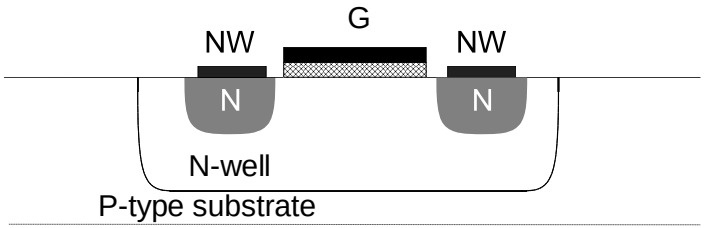
Inversion-mode PMOS



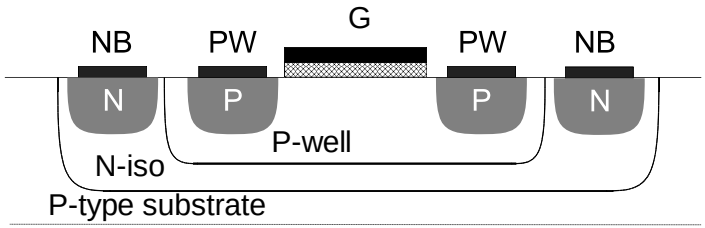
Inversion-mode NMOS



N-type accumulation-MOS



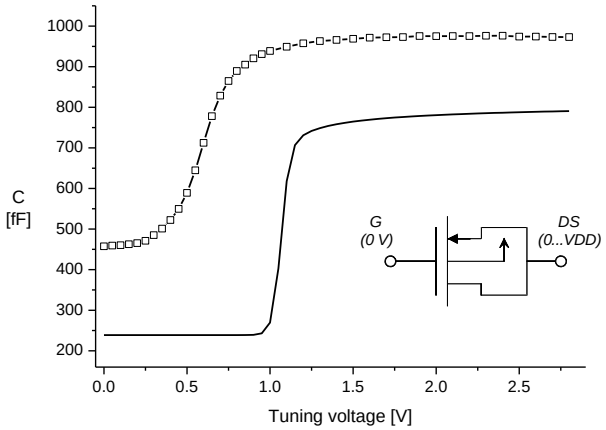
P-type accumulation-MOS



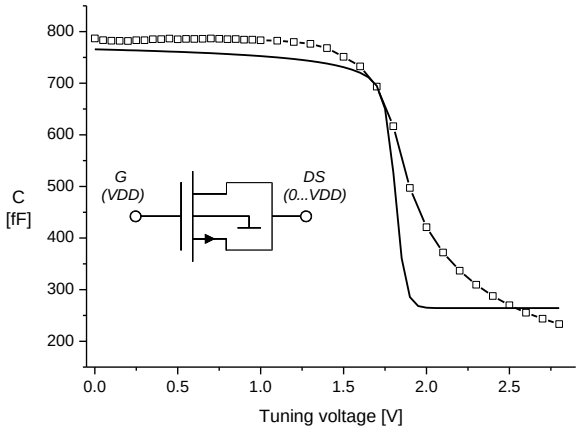
- Four types are available, inversion-mode are “ordinary” MOSFETs
- Quality factor and tuning range (Cmax/Cmin) are competing properties
- Typ. Q~50 at 2 GHz and Cmax/Cmin ~3
- Process variation tracks to MOSFET variation

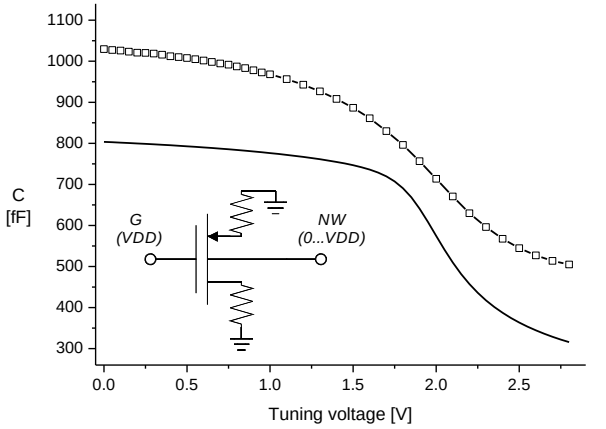
MOS Varactors

inversion-mode PMOS

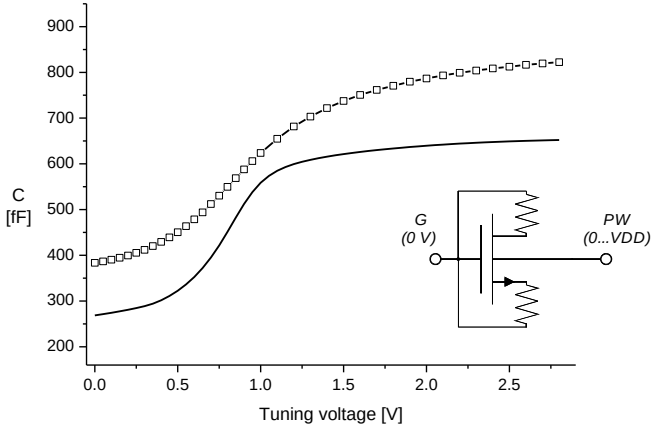


inversion-mode NMOS





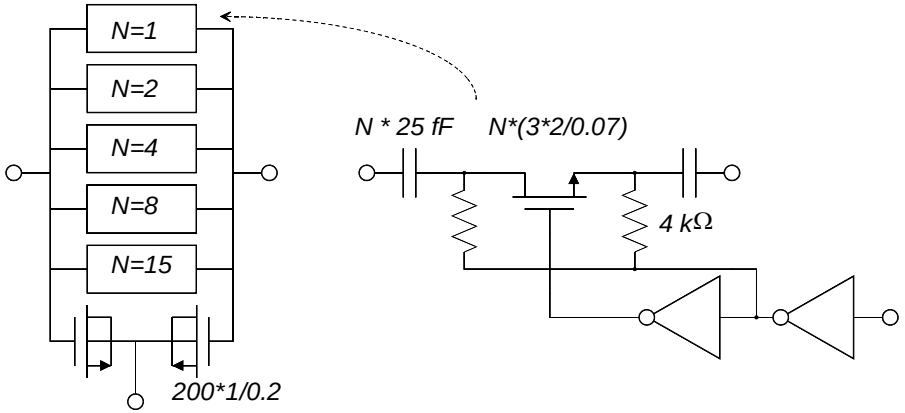
N-type accumulation MOS

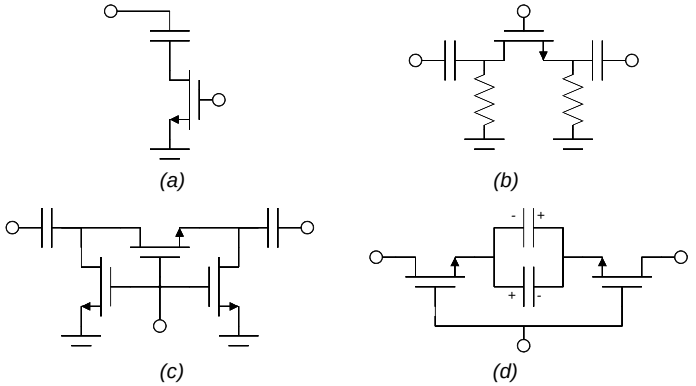


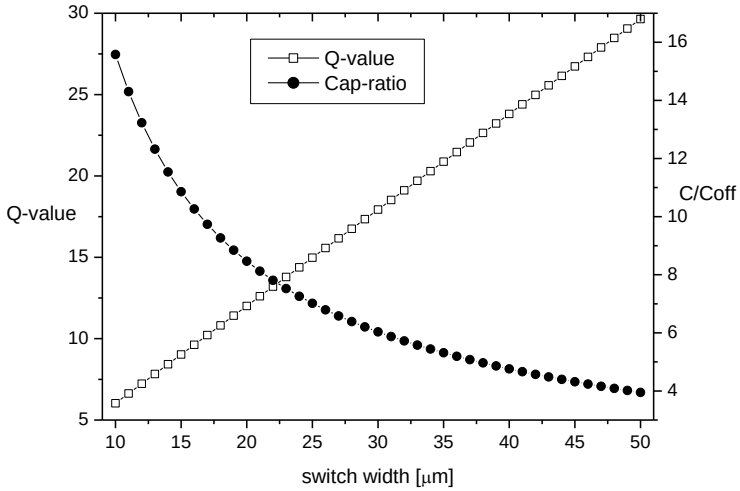
P-type accumulation MOS

Switched-Capacitor Network

- Switched capacitors for tuning
- Large switch = low RON & big Cpar
- Small switch = high RON & small Cpar
  → Q vs. TR trade-off here as well



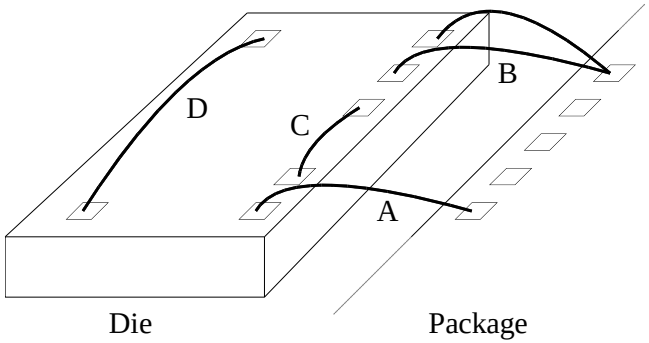


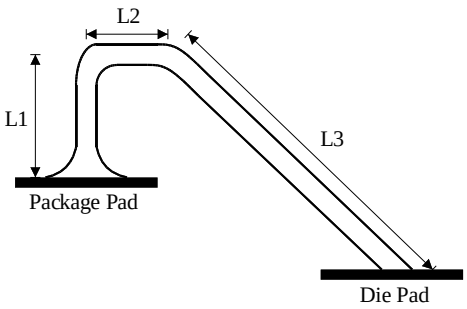


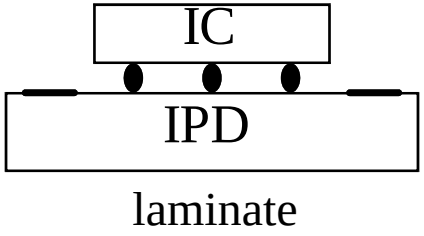
BTW, switched resistor networks are feasible as well

0.1-pF SC-unit for a 4-GHz VCO in the 65-nm CMOS technology.

Wire Bonding and Flip-Chip Assembly





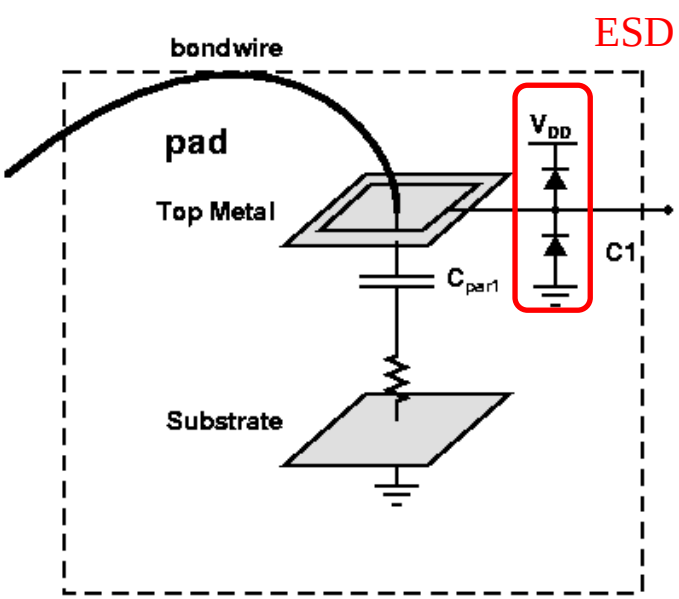


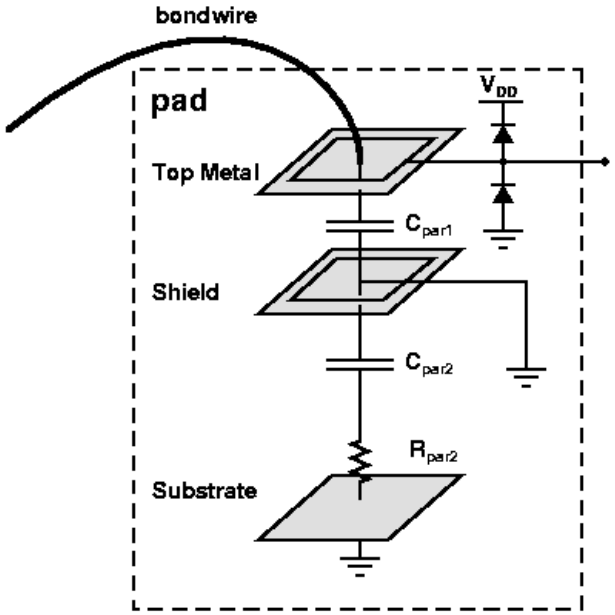
- Bond wire = high-Q inductor, **L=1nH / mm,** typ. 1-3 mm
- Ball-grid array solder bumb

  H=100-200 um, Ø~50 um

  small high-Q inductor
- Flip-chip requires substrate (laminate) and second bonding → modeling !

Bonding Pad





- Pad produces parasitic capacitance
- ESD protection circuit produces a large parasitic capacitance
- “RF pad” model needed in a design kit

Recap

RFIC technologies

- CMOS is the prevalent tech – best for mixed mode apps
- SiGe BiCMOS for mmWave applications
- GaN for power amplifiers
- InP for very high frequencies

RF IC components

- Model availability / accuracy is the key question
- Coils are a specialty of RF ICs
- Transmission lines appear at above 50 GHz

Next Meeting

Topics will be

- concepts related to amplifiers
- low-noise amplifiers
- power amplifiers
- buffers

Self-Learning Assignment 2

Objectives are to familiarize yourself with properties of **monolithic coils** and transformers

Session continues at 14:15

Introduction & guidance on

homeworks and CAD exercises.