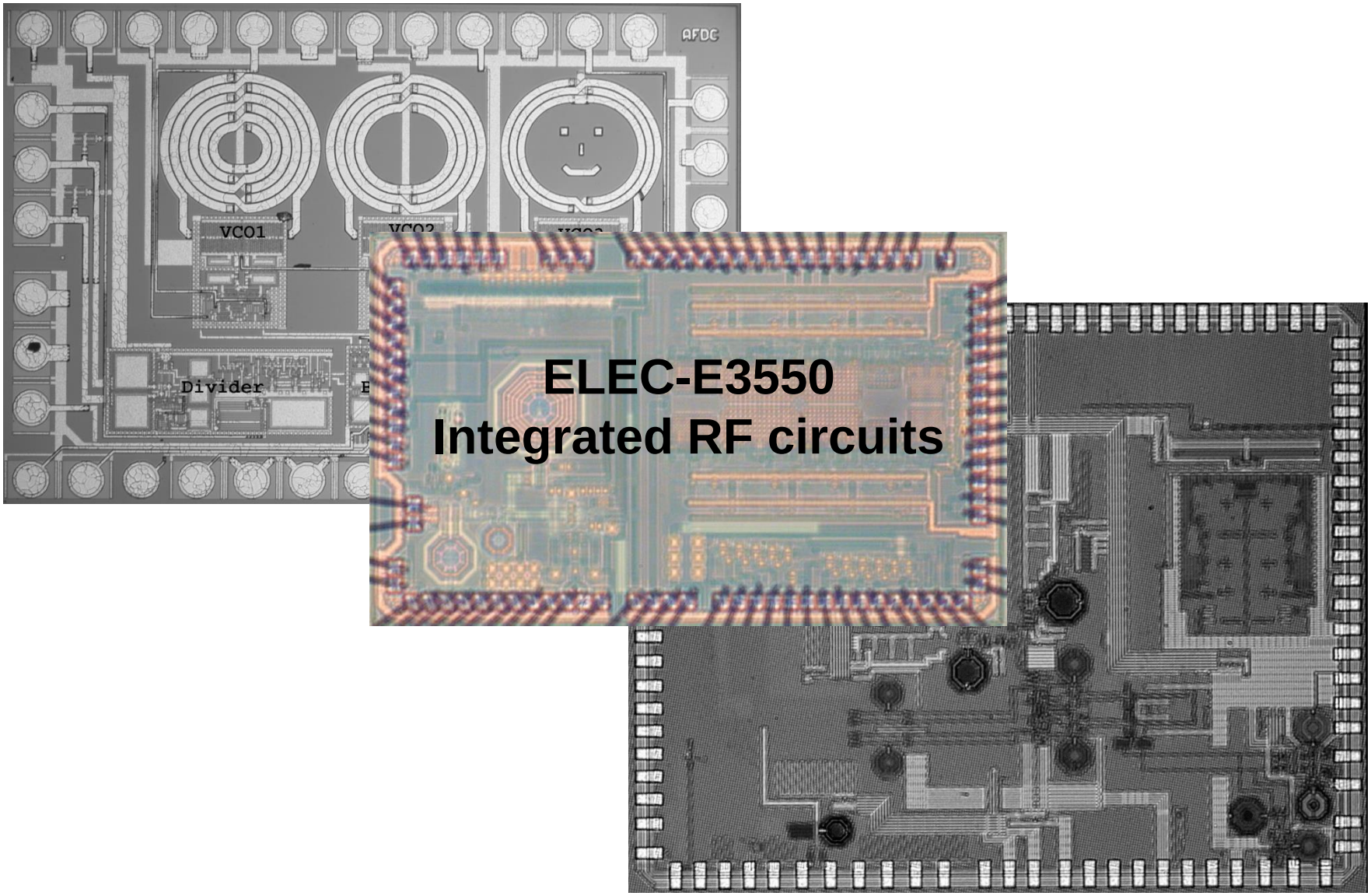


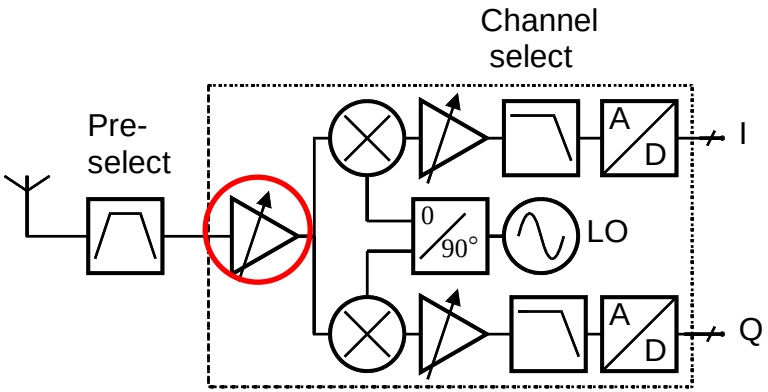
ELEC-E3550
Integrated RF circuits

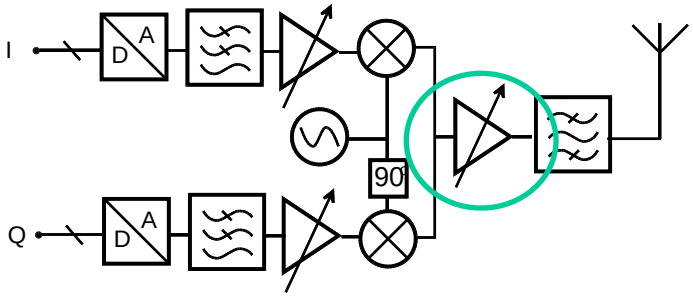
Aalto University
School of Electrical
Engineering

Department of Electronics and Nanoengineering
Kari Stadius, Saeed Naghavi, Kimi Jokiniemi

Integrated RF circuits
Spring 2023

RF IC Amplifiers





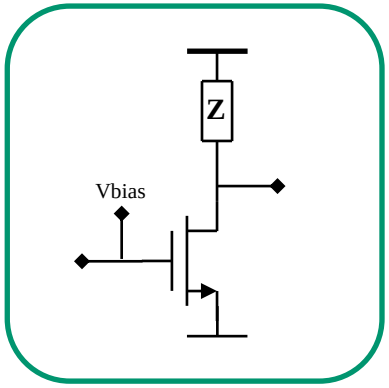
- Focus on specific RF IC amplifiers

  LNA and PA

- Some words on buffers

- Exercises & Homework
  - Self-learning material
  - CAD exercise
  - Homeworks

Basic Small-Signal Amplifiers & Analysis



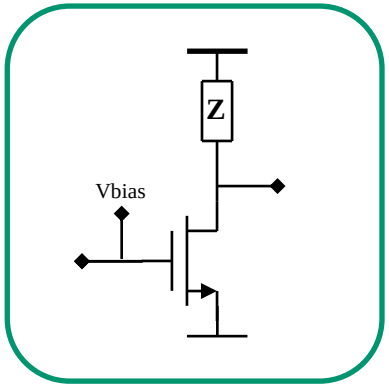
DC Analysis

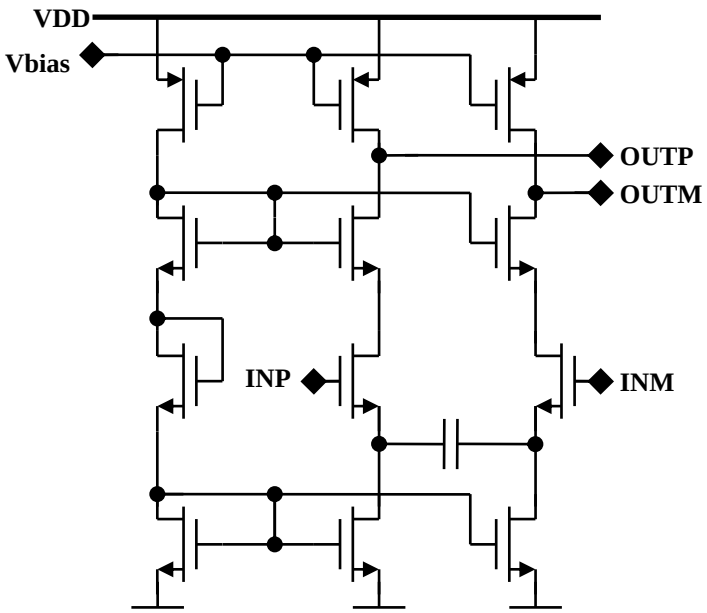
- Operating point
- DC current

AC Analysis

- Gain
- Frequency response
- Input & output impedance
- Stability

Basic Small-Signal Amplifiers & Analysis





DC Analysis

- Operating point
- DC current

AC Analysis

- Gain
- Frequency response
- Input & output impedance
- Stability

Main message: RF ICs include conventional amplifier stages and their design resembles that of low frequency basic stages.

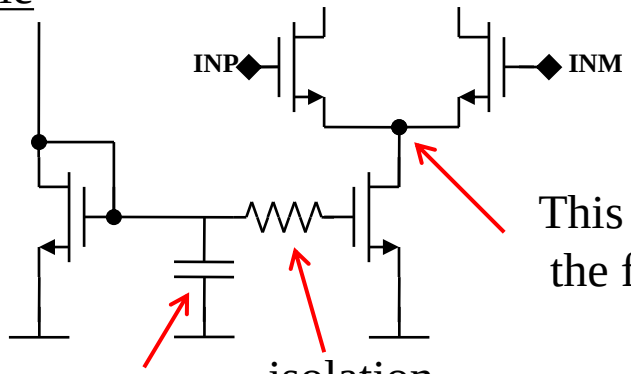
Bias Circuits

CMOS RF IC circuits have same type of bias arrangments as LF circuits.

Guidelines:

1) Isolate RF signals from bias circuits
2) Add a low-impedance node to bias circuit
3) Consider noise coupling, stability, VDD droop etc. just like in LF circuits
   Interference reduction important; e.g. harmonics of a digital clock

Example

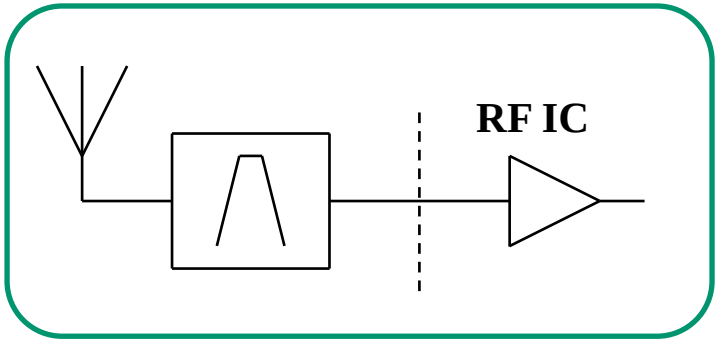


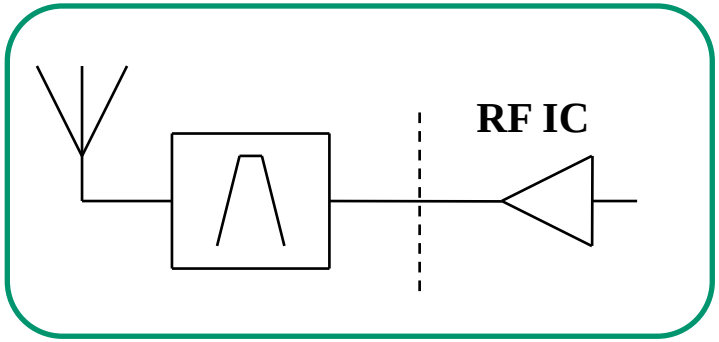
This node is a virtual ground node for
the fundamental but not for the 2. harmonic

Layout: Resistor often same size as all FETs
Cap bigger than all the rest

Impedance Matching ”S11” and ”S22”

Why do we need input matching for LNA and output matching for PA ?

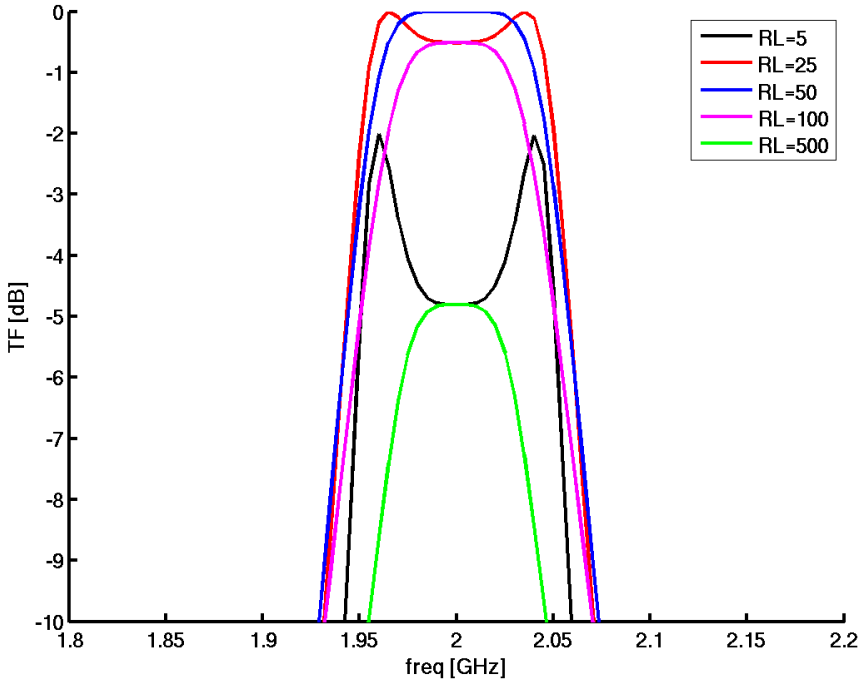




Impedance Matching ”S11” and ”S22”

Why do we need input matching for LNA and output matching for PA ?

Reason 1:Matching is needed to maintain the correct frequency response of external passive filters.



Reason 2: in LONG interconnections, **signal reflections** results in frequency-depent signal level variations.

Low-Noise Amplifier

Four basic circuit arrangements

1. Resistive termination
2. Parallel feedback
3. Common gate
4. Inductive degeneration

LNA critical design targets

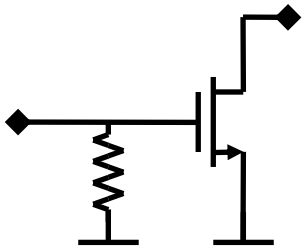
1. Gain
2. Noise Figure
3. Linearity
4. Matching

All are frequency dependent !!
Best performance for all these
is not met with same dimensioning
→ Compromize is needed

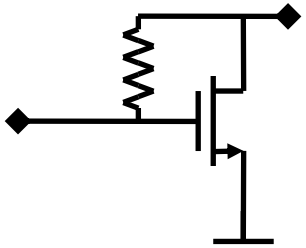
Examples of advanced circuits; “noise cancellation”

Basic LNA Configurations

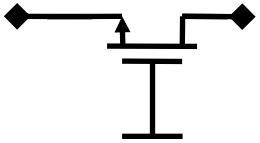
Resistive termination



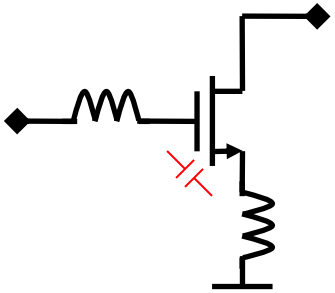
Parallel feedback



Common gate



Inductive degeneration



Input Matching

- Resistively terminated $Z_{in} = R_m \| Z_{in,T}$
- Feed-back $Z_{in} = \dfrac{1}{1/Z_{in,T} + g_{m,T}}$
- Common gate $Z_{in} = \dfrac{1}{g_{m,T}}$
- Inductively degenerated $Z_{in} = \dfrac{g_{m,T} L_s}{C_{gs}} + j\left(\omega\left(L_g + L_s\right) - \dfrac{1}{\omega C_{gs}} \right)$

Voltage Gain

The voltage gain of the four configurations can be compared by comparing the transconductance ($G_m = |I_{out}/v_{in}|$) of each LNA

$$A_v = G_m |Z_L(j\omega)|$$

- Resistively terminated $G_m = g_m$
- Feed-back $G_m = \left|\frac{g_m R_{fb} - 1}{R_{fb} + Z_L}\right|$ $A_v \approx |g_m R_{fb} - 1|$
- Common gate (matching req Rin=1/gm≈50) $A_v = \left|\frac{Z_L(j\omega)}{R_{in}}\right|$
- Inductively degenerated $G_m = \frac{1}{\omega_r L_s}$ (independent of g_m !)

$$G_m = \left|\frac{g_m}{\left(j\omega L_g + j\omega L_s - j/\omega C_{gs}\right) j\omega C_{gs} + j\omega L_s g_m}\right|$$

Noise Figure

- Resistively terminated $$NF = 10\log\left(2 + \frac{\overline{e_{n,out,q}^2}}{kTBR_s(A_v)^2}\right)$$
- Feed-back $$NF = 10\log\left(1 + \frac{R_s}{R_{fb}}\left(1 + \frac{R_{fb} + R_s}{R_{fb} - R_s}\right)^2 + \frac{\overline{e_{n,out,q}^2}}{kTBR_s(A_v)^2}\right)$$
- Common gate $$NF = 10\log(1+\gamma) \approx 3...5\,dB$$
- Inductively degenerated $$NF = 10\log\left(1 + \frac{e_{n,out,q}^2}{kTBR_s(A_v)^2}\right)$$

Linearity - IIP3

- The IIP3 for the memoryless and time-invariant system

$$A_{IIP3} = \sqrt{\frac{4}{3}\left|\frac{\alpha_1}{\alpha_3}\right|} \qquad IIP3(dBm) = 10\log\left(\frac{A_{IIP3}^2}{2R_S}\cdot 1000\right)$$

- For a MOSFET IIP3 related math goes quite complicated
  → we'll rely on simulations

- Traditional study is for BJT collector current

$$I_c = I_S e^{\frac{V_{BE}+v_{in}}{V_T}} = I_S e^{\frac{V_{Be}}{V_T}}\left[1+\frac{v_{in}}{V_T}+\frac{1}{2}\left(\frac{v_{in}}{V_T}\right)^2+\frac{1}{6}\left(\frac{v_{in}}{V_T}\right)^3+..\right]$$

$$IIP3 = 10\log\left(\frac{4V_T^2}{R_S}\cdot 1000\right)$$

Estimated IIP3 for resistively terminated and common-base BJT LNAs is **–13 dBm**

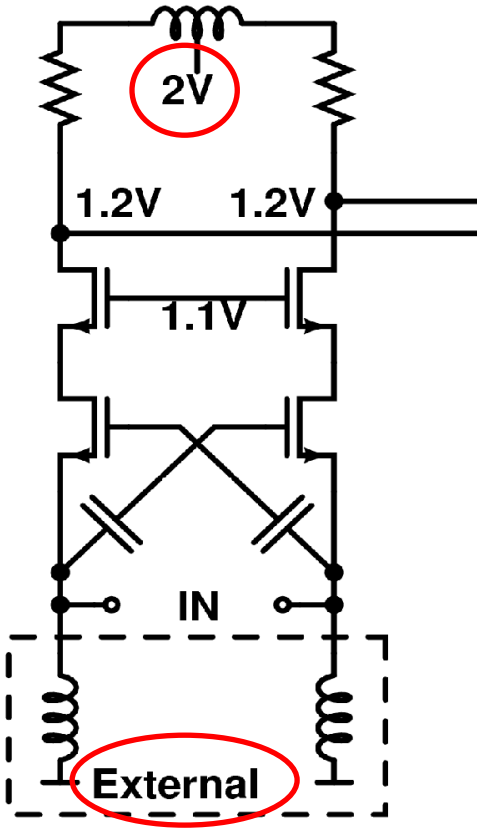
Comparison of LNA stages

	Resistive termination	Resistive feedback	Common gate	Inductively degenerated
S11	★	★	★	★
Gain	★	—	—	—
NF	💣💣	💣	💣	★
IIP3	—	★	—	★
Bandwidth	★	★	★	💣

Broadband high-linearity LNA (RX) is a BIG challenge !

Advanced Example I

CG / CS topology with cross-coupled capacitors



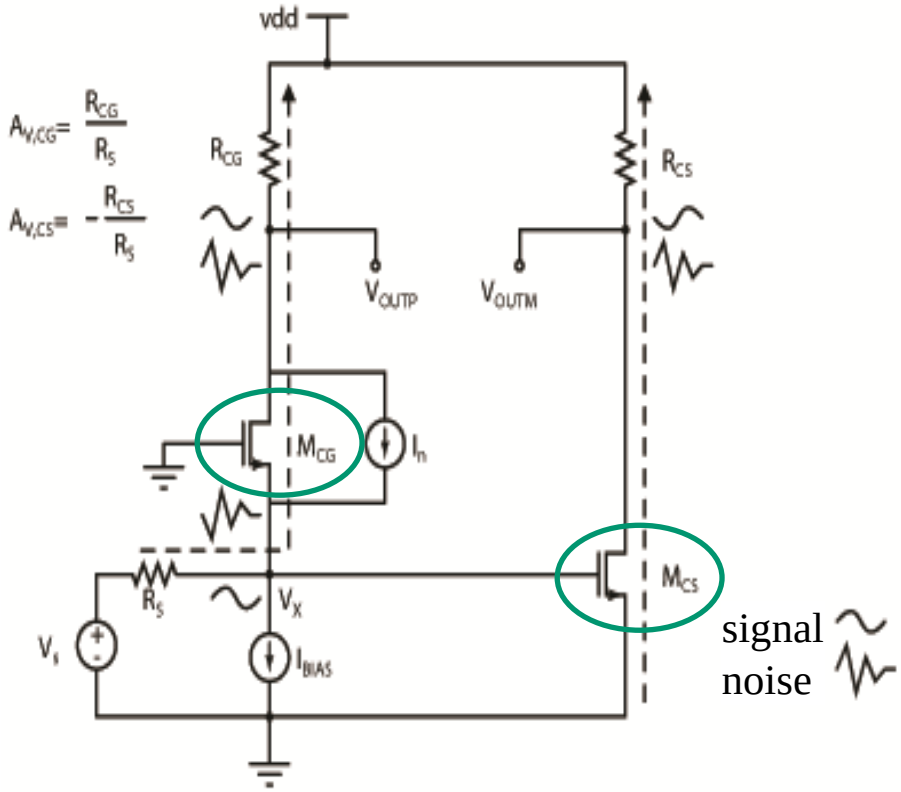
Gain	15 dB
NF	3 dB
IIP3	8 dBm
ICP	-12 dBm

20 dB diff !!

[1] W. Zhuo et al, “Using capacitive cross-coupling technique …”, ESSCIRC 2000
[2] W. Zhuo et al, ” A Capacitor Cross-Coupled Common-Gate Low-Noise Amplifier”, IEEE CAS-II, Dec. 2005
[3] J. Borremans et al, “A sub-3dB NF voltage-sampling front-end …”, ESSCIRC 2010

Advanced Example II

CG - CS topology with signal summing

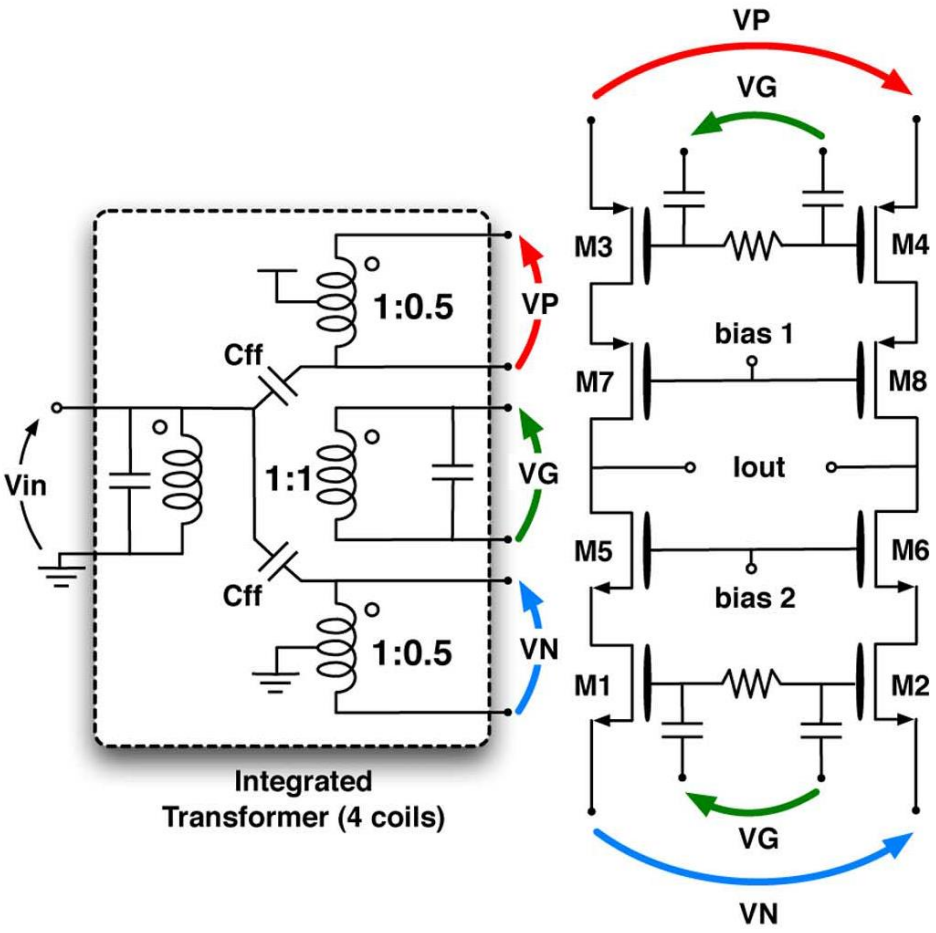


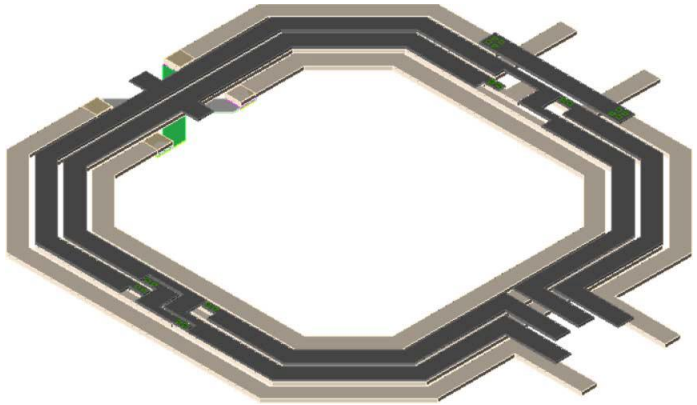
Frequency range	0.7 - 2.6 GHz
Gain	7 dB
NF	5 dB
IIP3	6 dBm
ICP	-7 dBm
power cons.	24 mW
Vdd	1.2 V (or even less)

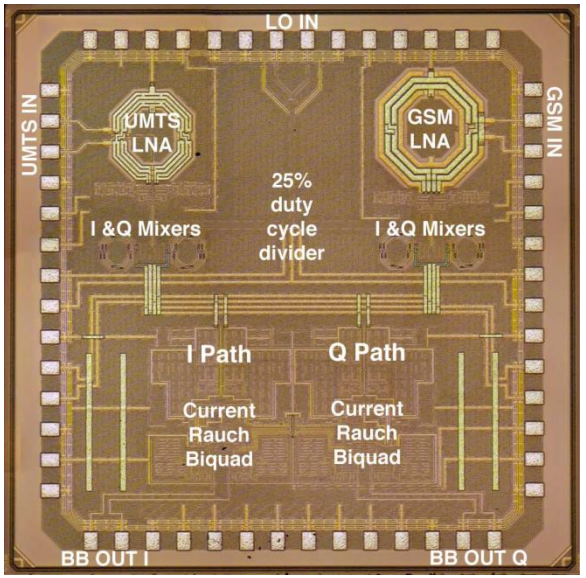
[1] S. C. Blaakmeer et al, "Wideband balun-LNA …," IEEE J. Solid-State Circuits, June 2008
[2] J. Jussila et al, "A 1.2-V highly linear balanced noise-cancelling LNA …," IEEE J. Solid-State Circuits, March 2008
[3] K. Stadius et al, " A 0.7 - 2.6 GHz High-Linearity RF Front-End for Cognitive Radio Spectrum Sensing," ISCAS 2011

Advanced Example III

I. Fabiano, M. Sosio, A. Liscidini, R. Castello, "**SAW-Less Analog Front-End Receivers for TDD and FDD**",
IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 48, NO. 12, DECEMBER 2013



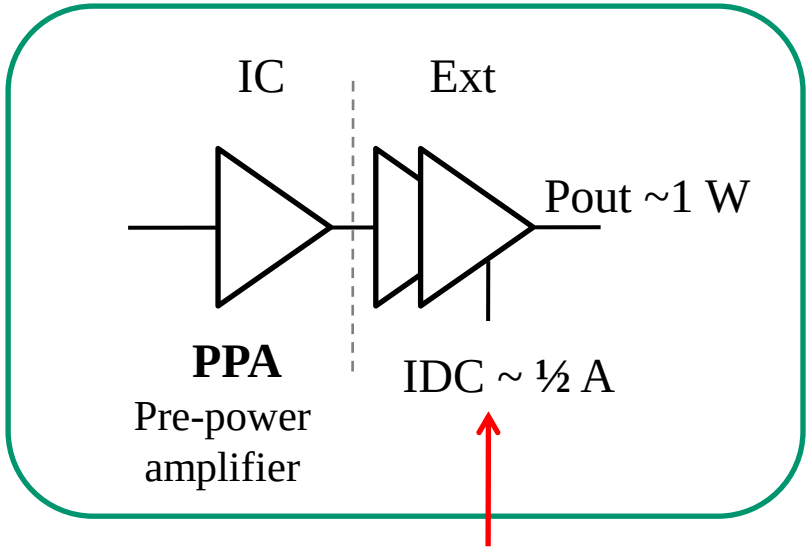




Break

Power Amplifiers

- PA is an amplifier, which has significant output power
  → cannot be treated as a small-signal amplifier
- PA design differs significantly from the other RF IC building blocks:
  - Large signal behavior
  - thermal effects
  - Wiring & transistor size, layout
  - Packaging & Interconnections
  - breakdown voltages



Large current
→large FET
→ large die area
→ expensive IC

Topics

- Figures of Merit
- Classes of Operation (A, B, AB, C, D, E, F, S)
- Comparison on PA classes

Figures of Merit

- PA must deliver a sufficient power to the antenna with good efficiency and appropriate linearity.
- Available current through the transistor, supply voltage and load impedance effect on the output power.

$$P_L = V_{OUT,RMS} \cdot I_{OUT,RMS}$$

$$R_L = \frac{V_{OUT,RMS}^2}{P_L}$$

Figures of Merit

- Efficiency
  - Describes how effectively the power amplifier transforms the power taken from supply as signal power
  - How much of the supply power transforms as unwanted heat

$$\eta = \frac{P_{OUT}}{P_{DC}}$$

Figures of Merit

- Efficiency
  - Describes how effectively the power amplifier transforms the power taken from supply as signal power
  - How much of the supply power transforms as unwanted heat

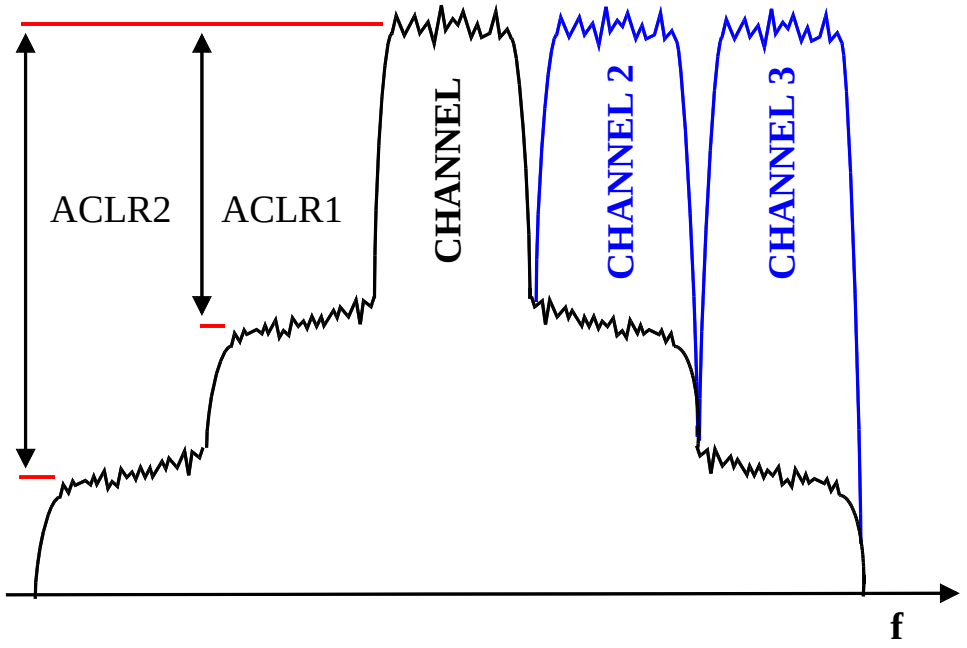
$$\eta = \frac{P_{OUT}}{P_{DC}}$$

  - Efficiency does not take into account the input signal
  - Power added efficiency (PAE) does take it into account

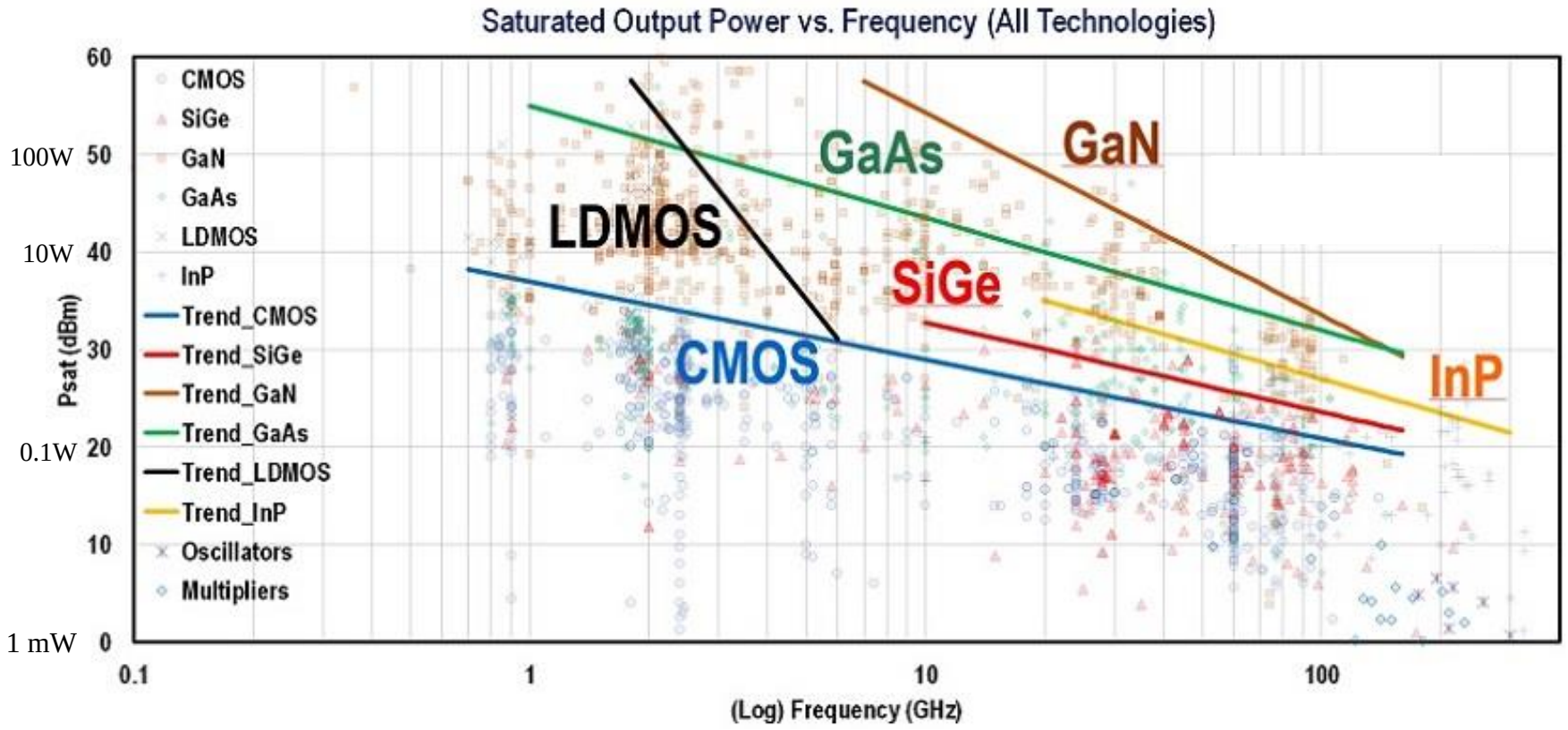
$$PAE = \frac{P_{OUT} - P_{IN}}{P_{DC}} = \frac{P_{OUT}}{P_{DC}}\left(1 - \frac{1}{G}\right) = \eta\left(1 - \frac{1}{G}\right)$$

Linearity Requirements

- Use a modulated signal as input signal and examine its behavior at PA output.
- Signal spreading is characterized with **adjacent channel leakage ratio** (ACLR).



PA Technologies



LDMOS = laterally diffused MOSFET, most common discreate RF PA

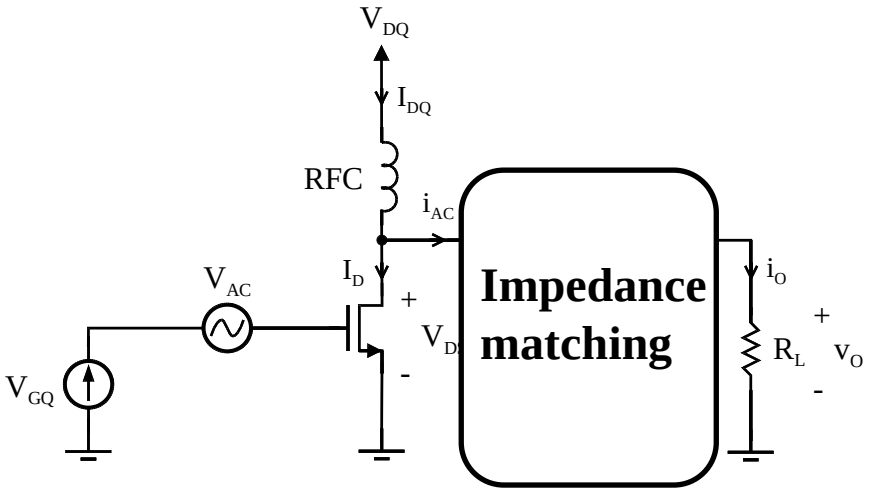
Hua Wang, Tzu-Yuan Huang, Naga Sasikanth Mannem, Jeongseok Lee, Edgar Garay, David Munzer, Edward Liu, Yuqi Liu, Bryan Lin, Mohamed Eleraky, Hossein Jalili, Jeongsoo Park, Sensen Li, Fei Wang, Amr S. Ahmed, Christopher Snyder, Sanghoon Lee, Huy Thong Nguyen, and Michael Edward Duffy Smith, "Power Amplifiers Performance Survey 2000-Present," [Online]. Available: https://gems.ece.gatech.edu/PA_survey.html

Power Amplifier Classes

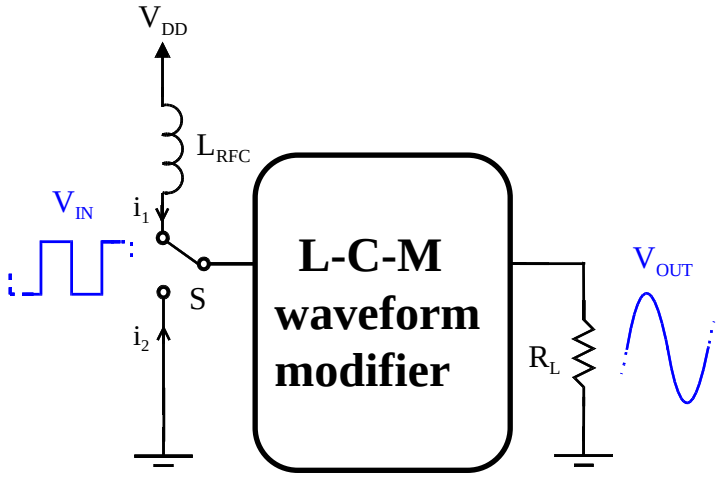
Current mode
”Linear PA”

Switching mode
”Non-linear PA”

Class **A** | Class **B** | Class **C** | Class **D** | Class **E** | Class **F** | ••• | Class **S**

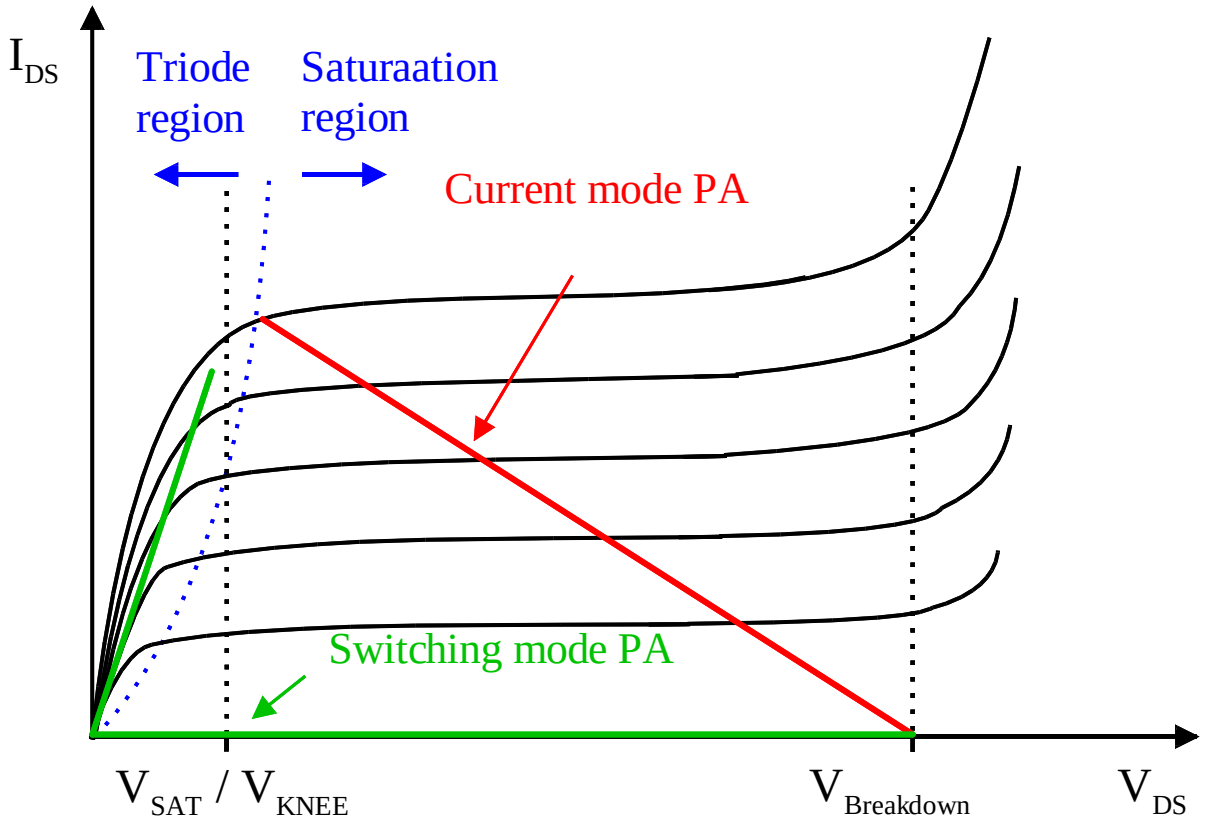


”Ordinary” amplifier,
Idrain off only for a while

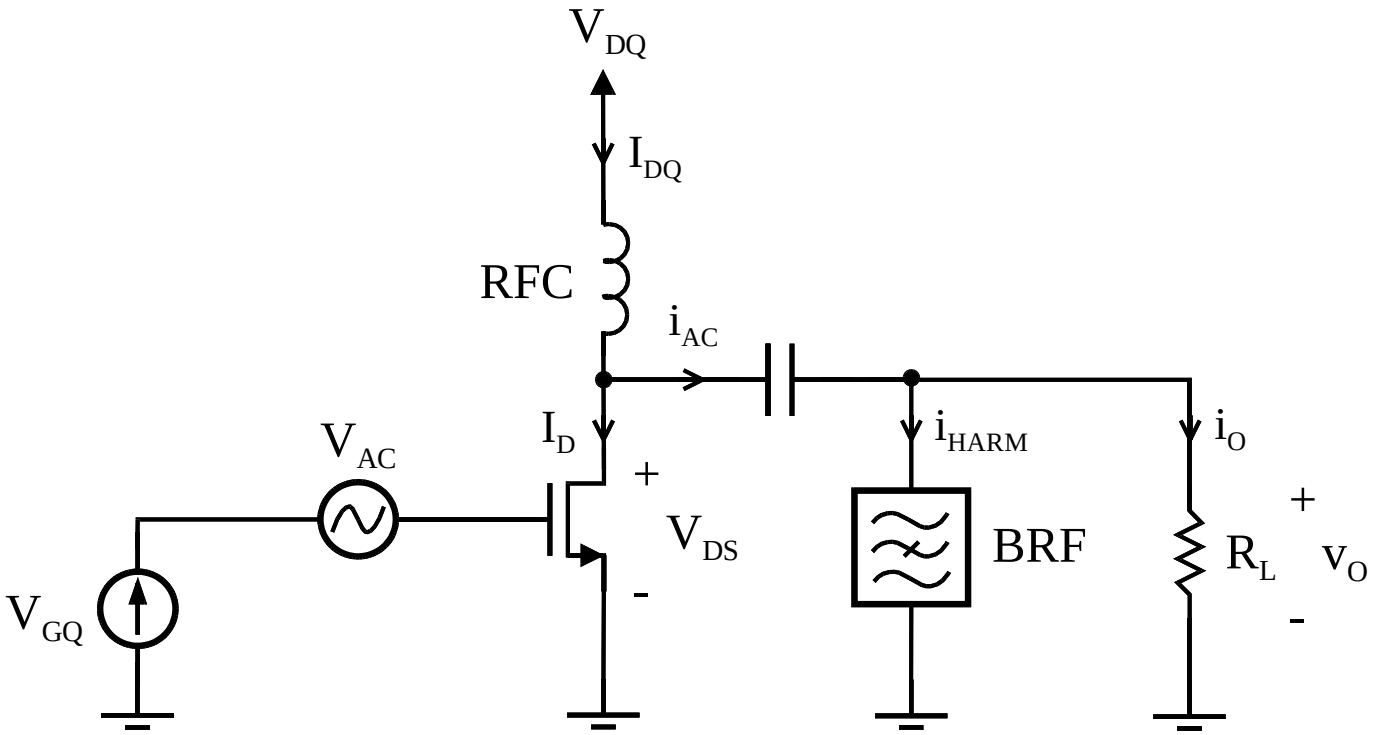


Transistor is a switch
Idrain on-off
Output network modifies signals

Operation Principles

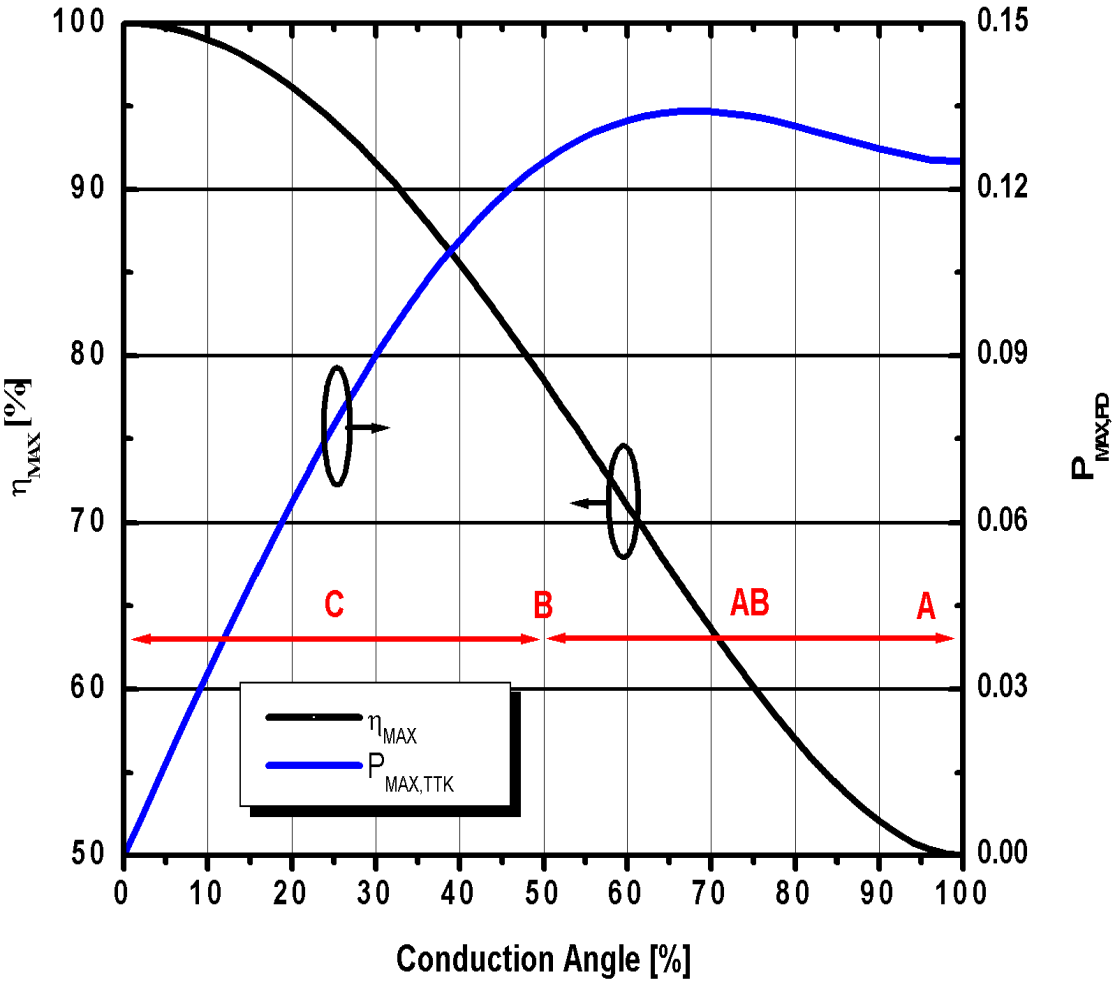


Linear PA (class A, B, C)



Class A: conduction angle 100% (I_{DD} flows all the time)
Class B: conduction angle 50%
Class C: conduction angle → 0%

Linear PAs


100
90
80
70
60
50
0.15
0.12
0.09
0.06
0.03
0.00
0
10
20
30
40
50
60
70
80
90
100
η_{MAX} [%]
$P_{MAX,PD}$
Conduction Angle [%]
C
B
AB
A
η_{MAX}
$P_{MAX,TTK}$

Class A

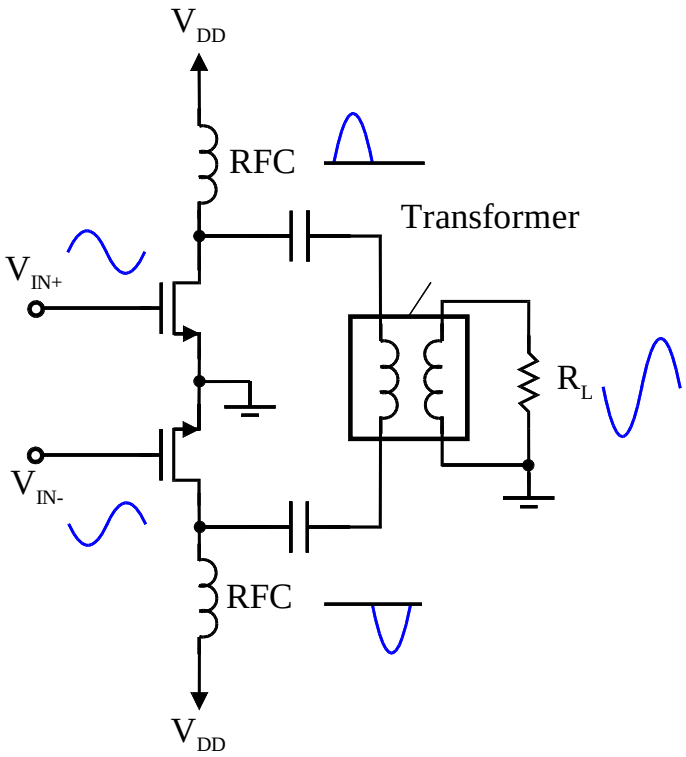
- Conduction angle 100%
- 50% efficiency is reached at maximum output power
- Rapid degradation in lower powers
- Consumes significant power without input signal

Class B

- Conduction angle 50% $\rightarrow$ lower DC power
- maximum efficiency 78,5%
- Slower degradation in lower powers
- Gain 2-6 dB lower compared to class A

Class B push-pull

- Linearity of class B PA can be improved by using a push-pull topology
- Each PA branch must produce only half of the output power →relaxes the design of output matching network
- Optimum output load resistance of each branch is double
- Requires additional inductors



Class C

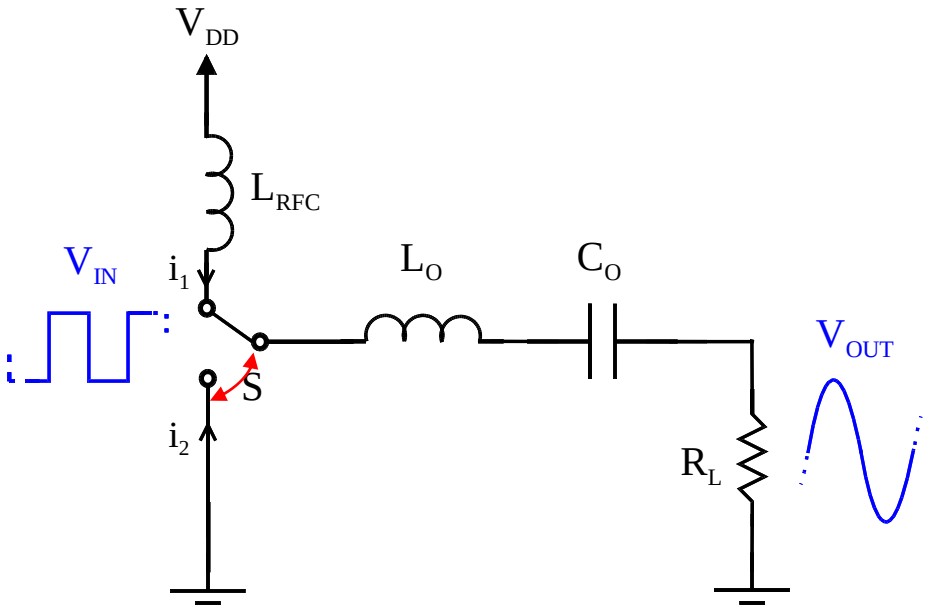
- Conduction angle 0% - 50% $\rightarrow$ low DC power
- In ideal case PA has a negative biasing point $\rightarrow$ reverse breakdown voltage requirement
- Nonlinear
  - Class C PA is most suitable for phase modulation systems.
- Class C PA can be designed using similar equations as class A and B PAs.

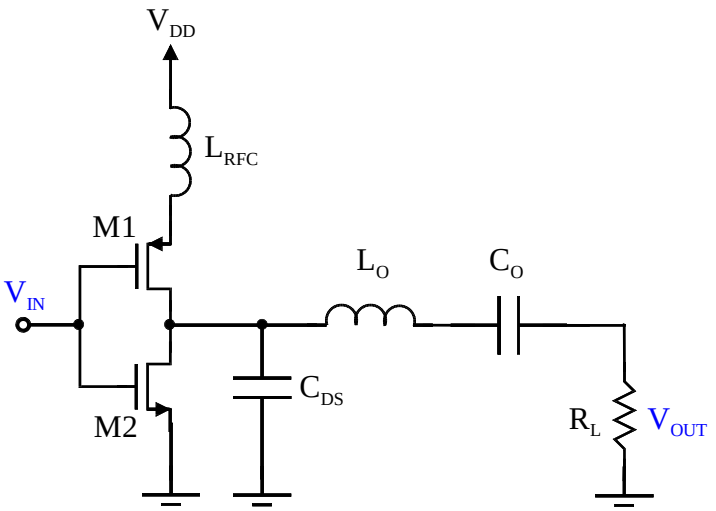
Nonlinear PAs

- Class D, E, F, and S power amplifiers
- In high efficiency PAs the design principle is to minimize the voltage-current product over the transistor.
- The losses degrading efficiency arise from transistor nonidealities (internal capacitors, resistors, finite rise and fall times) and from losses in matching networks and losses to substrate.

Class D

- PA includes switch S, series resonator (L_o, C_o, and R_L) and biasing inductor L_{RFC}.





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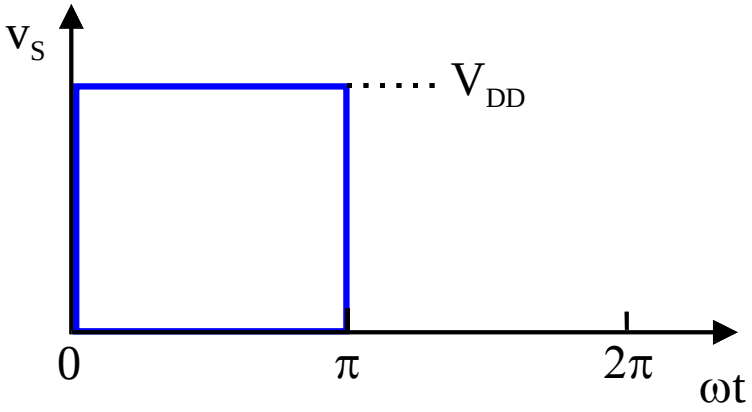
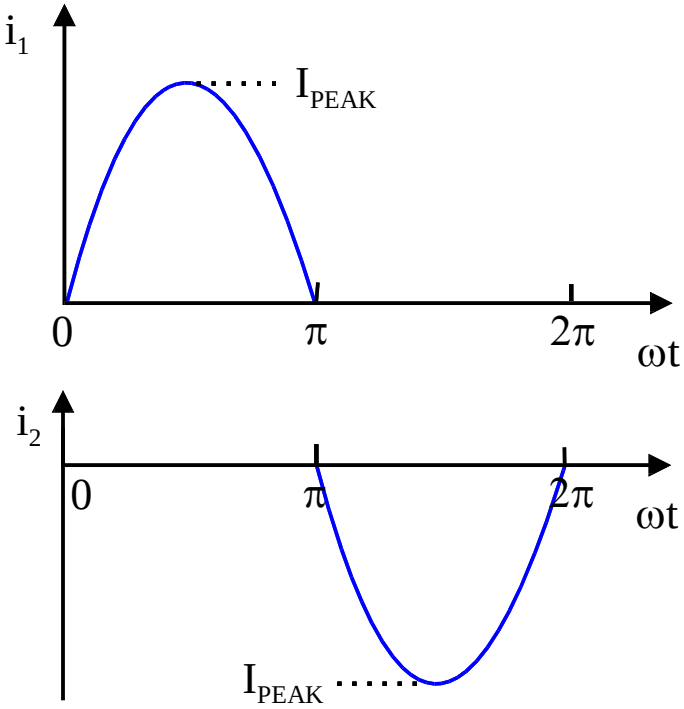
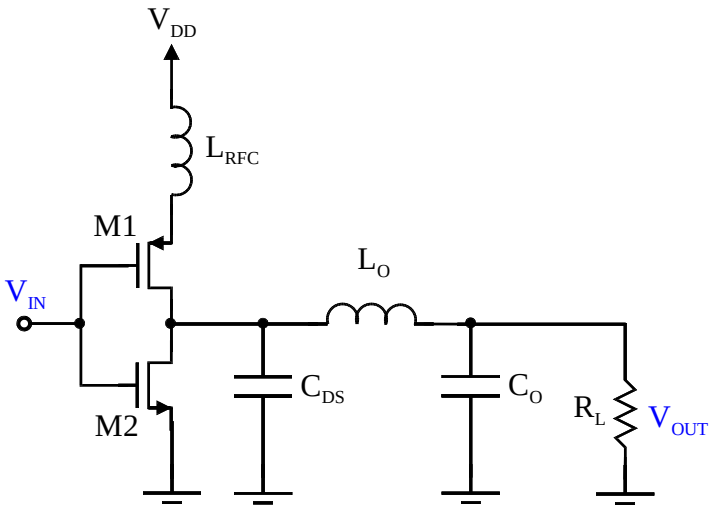
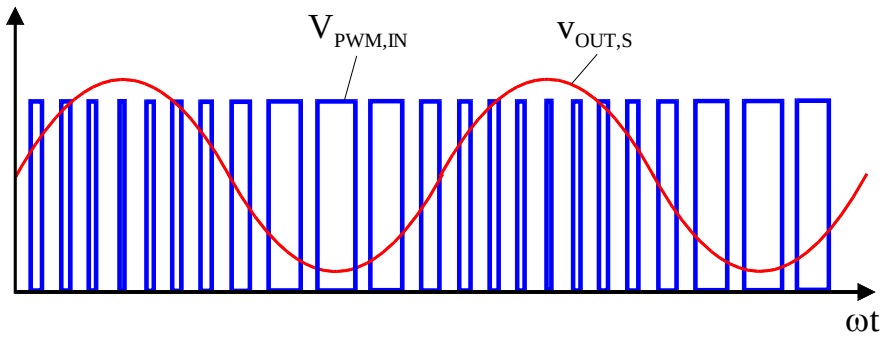




Class S

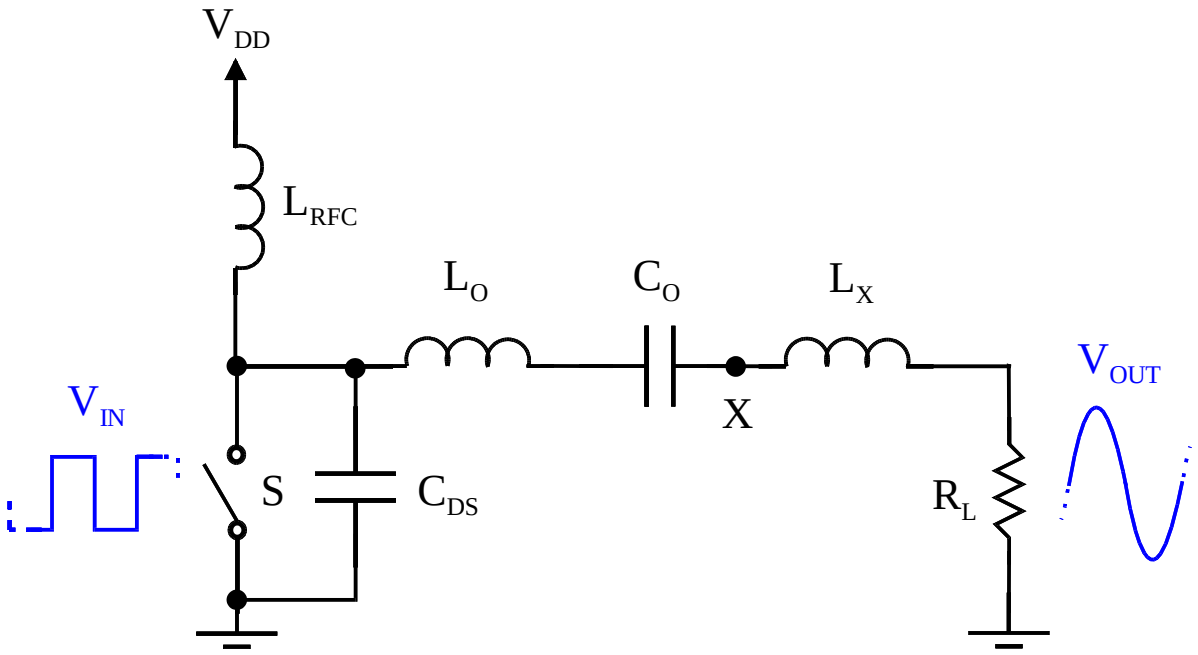
- Class S PA is identical to class D PA when comparing its analysis and design equations.
- Difference in these PAs is in the topology.
- Applications of class S PA can be typically found from audio frequency amplifies.





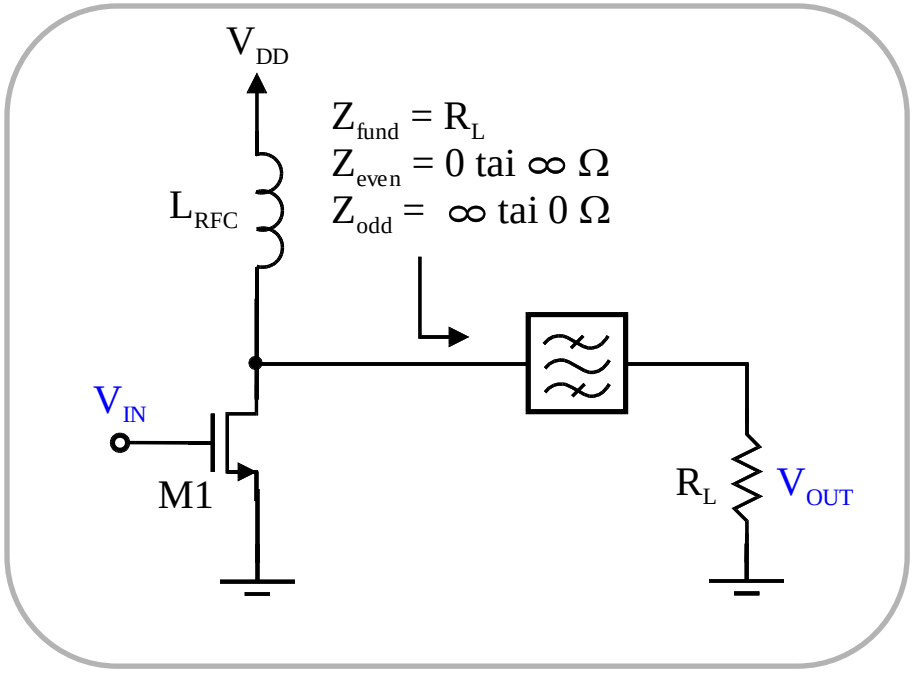
Class E

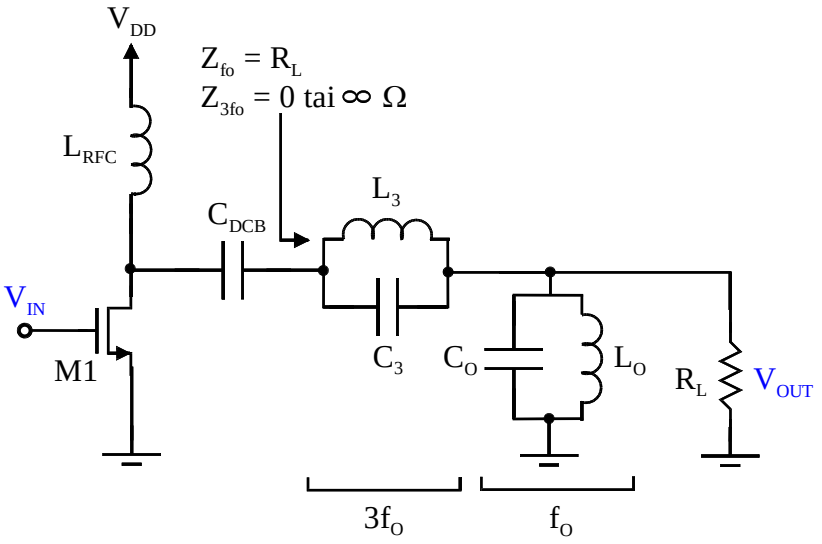
- Operation principle of the class E PA is to minimize the losses caused by the nonidealities of switch.



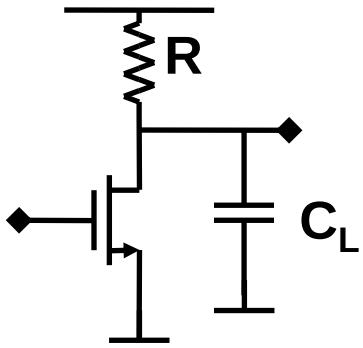
Class F

- In class F PA the efficiency is increased by using harmonic resonators to modify the output current and voltage waveforms
  - Adding harmonics to transistor current and voltage waveforms the transistor waveform begins to approach the ideal switch waveform





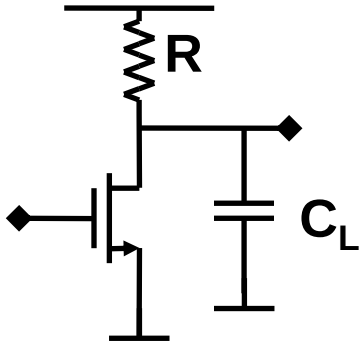
Buffers



How to drive large devices i.e. low-impedance nodes ?

- High gain = large R, but C_L in parallel → low gain
- Driving capability ~ $\frac{I_{bias}}{\omega C_L V_{sig}}$

Buffers



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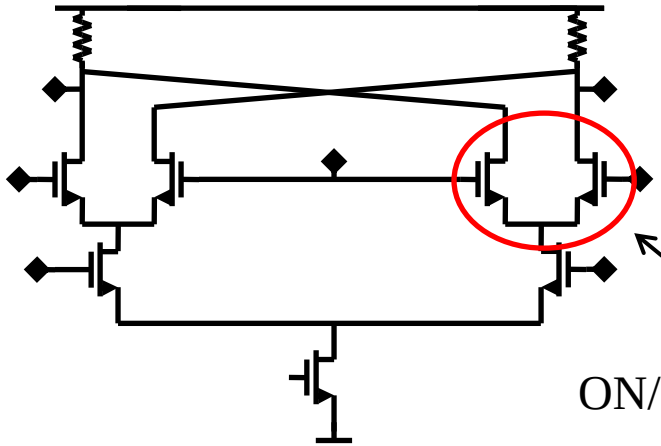
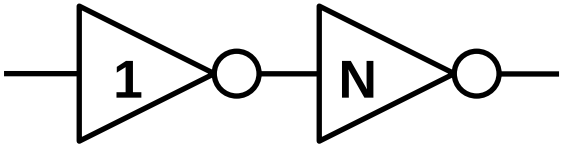
Examples



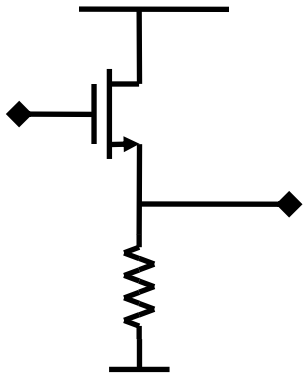
ON/OFF driven large switches

What is the maximum N?

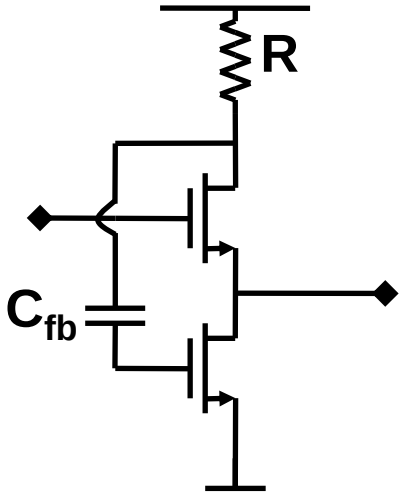


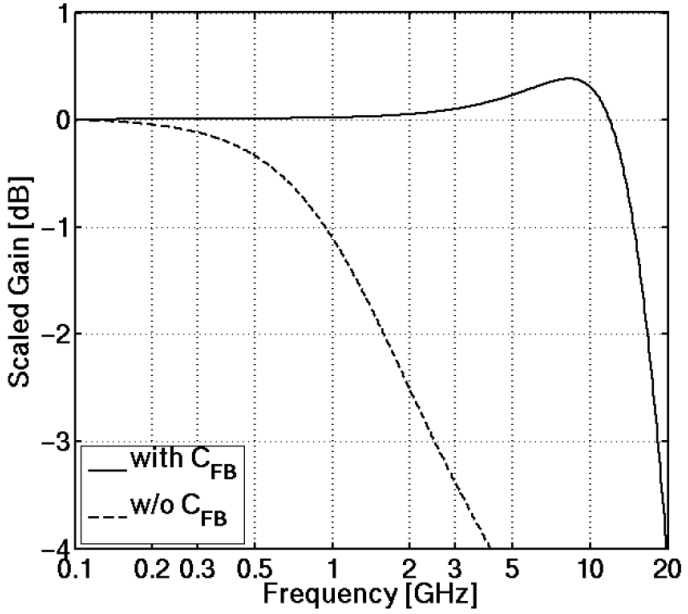
Buffers

Source follower



Super source-follower





$$voltage\ gain \approx 1$$

$$R_{out} \sim 1/g_m + caps$$

BTW, you can almost always replace resistor R with a FET
i.e. active load or current source.

Self-Learning Assignment 3

Objectives are to familiarize yourself with

- typical RF IC LNA design issues
- doctoral dissertation on the RF IC field

You can find the assignment from

MyCourses / Assignments - SLA / Self-learning assignment 3

Return your answer as a pdf-file to Return Box in the same page

Next Meeting Tuesday 18.4.

Topics will be

- concepts related to mixers
- active mixers
- passive mixers
- examples