ELEC-E9210 Organic Electronics: Materials, Devices & Applications

Organic Field-Effect Transistors I

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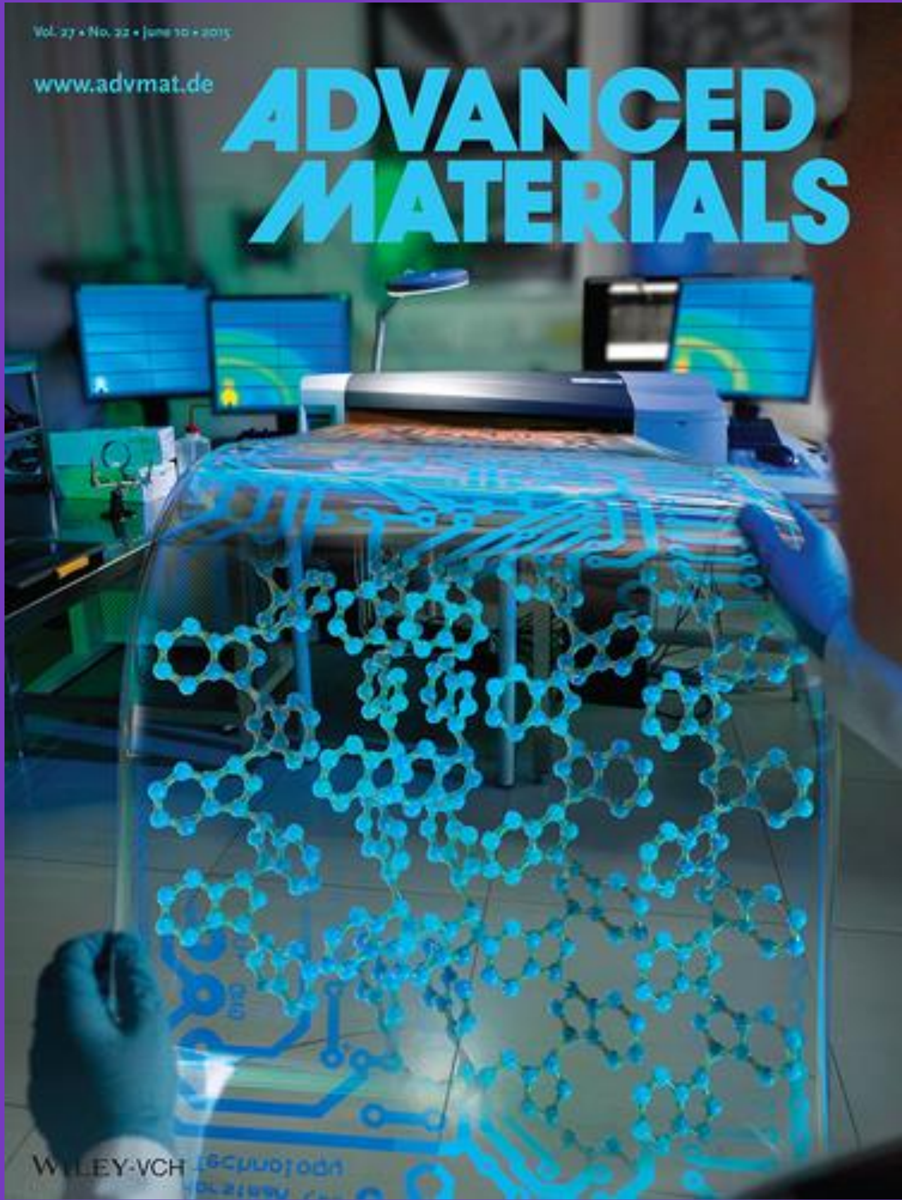


Today´s Class: Organic Field-Effect Transistors

Previously…

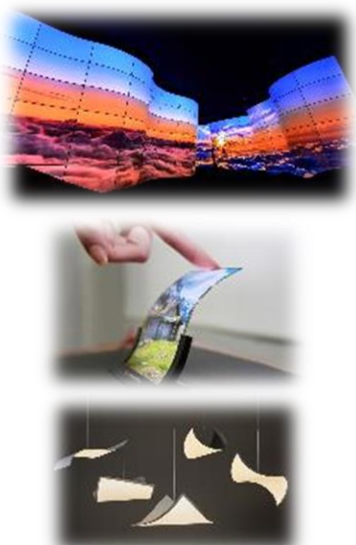
- organic semiconductors electronic properties are strongly affected by ***molecular assembly/surface organization*** and amount of ***disorders*** (mobility depends from these parameters)
- excitation in organic materials can lead to ***emission of light*** (fluorescence, phosphorescence)
- organic materials ***morphology*** and ***packing*** are crucial in understanding and engineering ***electrical*** and ***optical*** properties

Today

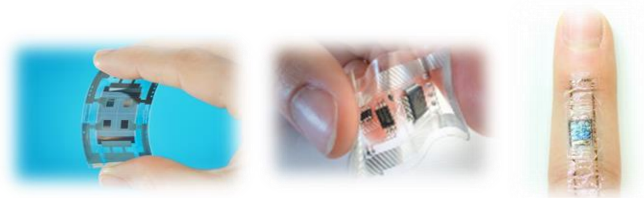
- Basic ***working principle*** of organic *field-effect* ***transistor*** and main features
- ***Building blocks*** of organic transistor and how to engineer those to improve

Organic Electronics Domains

Light Emitting Devices



Photodiodes & (Bio)Sensors

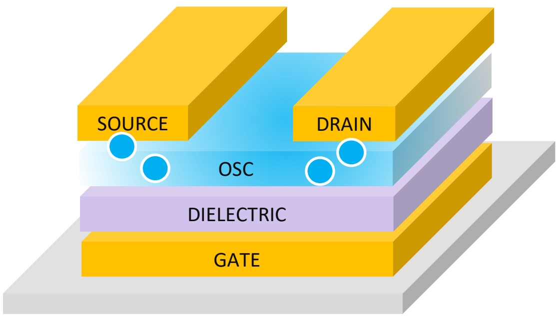


Wearable/Flexible Electronics

Solar Cells

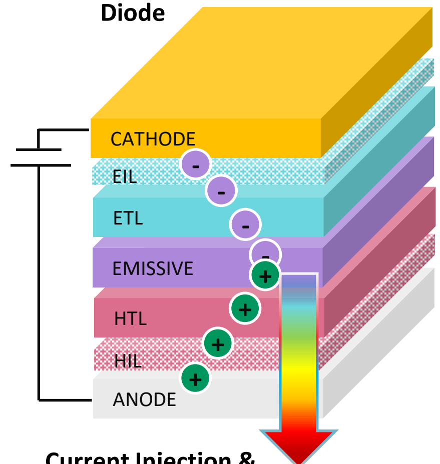
Key (Organic) Electronics Devices

Transistor



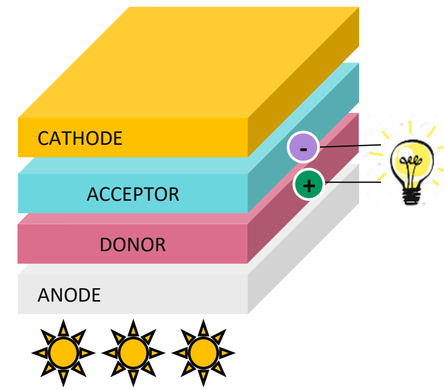
Field-Effect Transport (FET)
(*w/* Light Emission)

Diode



Current Injection &
Light Emission

Solar Cells



Light Absorption &
Charge Collection

- fundamental mechanism are similar to inorganic counterparts
- interfaces are crucial for device functioning

Organic (Field-Effect) Transistors

OFET or OTFT?

transport mechanism

OFET: Organic Field-Effect Transistor
OTFT: Organic Thin Film Transistor

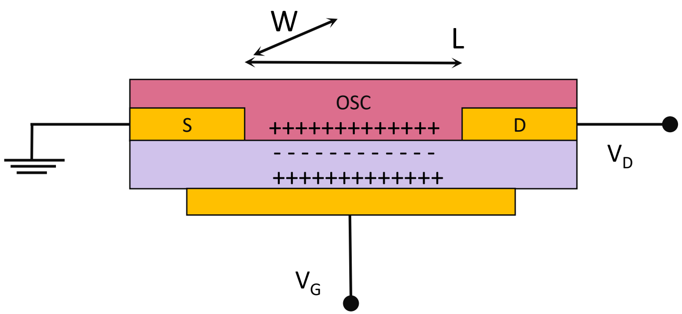
configuration of the active material

transistor device is based on *field-effect transport*, but there is no strict limitation on the nature of the active materials (*i.e.* thin film, large crystals, …)

FET: Organic *vs.* Inorganic

- different structures (lattice *vs.* orbitals)
- similar concepts but possible different behavior
- transistor:
  - → similar fundamental principles
  - → fabrication techniques might be different

(Organic)Field-Effect Transistor (OFET)



- ***3 terminals*** device (S, D, G)
- ***channel length, L*** (distance S & D) 10-100s µm
- ***channel width, W*** (distance between S and D- orthogonal to L (~several mm)

Application of gate bias induces polarization at the interface → current can flow between source and drain (no traps/Ohmic contact)

capacitance/unit area

$$Q_{mob} = C_i[V_G - V_{th} - V(x)]$$

induced mobile charge at distance x from S

threshold bias at which current starts to flow (device is ON)

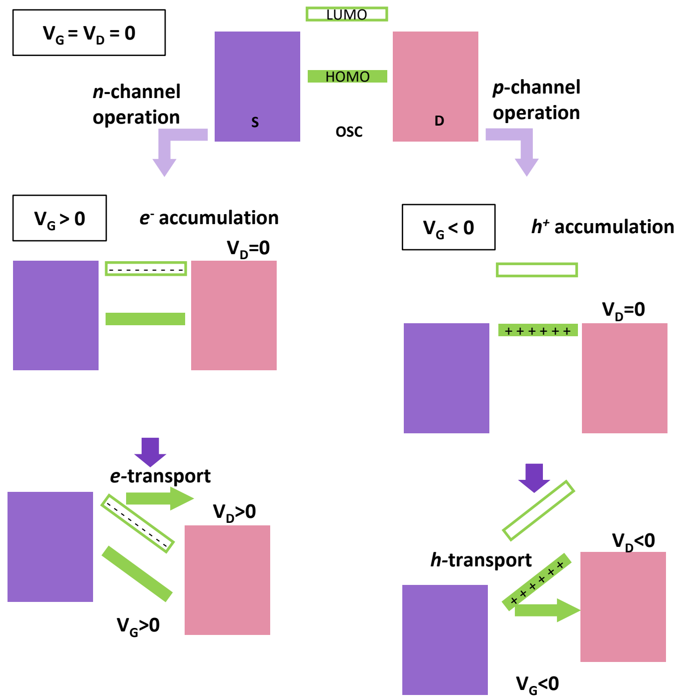
$E_x = {}^{dV}/_{dx}$

$$I_D = W\mu Q_{mob} E_x$$

$$\rightarrow I_D dx = W\mu Q_{mob} dV = W\mu C_i[V_G - V_{th} - V(x)]dV$$

$$I_D = \int_0^L I_D\, dx = \frac{W}{L}\mu C_i\left[(V_G - V_{th})V_D - \frac{1}{2}V_D^2\right]$$

(O)FET: *p-* & *n-* Transport

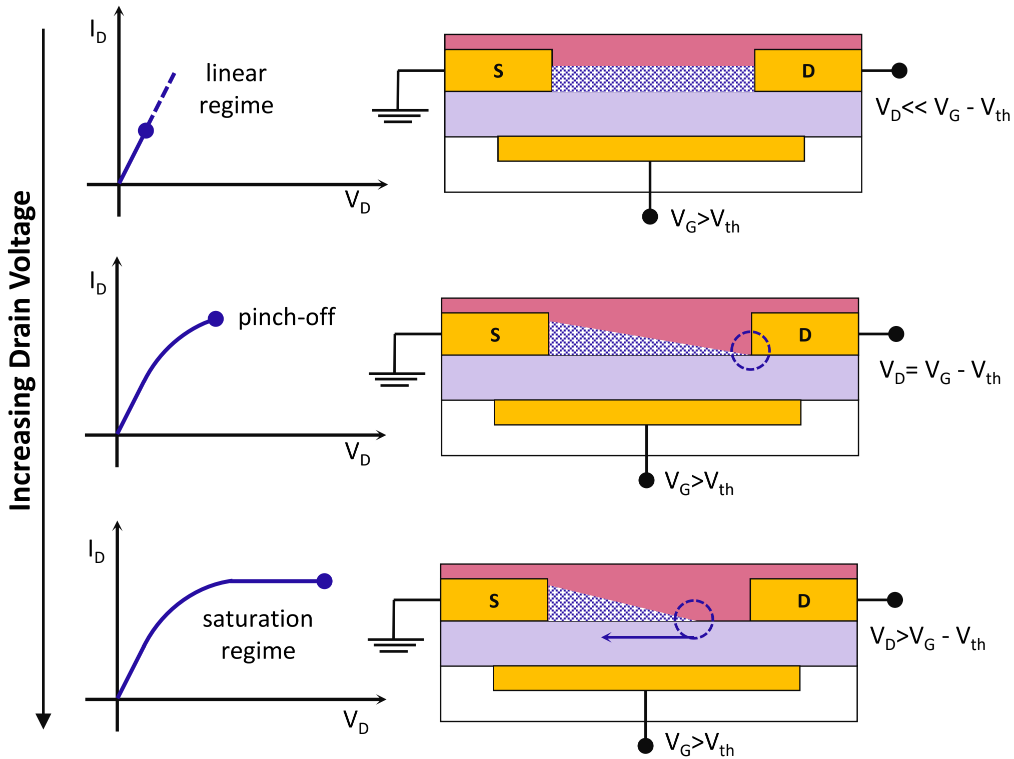


energy level diagram for an transistor in OFF state
($V_G = V_D = 0$)

electric field draws positive charges from the source into a narrow (≤ few nm) region, next to the dielectric
→ charges accumulate in the narrow interfacial OSC region

$V_D < 0$ → current starts to flow, however due to OSC traps, these first injected charges will fill the traps
$V_G > V_{th}$ → accumulation layer can actually flow and contribute to the transistor current

(O)FET: Conduction Regimes



charge carrier concentration gradient
(Ohm´s law with $Q_{mob} = C_i\,(V_G\text{-}V_{th}\text{-}V(x))$)

$$I_{D,lin} = \frac{W}{L}\,\mu\, C_i(V_G - V_{th})\,V_D$$

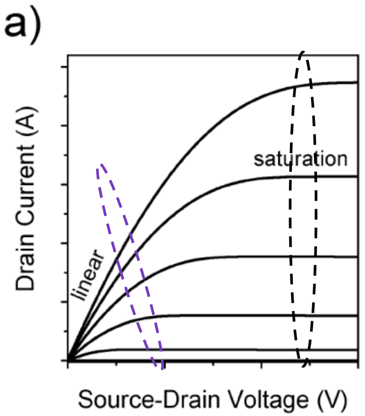
mobile charges concentration reduces to zero at x = L (drain). Transistor is *pinched off.*

pinch-off point moves towards S, shortening L and narrowing the depletion zone near D. Current flows within the channel and remains constant

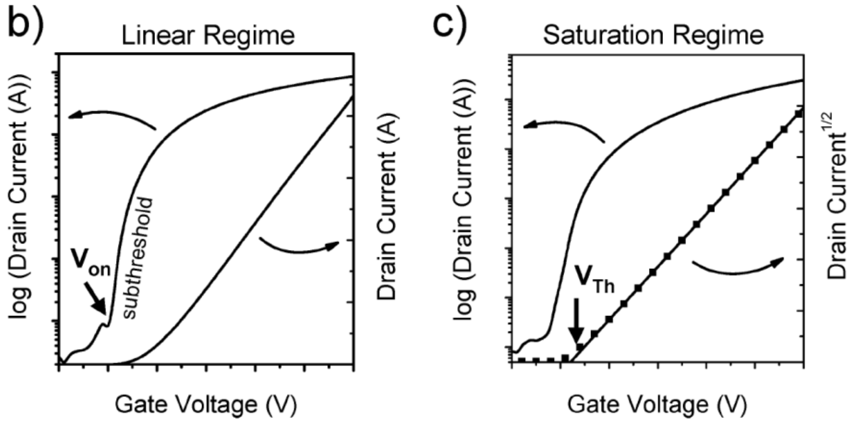
$$I_{D,sat} = \frac{W}{2L}\,\mu\, C_i(V_G - V_{th})^2$$

(O)FET Characteristic Curves

Output Characteristics
(I_D-V_D sweep)



Transfer Characteristics
(I_D-V_G sweep)



linear: current increases with voltage (Ohm´s law)

saturation: current reaches a maximum value prior to leveling with increasing applied voltage

subthreshold regime: device is turning from OFF (low-current) to ON (high-current)

high V_G-regime: slope of $I^{1/2}$ can be used to estimate OSC mobility

Chem. Rev. **107**(4), 1296 (2007)

(O)FET Parameters: Mobility & Threshold

Mobility, μ

charge carriers move accordingly to the direction of the applied electric field (depending on the sign of the charge)

$$\boldsymbol{v} = \mu \boldsymbol{E} \qquad [\mu] = [cm^2 V^{-1} s^{-1}]$$

this relation is not linear in the limit of high field and depends on charge carrier concentration

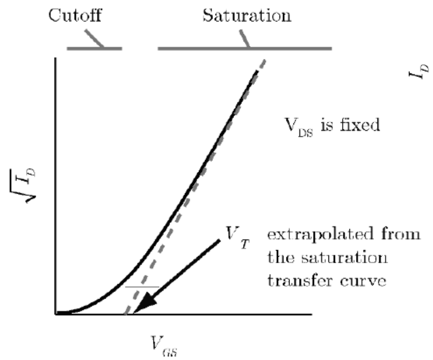
$$\mu = \frac{velocity}{E} = \frac{I_D}{QWE} = \frac{I_D L^2}{C(V_{GS} - V_{th}) V_{DS}}$$

$$Q = \frac{C\,(V_{GS} - V_{th})}{WL}$$

Threshold Voltage, V_{th}

bias for the onset of charge accumulation (bias at which inversion in the channel is achieved)

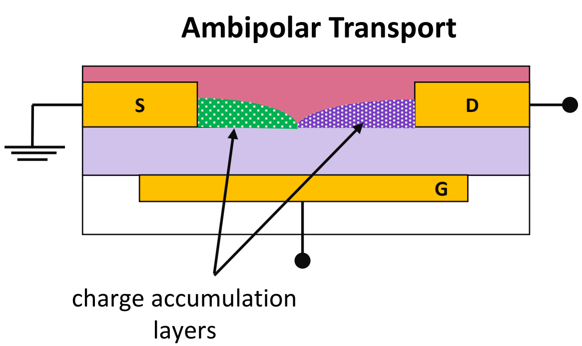
$$I_D = \frac{W}{2L}\,\mu\, C_i (V_G - V_{th})^2$$

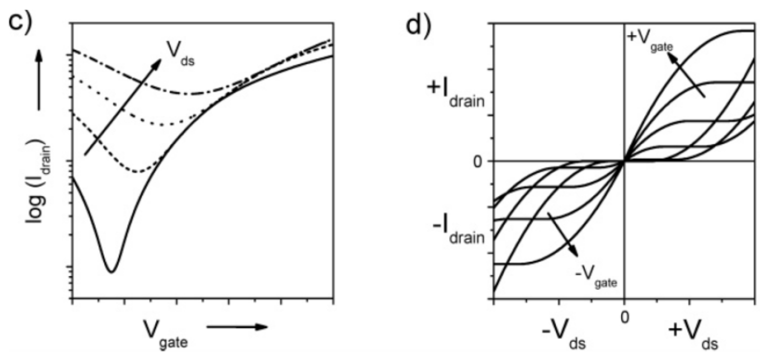


- small currents might flow below V_{th}
- linear/saturation might not closely follow a linear relation
- dependent on choice of linear region

OFET: Ambipolar Behavior

Due to the nature of the molecular orbitals and defects, an organic semiconductor can ***conduct both charge carriers (ambipolar OSC)***





Chem. Rev. **107**(4), 1296 (2007)

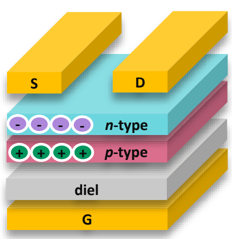
$$|I_{DS}| = \frac{WC_i}{2L}\left\{\mu_e\left(V_G - V_{th,e}\right)^2 + \mu_h\left(V_D - \left(V_G - V_{th,h}\right)^2\right)\right\}$$

Ambipolar OFET shows an overall behavior which is an ***overlap between p-*** and ***n-type*** charge transport regimes

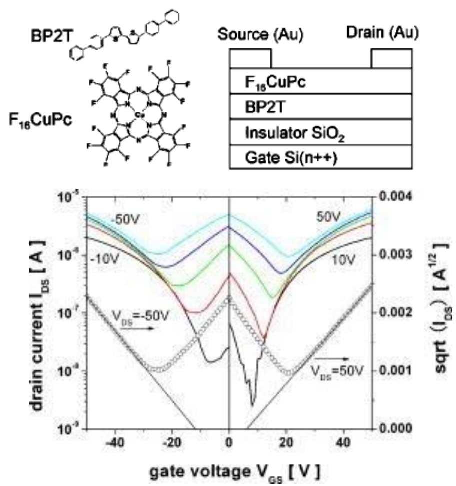
Ambipolar OFET: Configurations

Ambipolar behavior in transistor can be mainly reached though three approaches:
single ambipolar material, ***bi-layer*** and ***blend*** structure

bi-layer

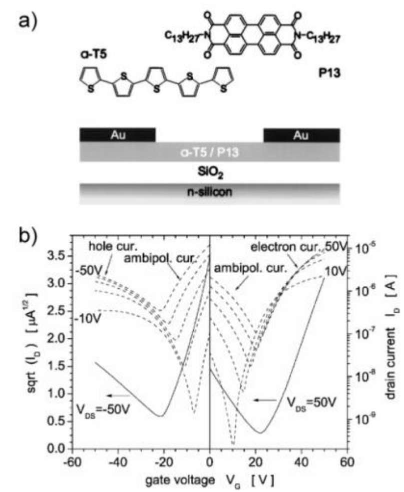


solution-processed bi-layer are challenging to fabricate (solvents compatibility)



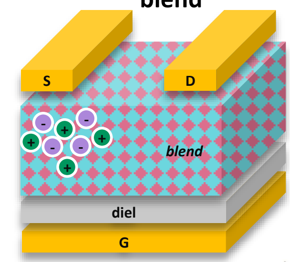
Appl. Phys. Lett. **88**(13), 133508 (2006)

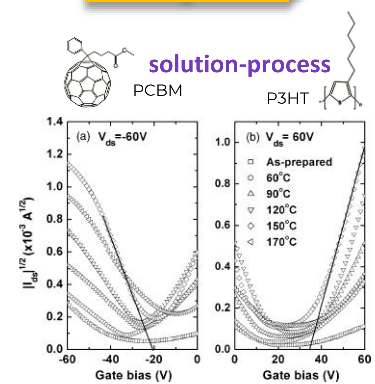
co-evaporation



Appl. Phys. Lett. **85**, 1613 (2004)

blend





J. Appl. Phys. Lett. **89**, 153505 (2006)

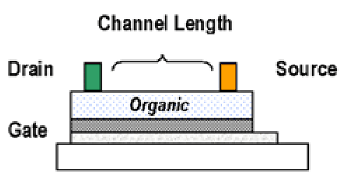
presence of both charges can lead to exciton formation and radiative decay

Vertical OFET (*v*-OFET): A New Concept

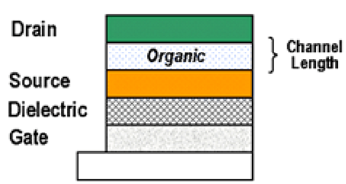
channel length is defined as the ***OSC thickness*** between (stacked) source and drain → nm scale channel length

- by reducing transistor dimension, number of devices in a chip can be (exponentially) increased (Moore's law)
- transistor speed in the 100s GHz range

OFET *vs.* (V)OFET



- applying V(G-S) → charge density at the OSC/dielectric interface is modulated, switching the device from ON to OFF-state (accumulation → depletion)
- electric field between D and S pulls the charge carriers toward the drain, thus leading to net drain current



(VOFET) transport is no longer limited to OSC/diel interface but becomes distributed, with contributions in lateral and vertical direction to the gate insulator interface

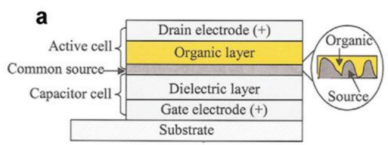
flexible applications
(bending radius does not affect transistor properties)

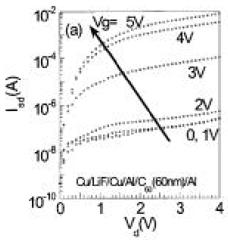
VOFET Structure & Properties

Controlling the barrier if the electric field (G) is not completely screened by the free charge in the S

- electrodes thickness of ≤1nm
- *discontinuous* source electrode

rough metal electrodes

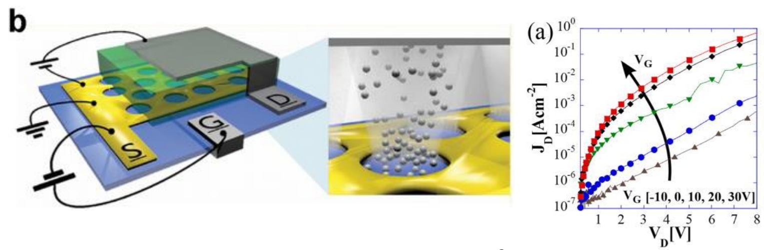




Appl. Phys. Lett. **85**, 5084 (2004)

V-OFET with low working voltage (<5V), high current output (up to 4A/cm^2) and high ON/OFF ratio (4×10^6)

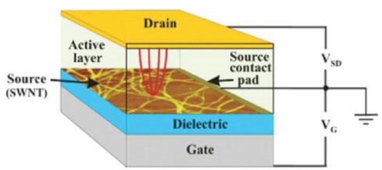
(nano)patterned electrode

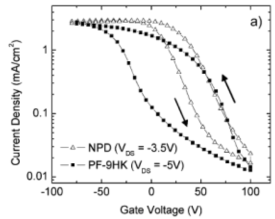


V-OFET exhibits *n*-type ON/OFF ratio >10^3, current density >50mA/cm^2 @V_{DS} = 5 V, as well as *p*-type operation

Appl. Phys. Lett. **100**, 263306 (2012)

SWNT network

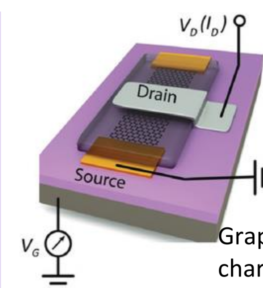


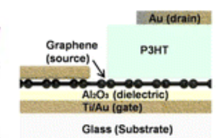


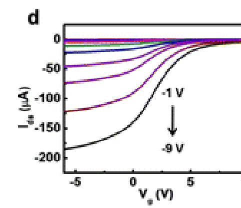
Adv. Mat. **20**(19), 3605 (2008)

SWNT-network VOFET with transfer characteristics for PF-9HK and NPD-based device

graphene







Graphene-P3HT-Au VOFET on glass with (d) transfer characteristics (−1→−9 V, 1V steps)

ACS Nano **9**, 11, 11102 (2015)

Summary

Today´s Class

- Basic ***working principle*** of organic field-effect transistor and some characteristics

Next

- ***Building blocks*** of organic field-effect transistor
- ***Applications*** of **organic field-effect transistors**