ELEC-E9210 Organic Electronics: Materials, Devices & Applications

Organic Field-Effect Transistors II



organicelectronics.aalto.fi



Today's Class

Previously

• basic working principle of organic field-effect transistor and main features

Today's class

• building blocks of organic transistor and how to engineer those to improve



OFET in Brief



- 3 electrodes (S, D, G)
- horizontal field-effect





OFET Configuration(s)



- is any fabrication process interfering/affecting OSC properties (*i.e.* electrode fabrication)?
- OSC packing and film parameters (*i.e.* mobility) depends on the underlying surface
 - interface(s) become crucial

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OFET: Top vs. Bottom Contacts



Contact resistance also changes based on underlying growth surface and the electrode



OFET: Improving Contacts with SAM

Self-Assembled Monolayer (SAM) can be used to improve (bottom) contacts, while enhancing adhesion and/or affinity t=2nm



thiols attach to Au, Pt and other metals and creates low-surface energy layer on electrodes (thin enough to allow tunneling)

SAM can be selective:

- attachment selectivity
- cross-linking
- hydrophobic/hydrophilic nature
- amine termination
- fluorination
- selective tail reactivity









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Different morphology of pentacene depending on the presence of SAM (p-6P) on underlying surface



OFET: Gate Dielectric

Charge redistribution at the dielectric surface can affect the properties of adjacent materials (electronic states and transport)



Carrier mobility depends on device features and OSC/diel interface:

- W, L, dielectric geometry and properties (C_i)
- conduction regime (linear and/or saturation)

 V_{th} strongly depends *dielectric/OSC interface* due to *impurities* and *charge trapping sites* tend to increase this value. V_{th} can be modulated through value of C (tuning charge density at interface)



Temperature dependence of the mobility in single-crystal rubrene FETs with six different gate dielectrics ($@V_G^{\sim}-15 \text{ V}$)



OFET: SAM as Gate Dielectrics

SAM: ultimate thinnest gate dielectric with high capacitance and low leakage current



Schematics and electrical characterization of (left) capacitor-like structure and (middle) BG-TC and (right) BG-BC pentacene-based OFETs using PhO-OTS as dielectric layer.

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Aalto University School of Electrical Engineering

Time (s)

OFET: Hybrid SAM/Oxide Gate Dielectrics



Transfer characteristics (solid) and $sqrt(I_{DS})$ (dashed) of OFETs with hybrid dielectrics with various PA-SAMs (as labelled)



b. capacitive densities–frequency $(C_i - F)$ and **c.** leakage current densities-voltage (J - V) of hybrid dielectrics with various PA-SAMs

Dielectric	Contact angle (°)	μ_{sat} (cm ² /Vs)	V_{Th} (V)	I on /I off
Al ₂ O ₃	< 10	0.05	- 2.18	~ 10 ⁵
HPA	102	0.35	- 1.71	~ 10 ⁶
DDPA	105.5	0.41	- 1.83	~ 10 ⁶
ODPA	109.8	0.58	- 1.84	~ 10 ⁶
PHDA	25.9	0.02	- 2.35	~ 10 ⁴
MDPA	65.1	0.05	- 1.64	~ 10 ⁵
PFPA	102	0.27	- 0.58	~ 10 ⁶
HUPA	28.5	0.03	- 1.95	~ 10 ⁵

 $Al_2O_3 \rightarrow high-k dielectric$ SAM \rightarrow favor interface with OSC



OFET: Gate Leakage

220	For an ideal (gate) dielectric, I _G	= 0A for any applied bias (V_D, V_G)
$ Q_{net} = 0C $	$ conservation of charge I_D + I_S + I_g = 0 $	ideal OFET ($I_G = 0$) $I_D = -I_S$
V _G ●		
	$\frac{1}{2} \frac{1}{2} \frac{1}$	 leakage current imperfect gate dielectrics surface conduction bulk device transport no OSC patterning



Self-assembled monolayer dipole as an electrostatic barrier to reduce leakage currents in n-channel OFETs on SiO₂ dielectrics



OFET: Hysteresis

Hysteresis appears when *gate voltage sweeps result in shift* (left or right) of the transfer characteristic, with subsequent change of the device V_{th}



- *dielectric charge storage* injection of charge in the dielectric reduces the field felt by the OSC
- *water incorporation* in the gate dielectric (*i.e.* polymer dielectric with strong polar group), which leads to *slow dielectric relaxation*
- traps in the OSC can decrease/increase I_D; traps are often extrinsic (i.e. water, oxygen) and this process can be reversible



OFET: *Reducing* Hysteresis



Pentacene, P6 (50nm)



- charges from pentacene are trapped at the PVA/pentacene interface and PVA bulk
- charge (from gate) are trapped at PVA/gate interface and PVA bulk



sandwich structure (PMMA/PVA/PMMA) allows controlling hysteresis in 0-10V range



OFET: *Exploiting* Hysteresis

Hysteresis is NOT ALWAYS DETRIMENTAL (if controllable) **memory devices:** modulation of channel conductance by remnant polarization of dielectrics after programming (P)/erasing (E) bias

 \rightarrow pentacene with

different grain size



ferroelectric P(VDF-TrFE-CTFE)

- high dielectric constant
- remnant polarization (P_r) of 12.9mC/m² @150MV/m
- low coercive field ~14V/ μm





- high mobility of 0.8 cm²/Vs, low P/E voltage of ±15 V
- large memory window (ΔV_{τ}) of 15.4~19.2 V
- good memory ON/OFF ratio ~10³
- endurance over 100 cycles, stable retention ability



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Summary

Today's Class

• **Building blocks** and **characteristics** of **OFET** (electrodes, dielectric, hysteresis)

Next

• Applications of organic field-effect transistors

