10

Series and Parallel Device Operation and Protection

This chapter considers various areas of power device application that are often overlooked. Such areas include parallel and series device utilisation, overcurrent and overvoltage protection, radio frequency interference (rfi) noise, filtering, and interactive noise effects.

10.1 Parallel and series operation of power devices

The power-handling capabilities of power devices are generally limited by device area utilisation, encapsulation, and cooling efficiency. Many high-power applications exist where a single device is inadequate and, in order to increase power capability, devices are paralleled to increase current capability or series-connected to increase voltage ratings. Extensive series connection of devices is utilised in HVDC transmission thyristor and IGBT modules while extensive paralleling of IGBTs is common in inverter applications.
When devices are connected in series for high-voltage operation, both steady-state and transient voltages must be shared equally by each individual series device. If power devices are connected in parallel to obtain higher current capability, the current sharing during both switching and conduction is achieved either by matching appropriate device electrical and thermal characteristics or by using external forced sharing techniques.

10.1.1 Series operation

Owing to variations in blocking currents, junction capacitances, delay times, on-state voltage drops, and reverse recovery for individual power devices, external voltage equalisation networks and special gate circuits are required if devices are to be reliably connected and operated in series.

10.1.1i - Steady-state voltage sharing

Figure 10.1 shows the forward off-state voltage-current characteristics of two typical power switching devices, such as SCRs or IGBTs. Both series devices conduct the same off-state leakage current but, as shown, each supports a different voltage. The total voltage blocked is $V_1 + V_2$ which can be significantly less than the sum of the individual capabilities. Forced voltage sharing can be achieved by connecting a resistor of suitable value in parallel with each series device as shown in figure 10.2.

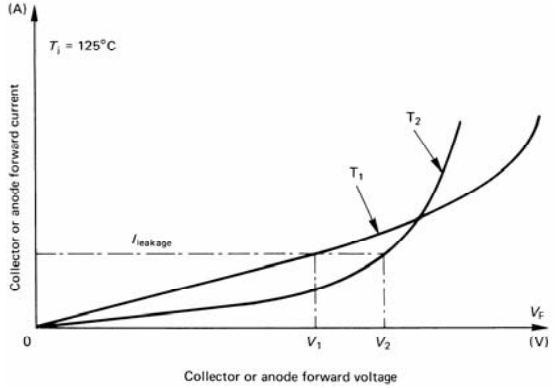

Figure 10.1. *Collector (transistor) or anode (thyristor) forward blocking I-V characteristics showing voltage sharing imbalance for two devices in series.*

These equal value sharing resistors will consume power and it is therefore desirable to use as large a resistance as possible. For worst case analysis consider *n* cells in series, where all the cells pass the maximum leakage current except cell D_1 which has the lowest leakage. Cell D_1 will support a larger blocking voltage than the remaining *n* - 1 which share voltage equally.
Let V_D be the maximum blocking voltage for any cell which in the worst case analysis is supported by D_1. If the range of maximum rated leakage or blocking currents is from $\hat{I}_b$ to $\check{I}_b$ then the maximum imbalance occurs when member D_1 has a leakage current of $\check{I}_b$ whilst all the remainder conduct $\hat{I}_b$. From figure 10.2, Kirchhoff's current law gives

$$\Delta I = \hat{I}_b - \check{I}_b \quad \text{(A)} \tag{10.1}$$

$$= I_1 - I_2 \quad \text{(A)} \tag{10.2}$$

where $I_1 > I_2$. The voltage across cell D_1 is

$$V_D = I_1 R \quad \text{(V)} \tag{10.3}$$

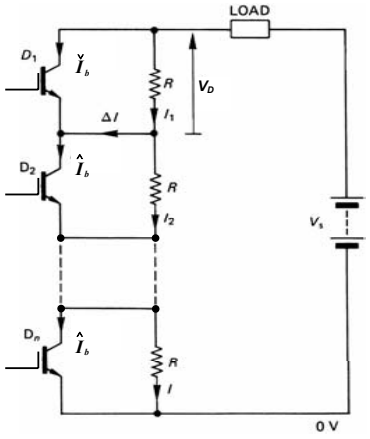

Figure 10.2. *Series IGBT string with resistive shunting for sustaining voltage equalisation in the off-state.*

By symmetry and Kirchhoff's voltage law, the total string voltage to be supported, V_s, is given by

$$V_s = (n - 1) I_2 R + V_D \quad \text{(V)} \tag{10.4}$$

Eliminating ΔI, I_1, and I_2 from equations (10.1) to (10.4) yields

$$\hat{R} \le \frac{nV_D - V_s}{(n-1)\left(\hat{I}_b - \check{I}_b\right)} \quad \text{(ohms)} \tag{10.5}$$

for $n \ge 2$.

Generally only the maximum leakage current at rated voltage and maximum junction temperature is specified. By assuming $\check{I}_b = 0$, a conservative value of the maximum allowable resistance is obtained, namely

$$\hat{R} \le \frac{nV_D - V_s}{(n-1)\hat{I}_b} = \frac{n(1-k_s)V_D}{(n-1)\hat{I}_b} \quad \text{(ohms)} \tag{10.6}$$

The extent to which nV_D is greater than V_s, is termed the voltage sharing factor, namely

$$k_s = V_s / nV_D \le 1 \tag{10.7}$$

As the number of devices is minimized the sharing factor approaches one, but equation (10.5) shows that undesirably the resistance for sharing decreases, hence losses increase.

The power dissipation of the resistor experiencing the highest voltage is given by

$$\hat{P}_d = V_D^2 / \hat{R} \quad \text{(W)} \tag{10.8}$$

If resistors of ± l00a per cent resistance tolerance are used, the worst case occurs when cell D_1 has a parallel resistance at the upper tolerance while all the others have parallel resistance at the lower limit. After using $V_D=(1+a)I_1R$ and $V_s=(n-1)(1-a)I_2R+V_D$ for equations (10.3) and (10.4), the maximum resistance is given by

$$\hat{R} \le \frac{n(1 - a)V_D - (1 + a)V_s}{(n - 1)\left(1 - a^2\right)\hat{I}_b} \quad \text{(ohms)} \tag{10.9}$$

for $n \ge 2$.

The maximum loss in a resistor is

$$\hat{P}_D = V_D^2 / \hat{R}(1 - a) \tag{10.10}$$

If the supply toleration is incorporated, then V_s in equations (10.6) and (10.9) is replaced by $(1+b)\times V_s$ where 100b is the supply percentage upper tolerance. This leads to a decreased resistance requirement, hence increased resistor power losses.

$$\hat{R} \le \frac{n(1-a)V_D - (1+a)(1+b)V_s}{(n - 1)\left(1 - a^2\right)\hat{I}_b} \quad \text{(ohms)} \tag{10.11}$$

The effects and importance of just a few per cent resistance or supply voltage tolerance on the maximum value for the sharing resistors and their power losses, are illustrated by the following example.

Example 10.1: ***Series device connection – static balancing***

Ten, 200 V reverse-blocking, ultra fast 35 ns reverse recovery diodes are to be employed in series in a 1500 V peak, string voltage application. If the maximum device reverse leakage current is 10 mA calculate the sharing factor, and for worst case conditions, the maximum value of sharing resistance and power dissipation.

- If 10 per cent tolerance resistors are employed, what is the maximum sharing resistance and its associated power rating?
- If a further allowance for supply voltage tolerance of ±5% is incorporated, what is the maximum sharing resistance and its associated power rating?

Solution

When n = 10, V_D = 200 V, V_s = 1500 V, and $\hat{I}_b$ = 10 mA, the sharing factor is k_s = 1500V/10×200V = 0.75. Equation (10.6) yields the maximum allowable sharing resistance

$$\hat{R} \le \frac{nV_D - V_s}{(n-1)\hat{I}_b} = \frac{10\times 200\text{V} - 1500\text{V}}{(10\text{-}1)\times 10\text{mA}} = 5.55\text{k}\Omega$$

The nearest (lower) preferred value, 4.7 kilohms, would be used.

Maximum resistor power losses occur when the diodes are continuously blocking. The maximum individual supporting voltage appears across the diode which conducts the least leakage current. Under worst case conditions this diode therefore supports voltage V_D, hence maximum power loss $\hat{P}_D$ is

$$\hat{P}_D = V_D^2 / \hat{R}$$
$$= 200^2/4700\Omega = 8.5\text{ W}$$

Since the worse device, (in terms of sharing has lowest leakage current), is randomly located in the string, each resistor must be capable of dissipating 8.5W.
The maximum 1500V supply leakage current is 42.5mA (10mA+1500V/10×4.7kΩ) giving 63.8W total losses (1500V×42.5mA), of which 15W (10mA×1500V) is lost in the diodes.
If resistance tolerance is incorporated, equation (10.9) is employed with a = 0.1, that is

$$\hat{R} \le \frac{n(1 - a)V_D - (1 + a)V_s}{(n - 1)\left(1 - a^2\right)\hat{I}_b}$$

$$\hat{R} \le \frac{10 \times (10 - 0.1) \times 200\text{V} - (1 + 0.1) \times 1500\text{V}}{(10 - 1) \times \left(1 - 0.1^2\right) \times 10\text{mA}}$$

$$= 2.13\ \text{k}\Omega$$

The nearest (lower) preferred value is 1.8 kilohms, which is much lower resistance (higher losses) than if matched resistors were to be used.
Worst case resistor power dissipation is

$$\hat{P}_D = V_D^2 / \hat{R}(1 - a)$$

$$= 200^2 / 1800\Omega \times (1 - 0.1)$$

$$= 27.7\ \text{W}$$

The maximum total module losses are 165W (1500V×103mA) arising from 103 mA (10mA + 1500V/1.8kΩ×(1- 0.1)) of leakage current.
If the device with the lowest leakage is associated with the worse case resistance (upper tolerance band limit), and simultaneously the supply is at its upper tolerance limit, then worse case resistance is given by equation (10.11), that is

$$\hat{R} \le \frac{n(1-a)V_D - (1+a)(1+b)V_s}{(n - 1)\left(1 - a^2\right)\hat{I}_b}$$

$$= \frac{10 \times (1 - 0.1) \times 200\text{V} - (1 + 0.1) \times (1 + 0.05) \times 1500\text{V}}{(10 - 1) \times \left(1 - 0.1^2\right) \times 10\text{mA}} = 758\Omega$$

Each resistor (preferred value 680Ω) needs to be rated at

$$200^2 / 680\Omega \times (1 - 0.1) = 68.6\ \text{W}$$

♣

When resistance tolerances are considered, sharing resistors of lower value must be used and the wider the tolerance, the lower will be the resistance and the higher the power losses. A number of solutions exist for reducing power losses and economic considerations dictate the acceptable trade-off level. Matched devices would allow a minimum number of string devices (sharing factor $k_s \rightarrow 1$) or, for a given string device number, a maximum value of sharing resistance (lowest losses). But matching is complicated by the fact that leakage current varies significantly with temperature. Alternatively, by increasing the string device number (decreasing the sharing factor k_s) the sharing resistance is increased, thereby decreasing losses. By increasing the string device number from 10 (k_s = ¾)

to 11 (k_s = 0.68) in the previous example, the sharing resistance requirement increases from 4.7 kilohms to 6.8 kilohms and resistor losses are reduced from a total of 50.8 W to 31 W. Another method of minimising sharing resistance losses is to minimise resistance tolerances. A tolerance reduction from 10 per cent to 5 per cent in the previous example increases the sharing resistance requirements from 1.8 kilohms to 3.9 kilohms, while power losses are reduced from 140 W to 64 W. These worse case losses assume a 100% on-state duty cycle.

10.1.1ii - Transient voltage sharing

During steady-state or at very low frequencies, sharing resistors as shown in figure 10.2 are sufficient to prevent individual device overvoltage. Mismatching of turn-on delay times of thyristors and transistors can be minimised by supplying high enough turn-on drive with very fast rise times. A higher initial *di/dt* is allowable.
Before a conducting string of diodes or thyristors can reverse-block, reverse recovery charge must flow. Those elements with least recovery charge requirements recover first and support the reverse bias. The un-recovered devices recover slowly, since recovery now occurs as a result of the low leakage current though the recovered devices, and natural recombination.
The reverse-blocking voltage can be shared more equally by placing capacitance across each string element as shown in figure 10.3. The capacitor action is to provide a transient current path bypassing a recovered device to allow a slower device to recover and to support volts. In the case of thyristors, low value resistance is connected in series with each capacitor to avoid high capacitor discharge through the thyristors at turn-on. Figure 10.4 shows the *I-V* characteristics of two unmatched thyristors or diodes during reverse recovery.
The worst case assumptions for the analysis of figure 10.3 are that element D_1 has minimum stored charged $\check{Q}$ while all other devices have the maximum requirement, $\hat{Q}$. The charge difference is

$$\Delta Q = \hat{Q} - \check{Q} \quad \text{(C)} \qquad (10.12)$$

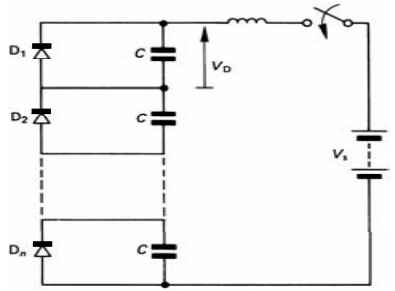

Figure 10.3. *A series diode string with shunting capacitance for transient reverse blocking voltage sharing.*

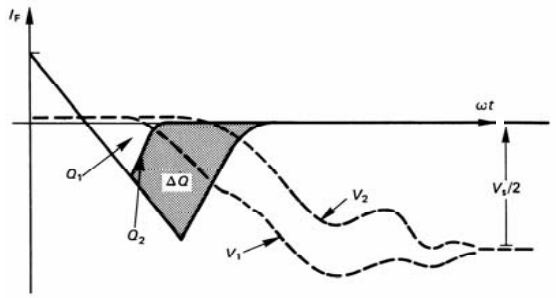

Figure 10.4. *Reverse recovery current and voltage for two mismatched series connected diodes.*

The total string voltage V_s, comprises the voltage across the fast-recovery device V_D plus the sum of the voltages across the slow n - 1 devices, V_{slow}. That is

$$V_s = V_D + (n - 1)V_{slow} \quad \text{(V)} \qquad (10.13)$$

The voltage across the slow devices is given by

$$V_{slow} = \frac{1}{n}\left(V_s - \Delta\hat{V}\right) \quad \text{(V)} \qquad (10.14)$$

where $\Delta\hat{V} = \Delta\hat{Q}/C$.

Eliminating V_{slow} from equations (10.13) and (10.14) yields

$$\breve{C} \geq \frac{(n-1)\Delta Q}{nV_D - V_s} = \frac{(n-1)\Delta Q}{n(1-k_s)V_D} \quad \text{(F)} \qquad (10.15)$$

This equation shows that as the number of devices is minimized, the sharing factor, k_s, which is in the denominator of equation (10.15), tends to one and the capacitance requirement undesirably increases.

Manufacturers do not specify the minimum reverse recovery charge but specify the maximum reverse recovery charge for a given initial forward current, reverse recovery *di/dt,* and temperature. For worst case design, assume $\breve{Q}$ = 0, thus

$$\breve{C} \geq \frac{(n-1)\hat{Q}}{nV_D - V_s} \quad \text{(F)} \qquad (10.16)$$

Sharing circuit design is complicated if the effects of reverse steady-state leakage current in ac thyristor blocking are taken into account.

Supply and sharing capacitance tolerances significantly affect the minimum capacitance requirement. Worst case assumptions for capacitance tolerances involve the case when the fastest recovering diode is in parallel with capacitance at its lower tolerance limit while all the other sharing capacitances are at their upper tolerance limit. Assuming the minimum reverse recovery charge is zero, then the minimum sharing capacitance requirement is

$$\breve{C} \geq \frac{(n-1)\hat{Q}}{(1-a)(nV_D - V_s)} \quad \text{(F)} \qquad (10.17)$$

where -100a is the capacitor negative percentage tolerance and $n \geq 2$. Voltage sharing resistors help minimise capacitor static voltage variation due to capacitance variations.

If the supply tolerance is incorporated, then V_s in equations (10.16) and (10.17) are replaced by $(1+b)\times V_s$ where +100b is the supply percentage upper tolerance. This leads to an increased capacitance requirement, hence increased energy losses, $\frac{1}{2}CV_D^2$.

$$\breve{C} \geq \frac{(n-1)\hat{Q}}{(1-a)(nV_D - (1+b)V_s)} \quad \text{(F)} \qquad (10.18)$$

Example 10.2: ***Series device connection – dynamic balancing***

The string of ten, 200 V diodes in worked example 10.1 is to incorporate capacitive reverse recovery transient sharing. Using the data in chapter 5, figure 5.9, specify a suitable sharing capacitance based on zero capacitance and supply tolerances (a = b = 0), ± 10 per cent capacitance tolerances (a = 0.1, b = 0), ± 5 per cent supply tolerance (a = 0, b = 0.05), then both tolerances (a = 0.1, b = 0.05). Estimate in each case the energy loss due to capacitor discharge.

Solution

Figure 5.9 shows that worst case reverse recovery conditions occur at maximum junction temperature, *di/dt,* and I_F, and a value of $\hat{Q}$ =6μC is appropriate.

The minimum possible sharing capacitance occurs when the capacitance and dc rail voltage are tightly specified. From equation (10.16)

$$\breve{C} \geq \frac{(n-1)\hat{Q}}{nV_D - V_s} = \frac{(10\text{-}1)\times 6\mu C}{10\times 200 - 1500V} = 108nF$$

The sharing capacitance requirement with 10% tolerance capacitors, is given by equation (10.17),

$$\breve{C} \geq \frac{(n-1)\hat{Q}}{(1-a)(nV_D - V_s)} = \frac{(10 - 1)\times 6\mu C}{(1 - 0.1)\times(10\times 200V - 1500V)} = 0.12\mu F \text{ @ } 200Vdc$$

A further increase in capacitance requirements results if the upper tolerance dc rail voltage is used. From equation (10.18)

$$\breve{C} \geq \frac{(n-1)\hat{Q}}{(1-a)(nV_D - (1+b)V_s)}$$

$$= \frac{(10 - 1)\times 6\mu C}{(1 - 0.1)\times(10\times 200V - (1+0.05)\times 1500V)} = 0.14\mu F \text{ @ } 200Vdc$$

In each tolerance case the next larger preferred capacitance value should be used, namely, 120nF, 120nF, and 150nF respectively.

The total series capacitance, using the upper tolerance limit is

$$C_T = \frac{(1+a)\overset{\vee}{C}}{n}$$

The stored energy with a 1500V dc rail in the 10 series connect 120nF capacitors, and subsequently loss when the string voltages reduces to zero at diode forward bias, is therefore

$$W_T = ½C_T\hat{V}_s^2 = ½\frac{(1+a)\overset{\vee}{C}}{n}V_s^2(1+b)^2$$

$$= ½\frac{(1+0.1)\times 120\text{nF}}{10}\times 1500^2\times(1+0.05)^2 = 16.4\text{mJ}$$

The energy stored in the 10 series connect 150nF capacitors, and subsequently loss when the string voltages reduces to zero at diode forward bias, is

$$W_T = ½\times\frac{(1+0.1)\times 150\text{nF}}{10}\times 1500^2\times(1+0.05)^2 = 20.5\text{mJ}$$

♣

When capacitive sharing is used with switching devices, at turn-on the transient sharing capacitor discharges into the switching device. The discharge current magnitude is controlled by the turn-on voltage fall characteristics. If a linear voltage fall at turn-on is assumed, then the transient sharing capacitor maximum discharge current i_{dis} is a constant current pulse for the fall duration of magnitude

$$i_{dis} = C\frac{V_D}{t_{tv}} \quad \text{(A)} \qquad (10.19)$$

The discharge current can be of the order of hundreds of amperes, incurring initial *di/dt* values beyond the capabilities of the switching device. In example 10.2 the discharge current for a switch rather than a diode is approximately 150nF×200V/1μs =30A, assuming a 1μs voltage fall time. This 30A may not be insignificant compared to the switches current rating. But, advantageously, the sharing capacitors do act as turn-off snubbers, reducing switch turn-off stressing.

In the case of the thyristor, the addition of low-valued resistance in series with the transient capacitor can control the capacitor discharge current, yet not significantly affect the transient sharing properties. The resultant *R-C* discharge current can provide thyristor latching current while still offering transient recovery sharing, *dv/dt,* and voltage spike suppression. Thyristor snubber operation and design have been considered in section 8.1.2.

Figure 10.5 shows the complete steady-state and transient-sharing networks used for diodes, thyristors, and transistors. Transient voltage sharing for transistors involves the use of the conventional *R-D-C* snubber shown in figure 10.5c and considered in chapter 8. The series inductor used with thyristor and transistor strings provides transient turn-on voltage protection. The inductor supports the main voltage while each individual element switches on. Such an inductive turn-on snubber is mandatory for the GTO thyristor and the GCT. No one device is voltage-stressed as a consequence of having a longer turn-on delay time, although gate overdrive at turn-on minimises delay variations.

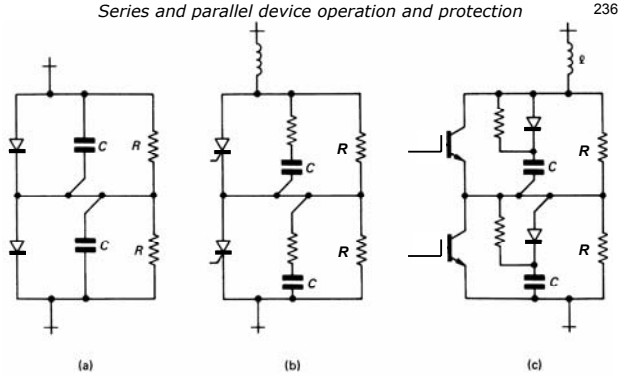

Figure 10.5. *Transient and steady-state voltage sharing circuits for series connected: (a) diodes; (b) thyristors; and (c) igbt transistors.*

10.1.2 Parallel operation

It is common practice to parallel devices in order to achieve higher current ratings or lower conducting voltages than are attainable with a single device. Although devices in parallel complicate layout and interconnections, better cooling distribution is obtained. Also, built-in redundancy can give improved equipment reliability. A cost saving may arise with smaller, cheaper, high production volume, devices.

The main design consideration for parallel device operation is that all devices share both the steady-state and transient currents. Any bipolar device carrying a disproportionately high current will heat up and conduct more current, eventually leading to thermal runaway as considered in section 4.1.

The problem of current sharing is less severe with diodes because diode characteristics are more uniform (because of their simpler structure and manufacturing) than those of thyristors and transistors. Two basic sharing solutions exist

- matched devices
- external forced current sharing.

10.1.2i - Matched devices

Figure 10.6 shows the static *I-V* on-state characteristics of two SCR's. If these two devices are connected in parallel, for the same on-state voltage, the resultant current flow is $I_1 + I_2$ where I_1 and I_2 can be very different in value. The total current rating of the pair is not the sum of the maximum current rating for each but rather a value which can be just larger than the rating of one device alone. The percentage parallel derating *pd* for *n* parallel connected devices is defined as

$$pd = \left(1 - \frac{I_T}{nI_m}\right) \times 100 \quad = \left(1 - k_p\right) \times 100 \quad \text{per cent} \qquad (10.20)$$

where I_T = total current through the parallel arrangement
I_m = maximum allowable single device current rating
n = number of parallel devices
k_p = parallel sharing factor $= I_T/nI_m$

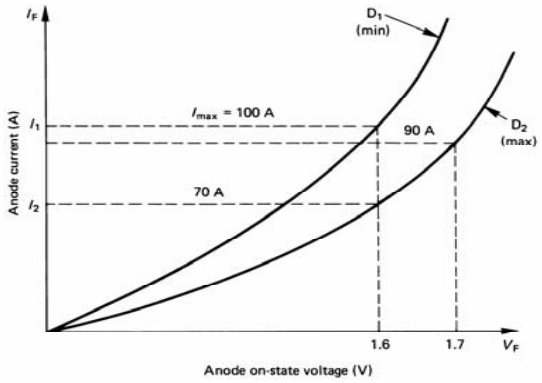

Figure 10.6. *Forward conduction characteristics of two unmatched devices.*

10.1.2ii - External forced current sharing

Derating does not account for effects such as layout and electrical and thermal impedance imbalance. The amount of derating is traded off against the extra cost involved in selecting devices with closer (matched) static characteristics.
Forced current sharing is applicable to both steady-state and transient conditions. For a current derating of less than 5 per cent it is usually cheaper to use forced sharing techniques rather than matched devices.
Figure 10.6 shows the maximum variation of *I-V* characteristics in devices of the same type. When parallel connected the maximum current is restricted to I_m+I_2, (= 100A+70A = 170A). The maximum current rating for each device is I_m, (100A); hence with suitable forced sharing a combination in excess of I_m+I_2 should be possible. The resistive network in figure 10.7 is used for current sharing and in example 10.3 it is required that I_m, 100A, flows through D_1 and $(1-2\times pd)\times I_m > I_2$, (90A) flows through D_2, for a *pd* (5%) overall derating.
From Kirchhoff's voltage law in figure 10.7

$$\begin{aligned} V_1 + V_3 &= V_2 + V_4 \\ V_{D_1} + I_m R &= V_{D_2} + \left(I_T - I_m\right) R \end{aligned} \qquad (10.21)$$

From equation (10.20), rearranged for two devices, $n = 2$

$$I_T = 2 \times (1 - pd) I_m$$

Substituting for I_T in equation (10.21) gives

$$R = \frac{V_{D_2} - V_{D_1}}{2\ pd\ I_m} \quad \text{(ohms)} \qquad (10.22)$$

For n devices connected in parallel, equation (10.21) becomes

$$V_{D_1} + I_m R = V_{D_2} + \frac{\left(I_T - I_m\right)}{n-1} R \qquad (10.23)$$

which after substituting for I_T from equation (10.20), for maximum device voltage variation, gives

$$R = \frac{\hat{V}_D - \check{V}_D}{I_m} \frac{(n-1)}{n \times pd} \quad \text{(ohms)} \qquad (10.24)$$

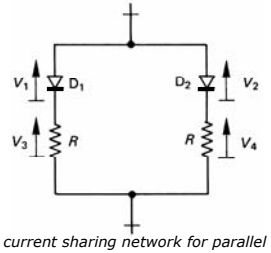

Figure 10.7. *Forced current sharing network for parallel connected devices.*

Although steady-state sharing is effective, sharing resistor losses can be high. The resistor losses in general terms for n parallel connected devices and a conduction duty cycle δ, are given by

$$P_r = \delta \left\{1 + \left(1 - \frac{n}{n-1} \times pd\right)^2\right\} I_m^2 R \quad \text{(W)} \qquad (10.25)$$

Example 10.3: ***Resistive parallel current sharing - static balancing***
For the two diodes shown in figure 10.6, with $\hat{I} = 100\text{A}$, what derating result when they are parallel connected, without any external sharing circuits?
The maximum current rating for each device is I_m, 100A; hence with suitable forced sharing a 190A combination should be possible. Using the network in figure 10.7 for current sharing, it is required that 100A flows through D_1 and 90A through D_2. Specify the per cent overall derating, the necessary sharing resistors and their worse case losses.

Solution
The derating for the parallel situation depicted in figure 10.6, without external sharing, is

$$pd = \left(1 - \frac{170\text{A}}{2\times 100\text{A}}\right)\times 100 = 15 \text{ per cent} \qquad (k_p = 0.85)$$

With forced resistive sharing, the objective derating is reduced from 15% to

$$pd = \left(1 - \frac{190\text{A}}{2\times 100\text{A}}\right)\times 100 = 5 \text{ per cent} \qquad (k_p = 0.95)$$

From figure 10.6

$$1.6\text{V} + 100\text{A}\times R = 1.7\text{V} + 90\text{A}\times R$$

that is

$$R = 10 \text{ milliohm}$$

Equation (10.22), being based on the same procedure, gives the same result. The cell voltage drop is increased to $1.6\text{V}+100\text{A}\times 0.01\Omega = 1.7\text{V}+90\text{A}\times 0.01\Omega = 2.6\text{V}$.

For $\delta = ½$

$$\bar{I}_{D1} = \delta \times I_{D1} = ½\times 100\text{A} = 50\text{A} \qquad \bar{I}_{D2} = \delta \times I_{D2} = ½\times 90\text{A} = 45\text{A}$$

$$I_{D1^{rms}} = \sqrt{\delta}\times I_{D1} = \sqrt{½}\times 100\text{A} = 70.7\text{A} \qquad \bar{I}_{D2^{rms}} = \sqrt{\delta}\times I_{D2} = \sqrt{½}\times 90\text{A} = 63.6\text{A}$$

$$I_{D1^{ac}} = \sqrt{I_{D1rms}^2 - \bar{I}_{D1}^2} \qquad I_{D2^{ac}} = \sqrt{I_{D2rms}^2 - \bar{I}_{D2}^2}$$

$$= \sqrt{70.7^2 - 50^2} = 50\text{A} \qquad = \sqrt{63.6^2 - 45^2} = 45\text{A}$$

$$P_{R1} = I_{D1rms}^2 R_1 = 70.7^2 \times 0.01\text{m}\Omega = 50\text{W} \qquad P_{R2} = I_{D2rms}^2 R_2 = 63.6^2 \times 0.01\text{m}\Omega = 40.5\text{W}$$

$$P_{D1} = \bar{I}_{D1} V_{D1} = 50\text{A}\times 1.6\text{V} = 80\text{W} \qquad P_{R2} = \bar{I}_{D2} V_{D2} = 45\text{A}\times 1.7\text{V} = 76.5\text{W}$$

$$P_{total} = P_R + P_D = (50\text{W} + 40.5\text{W}) + (80\text{W} + 76.5\text{W}) = 90.5\text{W} + 156.5\text{W} = 247\text{W}$$

For worse case losses, $\delta \rightarrow 1$

$$\bar{I}_{D1} = \delta \times I_{D1} = 1\times 100\text{A} = 100\text{A} \qquad \bar{I}_{D2} = \delta \times I_{D2} = 1\times 90\text{A} = 90\text{A}$$

$$I_{D1^{rms}} = \sqrt{\delta}\times I_{D1} = \sqrt{1}\times 100\text{A} = 100\text{A} \qquad \bar{I}_{D2^{rms}} = \sqrt{\delta}\times I_{D2} = \sqrt{1}\times 90\text{A} = 90\text{A}$$

$$I_{D1^{ac}} = \sqrt{I_{D1rms}^2 - \bar{I}_{D1}^2} \qquad I_{D2^{ac}} = \sqrt{I_{D2rms}^2 - \bar{I}_{D2}^2}$$

$$= \sqrt{100^2 - 100^2} = 0\text{A} \qquad = \sqrt{90^2 - 90^2} = 05\text{A}$$

$$P_{R1} = I_{D1rms}^2 R_1 = 100^2 \times 0.01\text{m}\Omega = 100\text{W} \qquad P_{R2} = I_{D2rms}^2 R_2 = 90^2 \times 0.01\text{m}\Omega = 81\text{W}$$

$$P_{D1} = \bar{I}_{D1} V_{D1} = 100\text{A}\times 1.6\text{V} = 160\text{W} \qquad P_{R2} = \bar{I}_{D2} V_{D2} = 90\text{A}\times 1.7\text{V} = 153\text{W}$$

$$P_{total} = P_R + P_D = (100\text{W} + 81\text{W}) + (160\text{W} + 153\text{W}) = 181\text{W}+313\text{W} = 494\text{W}$$

The general form in equation (10.25) gives the same total losses in each duty case.

♣

A more efficient method of current sharing is to use coupled reactors as shown in figure 10.8. In this feedback arrangement, in figure 10.8a, if the current in D_1 tends to increase above that through D_2, the voltage across L_1 increases to oppose current flow through D_1. Simultaneously a negative voltage is induced across L_2 thereby increasing the voltage across D_2 thus its current. This technique is most effective in ac circuits where the core is more readily designed to not saturate.

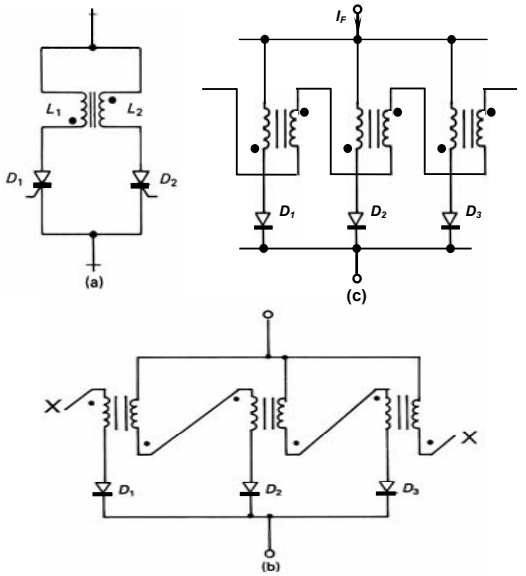

Figure 10.8. *External forced current sharing network using cross-coupled reactors: (a) for two devices; and (b) and (c) for many devices.*

Equalising reactor arrangements are possible for any number of devices in parallel, as shown in figure 10.8b and c, but size and cost become limiting constraints. The technique is applicable to steady-state and transient sharing. At high current densities, the forward *I-V* characteristic of diodes and thyristors has a positive temperature dependence which provides feedback aiding sharing.

The mean current in the device with the highest current, therefore lowest voltage, of *n* parallel connected devices, is given by

$$\bar{I}_F = \frac{I_F}{n} + \Delta I_F = \frac{I_F}{n} + \frac{n}{n-1}\frac{\tau^2}{2TL_M}\Delta V_F \qquad (10.26)$$

where ΔV_F is the maximum on-state voltage drop difference
L_M is the self-inductance (magnetising inductance) of the coupled inductor
T is the cycle period, $1/f_s$ and
τ is the conduction period

Consider two thyristors ($n = 2$) connected in parallel as show in figure 10.9. The coupled circuit magnetising current is modelled by the magnetising inductor L_M. The transformer turns ratio is 1:1, hence the winding voltages and currents are equal, taking into account the relative winding flux orientation shown by the dots.

From Kirchhoff's voltage law

$$v_{T1} + v_1 = v_{T2} - v_1 \tag{10.27}$$

That is

$$v_1 = ½ \times \left(v_{T1} - v_{T2}\right) = ½ \times \Delta v \tag{10.28}$$

From Kirchhoff's current law

$$I_M = i_1 - i_2 \tag{10.29}$$

From Faraday's equation

$$v_1 = L_M \frac{dI_M}{dt} \tag{10.30}$$

which after integrating both sides gives

$$\begin{aligned} I_M &= \frac{1}{L_M}\int_0^\tau v_1 dt \\ &= ½ \frac{1}{L_M} \Delta V_F \tau \end{aligned} \tag{10.31}$$

As a worst case condition it is assumed that the voltage difference Δv does not decrease as the operating point moves along the *I-V* characteristics, that is $\Delta v = \Delta V_F$. Specifically D1 moves further up the *I-V* characteristic with time as it conducts more current while D2 moves towards the origin.

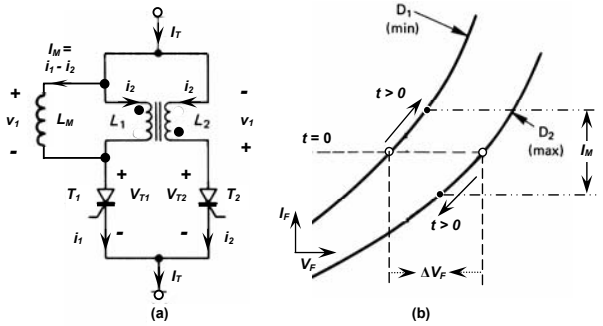

Figure 10.9. *External forced current sharing network using cross-coupled reactors: (a) circuit for two devices and (b) I-V operating points.*

Example 10.4: ***Transformer current sharing – static and dynamic balancing***

Two thyristors with the same forward conduction characteristics as the diodes in figure 10.6 are parallel connected using the coupled circuit arrangement in figure 10.8a.

The maximum current rating for each device is I_m, 100A; hence with suitable forced sharing a 190A combination should be possible. Using the network in figure 10.9a for current sharing, it is required that no more than rated current flow through the lower conducting voltage device, D_1. Specify the per cent overall derating and the necessary sharing transformer properties assuming a half-wave, 180º conduction, phase-controlled, 50Hz, highly inductive load application.
What are the transformer core reset requirements?

Solution

As in example 10.3, the derating for the parallel situation depicted in figure 10.6, without external sharing, is

$$pd = \left(1 - \frac{170\text{A}}{2\times 100\text{A}}\right)\times 100 = 15 \text{ per cent}$$

With forced transformer sharing, the objective derating is reduced from 15% to

$$pd = \left(1 - \frac{190\text{A}}{2\times 100\text{A}}\right)\times 100 = 5 \text{ per cent}$$

When the two thyristors are turned on, the magnetizing current is assumed zero and transformer action will force each device to conduct 95A, giving 190A in total. From figure 10.6, the voltage difference between the thyristors, ΔV_F is about 0.1V, thus the transformer winding voltages will be 0.05V each, with polarities as shown in figure 10.9a. In time the magnetizing current increases and the current in T1 increases above 95A due to the increasing magnetizing current, while the current in T2 decreases below 95A, such that the total load current is maintained at 190A.
The worse case conduction period, giving maximum magnetising current, is for 180º conduction, that is, 10ms. Thus it is required that T1 current rises to 100A and T2 current falls to 90A after 10ms, that is, the magnetising current is 100A-90A = 10A.
Substitution into equation (10.31) gives

$$L_M = ½ \frac{1}{I_M}\int_0^{10\text{ms}} \Delta v dt = ½ \times \frac{1}{10\text{A}} \times 0.1\text{V} \times 10\text{ms} = 50\mu\text{H}$$

where it is assuming that the voltage differential ΔV_F between the two devices is constant during the conduction period. In fact figure 10.9b shows that the voltage difference decreases, so assuming a constant value gives an over-estimate of requirements.
The core volt-µs during conduction is 0.05V×10ms = 500 V-µs. That is, during core reset the reverse voltage time integral must be at least 500 V-µs to ensure the core flux is reset, (magnetising current reduced to zero).

♣

10.2 Protection

A fault can be caused by a device failure or noise which causes undesired device turn-on. This will cause semiconductor device and equipment failure unless protective measures are utilised.
Protection against fault current effects usually involves fuses which clear in time

to protect endangered devices, or voltage transient absorption devices which absorb spike energy and clamp the equipment voltage to a safe level. The crowbar fault protection technique can be employed to divert the fault from sensitive components to the crowbar which is a robust circuit. The crowbar clamps the sensitive circuits to zero volts and initiates an isolation breaker or fuse action.

10.2.1 Overcurrent

It is not economical to design a circuit where fault overloads are catered for by using devices and components which will withstand worst case faults. A fuse link is normally used for circuit fault current protection. A fuse link protecting a semiconductor is required to carry normal and overload currents but to open the circuit under fault conditions before the semiconductor is damaged. The resultant circuit induced arcing voltage must not cause damage to the circuit. Other fuse links or circuit breakers should be unaffected when the defective cell is disconnected. This non-interaction property is termed *discrimination.*

The fuse element is one or more parallel conductors of pure silver rolled into thin bands, 0.04-0.25 mm thick. Each silver band has a number of traverse rows of punched holes (or notches) as shown in figure 10.10. The area between the holes determines the pre-arcing I^2t integral of the fuse and, along with thermal aspects, is related to the fuse current rating. The number of rows of holes determines the fuse voltage rating. When fusing occurs the current is shared between the holes (the necks), while the arcing voltage is supported between the series of rows of holes. The arcing characteristics are enhanced by packing the silver element in sand or glassed sand. The sand and silver element are contained in a ceramic body and the end connector plates are copper flashed and tinned.

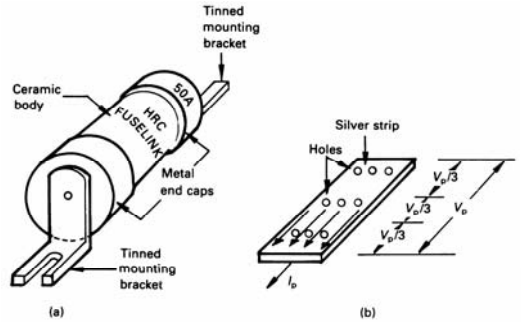

Figure 10.10. *The current fuse link:*
(a) a 50 A 660 V ac fuse link and (b) a silver fuse link element.

The action of a typical fuse link is shown in figure 10.11. Owing to the *prospective fault current* I_a the fuse melts at point A, time t_m. Depending on the fuse design and the circuit, the current may continue to rise further to point B, termed the *peak let-through current* I_p. Beyond this point the impedance of the arcing fuse forces the fault current down to zero at the point C. Thus *fuse-clearing* or *total interrupting time* t_c consists of a *melting time* t_m and an *arcing time* t_a.

The load fault energy, for a fuse link resistance R, is

$$W_{tot} = \int_0^{t_c} i^2 R \, dt \qquad \text{(J)}$$

If the load current, shown in figure 10.l0a, during fuse action is assumed to be triangular, then the clearing integral of the fuse is

$$W_c = \tfrac{1}{3} I_p^2 t_c R \qquad \text{(J)} \qquad (10.32)$$

If the resistance R is assumed constant (because of its low resistivity temperature co-efficient), the value of I^2t ($\frac{1}{3}I_p^2t_c$) is proportional to the energy fed to the protected circuit. The I^2t term is called the *total let-through energy* or the *virtual clearing integral* of the fuse. The energy which melts the fuse is proportional to $\frac{1}{3}I_p^2t_m$ and is termed the *pre-arcing* or *melting* I^2t.

10.2.1i - Pre-arcing I^2t

Before a fuse melts, the fuse is affected only by the current flowing. The pre-arcing or melting I^2t characteristics of fuse links are therefore only a function of prospective fault current and are independent of voltage. For melting times longer than 5-10 ms, the time-current characteristics are usually used for design. Typical time-current characteristics for four different current rated fuses are shown in figure 10.12. For times less than a millisecond, the melting I^2t reduces to a minimum and the pre-arcing I^2t characteristics shown in figure 10.13 are most useful.

The peak let-through current I_p, is a function of prospective fault current I_a for a given supply voltage. Typical current cut-off characteristics are shown in figure 10.14.

10.2.1ii - Total I^2t let-through

For fuse operating times of less than about 10 milliseconds the arcing I^2t can be considerably larger than the pre-arcing I^2t and it varies considerably with system voltage, fault level, power factor, and the point on the wave when the fault is initiated. The higher the voltage the more onerous is the duty of the fuse link because of the increase in energy absorbed by the fuse link during the arcing process. Under short-circuit conditions this leads to an increase in I^2t let-through with voltage. The I^2t let-through will decrease with increased supply frequency whereas the cut-off current will increase.

The peak arc voltage after melting is usually specified for a given fuse link type and is a function of supply voltage, as indicated by the typical arcing voltage characteristics in figure 10.15. The faster the fault is cleared, the higher the arc voltage V_p. Typical total I^2t let-through values for total operating times of less than 10 ms, at a given voltage, are shown in figure 10.16. Derating factors are shown in figure 10.17.

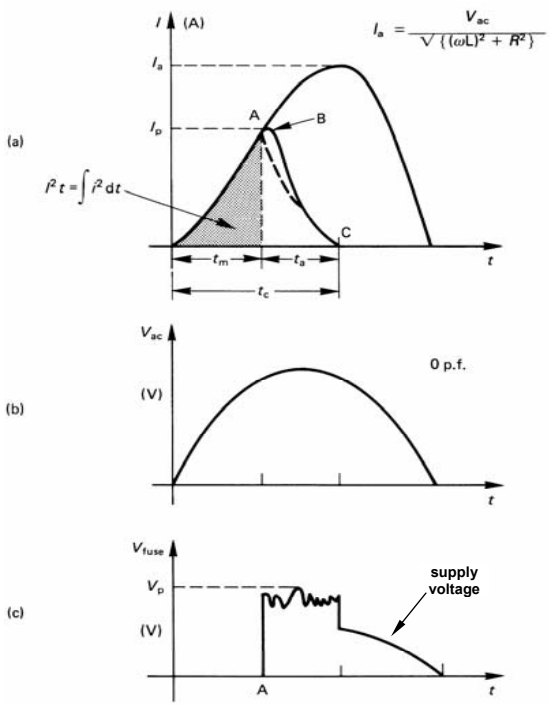

Figure 10.11. *Parameters of a fuse link operating: (a) current waveforms; (b) supply voltage; and (c) fuse arcing voltage.*

10.2.1iii - Fuse link and semiconductor I^2t co-ordination

Difficulties arise in matching fuses with semiconductors because each has very different thermal and electrical properties.

Semiconductor manufacturers publish (mainly for diodes and thyristors) I^2t withstand values for their devices for times less than 10 ms. To ensure fuse link protection the total I^2t let-through by the fuse link under appropriate circuit conditions should be less than the I^2t withstand ability of the semiconductor.

Fuse link manufacturers usually give the data shown in figures 10.12-10.17. In ac applications the parameters on which the semiconductor withstand capability is normally compared to the fuse link are

- Peak let-through current versus clearing time or clearing I^2t
- Applied voltage
- Power factor.

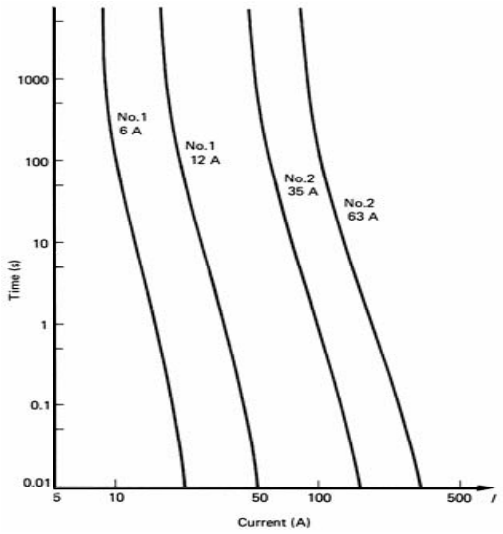

Figure 10.12. *Fuse-link time-current characteristics for four fuses and symmetrical sinusoidal 50 Hz currents.*

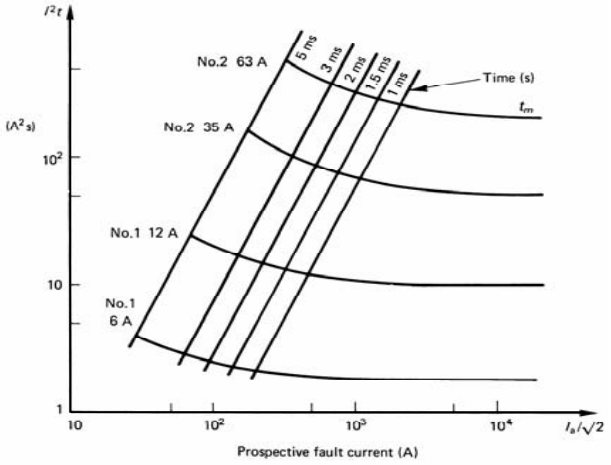

Figure 10.13. *Pre-arcing I^2t characteristics of four fuse links.*

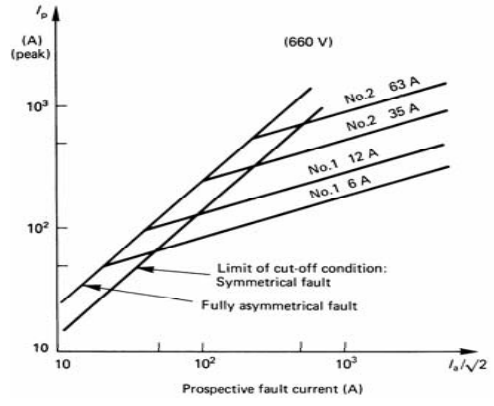

Figure 10.14. *Fuse-link cut-off characteristics at 660 V rms.*

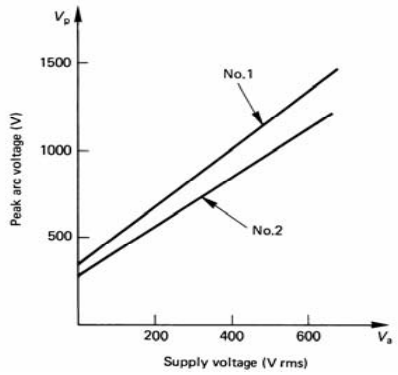

Figure 10.15. *Typical peak arc voltage for two different fuse-link types.*

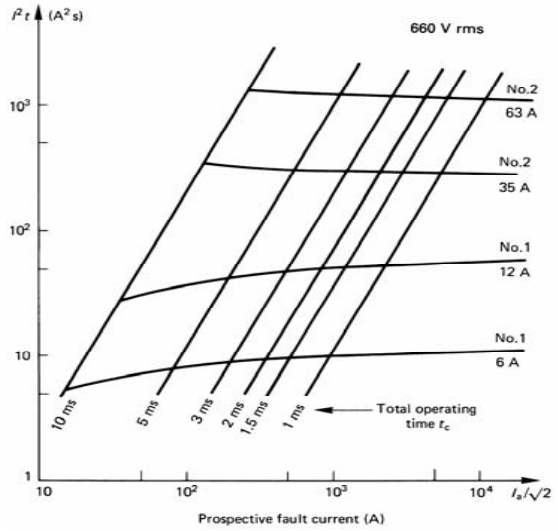

Figure 10.16. *Total let-through current for total fuse-link operating times of less than 10 ms and at 660 V rms.*

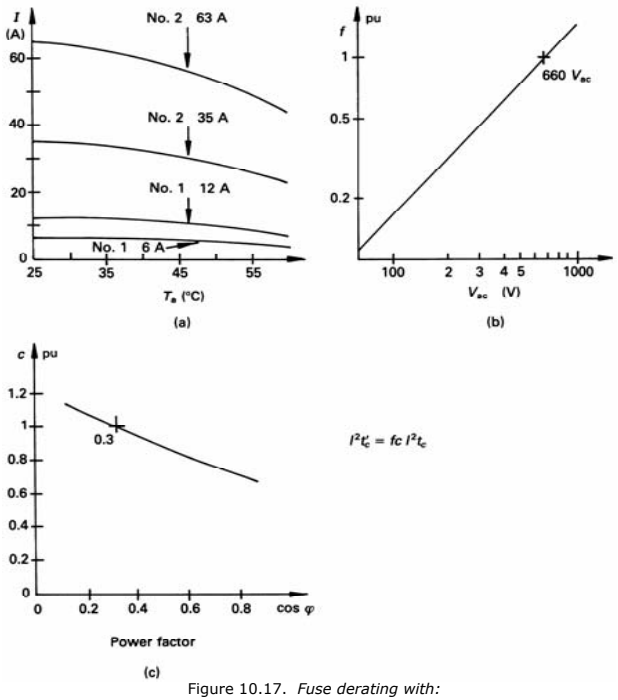

Figure 10.17. *Fuse derating with:*
(a) ambient temperature; (b) ac supply voltage; and (c) power factor.

Fuse protection in dc circuits represents greater difficulty than for ac circuits. No natural ac period current zeros exist and faults can result in continuous arcing, depending on the circuit L/R time constant, prospective fault, and supply voltage. Thus in dc applications the essential parameters are

- Peak let through current versus clearing time or clearing I^2t
- Applied voltage
- Prospective fault *di/dt*
- Time constant.

It may be possible in some applications to use an ac fuse in a dc circuit, before the rectification stage. Generally low voltage fuses are more effective than high voltage fuses. In high voltage transformer applications satisfactory protection may be afforded by transferring the fuse to the low voltage side. The fuse I^2t rating is transferred as with impedance transferring, that is, in the turns ratio squared.

$$I^2t_{fuse}^{primary} = \left(\frac{V_s}{V_p}\right)^2 \times I^2t_{semiconductor}^{secondary} \qquad (10.33)$$

Alternatively an mcb (miniature circuit breaker) may offer better protection in cases when the fault is more of an overload such that the current magnitude is limited. On overload, the mcb takes a longer time to clear than a fuse, thus the mcb is less prone to nuisance tripping.
Fuse protection is mainly applicable to more robust devices such as thyristors and diodes. Transistors (MOSFETs more readily than IGBTs) usually fail as a result of overcurrent before any fuse link can clear the fault.

Example 10.5: ***AC circuit fuse design***

A fast acting fuse is connected in series with a thyristor in a 415 V ac, 50 Hz ac application. The average current in the thyristor is 30 A at a maximum ambient temperature of 45°C. The ratings of the thyristor are

$I_{T(AV)}$ = 45 A @ T_c = 85°C
I_{TRMS} = 80 A
I^2t = 5 k A^{2}s for 10 ms @ 125°C
I^2t = 20 k A$^2\sqrt{}$s
I_{TSM} = 1000 A for 10 ms @ 125°C and V_{RRM} = 0

The fault circuit inductance is 1.32 mH and the resistance is negligible. Using the figures 10.12 to 10.17, select a suitable fuse.

Solution

From figure 10.17a, the 35 A rms No. 2 fuse is rated at 30 A rms in a 45°C ambient.
From figure 10.15 the peak arc voltage for a type No. 2 fuse will be less than 1200 V, hence the thyristor voltage rating must be greater than 1200 V.
The short circuit or prospective rms symmetrical fault current is

$$I_{sc} = \frac{I_a}{\sqrt{2}} = \frac{V_s}{X_L} = \frac{415\text{V}}{2\pi \times 50\text{Hz} \times 1.32\text{mH}} = 100\text{A}$$

Figure 10.13 gives a fuse peak let through current of 500 A, which is less than the thyristor peak current rating of 1 kA.
Figure 10.16 gives the fuse total I^2t of 300 A^{2}s and the total clearing time of t_c =3.5 ms. Since the fuse clears in less than 10 ms (½ ac cycle), the thyristor re-applied V_{RRM} will be zero and an I_{TSM} = 1000 A rating is applicable. The total I^2t is corrected for voltage (415V ac) and power factor (0 pu) with f = 0.6 and c = 1.2 from figures 10.17b and c.

$$I^2t' = f \times c \times I^2t = 0.6 \times 1.2 \times 300\ \text{A}^2\text{s} = 216\ \text{A}^2\text{s}$$

which is significantly less than the thyristor I^2t rating of 5 kA^{2}s.
Since t_c is less than 10 ms, the $I^2\sqrt{t}$ rating of the thyristor is used.

$$I^2t'' = (I^2\sqrt{t})\sqrt{t_c}$$
$$= 20\ \text{kA}^2\sqrt{\text{s}} \times \sqrt{3.5\ \text{ms}} = 1.18\ \text{kA}^2\text{s}$$

which is significantly greater than the I^2t (216 A^2s) of the fuse.
Since the fuse peak let through current (500 A) is less than the thyristor peak surge current rating (1000 A), and the fuse I^2t rating (216 A^2s) is significantly less than that for the thyristor (1180 A^2s), the proposed 35 A fast acting fuse should afford adequate protection for the thyristor.
Generally, if the rms current rating of the fuse is less than the average current rating of the thyristor or diode, the fuse will provide adequate protection under fault conditions.

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10.2.2 Overvoltage

Voltage transients in electrical circuits result from the sudden release of previously stored energy, such as insulation breakdown arcing, fuses, contactors, freewheeling diode current snap, switches, and transformer energising and de--energising. These induced transients may be repetitive or random impulses. Repetitive voltage spikes are observable but random transients are elusively, unpredictable in time and location. A spike is usually brief but may result in high instantaneous power dissipation. A voltage spike in excess of a semiconductor rating for just a few microseconds usually results in catastrophic device failure. Extensive noise may be injected into low-level control logic causing spurious faults. Generally, high-frequency noise components can be filtered, but low-frequency noise is difficult to attenuate.
Effective transient overvoltage protection requires that the impulse energy be dissipated in the added transient absorption circuit at a voltage low enough to afford circuit survival.

10.2.2i - Transient voltage suppression devices

Two types of voltage transient suppression techniques can be employed.

- **Transient voltage attenuation**
  Low pass filters, such as an *L-C* filter, can be used to attenuate high frequencies and allow the low-frequency power to flow.
- **Diverter (to limit the residual voltage)**
  Voltage clamps such as crowbars or snubbers are usually slow to respond. The crowbar will be considered in section 10.2.3 while the snubber, which is for low-energy applications, has been considered in section 8.2.

The voltage-limiting function may be performed by a number of non-linear impedance devices such as reverse selenium rectifiers, avalanche (commonly called Zener) diodes, and varistors made of various materials such as silicon carbide or zinc oxide.

The relationship between the current in the non-linear device, *I,* and the voltage across its terminals, *V,* is typically described by the power law

$$I = kV^{\alpha} \quad \text{(A)} \qquad (10.34)$$

k is an element constant dependent on device geometry in the case of the varistor, and the non-linear exponent α is defined as

$$\alpha = \frac{\log I_2 - \log I_1}{\log V_2 - \log V_1} = \frac{\log I_2/I_1}{\log V_2/V_1} \qquad (10.35)$$

where I_1 and I_2 are taken a decade apart. The term alpha (α) represents the degree of non-linearity of the conduction. The higher the value of alpha, the better the clamp and therefore alpha may be used as a figure of merit. A linear resistance has an alpha of 1 ($I = \frac{1}{R}V^{+1}$).
The voltage-dependent resistance is given by

$$R = V/I = V/kV^{\alpha} = \tfrac{1}{k}V^{1-\alpha} \quad (\Omega) \qquad (10.36)$$

and the power dissipation is

$$P = VI = V\,kV^{\alpha} = kV^{\alpha+1} \quad \text{(W)} \qquad (10.37)$$

The most useful transient suppressors are the Zener diode and the varistor. They are compact devices which offer nanosecond response time and high energy capability.

1 - The Zener diode is a very effective clamp and comes the closest to being a constant voltage clamp, having an alpha of 35. Since the avalanche junction area is small and not highly uniform, substantial heating occurs in a small volume. The energy dissipation of the Zener diode is limited, although transient absorption Zener devices with peak instantaneous powers of 50 kW are available. These peak power levels are obtained by:

- Using diffusion technology, which leads to low metallisation contact resistance, narrow base width, and minimises the temperature coefficient.
- Achieving void-free soldering and thermal matching of the chip and the large area electrodes of copper or silver. Molybdenum buffer electrodes are used.
- Using bulk silicon compatible glass passivation which is alkali metal contamination free, and is cut without glass cracking.

Voltage ratings are currently limited to 280 V but devices can be series connected for higher voltage application. This high-voltage clamping function is unipolar and back-to-back series connected Zener diodes can provide high-voltage bipolar clamping.

2 - The varistor is a ceramic, bipolar, non-linear semiconductor utilising silicon carbide for continuous transient suppression or sintered zinc oxide for intermittent dissipation. Approximately 90 per cent by weight of zinc oxide and suitable additives such as oxides of bismuth, cobalt, and manganese, can give varistors with alphas better than 25. The structure of the plate capacitor like body consists of a matrix of conductive zinc oxide grains separated by grain boundaries, providing pn junction semiconductor-type characteristics. The grain sizes vary from

approximately 100 μm for low-voltage varistors down to 20 μm for high voltage components. The junctions block conduction at low voltage and provide non-linear electrical characteristics at high voltage. Effectively pn junctions are distributed throughout the structure volume, giving more uniformly distributed heat dissipation than the plane structure Zener diode. The diameter determines current capability, hence maximum power dissipation, while thickness specifies voltage. The structure gives high terminal capacitance values depending on area, thickness, and material processing. The varistor may therefore be limited in high-frequency applications. Functionally the varistor is similar to two Zener diodes connected back-to-back, in series.

10.2.2ii - Comparison between Zener diodes and varistors

Figure 10.18a illustrates the *I-V* characteristics of various voltage clamping devices suitable for 240 V ac application. The resistor with alpha equal to 1 is shown for reference. It is seen that the higher the exponent alpha, the nearer an ideal constant voltage characteristic is attained, and that the Zener diode performs best on these grounds. When considering device energy absorption and peak current and voltage clamping level capabilities, the Zener diode loses significant ground to the varistor.

The higher the alpha, the lower will be the standby power dissipated. Figure 10.18b shows the dependence of standby power dissipation variation on withstand voltage for various transient absorbers. A small increase in Zener diode withstand voltage produces a very large increase in standby power dissipation. Various device compromises are borne out by the comparison in table 10.1.

The current, power, and energy ratings of varistors are, typically, rated values up to 85°C, then linearly derated to zero at a case temperature of 125°C. Voltage-limiting diodes are typically linearly derated from rated values at 75°C to zero at 175°C. Reliability depends on the ambient temperature and applied voltage, and lifetime decreases with increased voltage or temperature. In the case of the varistor, an 8 per cent increase in applied voltage halves the mean time between failure, mtbf, for applied voltages less than 0.71 times the nominal voltage. Below 40°C ambient, the mtbf for a varistor is better than 7×10^8 hours.

The voltage temperature coefficient for the varistor is - 0.05 per cent/K while +0.1 per cent/K is typical for the power Zener.

The following design points will specify whether a Zener diode or varistor clamp is applicable and the characteristics of the required device.

- Determine the necessary steady-state voltage rating.
- Establish the transient energy to be absorbed by the clamp.
- Calculate the peak transient current through the clamp.
- Determine power dissipation requirements.
- Determine the clamping voltage to which the transient is to be suppressed.
- Estimate the number of fault cycles during the lifetime.

In order to meet higher power ratings, higher voltage levels or intermediate voltage levels, Zener diodes or varistors can be series-connected. The only requirement is

that each series device has the same peak current rating. In the case of the varistor this implies the same disc diameter. Then the *I-V* characteristics, energy rating, and maximum clamping voltages are all determined by summing the respective characteristics and ratings of the individual devices.

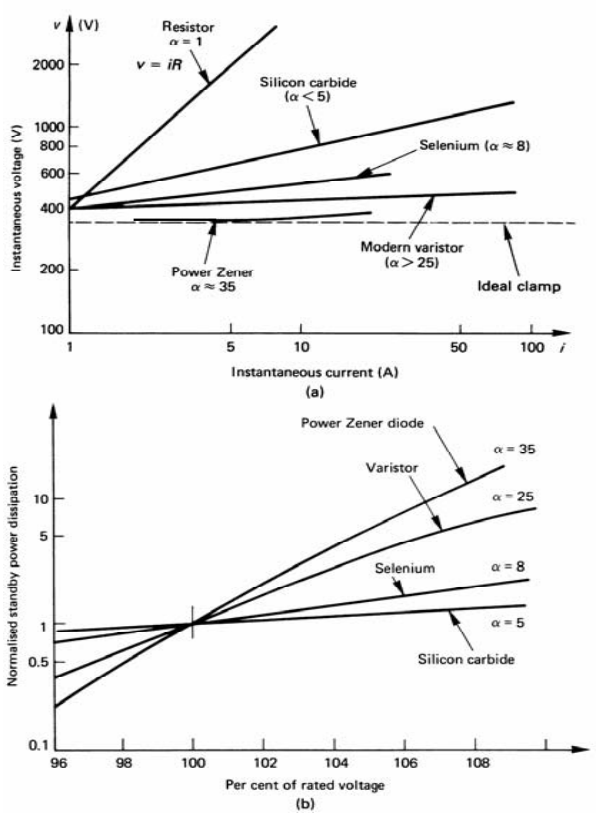

Figure 10.18. *(a) The I—V characteristics of four transient voltage suppressor devices, with resistance characteristics for reference and (b) standby power dissipation characteristics showing the higher the alpha the lower the standby power dissipation.*

Parallel operation is difficult and matched *I-V* characteristics are necessary. A feature of varistors often overlooked is deterioration. Figure 10.19a shows that at relatively low energy levels an infinite number of transients can be absorbed, while at rated absorbed energy only one fault is allowed. This single fault, lifetime, is defined as that energy level that causes a 10 per cent increase in clamping voltage level, for a specified current density.

Figure 10.19b shows that very high currents can be tolerated for short intervals. The lower the pulse number, the higher the allowable current.

The failure mode of the Zener diode and varistor is a short circuit. Subsequent high current flow may cause an explosion and disintegration of contacts, forming an open circuit. This catastrophic condition can be avoided by fuse protection.

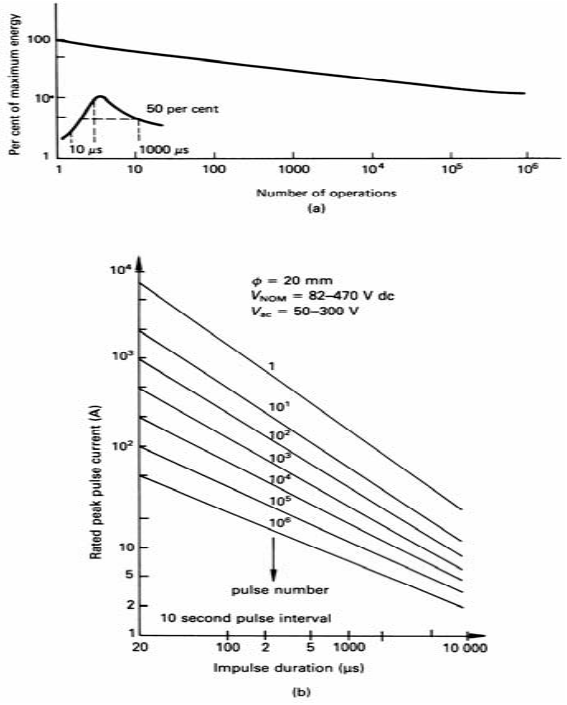

Figure 10.19. *Pulse lifetime ratings for a Zinc oxide varistor: (a) lifetime for fixed 10/100μs pulses and (b) lifetime number for variable-duration square-wave pulses.*

Table 10.1 A comparison of typical voltage transient suppressor characteristics

Suppressor type	Standby current (mA)	Peak current at 1 ms exp. (A)	Peak power at 1 ms (kW)	Peak energy (J)	Voltage clamping ratio at 10 A	Voltage range dc	Capacitance at 1 MHz (nF)
Silicon carbide varistor	5	-	-	50	4.6	15–300	-
Selenium	12	30	9	9	2.3	35–700	-
Metal oxide varistor	1	120	40	70	1.7	14–1200	2
Zener diode (5 W)	0.005	5.5	1.5	2	1.4	1.8–280	1

Example 10.6: ***Non-linear voltage clamp***

Evaluate the current of a 1mA @ 250 V Zener diode when used to clamp at 340V dc. Calculate the percentage decrease in voltage-dependent resistance and the per unit increase in power dissipation, assuming $\alpha = 30$.

Solution

From $I = kV^{\alpha}$, equation (10.34)

i. $I_2 = I_1(V_2/V_1)^{\alpha} = 1\text{ mA}\,(340\text{V}/250\text{V})^{30} = 10.14\text{ A}$
The Zener diode will conduct 10.14A when clamping at 340 V (a 10,140 increase on the standby current of 1mA)

ii. From equation (10.36), $R = V^{1-\alpha}/k$ therefore

$$1-\frac{R_2}{R_1} = 1-\left(\frac{V_2}{V_1}\right)^{1-\alpha} = 1-\left(\frac{340\text{V}}{250\text{V}}\right)^{-29} = 0.99987$$

The percentage decrease in resistance is 99.987 per cent.
The dynamic resistance decreases from (250 V / 1 mA) 250 kΩ to (340 V / 10.1 A) 33.5Ω. The incremental resistance (dv/di) reduces 10,000 to 1.

iii. $P = kV^{\alpha+1}$ (equation (10.37))

$$\frac{P_2}{P_1}-1 = \left(\frac{V2}{V1}\right)^{31} - 1 = \left(\frac{340\text{V}}{250\text{V}}\right)^{31} - 1 = 13793.5$$

The per unit power increase is 13,800.
The power increases from (250 V × 1 mA) 0.2 W at standby to (340 V × 10.14A) 3447.6 W when clamping at 340 V dc.

♣

10.2.3 Crowbar

A *crowbar* can be used for overvoltage and/or overcurrent protection in both ac and dc circuits. Figure 10.20 illustrates how an SCR can be used to provide fault protection for sensitive dc power electronic circuits and loads. Whenever a fault condition occurs the crowbar SCR is triggered, shorting the supply. The resultant high supply current flowing blows the fuse, or initiates a fast-acting circuit breaker/mcb, thereby isolating the load from the supply. The diode D_c provides a current path for inductive load energy.

The load current is measured by the voltage across the sense resistor *R.* When this voltage reaches a preset limit, that is the load current has reached the fault level, the SCR is triggered. The load or dc link voltage is measured from the resistor divider R_2-R_3. When this voltage exceeds the pre-determined limit the SCR is triggered and the fuse is blown by the crowbar short-circuit current, isolating the sensitive load from the supply.

A judiciously selected crowbar SCR can conduct many times its average current rating. For the few milliseconds in which the fuse is isolating, the SCR I^2t surge current feature can be exploited. The SCR I^2t rating must be larger than the fuse total I^2t rating. If the SCR crowbar is fuse-link protected then the total I^2t of the dc-link fuse link must be less than the pre-arcing I^2t of the SCR crowbar fuse link.

An ac crowbar can comprise two antiparallel-connected SCR's across the fuse-protected ac line, or alternatively one SCR in a four diode rectifying bridge.

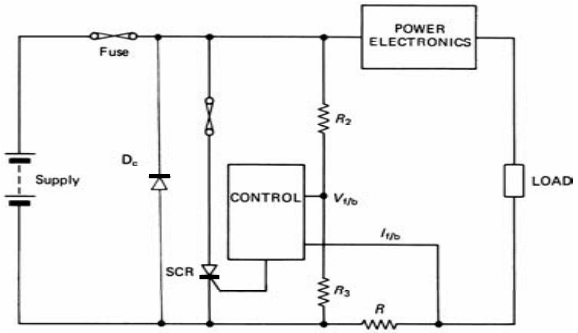

Figure 10.20. *An SCR crowbar for overvoltage and over-current protection.*

10.2.4 Noise

RFI noise (electromagnetic interference, EMI) and the resultant equipment interaction is an area of power electronic design that is often overlooked.

EMI is due to the effects of undesired energy transfer caused by radiated electromagnetic fields or conducted voltages and currents. The interference is

produced by a source emitter and is detected by a susceptible victim via a coupling path. The source itself may be a self-inflicted victim. The effects of this interference can vary from simple intermittent reset conditions to a catastrophic failure.

The coupling path may involve one or more of the following coupling mechanisms.

- *Conduction* - electric current
- *Radiation* - electromagnetic field
- *Capacitive coupling* - electric field
- *Inductive coupling* - magnetic field

10.2.4i - Conducted noise is coupled between components through interconnecting wiring such as through power supply (both ac and dc supplies) and ground wiring. This common impedance coupling is caused when currents from two or more circuits flow through the same wiring impedance. Coupling can also result because of common mode and differential currents, which are illustrated in figure 10.21.

10.2.4ii - Radiated electromagnetic field coupling can be considered as two cases, namely

- near field, $r \ll \lambda / 2\pi$, where radiation due to electric fields, *E*, and magnetic fields, *H*, are considered separate
- far field, $r \gg \lambda / 2\pi$, where the coupling is treated as a plane wave.

The boundary between the near and far field is given by $r = \lambda / 2\pi$ where λ is the noise wavelength and *r* is distance from the source.

In the far field, the characteristic impedance of free space Z_o, given by E / H, is constant, $\sqrt{\mu_o / \varepsilon_o} = 120\pi = 377\Omega$.

In the *near field* region, r^{-3} (as opposed to $r^{-2}$and r^{-1}) terms dominate field strength.

- A wire currying current produces $E \alpha r^{-3}$and $H \alpha r^{-2}$,
  - thus the electric field *E* dominates and the wave impedance $Z > Z_o$.
- A wire loop carrying current produces $H \alpha r^{-3}$and $E \alpha r^{-2}$,
  - thus the magnetic field *H* dominates and the wave impedance $Z < Z_o$.

In the near field, interference is dominated by the effective input impedance, Z_{in}, of the susceptible equipment and the source impedance R_s of its input drive.

- Electric coupling increases with increased input impedance, while
- magnetic coupling decreases with increased input impedance.

That is, electric fields, *E*, are a problem with high input impedance (because the induced current results in a high voltage similar to that given by equation (10.38)),

$$v = i_c \times R_s // Z_{in} = C_c \, dv / dt \times R_s // Z_{in} \qquad (10.38)$$

while magnetic fields, *H*, are a problem with low input impedance (because the induced voltage results in a high current similar to that given by equation (10.39)).

$$i = v_c / R_s // Z_{in} = M \, di / dt / R_s // Z_{in} \qquad (10.39)$$

In the *far field* the r^{-1} term dominates.

In the far field region both the *E* and *H* fields are in phase and at right angles. Importantly their magnitudes both decrease, inversely proportionally with distance *r*, so their magnitude ratio remains constant. That is, the characteristic impedance is $Z_o = \sqrt{\mu_o / \varepsilon_o} = 120\pi = 377\Omega$. The far field radiation wave with this constant

impedance is termed a plane wave. The electric field component of the plane wave tends to dominate interface problems in the far field region.

10.2.4iii - Electric field coupling is caused by changing voltage differences, *dv/dt*, between conductors. This coupling is usually modelled by capacitance.
The changing electric field produces a current according to $i = C_c dv/dt$, where coupling capacitance C_c is dependant distance of separation, area, and the permittivity of the media. The effect of the produced current is dependant on the source impedance R_s and the effective input impedance, Z_{in}, of the victim equipment as given by equation (10.38).

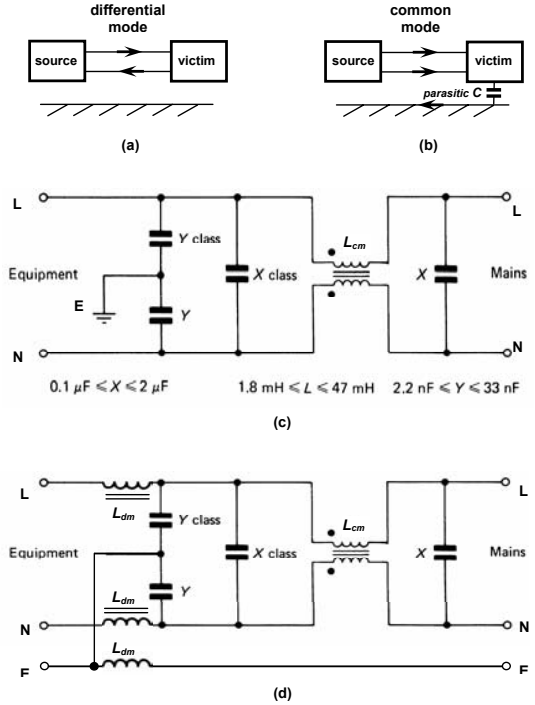

Figure 10.21. *Common mode and differential mode mains supply noise filtering: (a) differential mode noise paths; (b) common mode noise paths; (c) simple L-C mains filter; and (d) high specification mains filter.*

10.2.4iv - Magnetic field coupling is due to changing currents, *di/dt*, flowing in conductors. This coupling mechanism is usually modelled by a coupled circuit, or a transformer, according to $v=Mdi/dt$, where the resultant current is given by equation (10.39). The mutual inductance M is related to loop area, orientation, separation distance, and screening and its permeability. This induced voltage is independent of any ground connection or electrical connection between the coupled circuits. Magnetic field problems tend to be at low frequencies. Below 100kHz effective screen materials are steel, mu-metal (μ_r = 20,000), and permalloy, while at higher frequencies the good electrical conduction properties of copper and aluminium are more effective despite there much lower permeabilities.

10.2.5 Mains filters

The conducted ac mains borne noise can be attenuated to safe levels by filtering. The simplest type of filter is an inductor in series with the load in order to reduce any current *di/dt* changes. It is usual practice to use *L-C* filtering, which gives second-order attenuation. The typical circuit diagram of a mains voltage filter, with common mode noise filtering, is shown in figure 10.21c. The core inductance is only presented to any ampere turn imbalance (common mode current), not the much larger principle throughput (go and return) ac current, hence the core dimensional requirements can be modest. Extra non-coupled inductance is needed for differential mode filtering, as shown in figure 10.21d. Only the higher frequency noise components can be effectively attenuated since the filter must not attenuate the 50 Hz mains component.

10.2.6 Noise filtering precautions

For power electronics, circuit noise suppression and interaction is ultimately based on try-it and see. Logic does not necessarily prevail. The noise reduction precautions to follow are orientated towards power electronics applications.
Good circuit layout and construction (incorporated at the initial design stage) can greatly reduce the radiated noise, both transmitted and received. Obvious starting points are minimising wire loop lengths, using ground planes, capacitor decoupling, twisted wire pairs, and judicious placement of magnetic components. Use opto-couplers, not only to isolate signals but to allow flexible grounding that can bypass ground power noise around sensitive circuitry. Sensitive electronic circuitry should be rfi radiation protected by copper (electric and high frequency magnetic) or mild steel (low frequency magnetic) sheeting, depending on the type of radiation and frequency. Shielding, including isolated heatsinks, should be connected to a point that minimises interference. This may involve connection to supply rails (positive, zero, negative) or ground.
An *R-C* snubber across a diode decreases *dv/dt* while a series inductive snubber will limit *di/dt*. Mains series input inductors for bridge rectifiers (plus diode *R-C* snubbers) decrease the amount of diode recovery noise injected back into the mains and into the equipment. In ac circuit applications, zero-voltage turn-on and zero-current turn-off minimise any rapid changes in current, thus reducing radiation. To minimise diode recovery noise, slow down switch turn-on.

To minimise interactive noise effects, high noise immune circuit designs can be employed which utilise mos technology. The high-voltage input thresholds of cmos logic (4000 series), 74AC (not ACT) logic series, and power MOSFETs (high gate threshold and capacitance), offer circuit noise immunity. Since noise possesses both magnitude and duration, the much slower response times (but with high input thresholds) of 4000 HEF series cmos may result in better noise immunity in applications requiring clock frequencies below a few megahertz.
DSP core operating voltages below a few volts have necessitate: the use of a multilayer pcbs with ground planes, carefully layout separating of analogue and digital circuitry, low inductance ceramic chip decoupling, watchdog circuitry, etc.

Reading list

General Electric Company, *Transient Voltage Suppression,*
400.3, 1982.

Grafham, D.R. *et al., SCR Manual,*
General Electric Company, 6th Edition, 1979.

Williams, T., *EMC for Product Designers*,
Newnes, 2nd Edition, 1998.

Problems

10.1. Derive an expression for the worst case maximum allowable voltage-sharing resistance for n series devices each of voltage rating V_D and maximum leakage I_m across a supply V_s. The resistance tolerance is ± 100a per cent and the supply tolerance is ± 100b per cent.
If V_s = 1500 V, V_D = 200 V, I_m = 10 mA, n = 10 and tolerances are ±10 per cent, calculate resistance and maximum total power losses if

i. tolerances are neglected
ii. only one tolerance is considered
iii. both tolerances are included.

[i. R <5.5 kΩ, 63.8 W; ii. R <2.1 kΩ, 185 W; R <3.9 kΩ, 91 W; iii. R <280 Ω, 1234 W].

10.2. Derive a power loss expression for a voltage-sharing resistance network in which both supply and resistance tolerances are included. Assume a dc reverse bias of duty cycle δ.

10.3. Derive the power loss expression for an SCR string with voltage-sharing resistance and an ac supply.

10.4. Two diodes modelled as in figure 2.4a having characteristics approximated in the forward direction by

Diode D_1: $V_F = 1.0 + 0.01\ I_F$ (V)
Diode D_2: $V_F = 0.95 + 0.011\ I_F$ (V)

are connected in parallel. Derive general expressions for the voltage across and the current in each diode if the total current is 200 A.
At what total current and voltage will the diodes equally share?
[102.4 A, 97.6 A, 2.02 V; 100 A, 1.5 V]

10.5. In problem 10.4, what single value of resistance in series with each parallel connected diode match the currents to within 1 per cent of equal sharing? Calculate the resistor maximum power loss.
How will the current share at I_T = 100 A & I_T = 500A with the balancing resistors.
[14.5 mΩ, 148 W; 50 A, 50 A; 254 A, 246 A]

10.6. A Zener diode has an I-V characteristic described by $I = kV^{30}$. What percentage increase in voltage will increase the power dissipation by a factor of 1000? [25 per cent]

10.7. What is the percentage decrease in the dynamic resistance of the Zener diode in question 10.6? [99.845 per cent]

10.8. A string of three 2,600 V thyristors connected in series is designed to withstand an off-state voltage of 7.2 kV. If the compensating circuit consists of a series 33 Ω, 0.01 μF snubber in parallel with a 24 kΩ resistor, across each thyristor, and the leakage currents for the thyristors are 20 mA, 25 mA, and 15 mA, at 125°C, calculate the voltage across each thyristor, then the discharge current of each capacitor at turn-on.
[2400 V, 2280 V, 2520 V, 72.73 A, 69.09 A, 76.36 A]

10.9. The reverse leakage current characteristics of two series connected diodes are

Diode D_1: $I_1 = -10^{-4}\ V_1 + 0.14$ (A) for $V_1 < -1400$ V
Diode D_2: $I_2 = -10^{-4}\ V_2 + 0.16$ (A) for $V_2 < -1600$V

If the resistance across diode D_1 is 100 kΩ and $V_{D1} = V_{D2} = -2000$ V, what is the leakage current in each diode and what resistance is required across diode D_2?
[0.34 mA, 0.36 mA, ∞]

10.10. Two high voltage diodes are connected in series as shown in figure 10.5a. The dc input voltage is 5 kV and 10 kΩ dc sharing resistors are used. If the reverse leakage current of each diode is 25mA and 75mA respectively, determine the voltage across each diode and the resistor power loss.
[2750 V, 2250 V, 756.25 W, 506.25 W]

10.11. The forward characteristics of two parallel connected diodes are

Diode D_1: $I_1 = 200\ V_1 - 100$ (A) for $V_1 \geq 0.5$ V

Diode D_2: $I_2 = 200\ V_2 - 200$ (A) for $V_2 \geq 1$V

If the forward voltage of the parallel combination is 1.5V, determine the forward current through each diode. [200 A, 100 A]

10.12. Two diodes are connected in parallel and with current sharing resistances as shown in figure 10.7. The forward *I-V* characteristics are as given in problem 10.11. The voltage across the parallel combination is 2V and the balancing resistors are equal in value. Calculate each diode voltage and current. Calculate resistor maximum power loss. Let $I_{tot} = 400$ A.