Solution of Exercise 2

1- Module has 2 diodes. They are in parallel.
Conduction losses: Figure 1 gives us 30/2 = 15 A. Which with equal current sharing contributes to forward voltage V_F = 3.4 Conduction Energy = Eh = If * V_f * t_{on} = 15 A * 3.4 V * 20 us = 1.02 mJ
Blocking state losses: Figure 2 at 600 V and 175 C. Ir = 0 then No losses.
Switch on losses as negligible as datasheet page 1 shows diode has "zero forward recovery" meaning no conduction delay. Also, the voltage over diode is determined by the used transistor, not diode. so, the diode internal capacitance energy is lost inside the transistor, not diode.
During turn off the voltage transient happens through the diode and internal capacitance charging energy could be dimensioned to be fully lost inside the diode similarly to RC-protection circuit losses (assuming reverse recovery Irr = 0, as schottky-diode blocking voltage increases instantly after current direction reverses.)
$E_{REC} <= 1/2 *C*U^2 + 1/2*L*I_o^2 (=0) = 1/2\ CU^2$
Figure 4 shows, that internal capacitance is greatly dependent on voltage. Extrapolating to 600 V, C = 45 pF
$E_{REC} = 1/2 * 45\ pF * (600\ V)^2 = 8.1\ uJ$
It is noted that switching losses are only 0.8 % of the conduction losses. Therefore, it is not reasonable to study the effects of capacitance voltage dependence further.
Total losses are for single diode
$Ph = f*(E_H + E_{REC}) = 1/50\ us * (1.02\ mJ + 0.0081\ mJ) = 20.6\ W$
Losses for the whole module is 2*20.6 = 41.2 W
Datasheet shows that the whole module Rth(j-c) = 0.24 K/W. Because switching frequency is much greater than 1 kHz. We can safely use average power and steady state thermal resistances. In a precise dimensioning frequency converter phase current deviation and its effects should be accounted in the dimensioning.

2- $I_d=P/U_d=200kw/540=370A$
Thyristor average current: $ITav=\alpha*I_d/360^{\circ}=370/3=123A$
Cooling element Rth (h-a)=0.15k/w
Thyristor equivalent resistance Rth(j-c)=0.08 k/w
DSC, 120 deg, I_d constant
Then: $Rth_{j-a}=0.08+0.02+0.15=0.25$ k/w

From figure below $T_A<=82^{\circ}$ C

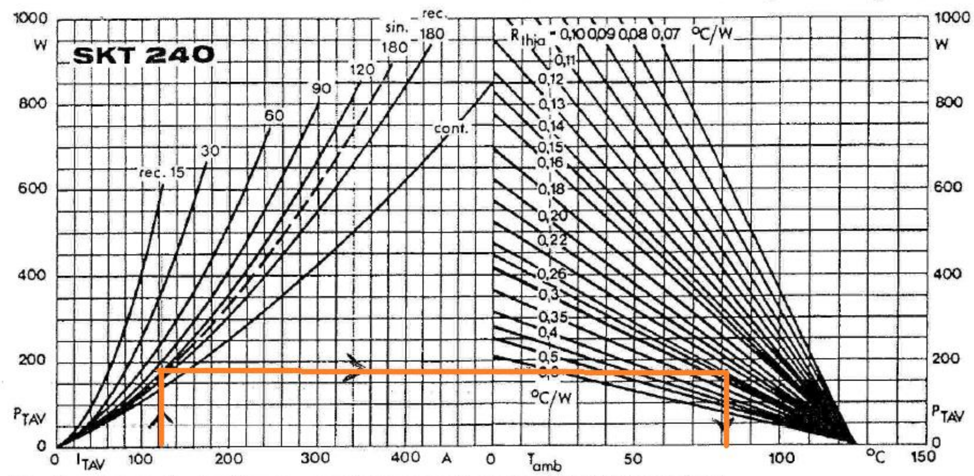
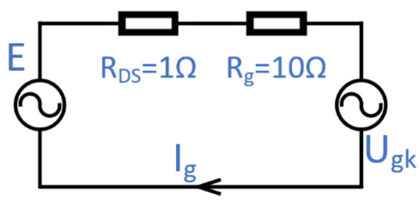


Fig. 1 a Power dissipation vs. on-state current and ambient temperature

3- Equivalent circuit:



$U_{gk}=E-(R_{DS}+R_g)*I_g=10-11*I_g$

U_{gk}	8.9	7.8	6.7	5.6	4.5	2.3	1.2	0.1
I_g	0.1	0.2	0.3	0.4	0.5	0.7	0.8	0.9

Reading from the datasheet figure 10 at -40 ° C

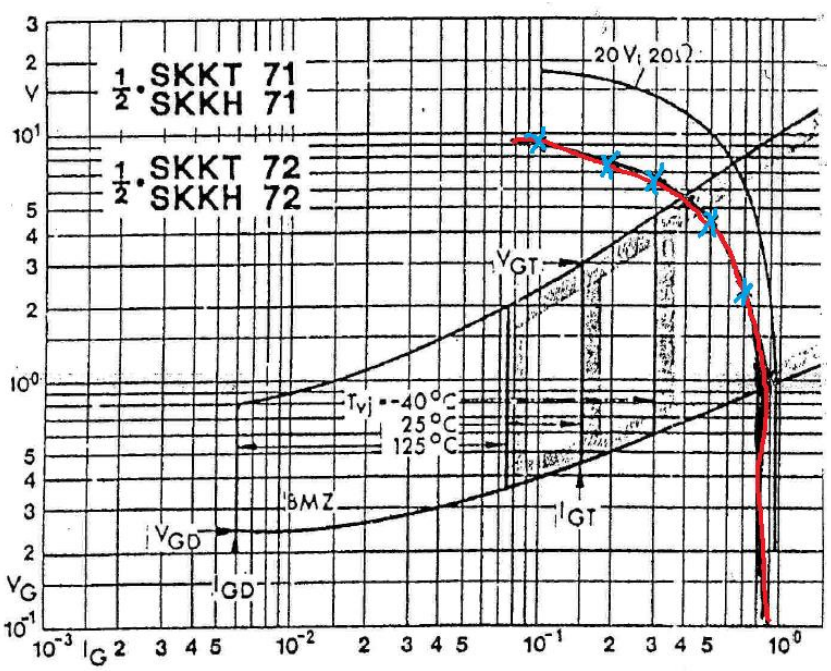


Fig. 10 Gate trigger characteristics

Maximum power occurs when source impedance is equal to load impedance.

Then $U_{gk}/I_g=R_{DS}+R_g \rightarrow E=2(R_{DS}+R_g)*I_g \rightarrow I_g=E/(2(R_{DS}+R_g))=5/11$ A

Then $P_{g\_max}=(R_{DS}+R_g)*I_g^2=2.3$ W