Process Flow Plan for Micronova Cleanroom Users

User name: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Has the process flow been accepted by Nanofab before: YES / NO (circle)

If yes, who has created the process and when: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

1. **General sample information**

* Device/structure name:
* Application:
* Substrate material (silicon, GaAs, glass...):
* Wafer size, thickness:
* Chip size:
* Number of chips:
* Sample state before your processing (blank, preprocessed):

1. **Planned processing schedule**

* Start date – end date:
* Volume (number of wafers, chips):

1. **Required equipment** (if known; see labbooking.micronova.fi for tool list)



1. **Samples outside the cleanroom?** Do you need to take out samples from the cleanroom and bring them back between process steps: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_
2. **Process flow**

Description of main process steps for sample preparation or analysis, illustrated by drawings (see the last page for an example). Below is the list of typical steps, but it is only a template! You must create your own process flow on separate page. **Remove the template/examples below and on the next page that are not part of your process!**

* + 1. chip (substrate) cleaning, e.g. RCA, dry cleaning, ultrasonic
    2. film deposition, e.g. ALD, PVD, (PE)CVD, oxidation, spin-on. Indicate film thickness!
    3. patterning, e.g. optical lithography, EBL, FIB. Tell about critical dimensions!
    4. etching, e.g. wet, RIE, ICP-RIE. Note about etching depth, if required
    5. resist removal, e.g. ultrasonic bath, plasma reactor
    6. sample tests and measurements in the cleanroom**An example of process flow**

Wafer oxidation at 1000°C resulting in 300 nm thick thermal SiO2.

Photoresist (AZ 5214E) spinning on the oxidized wafer.

Patterning including soft bake, exposure (mask aligner), development with AZ 351B and hard bake.

SiO2 etching with BHF/dry etching.

Photoresist stripping with acetone. Rinsing with IPA and DIW.

Titanium sputtering for adhesion (black) followed by copper seed layer sputtering (red). Typical thicknesses are 20 – 200nm. Patterning with lithography and etching in diluted HF/H2O2.

Copper electroplating. Layer thickness 5µm.

Tin electroplating followed by indium electroplating. Tin thickness 1 µm and indium thickness 1 µm.

Pressing of base wafer and cap wafer against each other in the pre-heat stage of bonding, 400 C, 5 minutes.

Actual bonding at 460 C, 6 kN, 1 hour.

Sawing of chips with the wafer saw.