Chapter 18

Utility Interface

- Power quality has become an important issue

Various Loads Supplied by the Utility Source

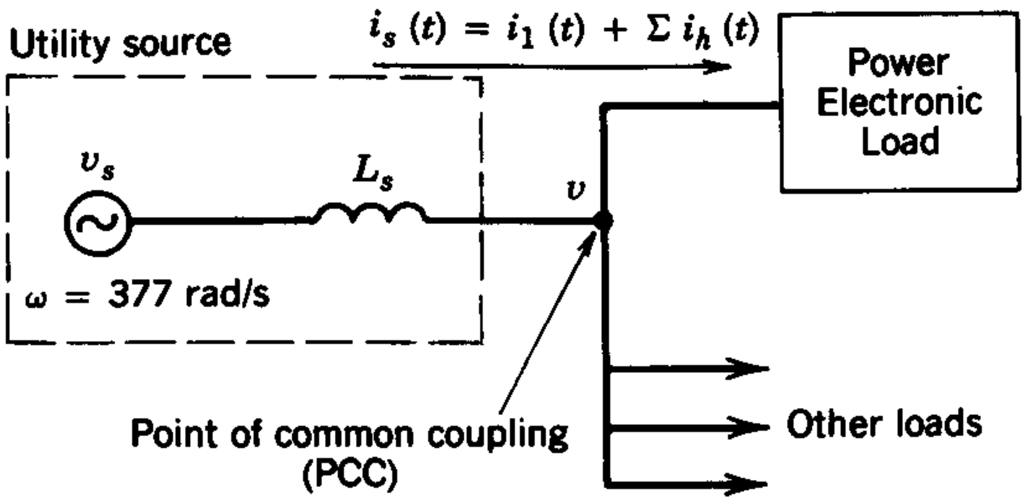

Figure 18-1 Utility interface.

- PCC is the point of common coupling

Diode-Rectifier Bridge

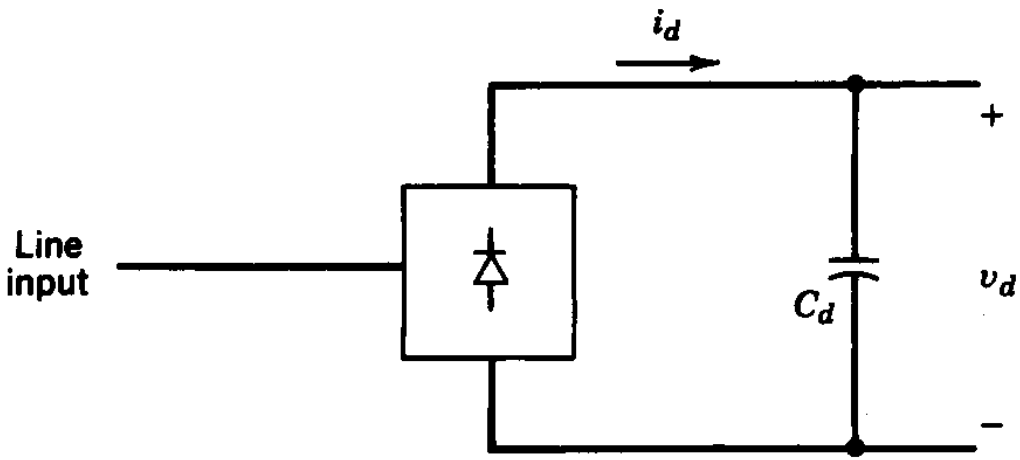

Figure 18-2 Diode rectifier bridge.

- Bock diagram

Typical Harmonics in the Input Current

Table 18-1 Typical Harmonics in a Single-Phase Input Current Waveform with No Line Filtering

h	3	5	7	9	11	13	15	17
$\left(\frac{I_h}{I_1}\right)\%$	73.2	36.6	8.1	5.7	4.1	2.9	0.8	0.4

- Single-phase diode-rectifier bridge

Harmonic Guidelines: IEEE 519

Table 18-2 Harmonic Current Distortion (I_h/I_1)

I_{SC}/I_1	Odd Harmonic Order *h* (%)					Total Harmonic Distortion (%)
	$h < 11$	$11 \le h < 17$	$17 \le h < 23$	$23 \le h < 35$	$35 \le h$	
<20	4.0	2.0	1.5	0.6	0.3	5.0
20–50	7.0	3.5	2.5	1.0	0.5	8.0
50–100	10.0	4.5	4.0	1.5	0.7	12.0
100–1000	12.0	5.5	5.0	2.0	1.0	15.0
>1000	15.0	7.0	6.0	2.5	1.4	20.0

Note: Harmonic current limits for nonlinear load connected to a public utility at the point of common coupling (PCC) with other loads at voltages of 2.4–69 kV. I_{sc} is the maximum short-circuit current at PCC. I_1 is the maximum fundamental-frequency load current at PCC. Even harmonics are limited to 25% of the odd harmonic limits above.

Source: Reference 1.

- commonly used for specifying limits on the input current distortion

Harmonic Guidelines: IEEE 519

Table 18-3 Harmonic Voltage Limits (V_h/V_1) (%) for Power Producers (Public Utilities or Cogenerators)

	2.3–69 kV	*69–138 kV*	*> 138 KV*
Maximum for individual harmonic	3.0	1.5	1.0
Total harmonic distortion	5.0	2.5	1.5

Note: This table lists the quality of the voltage that the power producer is required to furnish a user. It is based on the voltage level at which the user is supplied.

Source: Reference 1.

- Limits on distortion in the input voltage supplied by the utility

Reducing the Input Current Distortion

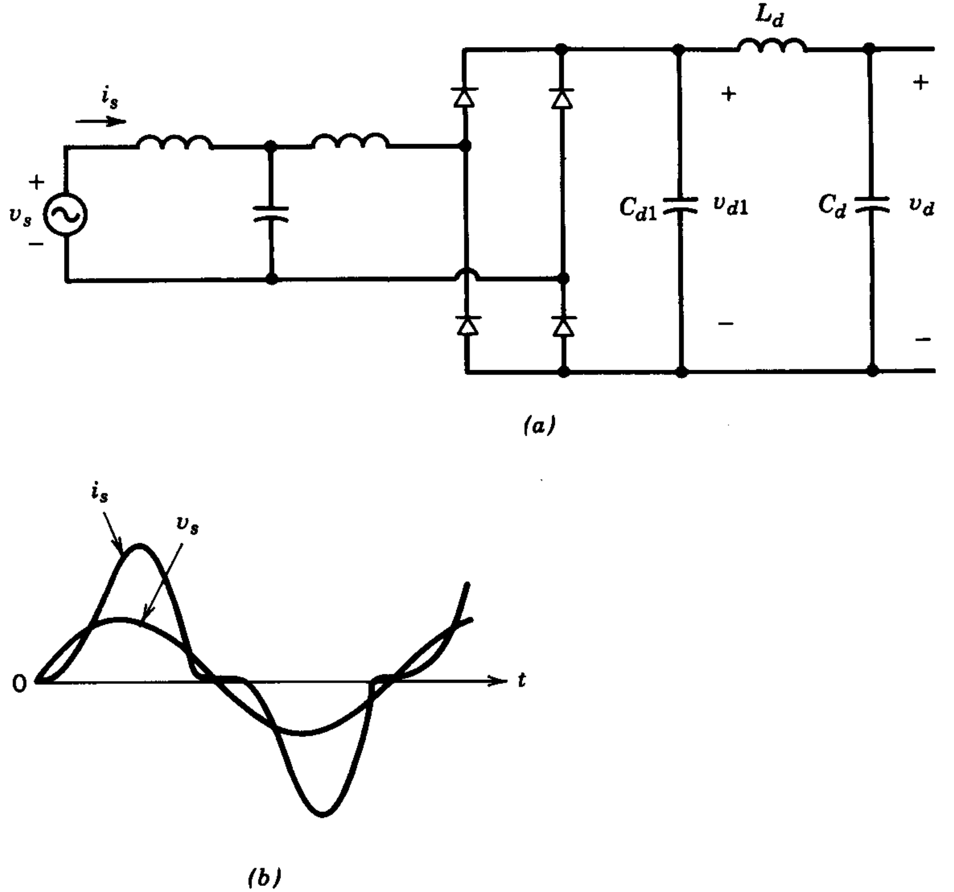

Figure 18-3 Passive filters to improve i_s waveform: (*a*) passive filter arrangement; (*b*) current waveform.

- use of passive filters

Power-Factor-Correction (PFC) Circuit

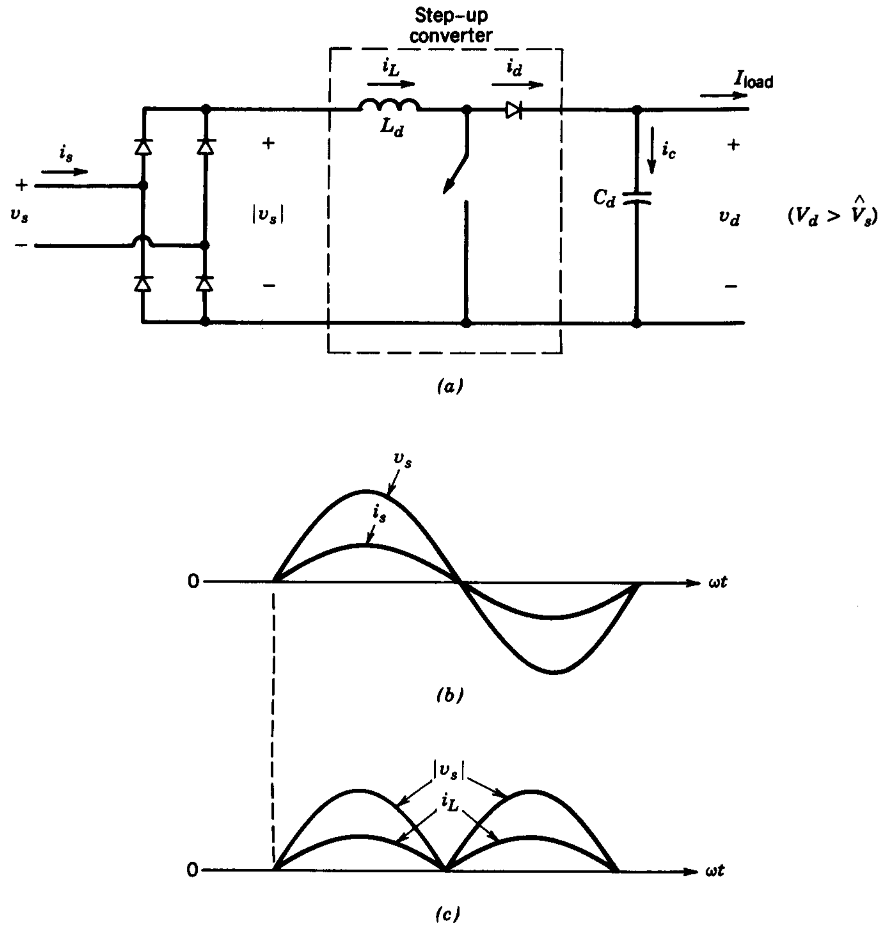

Figure 18-4 Active harmonic filtering: (*a*) step-up converter for current shaping; (*b*) line waveforms; (*c*) v_s and i_L.

- For meeting the harmonic guidelines

Dc current

- No losses and current sinusoidal in input side

$$p_{in} = \sqrt{2}U_s \left|\sin \omega t\right| \left|\sqrt{2}I_s \sin \omega t\right| = U_s I_s - U_s I_s \cos 2\omega t$$

- Dc voltage u_d can be assumed constant

$$p_d = U_d i_d$$

- Large switching frequency
  - L_d can be assumed small
  - Instantaneous powers are equal, $p_{in} = p_d$

$$i_d = I_d + i_C = \frac{U_s I_s}{U_d} - \frac{U_s I_s}{U_d} \cos 2\omega t$$

Voltage ripple

$$i_d = I_d + i_C = \frac{U_s I_s}{U_d} - \frac{U_s I_s}{U_d}\cos 2\omega t \qquad I_d = I_{load} = \frac{U_s I_s}{U_d}$$

- Capacitor current

$$i_C = -\frac{U_s I_s}{U_d}\cos 2\omega t = -I_d \cos 2\omega t$$

- Capacitor voltage ripple

$$u_{d,ripple} = \frac{1}{C_d}\int i_C dt = -\frac{I_d}{2\omega C_d}\cos 2\omega t$$

Power-Factor-Correction (PFC) Circuit Control

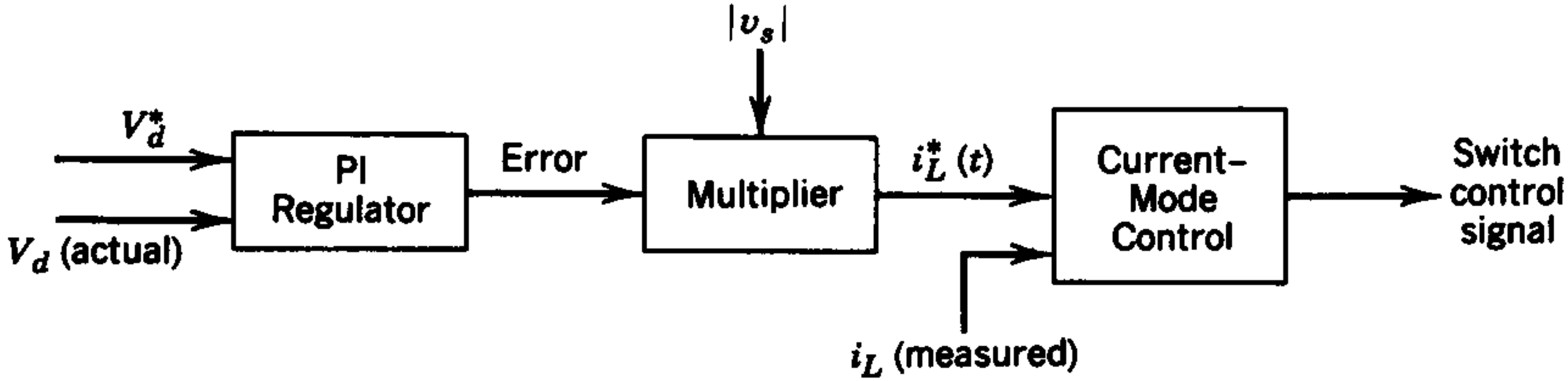

Figure 18-5 Control block diagram.

• generating the switch on/off signals

Power-Factor-Correction (PFC) Circuit

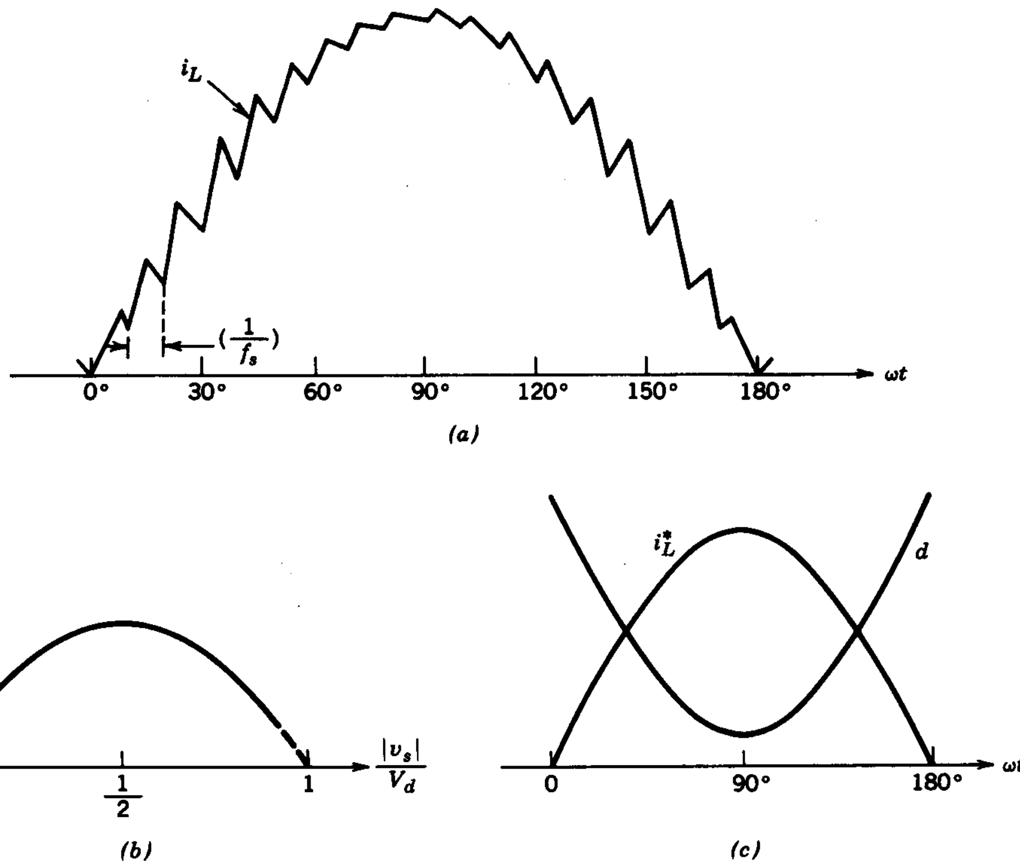

Figure 18-6 Constant-frequency control.

- Operation during each half-cycle

Current ripple

- Both dc voltage U_d and supply voltage assumed constant during switch conduction
  - times

$$t_{on} = \frac{L_d I_{hys}}{|u_s|} \qquad t_{off} = \frac{L_d I_{hys}}{U_d - |u_s|}$$

- Switching frequency

$$f_s = \frac{1}{t_{on} + t_{off}} = \frac{(U_d - |u_s|)|u_s|}{L_d I_{hys} U_d}$$

- Switching frequency is constant, current ripple and its maximum value

$$I_{hys} = \frac{(U_d - |u_s|)|u_s|}{f_s L_d U_d} \qquad I_{hys,\max} = \frac{U_d}{4 f_s L_d} \quad \text{kun} \quad |u_s| = \frac{U_d}{2}$$

Thyristor Converters for 4-Quadrant Operation

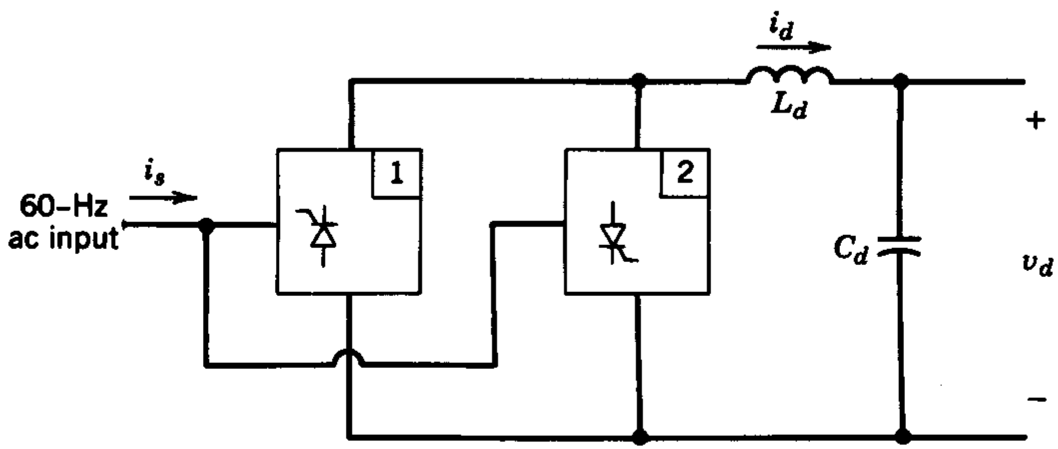

Figure 18-7 Back-to-back connected converters for bidirectional power flow.

- Two back-to-back connected 2-quadrant converters

Switch-Mode Converter Interface

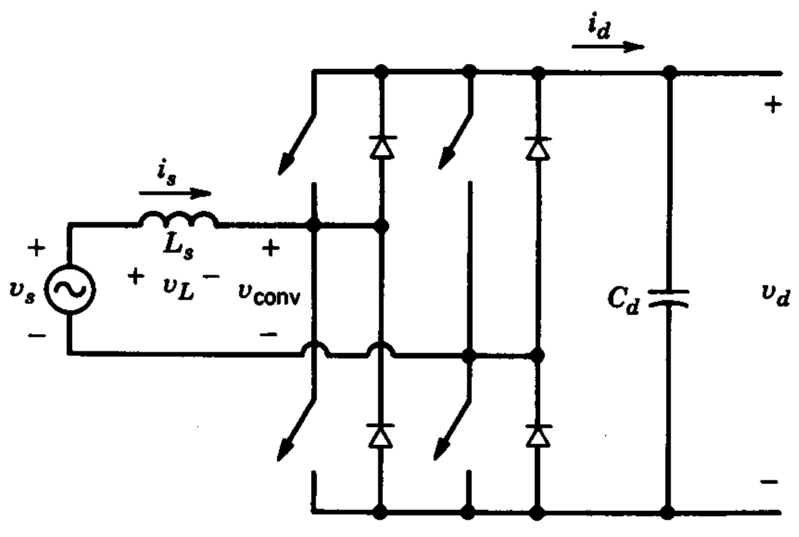

Figure 18-8 Switch-mode converter for the utility interface.

- Bi-directional power flow; unity PF is possible

Switch-Mode Converter Interface

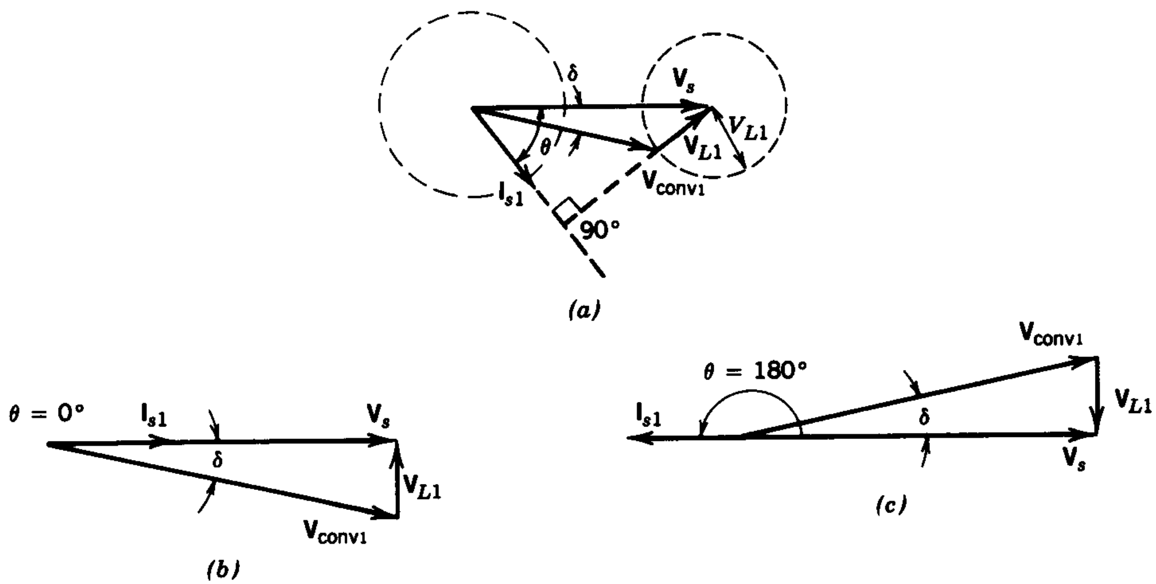

Figure 18-9 Rectification and inversion: (*a*) general phasor diagram; (*b*) rectification at unity power factor; (*c*) inversion at unity power factor.

- Rectifier and Inverter modes based on the direction of power flow

Switch-Mode Converter Control

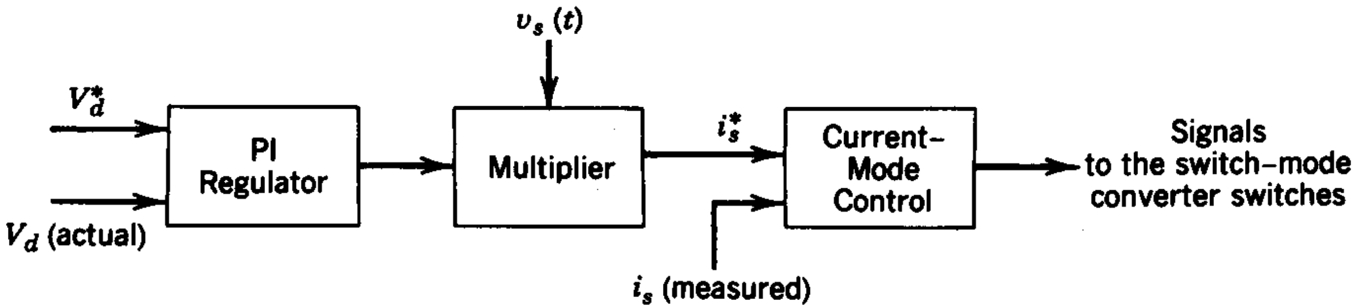

Figure 18-10 Control of the switch-mode interface.

- DC bus voltage is maintained at the reference value

Switch-Mode Converter Interface

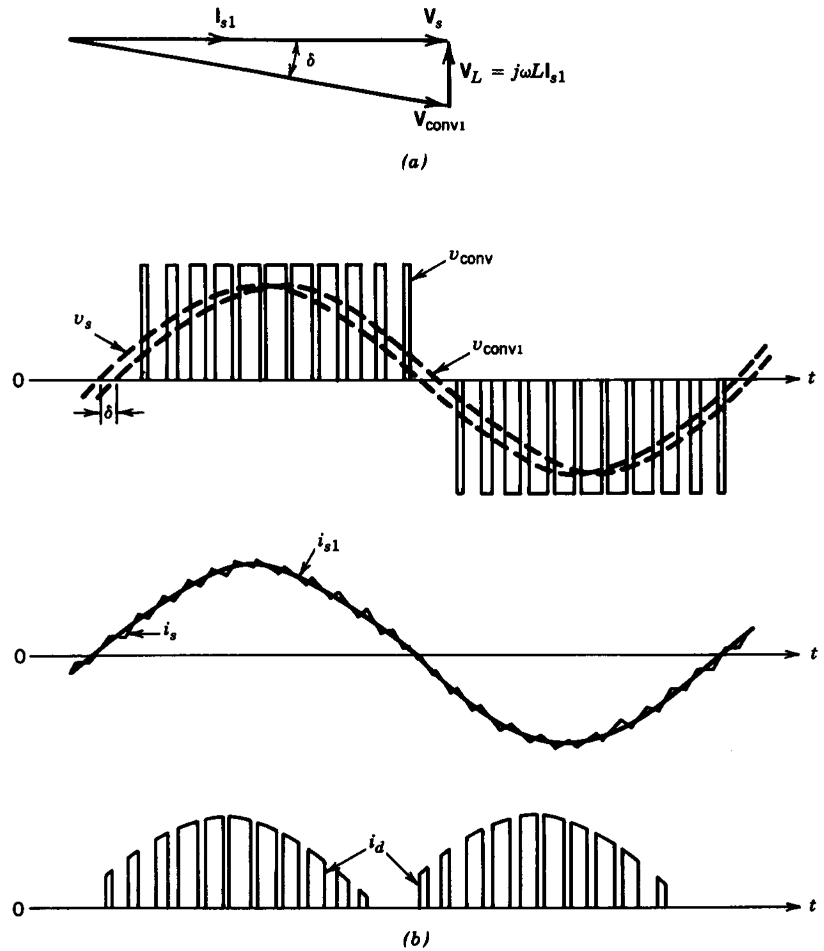

Figure 18-11 Waveforms in the circuit of Fig. 18-8 at unity power factor of operation: (*a*) phasor diagram; (*b*) circuit waveforms.

- Waveforms in the rectifier mode

3-Phase Switch-Mode Converter Interface

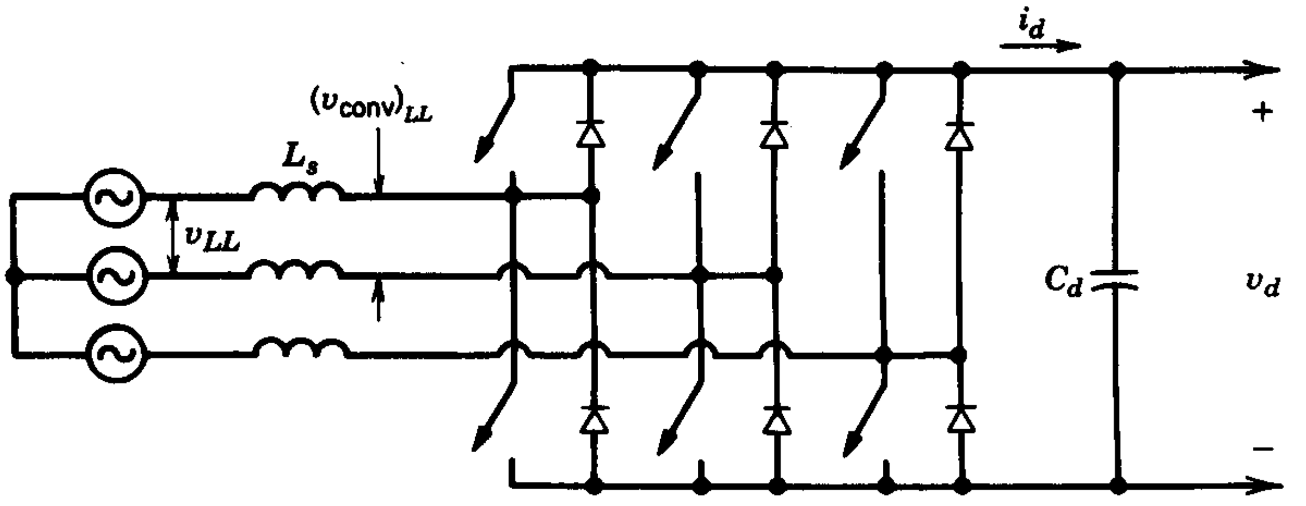

Figure 18-12 Three-phase, switch-mode converter.

- Rectifier and Inverter modes based on the direction of power flow

EMI: Conducted Interefence

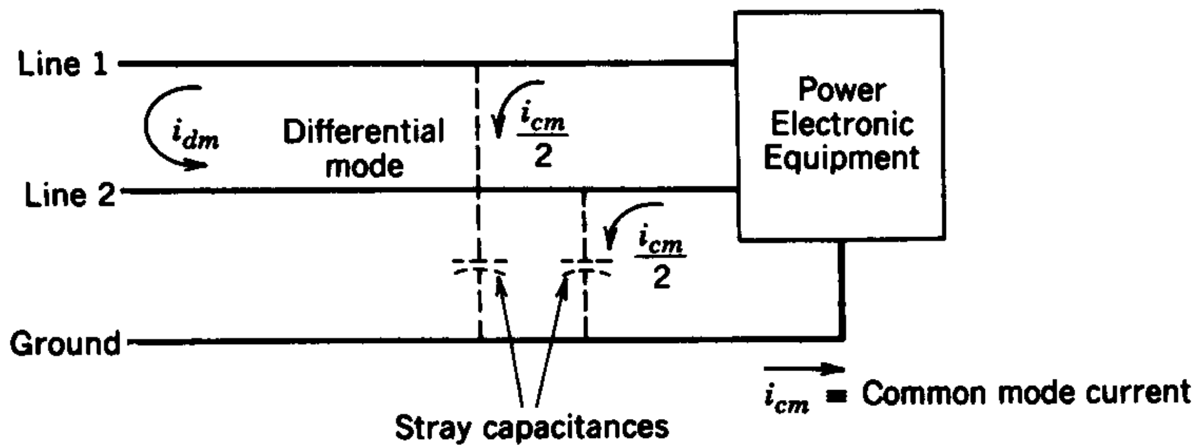

Figure 18-13 Conducted interference.

- Common and differential modes

Switching Waveforms

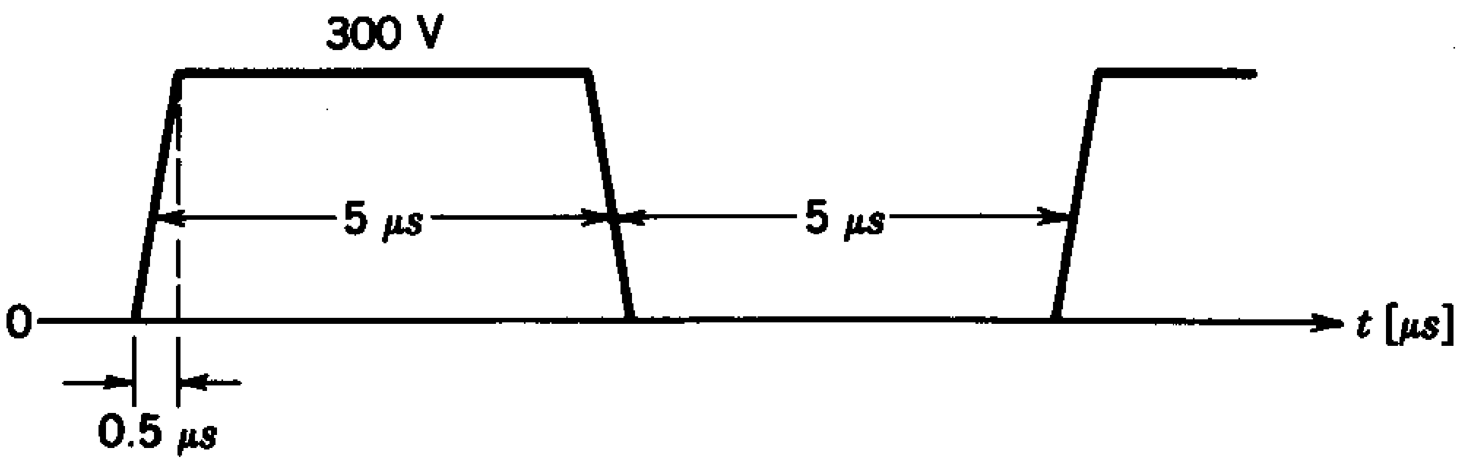

Figure 18-14 Switching waveform.

- Typical rise and fall times

Conducted EMI

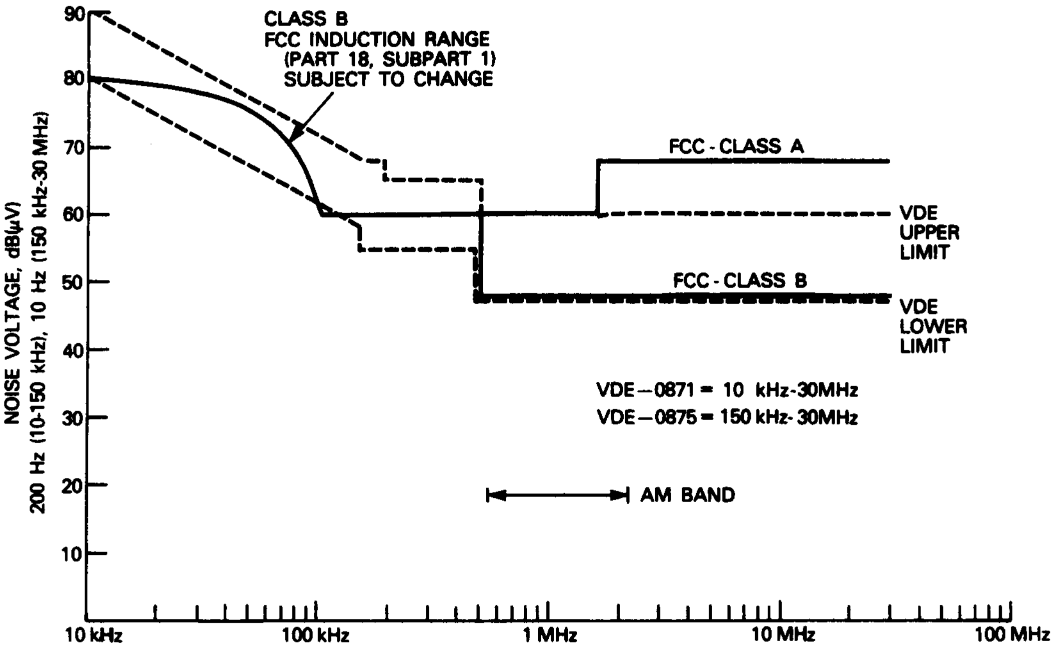

Figure 18-15 The FCC and VDE standards for conducted EMI.

- Various Standards

Conducted EMI

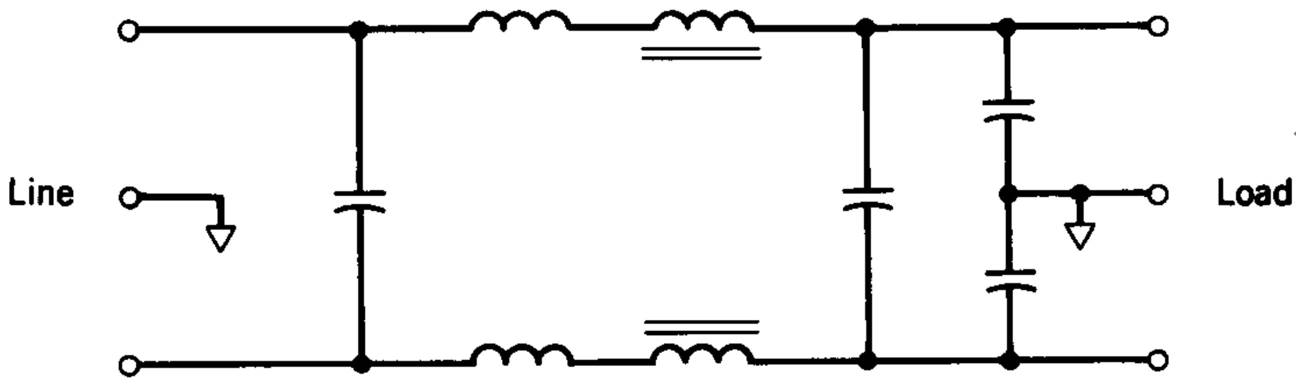

Figure 18-16 Filter for conducted EMI.

- Filter arrangement