School of Electrical Engineering Department of Electrical Engineering and Automation **ELEC 8201 Control and Automation**

> Exercise session 3 State-Based Design Implementation issues

> > Valeriy Vyatkin Pranay Jhunjhunwala Udayanto Dwi Atmojo



- State machine implementation in ST on the elevator example
- Oven controller design:

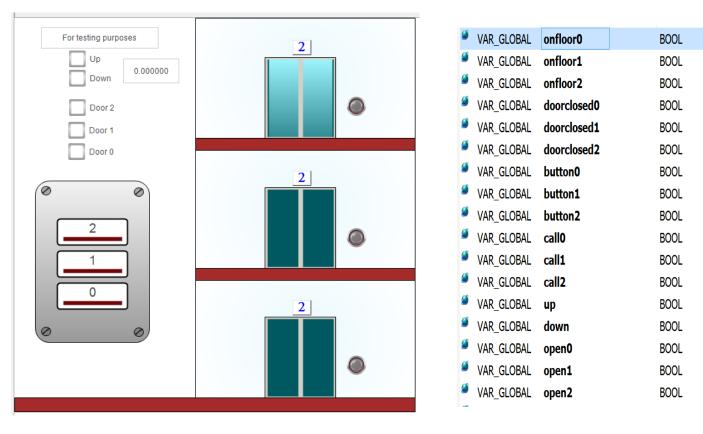
- From verbal spec to state machine

- Exercise on state machine implementation
 - As a ST code
 - As ECC in function block



State-based design example: 3-Floor Elevator

- There is no weight sensor and no stop button in the elevator
- All call buttons are constantly active

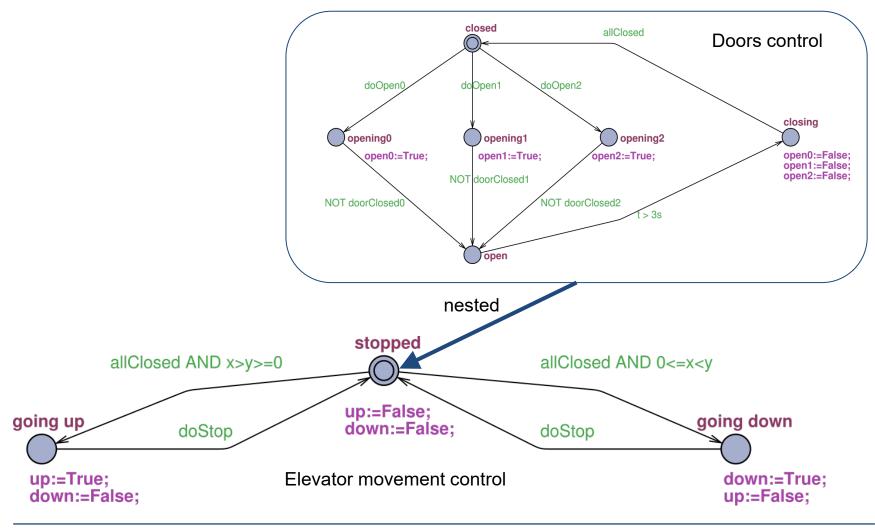


Elevator at floor U
Elevator at floor 1
Elevator at floor 2
Doors at floor 0 are closed
Doors at floor 1 are closed
Doors at floor 2 are closed
Call button at floor 0
Call button at floor 1
Call button at floor 2
Request floor 0 from inside the cabin
Request floor 1 from inside the cabin
Request floor 2 from inside the cabin
Control the elevator to go up
Control the elevator to go down
Open the doors at floor 0
Open the doors at floor 1
Open the doors at floor 2

Elevator at floor 0

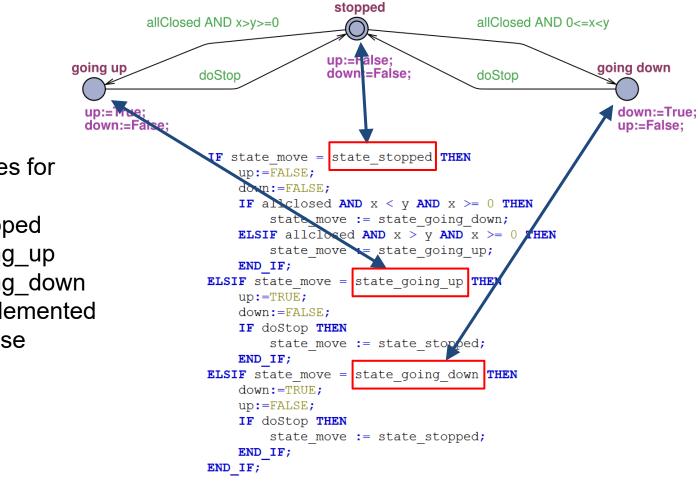


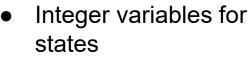
Final controller





Implementation of state machines in ST

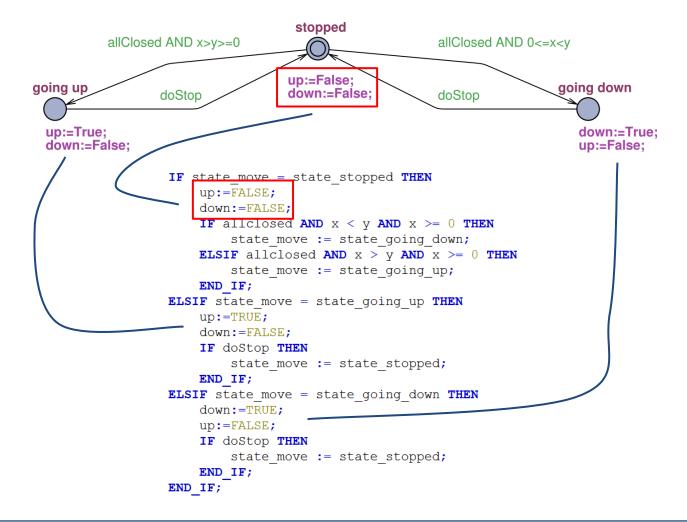




- state_stopped
- state_going_up
- o state_going_down
- transitions implemented using if-then-else

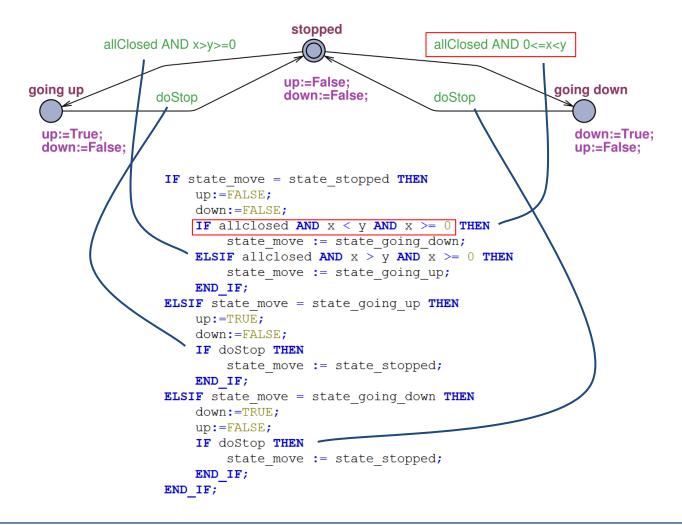


Implementation of state machines in ST





Implementation of state machines in ST



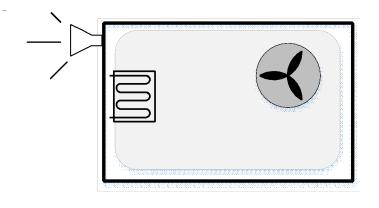


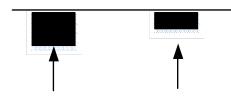
Example: heating oven

Verbal specification:

The oven is started with a **Start** button that seals in the Auto mode. This can be stopped if the **Stop** button is pushed. (Remember: **Stop** buttons are normally closed.)

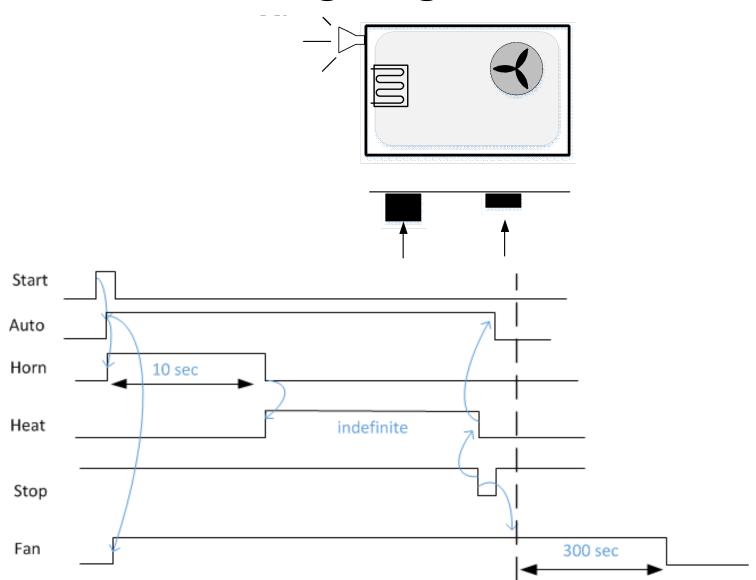
When the Auto goes on, the **horn** is used to sound for the first 10 seconds to warn that the oven will start, and after that the horn stops and the **heating coils** start. When the oven is turned off the **fan** continues to blow for 300s, or 5 minutes, after.





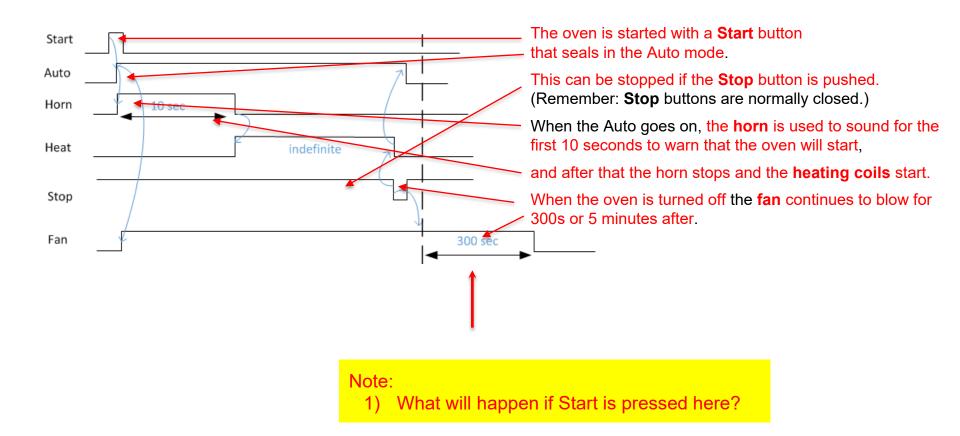


Timing Diagram



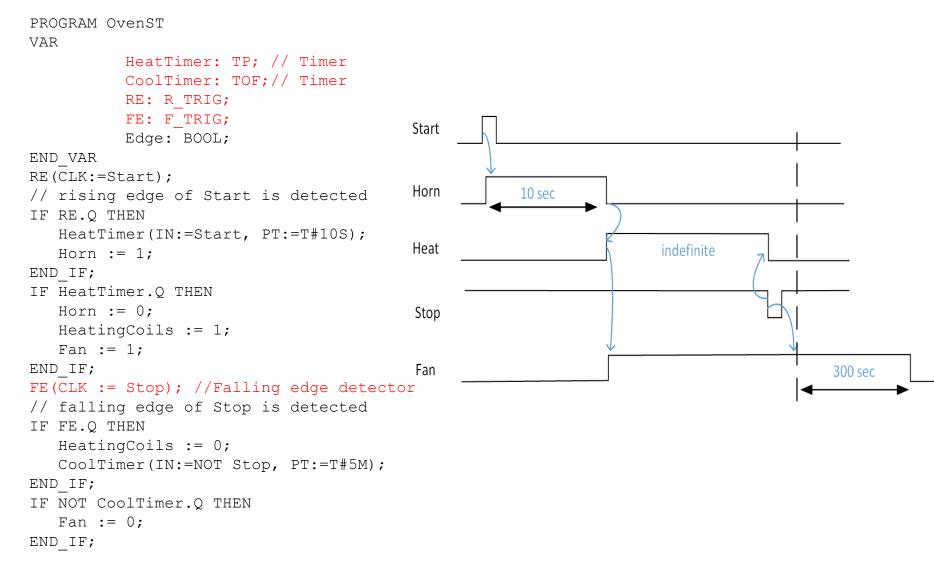


Timing diagram vs. Specification



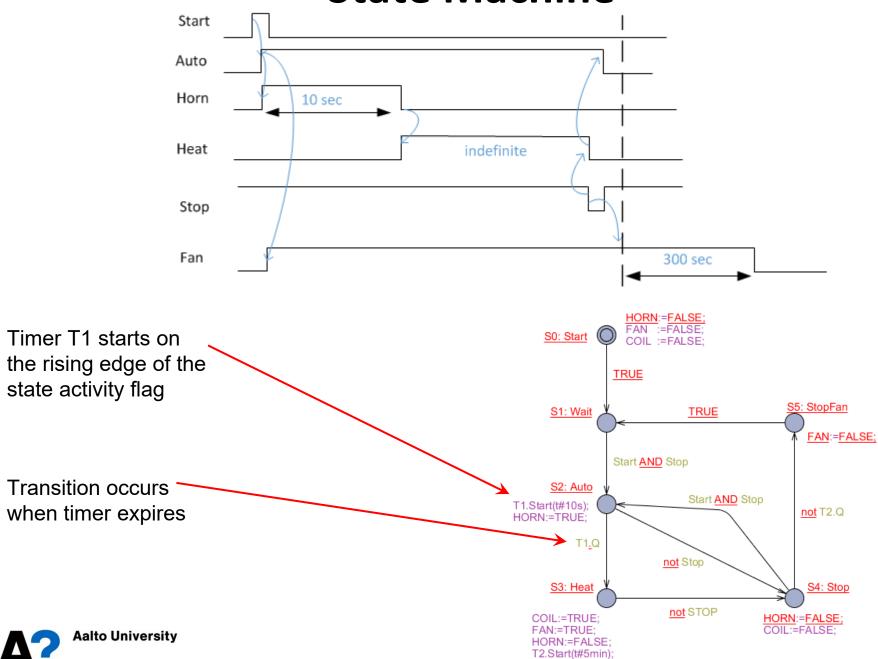


Let us follow the diagram ... (naive engineering)

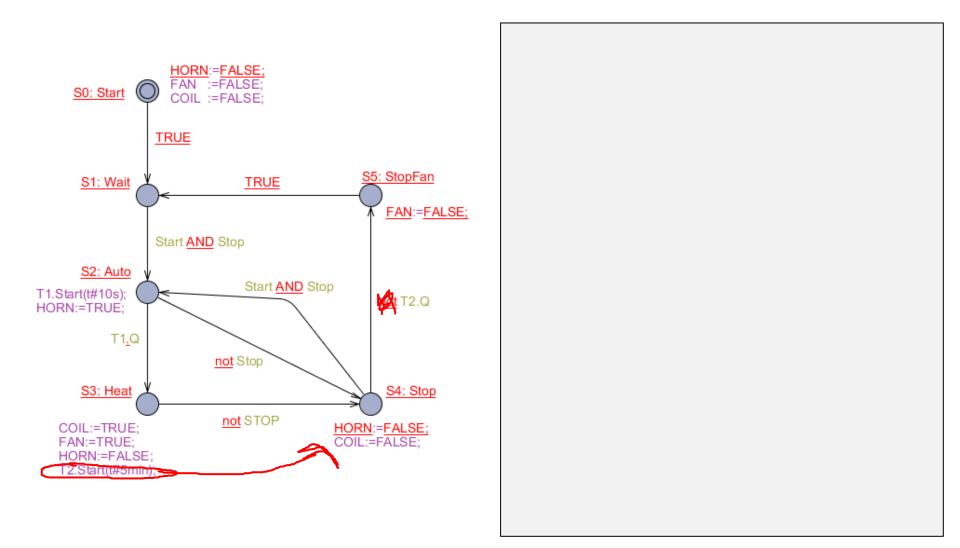




State Machine

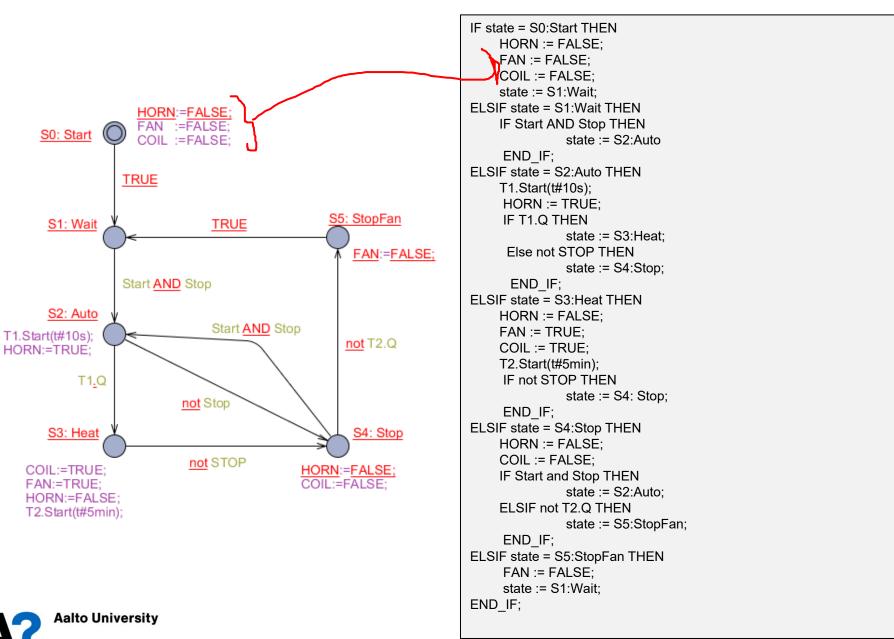


From State Machine to ST

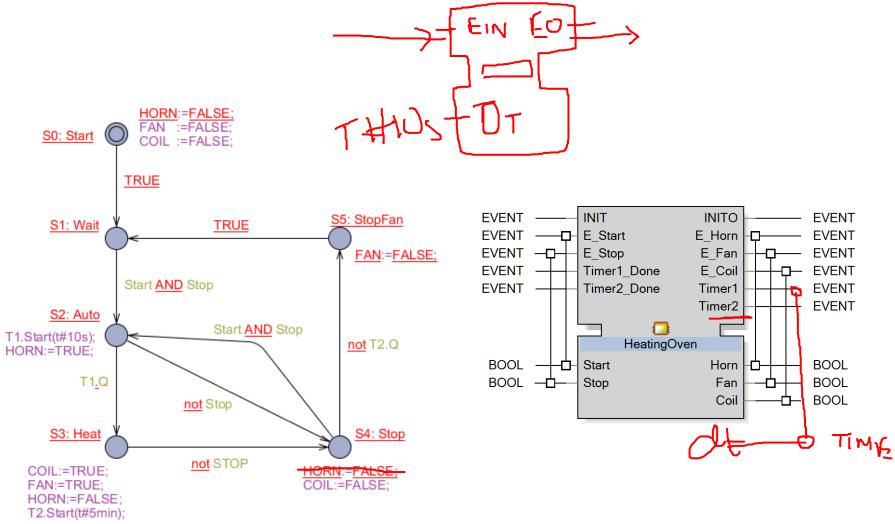




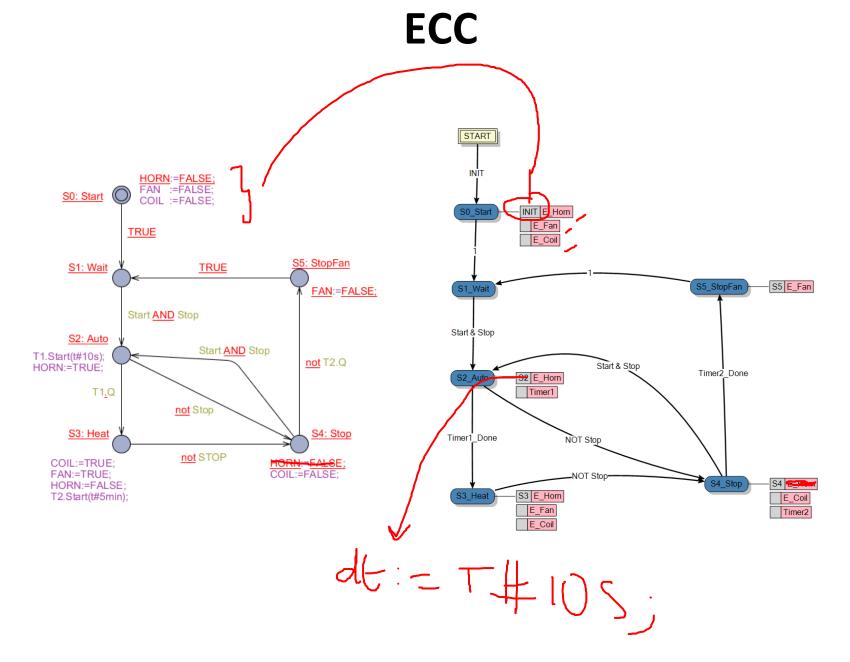
From State Machine to ST



From State Machine to Function block

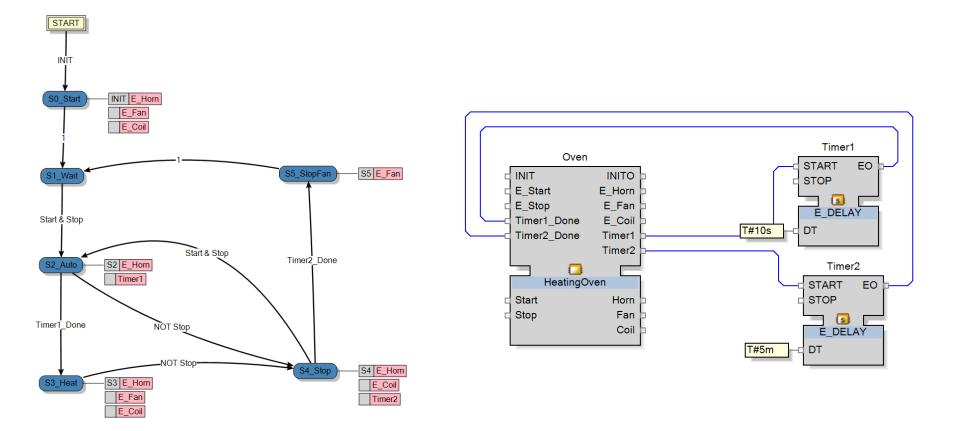








ECC & FB Network





Questions

