Microfabrication, Exercise 7: CMOS
(return by 30.04. 2023, 10 pm Sunday)

Session will be on May 2nd, 9:15 o'clock.

1. Identify materials, estimate layer thicknesses and design fabrication process for the high-voltage MOS shown below. Note, that there are shallow doping areas below gates, *p*-doped (dashed line) and *n*-dope (plain line), respectively. (2 p.)

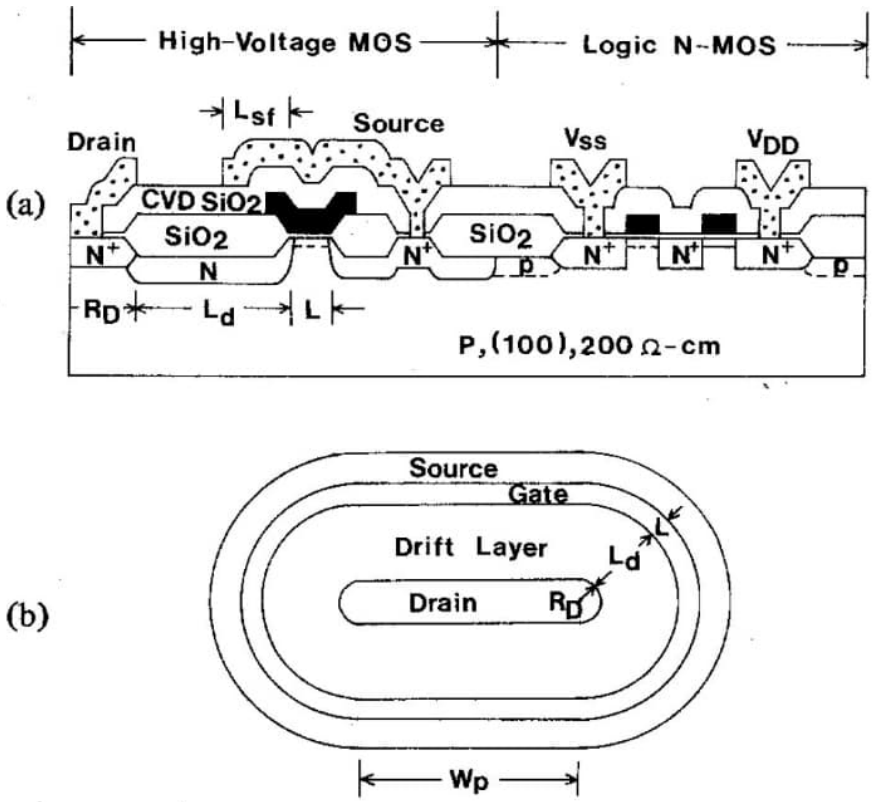

Fig. 1. (a) High-voltage MOS IC device structure. (b) High-voltage MOS device pattern.

2. A thin film MOS transistor is shown below. Propose a process flow to fabricate this device, including materials, layer thicknesses and deposition methods. Maximum process temperature is 300 ºC. Is your transistor a self-aligned one? How long is the channel? (2 p.)